VIA Labs, Inc.

Datasheet

VL102
DP Alt-mode & PD 3.0 Controller for USB-C Devices

Oct 18th, 2016

Revision 0.8

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Revision History

Rev	Date	Note	Initial
0.70	06/29/2016	Preliminary release	HC
0.80	10/18/2016	Convert to VLI latest datasheet format	HC

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Contents

List of Figures

List of Tables

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Product Features

VL102

DisplayPort Alt-mode & PD 3.0 Controller for USB-C Devices

■ **CC Logic & PD Engine supporting one charging UFP and one DRP**
– Compliant to USB Type-C Cable and Connector Specification Revision 1.2
– Compliant to USB Power Delivery Specification Revision 3.0 Version 1.0a
– Integrated Type-C transceivers, supporting one charging UFP and one DRP
– Built-in pull-up/pull down resistors, including Rp, Rd, and Ra
– Built-in Vconn power switch

■ **DP Alt-mode Configuration**
– Compliant to VESA DisplayPort Alt Mode on USB Type-C Standard Version 1.0a
– DP mode Discovery/Enter/Exit
– DP configure, status update, source/sink connection detection
– Built-in Aux_CH switch

■ **USB-C Charging UFP Capability**
– Charging connected PD hosts once external power is available
– Support Provider and Consumer roles
– Support PD Power Rule up to 100W
– Support charging dead battery and Fast Role Swap

■ **USB-C DRP Capability**
– Support Provider and Consumer roles
– Support PD Power Rule up to 100W as Sink and 15W as Source
– Built-in D+/D- Charging ePHY for chargers using D+/D- as protocol handshake
– Built-in USB HS data switch

■ **USB Billboard Device & USB C-Bridge**
– Compliant to USB Device Class Definition for Billboard Devices Revision 1.1
– Compliant to USB Type-C Bridge Spec Revision 1.0 RC
– Integrated in-house USB2.0 PHY

■ **Fast 8051 Macro cell 80C32-Compatible Microcontroller**
– Standard 1T 8051 instruction set
– Embedded Mask ROM and SRAM
– Support external SPI flash for firmware upgrade

■ **Built-in Voltage Regulators, Voltage Detector, and Current Detector**
– 5.0V to 3.3V LDO & 3.3V to 1.8V LDO
– Auto power source selection between Vbus and Vconn
– Vbus Voltage Detector and Vbus Current Detector for power monitoring

■ **GPIOs for Special Function and Control**
– 9 GPIOs for application customization and one I^2C master interface

■ **Physical**
– QFN 48 green package (6x6x0.85 mm)

■ **Certification**
– TBD

■ **Applications**
– USB-C video adapters
– USB-C Multi-function docks

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VL102 System Overview

VIA Lab's VL102 is a highly integrated single chip DisplayPort Alternate mode and Power Delivery 3.0 controller for USB-C devices that designed for applications like USB-C video adapters and USB-C multi-function docking stations. Integrated USB-C charging UFP, VL102 can perform DP alt-mode video out functionality and simultaneously enable charging connected PD host once external power is detected. Integrated USB-C DRP can either connect to USB-C power adapter to charge PD host or connect to USB-C devices to do data transfer. A D+/D- charging ePHY is integrated to support chargers using D+/D- to do protocol handshake. VL102's Device Policy Manager could negotiate power rules between its DRP and UFP then enable power charging-through. Charging a host under dead battery mode and fast role swap are supported. SBU1/SBU2 switch is built-in to support USB-C cable flipping feature. USB Billboard device and USB-C bridge function are implemented to meet "VESA DP Alt-Mode on USB Type-C" spec and let the USB host to communicate with PD products connected on downstream port.

Built-in required linear voltage regulators, Vbus voltage detector, and Vbus current detector, VL102 can work perfectly with power input either from Vconn power or from Vbus power and can monitor abnormal power behavior. Up to 9 GPIO pins are available for power discharge control, power switch control, data switch control, or other special application usage. The SPI interface can support external flash for firmware upgrades through USB Billboard device. VL102 is available in QFN 48L (6x6x0.85 mm) green packages to fit small form-factor design.

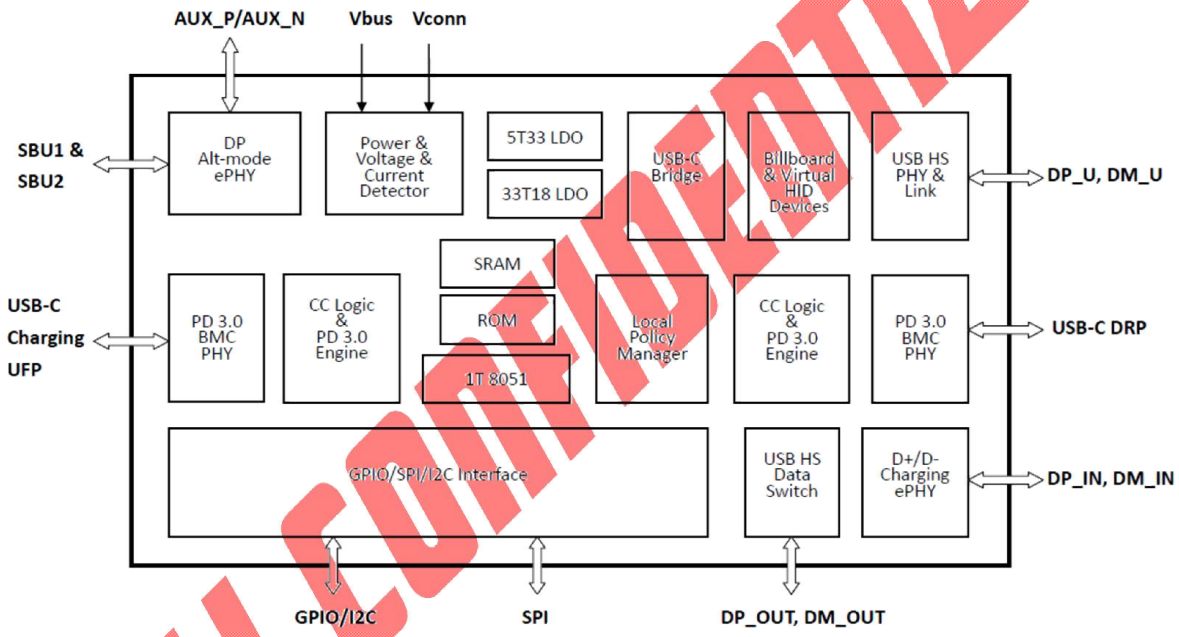

Figure 1 – VL102 Block Diagrm

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Typical Applications

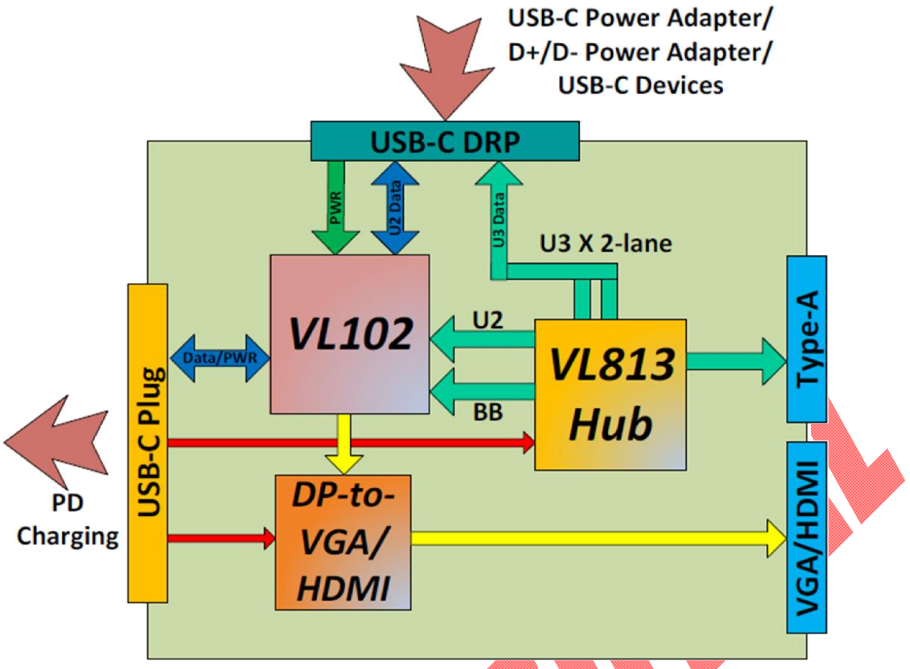

Figure 1 – VL102 USB-C Video Adapters with Hub and PD Charging-Thru

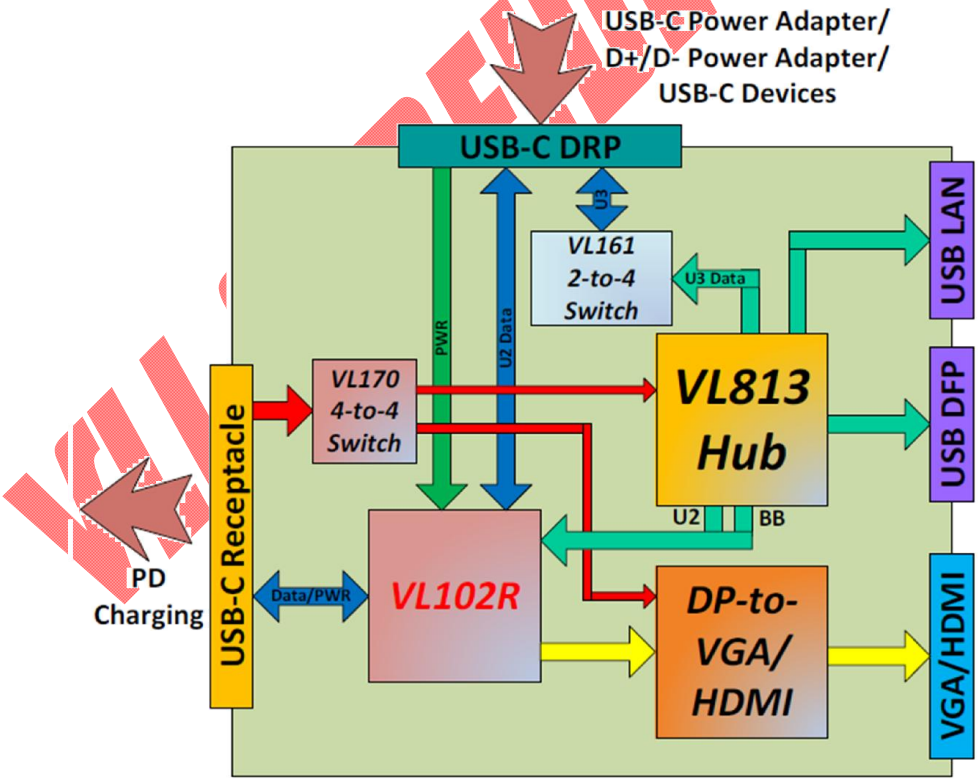

Figure 2 – VL102R USB-C Multi-function Dock

Pinout

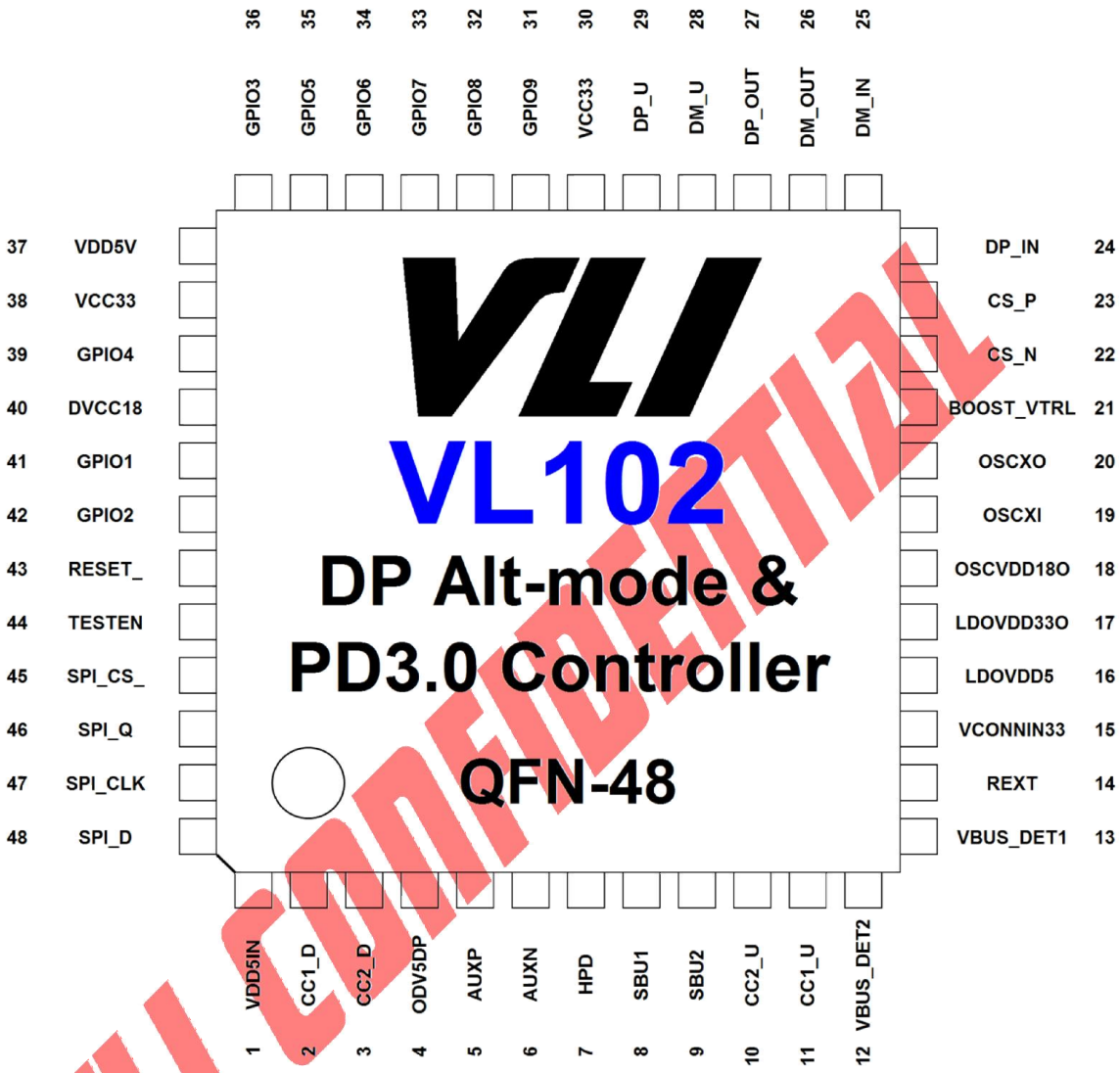

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Figure 3 – VL102 QFN-48 Pin Diagram

Pin List

Pin	Pin Name	Pin	Pin Name
1	VDD5IN	25	DM_IN
2	CC1_D	26	DM_OUT
3	CC2_D	27	DP_OUT
4	ODV5DP	28	DM_U
5	AUXP	29	DP_U
6	AUXN	30	VCC33
7	HPD	31	GPIO9
8	SBU1	32	GPIO8
9	SBU2	33	GPIO7
10	CC2_U	34	GPIO6
11	CC1_U	35	GPIO5
12	VBUS_DET2	36	GPIO3
13	VBUS_DET1	37	VDD5V
14	REXT	38	VCC33
15	VCONNIN33	39	GPIO4
16	LDOVDD5	40	DVCC18
17	LDOVDD33O	41	GPIO1
18	OSCVDD18O	42	GPIO2
19	OSCXI	43	RESET_
20	OSCXO	44	TESTEN
21	BOOST_VTRL	45	SPI_CS_
22	CS_N	46	SPI_Q
23	CS_P	47	SPI_CLK
24	DP_IN	48	SPI_D

Table 1 – VL102 QFN-48 Pin List

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Pin Descriptions

Signal Type Definition

Name	Type	Signal Description
Input	I	A standard input-only signal
Output	O	A standard active driver
Input/Output	I/O	A bi-directional signal
Analog bias	A_{BIAS}	Analog bias or reference signal. Must be tied to external resistor and/or capacitor bias network
Power	PWR	A power pin
Ground	GND	A ground pin

USB-C Interface

Pin Name	QFN48	I/O	Signal Description
CC1_U	11	I/O	Charging UFP Configuration Channel 1
CC2_U	10	I/O	Charging UFP Configuration Channel 2
CC1_D	2	I/O	DRP Port Configuration Channel 1
CC2_D	3	I/O	DRP Port Configuration Channel 2
SBU1	8	I/O	Sideband Use 1
SBU2	9	I/O	Sideband Use 2

USB Billboard Interface

Pin Name	QFN48	I/O	Signal Description
DP_U	29	I/O	D+ Data Line to USB Billboard Device
DM_U	28	I/O	D– Data Line to USB Billboard Device

USB2.0 Interface

Pin Name	QFN48	I/O	Signal Description
DP_IN	24	I/O	D+ Data Line Connect to Downstream Facing Port
DM_IN	25	I/O	D– Data Line Connect to Downstream Facing Port
DP_OUT	27	I/O	D+ Data Line Connect to Upstream Facing Port
DM_OUT	26	I/O	D– Data Line Connect to Upstream Facing Port

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DP Alt-mode Interface

Pin Name	QFN48	I/O	Signal Description
AUXP	5	I/O	DP AUX Channel Positive
AUXN	6	I/O	DP AUX Channel Negative
HPD	7	I	DP Hot Plug Detect

SPI Interface

Pin Name	QFN48	I/O	Signal Description
SPI_CS_	45	O	Serial Flash Chip Enable
SPI_D	48	O	Serial Flash Data Input
SPI_Q	46	I	Serial Flash Data Output
SPI_CLK	47	O	Serial Flash Clock

Analog Command Block

Pin Name	QFN48	I/O	Signal Description
OSCXI	19	I	24MHz Crystal Input
OSCXO	20	O	24MHz Crystal Output
REXT	14	A_{BIAS}	Connect to External Resistor (20.5K ohm, +/- 1% accuracy)
LDOVDD5	16	PWR	5V Input for 5V-to-3.3V LDO
LDOVDD33O	17	PWR	3.3V Output Pin for 5V-to-3.3V LDO
OSCVDD18O	18	PWR	Analog 1.8V Power Output
VCONNIN33	15	PWR	3.3V Vconn Power Input
VBUS_DET1	13	I	USB-C Charging UFP VBus Voltage Detector
VBUS_DET2	12	I	USB-C DRP Vbus Voltage Detector
CS_P	23	I	Current Sensing Positive Input
CS_N	22	I	Current Sensing Negative Input
BOOST_VTRL	21	I	Boost Voltage Control Input
VDD5IN	1	PWR	5V Power Input for Vconn Power Output
ODV5DP	4	O	Open-Drain IO for 5V Video Power Control

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General Purpose I/O and Miscellaneous

Pin Name	QFN48	I/O	Signal Description
RESET_	43	I	External Chip Reset
GPIO1	41	I/O	General Purpose I/O
GPIO2	42	I/O	General Purpose I/O
GPIO3	36	I/O	General Purpose I/O
GPIO4	39	I/O	General Purpose I/O
GPIO5	35	I/O	General Purpose I/O
GPIO6	34	I/O	General Purpose I/O
GPIO7	33	I/O	General Purpose I/O
GPIO8	32	I/O	General Purpose I/O
GPIO9	31	I/O	General Purpose I/O

Test Pin

Pin Name	QFN48	I/O	Signal Description
TESTEN	44	I	Test Mode Enable; Internal pull down Do not connect for normal operation.

Power and Ground

Pin Name	QFN48	I/O	Signal Description
VDD5V	37	PWR	E-fuse Power Input, Connecting to 3.3V in Normal Use
VCC33	30, 38	PWR	Digital 3.3V IO Power Input
DVCC18	40	PWR	Digital 1.8V Core Power Input

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Electrical Specification

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Note
T_{STG}	Storage Temperature	-55	125	°C	—
V_{DD33}	3.3V Power Input Voltage	-0.5	3.69	V	—
V_{DD50}	5V Power Input Voltage	-0.5	5.5	V	—
V_O	Output Voltage at any output	-0.5	VCC+ 0.5	V	—
V_{ESD}	Electrostatic Discharge	-2	2	kV	Human Body Model

Note: Stress above conditions may cause permanent damage to the device.
Functional operation of this device should be restricted to the conditions described.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
LDOVDD5	5V to 3.3V LDO 5V Power Input	4.5	5	5.5	V
VCONNIN33	3.3V Vconn power input	3.0	3.3	3.6	V
V_{CC33}	Digital IO power 3.3V	3.0	3.3	3.6	V
DV_{CC18}	Digital Core power 1.8V	1.62	1.8	1.98	V
DGND	Ground	—	0	—	V
T_A	Ambient Temperature	0		70	°C

General IO DC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Input Low Voltage	-0.30	0.8	V	—
V_{IH}	Input High Voltage	2.0	3.6	V	—
V_{OL}	Output Low Voltage	—	0.4	V	IOL=15.8mA
V_{OH}	Output High Voltage	2.4	—	V	IOH=26.5mA
I_{IL}	Input Leakage Current	—	+/-10	µA	0<VIN<VCC
I_{OZ}	Tristate Leakage Current	—	+/-10	µA	0<VOUT<VCC

Internal 3.3V to 1.8V LDO Regulator

Parameter	Min	Typ.	Max	Unit	Note
Input Voltage	3.0	3.3	3.6	V	
Output Voltage	1.71	1.8	1.89	V	
Max. Output Current			100	mA	
Output Voltage Tolerance		+/- 5%			

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Internal 5V to 3.3V LDO Regulator

Parameter	Min	Typ.	Max	Unit	Note
Input Voltage	4.5	5.0	5.5	V	
Output Voltage	3.135	3.3	3.465	V	
Max. Output Current			100	mA	
Output Voltage Tolerance		+/- 5%			

PD BMC DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
$V_{BMCSWING}$	Voltage Swing	1.05	1.2	V	—
Z_{BMCDRV}	Drive Output Resistance	33	75	Ω	—
T_{BMCR}	Rise Time	300		ns	—
T_{BMCF}	Fall Time	300		ns	—

USB Full Speed DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{FSIH}	Full-speed Input High	2.0		V	—
V_{FSIL}	Full-speed Input Low		0.8	V	—
V_{FSCM}	Differential Common Mode Voltage	0.8	2.5	V	—
V_{FSOL}	Full-speed Output Low	0.0	0.3	V	—
V_{FSOH}	Full-speed Output High	2.8	3.6	V	—
T_{FSR}	Full-speed Rise Time	4	20	ns	—
T_{FSF}	Full-speed Fall Time	4	20	ns	—
V_{FSCRS}	Full-speed Output Signal Crossover Voltage	1.3	2.0	V	—

USB High Speed DC/AC Characteristics

Symbol	Parameter	Min	Max	Unit	Note
V_{HSSQ}	High-speed squelch detection threshold	100	150	mV	—
V_{HSCM}	High-speed data signaling common mode voltage	-50	500	mV	—
V_{HSOI}	High-speed idle level	-10	10	mV	—
V_{HSOH}	High-speed data high	360	440	mV	—
V_{HSOL}	High-speed data low	-10	10	mV	—
V_{CHIRPJ}	Chirp J level	700	1100	mV	—
V_{CHIRPK}	Chirp K level	-900	-500	mV	—
Z_{HSDRV}	Drive output resistance	40.5	49.5	Ω	—
T_{HSR}	High-speed Rise Time	500		ps	—
T_{HSF}	High-speed Fall Time	500		ps	—

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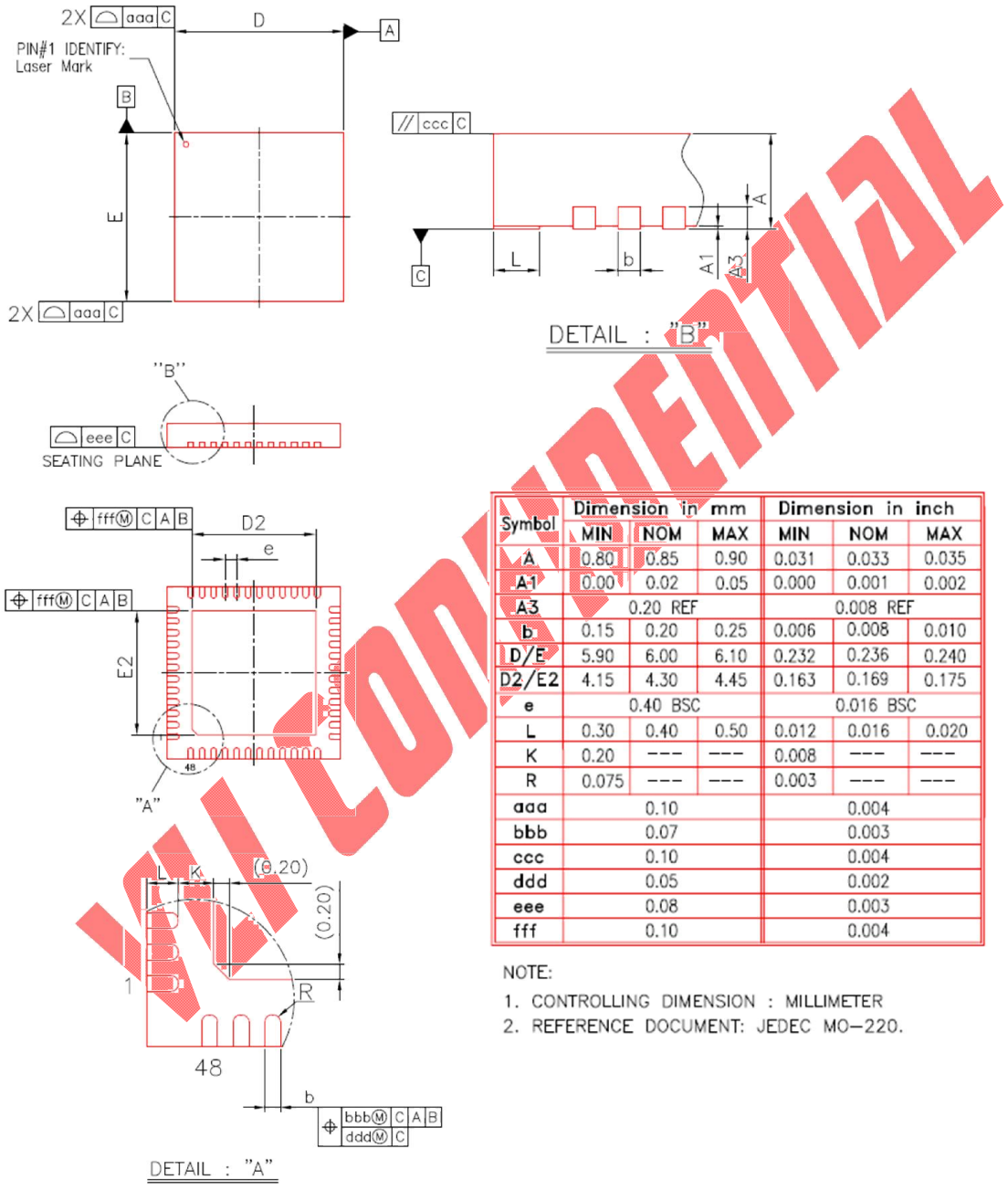
Package Mechanical Specifications

QFN-48 Pb-free Maximum Temperature for IR Reflow

Parameter	Value	Unit
Maximum Temperature Tp	250	°C
Max Time within 5°C of Tp	30	seconds



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	5.90	6.00	6.10	0.232	0.236	0.240
D2/E2	4.15	4.30	4.45	0.163	0.169	0.175
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.075	---	---	0.003	---	---
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

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Figure 4 – QFN 48L 6x6x0.85 mm Mechanical Specification

Package Top Side Marking

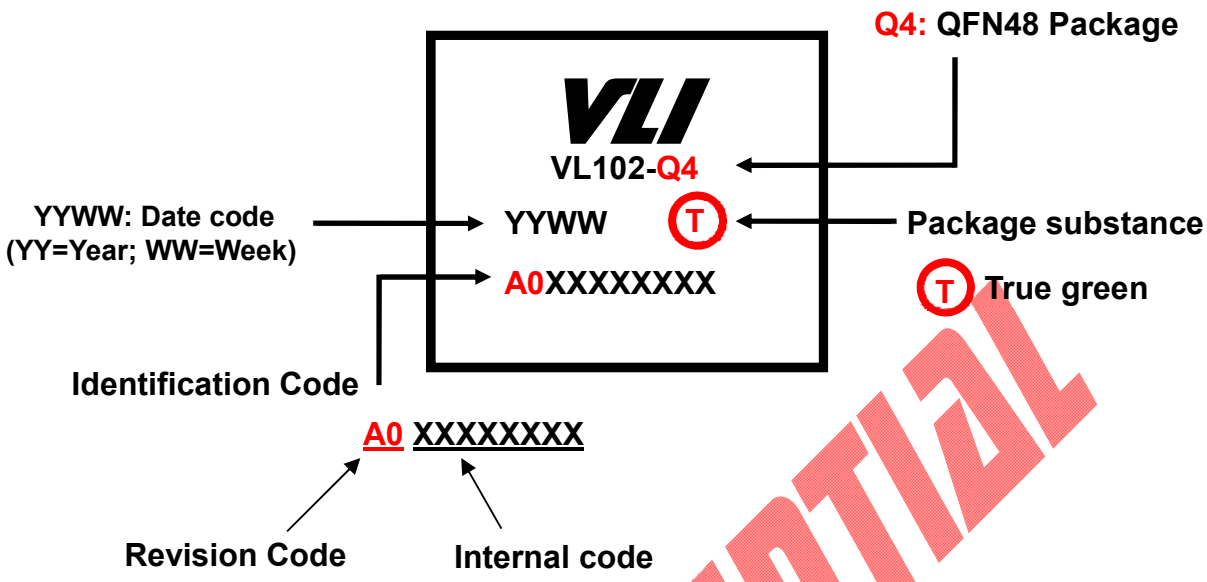

Figure 5 – VL102 Package Top Side Marking

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Ordering Information

Part Number	Description	Package
VL102-Q4	**USB-C Charging-Through w/ Captive Cable** (One charging UFP and one DRP; UFP CC2 bonding to Ra)	48-pin QFN (6x6mm)
VL102R-Q4	**USB-C Charging-Through w/ USB-C Receptacle** (One charging UFP and one DRP; UFP CC2 bonding to Rd)	48-pin QFN (6x6mm)

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