TEXAS INSTRUMENTS

TLV3201, TLV3202

SBOS561B – MARCH 2012 – REVISED DECEMBER 2016

TLV320x 40-ns, microPOWER, Push-Pull Output Comparators

1 Features

- Low Propagation Delay: 40 ns
- Low Quiescent Current: 40 µA per Channel
- Input Common-Mode Range Extends 200 mV Beyond Either Rail
- Low Input Offset Voltage: 1 mV
- Push-Pull Outputs
- Supply Range: 2.7 V to 5.5 V
- Industrial Temperature Range: –40°C to 125°C
- Small Packages: 5-Pin SC70, 5-Pin SOT-23, 8-Pin SOIC, 8-Pin VSSOP

2 Applications

- Inspection Equipment
- Test and Measurement
- High-Speed Sampling Systems
- Telecom
- Portable Communications

3 Description

The TLV3201 and TLV3202 are single- and dual-channel comparators that offer the ultimate combination of high speed (40 ns) and low-power consumption (40 µA), all in extremely small packages with features such as rail-to-rail inputs, low offset voltage (1 mV), and large output drive current. The devices are also very easy to implement in a wide variety of applications where response time is critical.

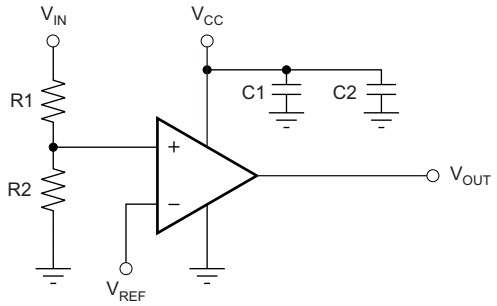
The TLV320x family is available in single (TLV3201) and dual (TLV3202) channel versions, both with push-pull outputs. The TLV3201 is available in 5-pin SOT-23 and 5-pin SC70 packages. The TLV3202 is available in 8-pin SOIC and 8-pin VSSOP packages. All devices are specified for operation across the expanded industrial temperature range of –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV3201	SOT-23 (5)	2.90 mm × 1.60 mm
	SC70 (5)	2.00 mm × 1.25 mm
TLV3202	VSSOP (8)	3.00 mm × 3.00 mm
	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Threshold Detector



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2012) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table; see *Package Option Addendum* at the end of the data sheet ... 1

Changes from Original (March 2012) to Revision A **Page**

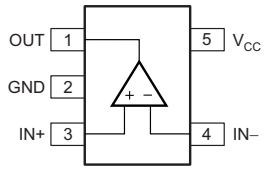
- Changed product status from Production Data to Mixed Status ... 1
- Added dual channel device ... 1

5 Device Comparison Table

DEVICE	DESCRIPTION
TLV3011	5-µA (maximum) open-drain, 1.8-V to 5.5-V with integrated voltage reference in 1.5-mm × 1.5-mm micro-sized packages
TLV3012	5-µA (maximum) push-pull, 1.8-V to 5.5-V with integrated voltage reference in micro-sized packages
TLV3501	4.5-ns, rail-to-rail, push-pull comparator in micro-sized packages
LMV7235	75-ns, 65-µA, 2.7-V to 5.5-V, rail-to-rail input comparator with open-drain output
REF3333	30-ppm/°C drift, 3.9-µA, SOT23-3, SC70-3 voltage reference

6 Pin Configuration and Functions

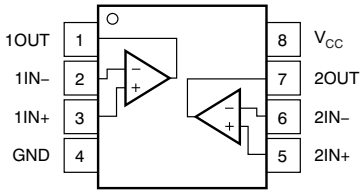
TLV3201 DCK and DBV Packages
5-Pin SC70-5 and SOT-23
Top View



Pin Functions: TLV3201

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	—	Negative supply, ground
IN–	4	I	Negative input
IN+	3	I	Positive input
OUT	1	O	Output
V_{CC}	5	—	Positive supply

TLV3202 D and DGK Packages
8-Pin SOIC and VSSOP
Top View



Pin Functions: TLV3202

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Negative input, comparator 1
1IN+	3	I	Positive input, comparator 1
1OUT	1	O	Output, comparator 1
2IN–	6	I	Negative input, comparator 2
2IN+	5	I	Positive input, comparator 2
2OUT	7	O	Output, comparator 2
GND	4	—	Negative supply, ground
V_{CC}	8	—	Positive supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage		7	V
	Signal input pins(2)	–0.5	(V_{CC}) + 0.5	
Current	Signal input pins(2)	–10	10	mA
	Output short circuit(3)		100	
Temperature	Operating	–55	125	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	TLV3201	±2000	
		TLV3202	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V_{S+}) – ($V_{S–}$)	2.7 (±1.35)	5.5 (±2.75)	V
	Specified temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TLV3201		TLV3202		UNIT
		DBV (SOT-23)	DCK (SC70)	DGK (VSSOP)	D (SOIC)	
		5 PINS	5 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	237.8	281.9	146.3	201.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	108.7	97.6	97.2	92.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.1	68.3	84.2	123.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.1	2.6	45.5	23	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.3	67.3	83.7	212.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics: V_{CC} = 5 V

at T_A = 25°C and V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{IO}	Input offset voltage	$V_{CM} = V_{CC} / 2$		1	5	mV
		T_A = –40°C to 125°C			6	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C		1	10	µV/°C
PSRR	Power-supply rejection ratio	$V_{CM} = V_{CC} / 2$, V_{CC} = 2.5 V to 5.5 V	65	85		dB
	Input hysteresis			1.2		mV
INPUT BIAS CURRENT						
I_{IB}	Input bias current	$V_{CM} = V_{CC} / 2$		1	50	pA
		T_A = –40°C to 125°C			5	nA
I_{IO}	Input offset current	$V_{CM} = V_{CC} / 2$		1	50	pA
		T_A = –40°C to 125°C			2.5	nA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage	T_A = –40°C to 125°C	(V_{EE}) – 0.2		(V_{CC}) + 0.2	V
CMRR	Common-mode rejection ratio	–0.2 V < V_{CM} < 5.2 V	60	70		dB
INPUT IMPEDANCE						
	Common mode			10^{13} || 2		Ω || pF
	Differential			10^{13} || 4		Ω || pF
OUTPUT						
V_{OL}	Voltage output swing from lower rail	I_{SINK} = 4 mA		175	190	mV
		T_A = –40°C to 125°C			225	
V_{OH}	Voltage output swing from upper rail	I_{SOURCE} = 4 mA		120	140	mV
		T_A = –40°C to 125°C			170	
I_{SC}	Short-circuit current (per comparator)	I_{SC} sinking	40	48		mA
		T_A = –40°C to 125°C	See Figure 14			
		I_{SC} sourcing	52	60		
		T_A = –40°C to 125°C	See Figure 14			
POWER SUPPLY						
V_{CC}	Specified voltage		2.7		5.5	V
I_Q	Quiescent current	T_A = 25°C		40	50	µA
		T_A = –40°C to 125°C			65	

7.6 Electrical Characteristics: V_{CC} = 2.7 V

at T_A = 25°C and V_{CC} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{IO}	Input offset voltage	$V_{CM} = V_{CC} / 2$		1	5	mV
		T_A = –40°C to 125°C			6	
dV_{OS}/dT	Input offset voltage drift	T_A = –40°C to 125°C		1	10	µV/°C
PSRR	Power-supply rejection ratio	$V_{CM} = V_{CC} / 2$, V_{CC} = 2.5 V to 5.5 V	65	85		dB
	Input hysteresis			1.2		mV
INPUT BIAS CURRENT						
I_{IB}	Input bias current	$V_{CM} = V_{CC} / 2$		1	50	pA
		T_A = –40°C to 125°C			5	nA
I_{IO}	Input offset current	$V_{CM} = V_{CC} / 2$		1	50	pA
		T_A = –40°C to 125°C			2.5	nA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage	T_A = –40°C to 125°C	(V_{EE}) – 0.2		(V_{CC}) + 0.2	V
CMRR	Common-mode rejection ratio	–0.2 V < V_{CM} < 2.9 V	56	68		dB

Electrical Characteristics: V_{CC} = 2.7 V (continued)

at T_A = 25°C and V_{CC} = 2.7 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT IMPEDANCE						
	Common mode			10^{13} || 2		Ω || pF
	Differential			10^{13} || 4		Ω || pF
OUTPUT						
V_{OL}	Voltage output swing from lower rail	I_{SINK} = 4 mA		230	260	mV
		T_A = –40°C to 125°C			325	
V_{OH}	Voltage output swing from upper rail	I_{SOURCE} = 4 mA		210	250	mV
		T_A = –40°C to 125°C			350	
I_{SC}	Short-circuit current (per comparator)	I_{SC} sinking	13	19		mA
		T_A = –40°C to 125°C	See Figure 14			
		I_{SC} sourcing	15	21		
		T_A = –40°C to 125°C	See Figure 14			
POWER SUPPLY						
V_{CC}	Specified voltage		2.7		5.5	V
I_Q	Quiescent current	T_A = 25°C		36	46	µA
		T_A = –40°C to 125°C			60	

7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PD}	Propagation delay time	Low to high	Input overdrive = 20 mV, C_L = 15 pF		47	50	ns
			Input overdrive = 100 mV, C_L = 15 pF		42	50	
			T_A = –40°C to 125°C			55	
		High to low	Input overdrive = 20 mV, C_L = 15 pF		40	50	
			Input overdrive = 100 mV, C_L = 15 pF		38	50	
			T_A = –40°C to 125°C			55	
	Propagation delay skew	Input overdrive = 20 mV, C_L = 15 pF			2		ns
	Propagation delay matching (TLV3202)	High to low or low to high, input overdrive = 20 mV, C_L = 15 pF				5	ns
t_R	Rise time	10% to 90%			4.8		ns
t_F	Fall time	10% to 90%			5.2		ns

7.8 Typical Characteristics

at T_A = 25°C, V_{CC} = 5 V, and input overdrive (V_{OD}) = 20 mV (unless otherwise noted)

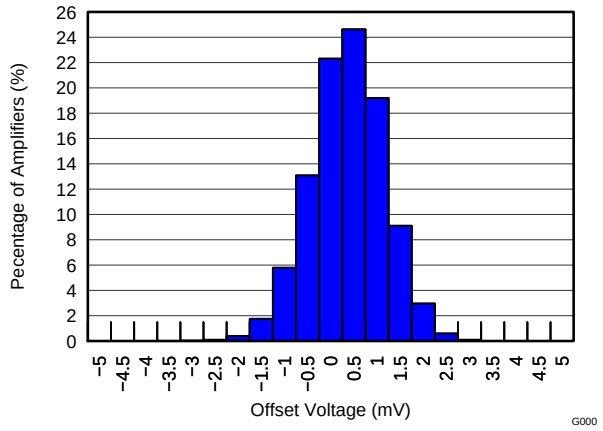


Figure 1. Offset Voltage Distribution

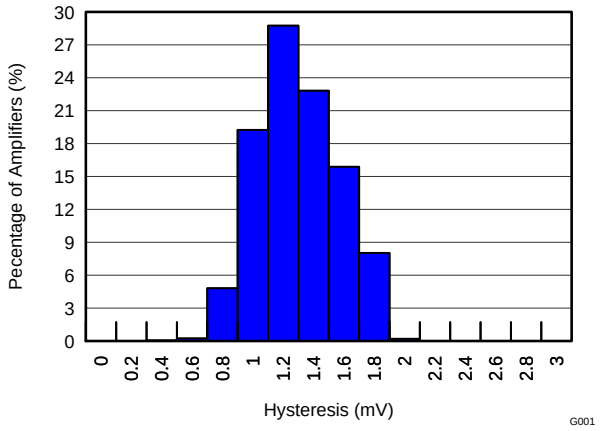


Figure 2. Hysteresis Distribution

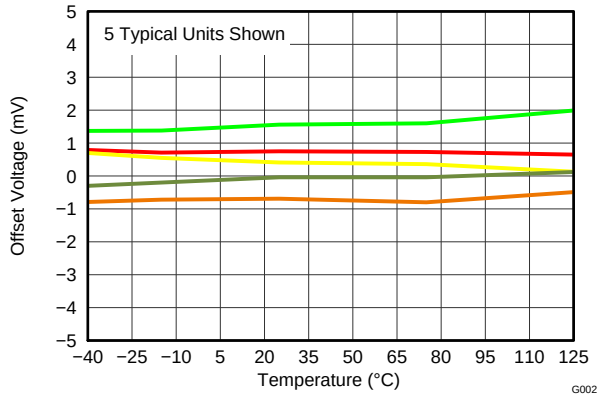


Figure 3. Offset Voltage vs Temperature

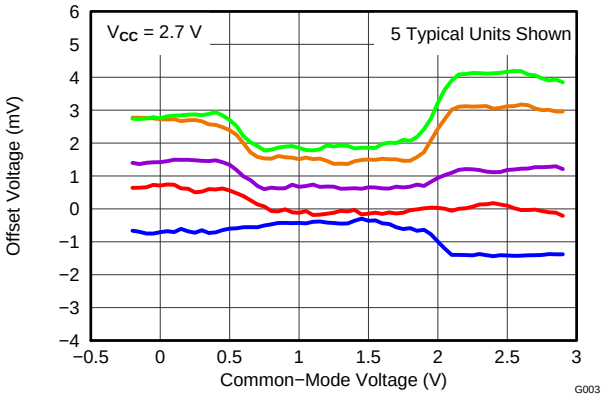


Figure 4. Offset Voltage vs Common-Mode Voltage

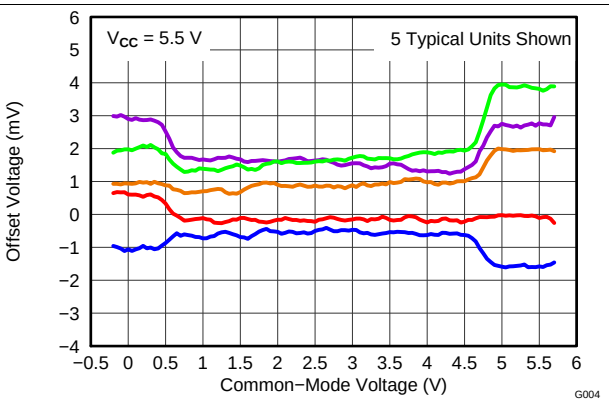


Figure 5. Offset Voltage vs Common-Mode Voltage

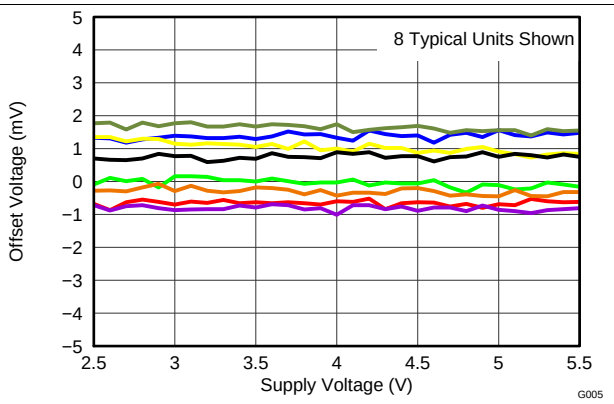


Figure 6. Offset Voltage vs Power Supply

Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 5 V, and input overdrive (V_{OD}) = 20 mV (unless otherwise noted)

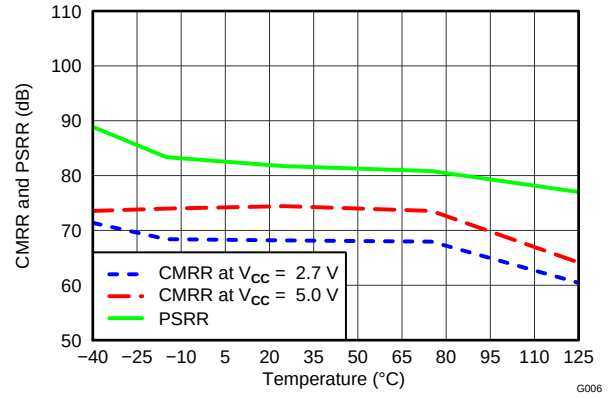


Figure 7. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Temperature

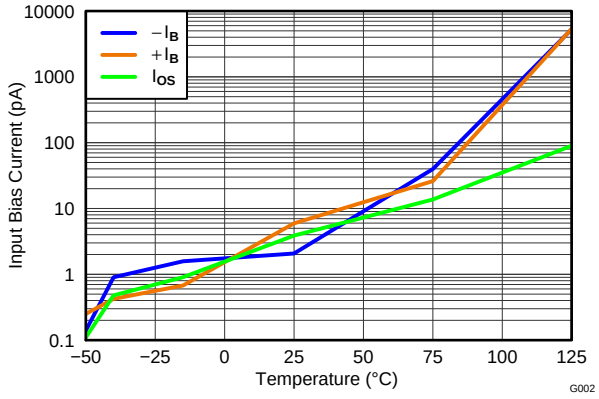


Figure 8. Input Bias Current and Input Offset Current vs Temperature

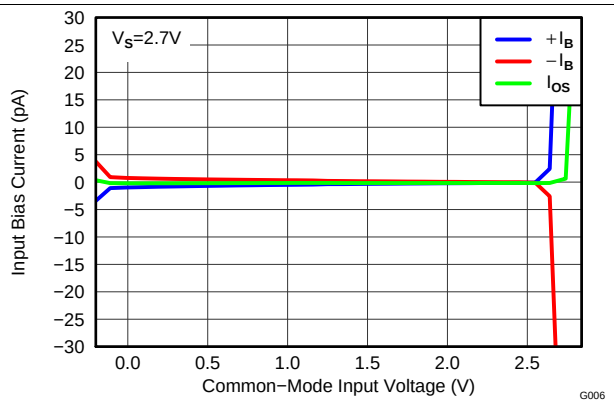


Figure 9. Input Bias Current and Input Offset Current vs Common-Mode Input Voltage

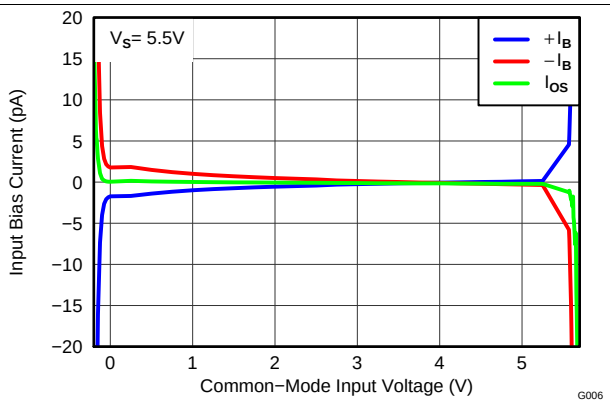


Figure 10. Input Bias Current and Input Offset Current vs Common-Mode Input Voltage

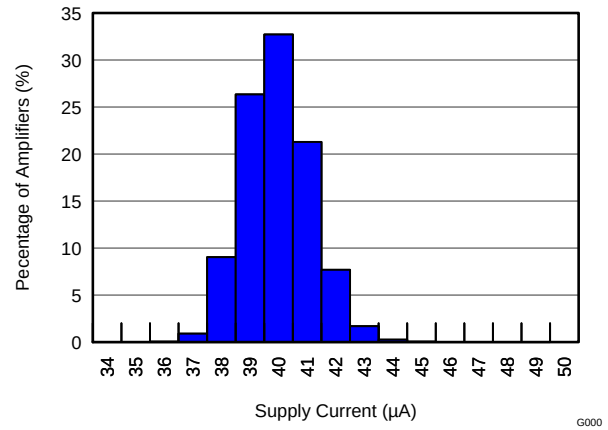


Figure 11. Quiescent Current Distribution

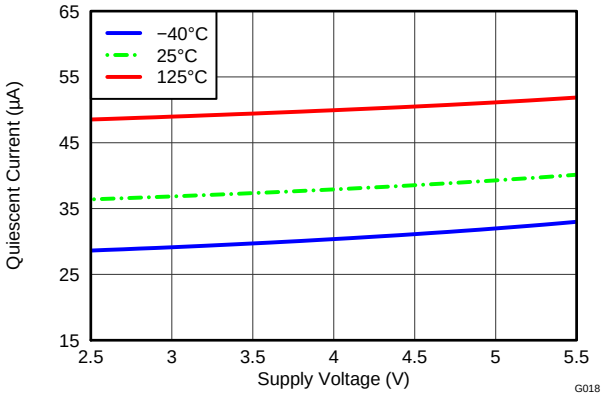


Figure 12. Quiescent Current vs Supply Voltage

Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 5 V, and input overdrive (V_{OD}) = 20 mV (unless otherwise noted)

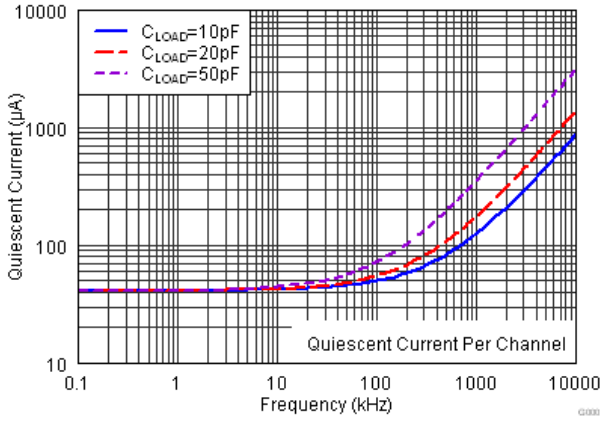


Figure 13. Quiescent Current vs Switching Frequency

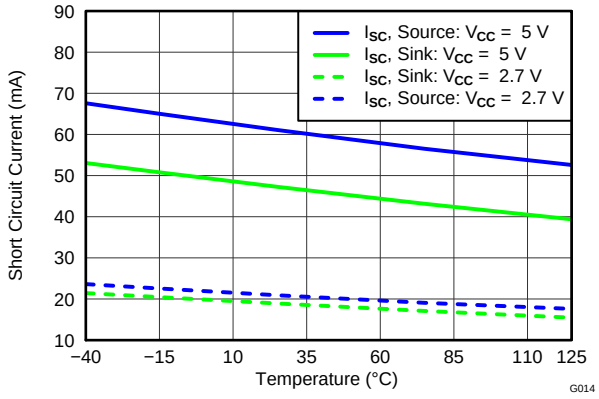


Figure 14. Short-Circuit Current vs Temperature

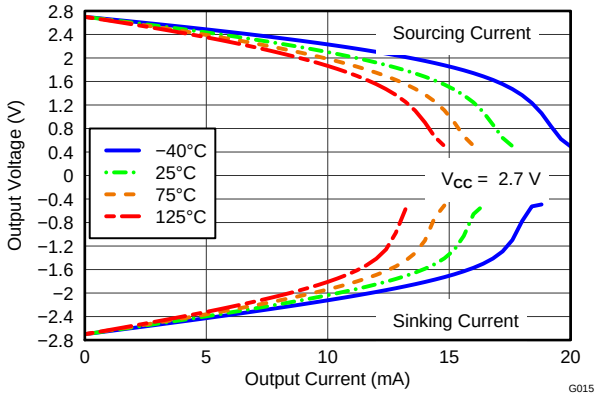


Figure 15. Output Voltage vs Output Current

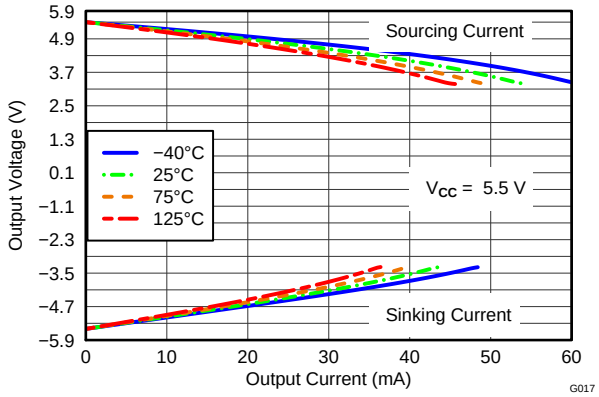


Figure 16. Output Voltage vs Output Current

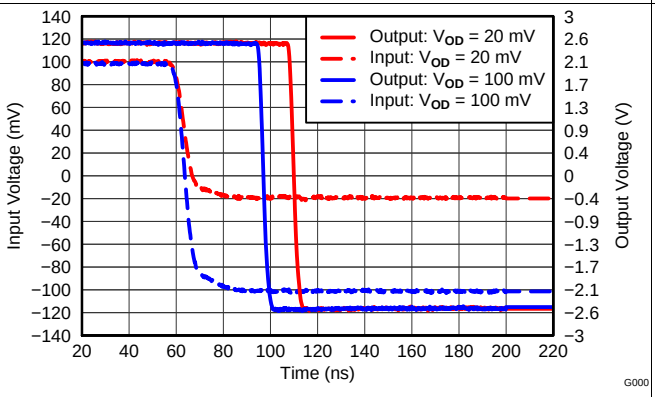


Figure 17. Propagation Delay Falling Edge

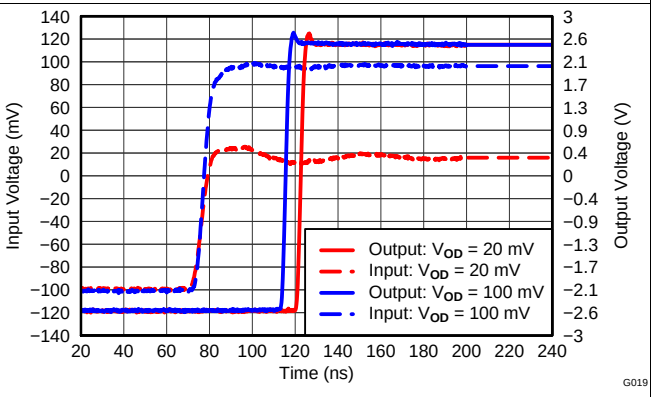


Figure 18. Propagation Delay Rising Edge

Typical Characteristics (continued)

at T_A = 25°C, V_{CC} = 5 V, and input overdrive (V_{OD}) = 20 mV (unless otherwise noted)

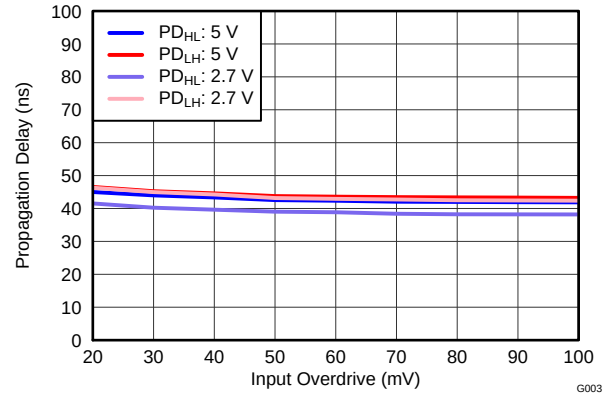


Figure 19. Propagation Delay vs Input Overdrive

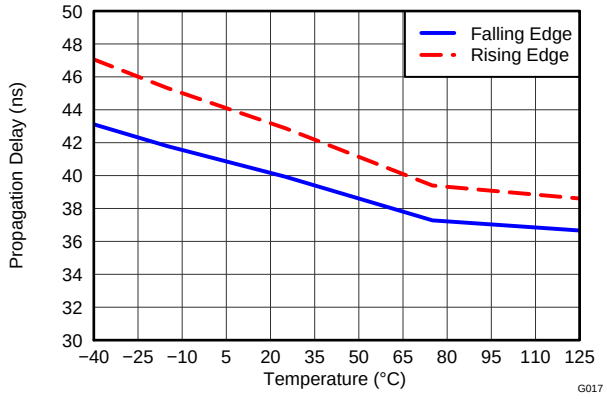


Figure 20. Propagation Delay vs Temperature

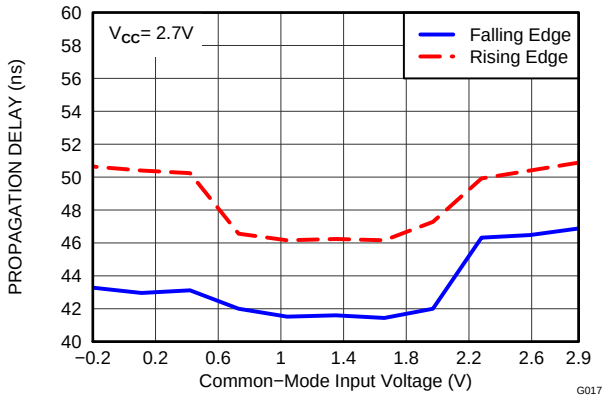


Figure 21. Propagation Delay vs Common-Mode Voltage

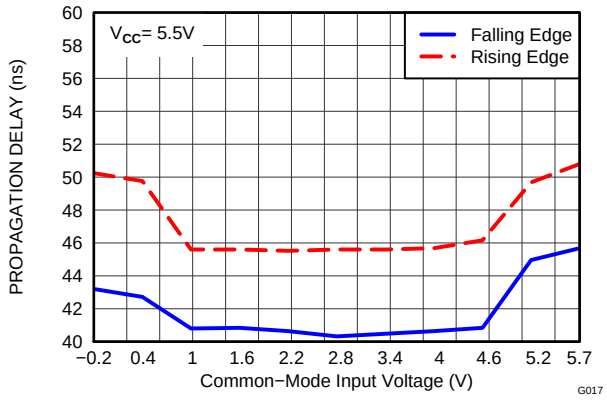


Figure 22. Propagation Delay vs Common-Mode Voltage

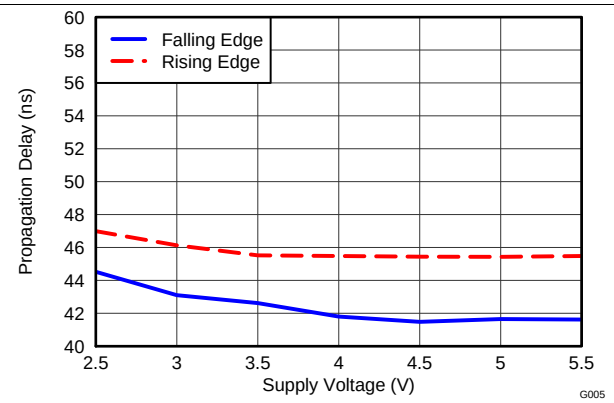


Figure 23. Propagation Delay vs Supply Voltage

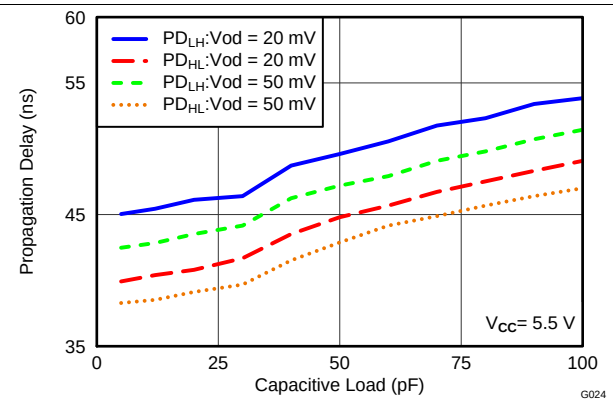


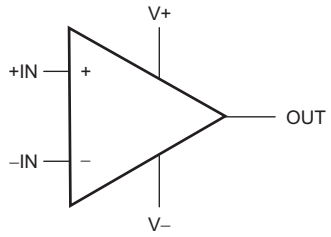
Figure 24. Propagation Delay vs Capacitive Load

8 Detailed Description

8.1 Overview

The TLV3201 and TLV3202 devices feature 40-ns response time, and include 1.2 mV of internal hysteresis for improved noise immunity with an input common-mode range that extends 0.2 V beyond the power-supply rails.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The TLV3201 and TLV3202 comparators are specified for use on a single supply from 2.7 V to 5.5 V (or a dual supply from ±1.35 V to ±2.75 V) over a temperature range of −40°C to 125°C. The device continues to function below this range, but performance is not specified.

8.3.2 Input Overvoltage Protection

The device inputs are protected by electrostatic discharge (ESD) diodes that conduct if the input voltages exceed the power supplies by more than approximately 300 mV. Momentary voltages greater than 300 mV beyond the power supply can be tolerated if the input current is limited to 10 mA. This limiting is easily accomplished with a small input resistor in series with the input to the comparator.

8.4 Device Functional Modes

The device is fully functional when powered by rail-to-rail supply voltage greater than 2.7 V. The device is off at any voltages below 2.7 V.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV3201 and TLV3202 are single- and dual-supply (respectively), push-pull comparators featuring 40 ns of propagation delay on only 40 µA of supply current. This combination of fast response time and minimal power consumption make the TLV3201 and TLV3202 excellent comparators for portable, battery-powered applications as well as fast-switching threshold detection such as pulse-width modulation (PWM) output monitors and zero-cross detection.

9.1.1 Comparator Inputs

The TLV3201 and TLV3202 are rail-to-rail input comparators, with an input common-mode range that exceeds the supply rails by 200 mV for both positive and negative supplies. The devices are specified from 2.7 V to 5.5 V, with room temperature operation from 2.5 V to 5.5 V. The TLV3201 and TLV3202 are designed to prevent phase inversion when the input pins exceed the supply voltage. Figure 25 shows the TLV320x response when input voltages exceed the supply, resulting in no phase inversion.

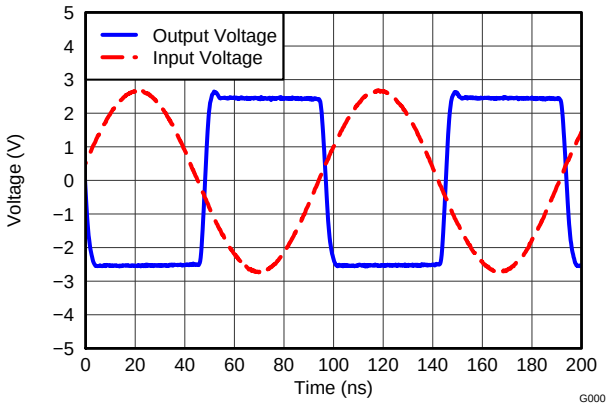


Figure 25. No Phase Inversion: Comparator Response to Input Voltage (Propagation Delay Included)

The electrostatic discharge (ESD) protection input structure of two back-to-back diodes and 1-kΩ series resistors are used to limit the differential input voltage applied to the precision input of the comparator by clamping input voltages that exceed V_{CC} beyond the specified operating conditions. If potential overvoltage conditions that exceed absolute maximum ratings are present, the addition of external bypass diodes and resistors is recommended, as shown in Figure 26. Large differential voltages greater than the supply voltage must be avoided to prevent damage to the input stage.

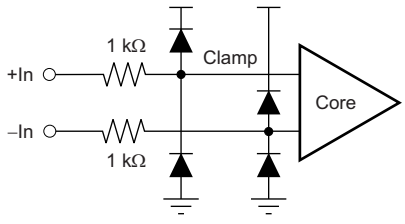


Figure 26. TLV3201 Equivalent Input structure

Application Information (continued)

9.1.2 External Hysteresis

The TLV3201 and TLV3202 have a hysteresis transfer curve (shown in Figure 27) that is a function of three components: V_{TH}, V_{OS}, and V_{HYST}.

- V_{TH}: the actual set voltage or threshold trip voltage
- V_{OS}: the internal offset voltage between V_{IN+} and $V_{IN–}$. This voltage is added to V_{TH} to form the actual trip point at which the comparator must respond to change output states.
- V_{HYST}: internal hysteresis (or trip window) that is designed to reduce comparator sensitivity to noise.

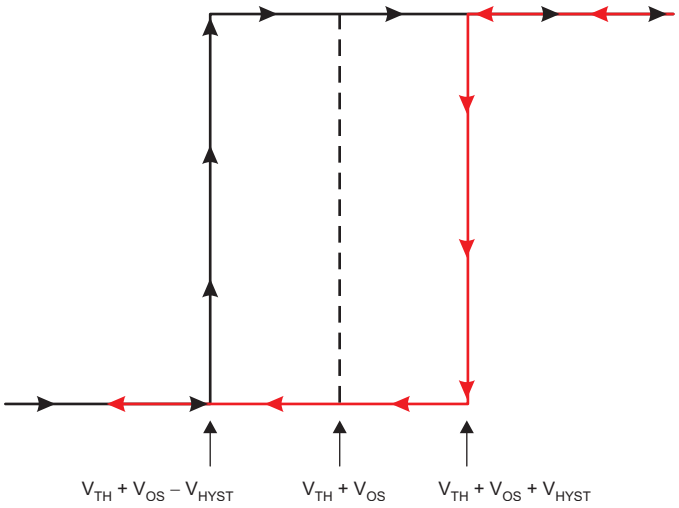


Figure 27. TLV320x Hysteresis Transfer Curve

9.1.2.1 Inverting Comparator with Hysteresis

The inverting comparator with hysteresis requires a three-resistor network that is referenced to the comparator supply voltage (V_{CC}), as shown in Figure 28. When V_{IN} at the inverting input is less than V_A, the output voltage is high (for simplicity, assume V_O switches as high as V_{CC}). The three network resistors can be represented as R1 || R3 in series with R2. The lower input trip voltage (V_{A1}) is defined by Equation 1.

$$V_{A1} = V_{CC} \times \frac{R2}{(R1 \parallel R3) + R2} \tag{1}$$

When V_{IN} is greater than [V_A × (V_{IN} > V_A)], the output voltage is low, very close to ground. In this case, the three network resistors can be presented as R2 || R3 in series with R1. The upper trip voltage (V_{A2}) is defined by Equation 2.

$$V_{A2} = V_{CC} \times \frac{R2 \parallel R3}{R1 + (R2 \parallel R3)} \tag{2}$$

The total hysteresis provided by the network is defined by Equation 3.

$$\Delta V_A = V_{A1} - V_{A2} \tag{3}$$

Application Information (continued)

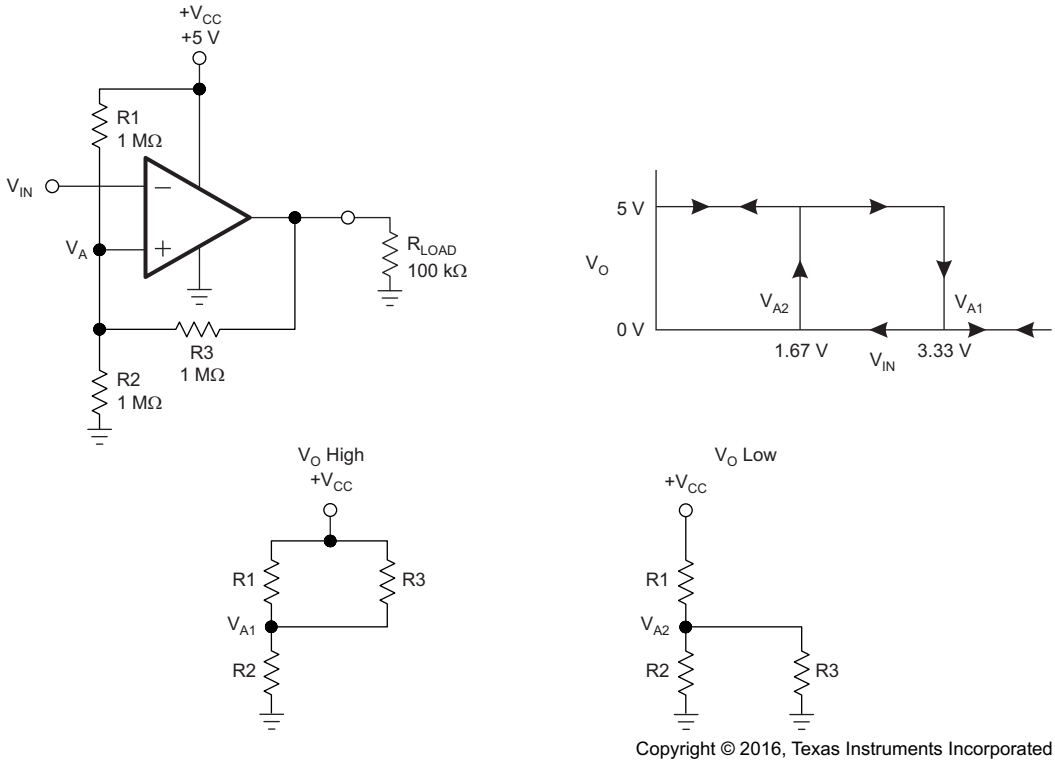


Figure 28. TLV3201 in Inverting Configuration With Hysteresis

9.1.2.2 Noninverting Comparator With Hysteresis

A noninverting comparator with hysteresis requires a two-resistor network, as shown in Figure 29, and a voltage reference (V_{REF}) at the inverting input. When V_{IN} is low, the output is also low. For the output to switch from low to high, V_{IN} must rise up to V_{IN1}. V_{IN1} is calculated by Equation 4.

$$V_{IN1} = R1 \times \frac{V_{REF}}{R2} \times V_{REF} \tag{4}$$

When V_{IN} is high, the output is also high. In order for the comparator to switch back to a low state, V_{IN} must equal V_{REF} before V_A is again equal to V_{REF}. V_{IN} can be calculated by Equation 5.

$$V_{IN2} = \frac{V_{REF}\,(R1 + R2) - V_{CC} \times R1}{R2} \tag{5}$$

The hysteresis of this circuit is the difference between V_{IN1} and V_{IN2}, as defined by Equation 6.

$$\Delta V_{IN} = V_{CC} \times \frac{R1}{R2} \tag{6}$$

Application Information (continued)

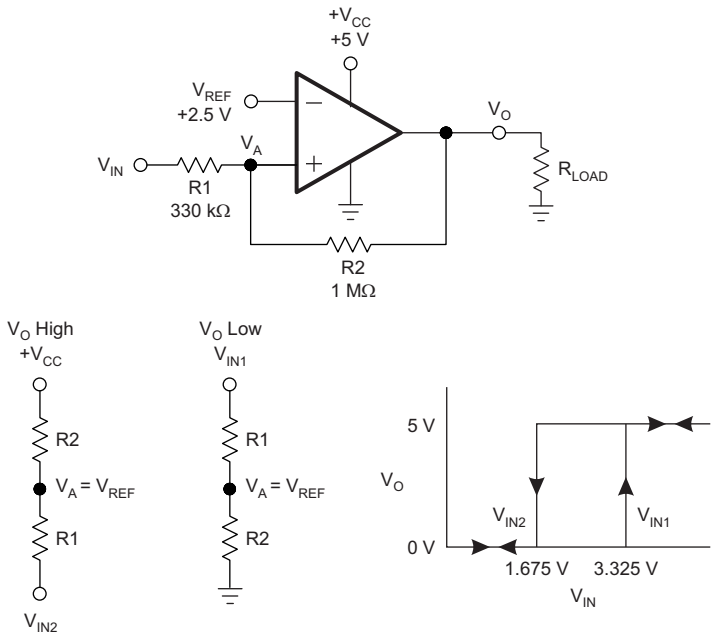


Figure 29. TLV3201 in Noninverting Configuration With Hysteresis

9.1.3 Capacitive Loads

The TLV3201 and TLV3202 feature a push-pull output. When the output switches, there is a direct path between V_{CC} and ground, causing increased output sinking or sourcing current during the transition. Following the transition the output current decreases and supply current returns to 40 µA, thus maintaining low power consumption. Under reasonable capacitive loads, the TLV3201 and TLV3202 maintain specified propagation delay (see *Typical Characteristics*), but excessive capacitive loading under high switching frequencies may increase supply current, propagation delay, or induce decreased slew rate.

9.2 Typical Applications

9.2.1 TLV3201 Configured as an AC-Coupled Comparator

One of the benefits of AC coupling a single-supply comparator circuit is that it can block dc offsets induced by ground-loop offsets that could potentially produce either a false trip or a common-mode input violation. Figure 30 shows the TLV3201 configured as an ac-coupled comparator.

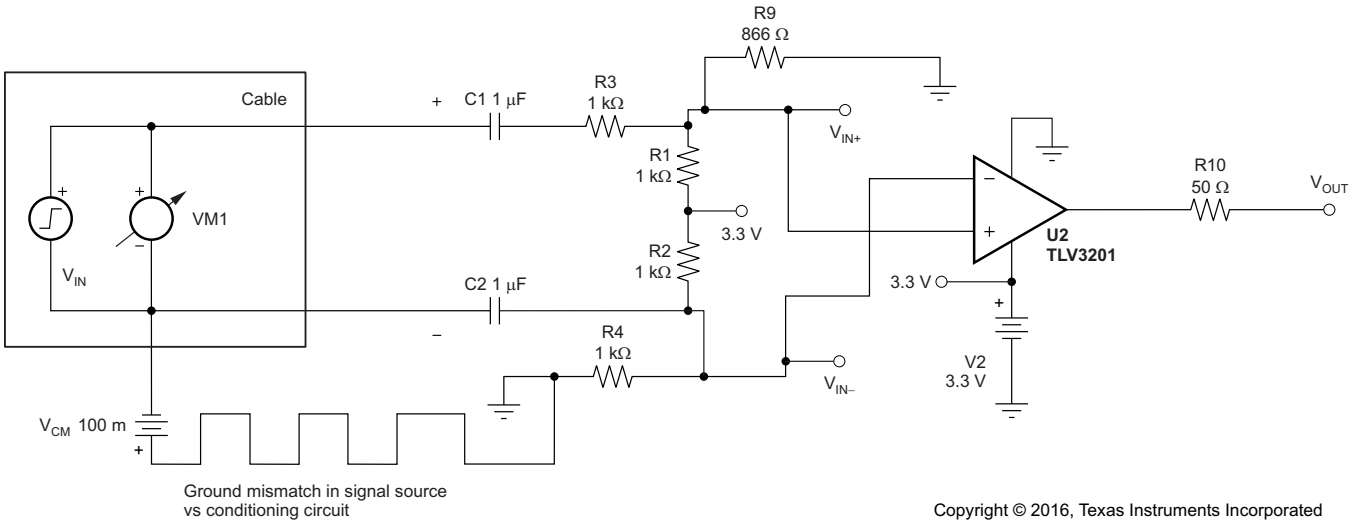


Figure 30. TLV3201 Configured as an AC-Coupled Comparator (Schematic)

9.2.1.1 Design Requirements

Design requirements include:

- Ability to tolerate up to ±100 mV of common-mode signal.
- Trigger only on AC signals (such as zero-cross detection).

9.2.1.2 Detailed Design Procedure

Design analysis:

- AC-coupled, high-pass frequency
- Large capacitors require longer start-up time from device power on
- Use 1-µF capacitor to achieve high-pass frequency of approximately 159 Hz
- For high-pass equivalent, use C_{IN} = 0.5 µF, R_{IN} = 2 kΩ

1. Set up input dividers initially for one-half supply (to be in center of acceptable common-mode range).
2. Adjust either divider slightly upwards or downwards as desired to establish quiescent output condition.
3. Select coupling capacitors based on lowest expected frequency.

Typical Applications (continued)

9.2.1.3 Application Curve

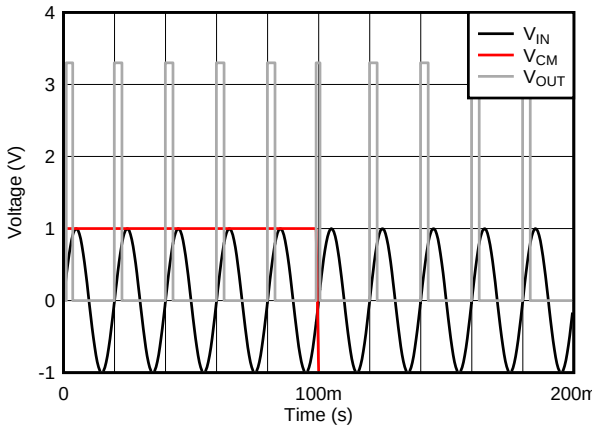


Figure 31. AC-Coupled Comparator Results

9.2.2 TLV3201 and OPA320 Configured as a Fast-Response Output Current Monitor

Figure 32 shows a single-supply current monitor configured as a difference amplifier with a gain of 50. The OPA320 was chosen for this circuit because of its gain bandwidth (20 MHz), which allows higher speed triggering and monitoring of the current across the shunt resistor followed by the fast response of the TLV3201.

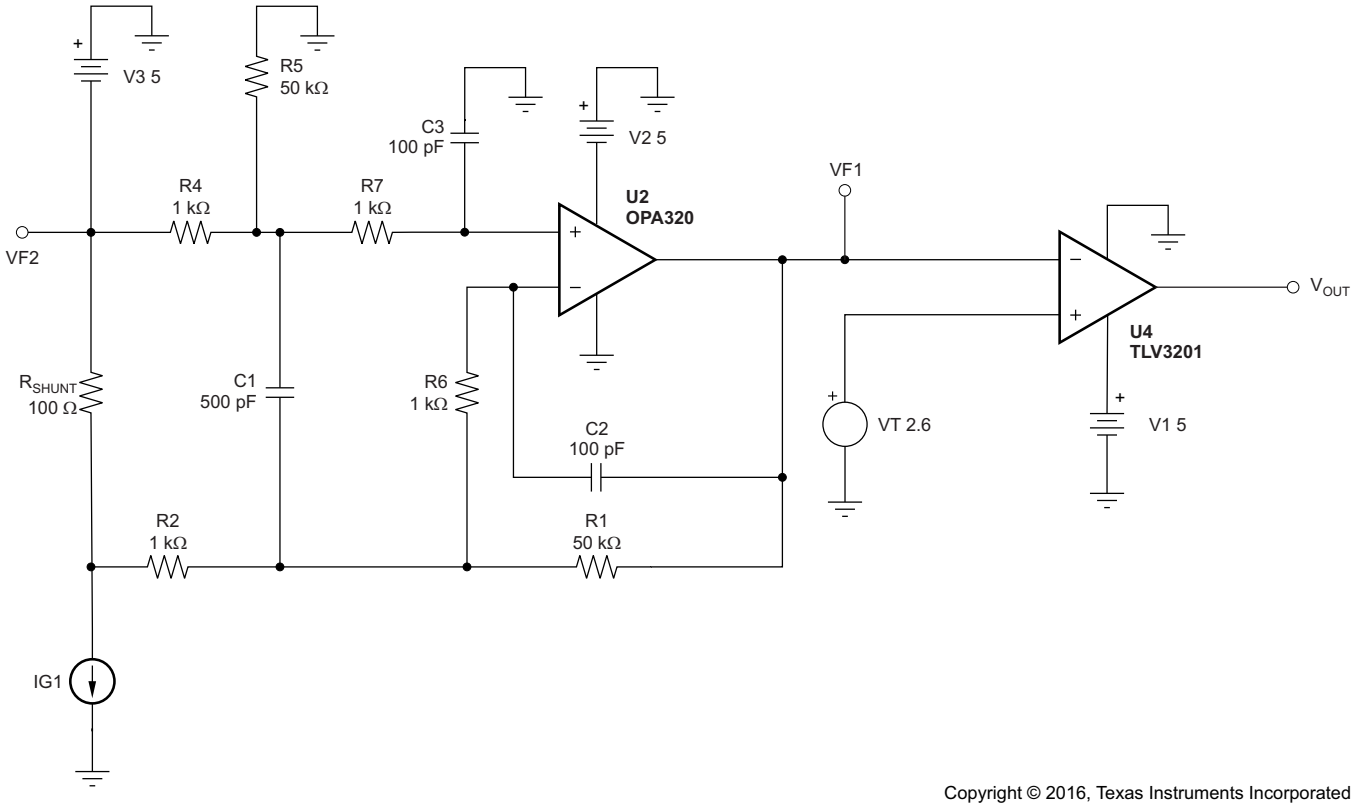


Figure 32. TLV3201 and OPA320 Configured as a Fast-Response Output Current Monitor

Typical Applications (continued)

9.2.3 TLV3201 and TMP20 Configured as a Precision Analog Temperature Switch

Figure 33 shows the TMP20 and TLV3201 designed as a high-speed temperature switch. The TMP20 is an analog output temperature sensor where output voltage decreases with temperature. The comparator output is tripped when the output reaches a critical trip threshold.

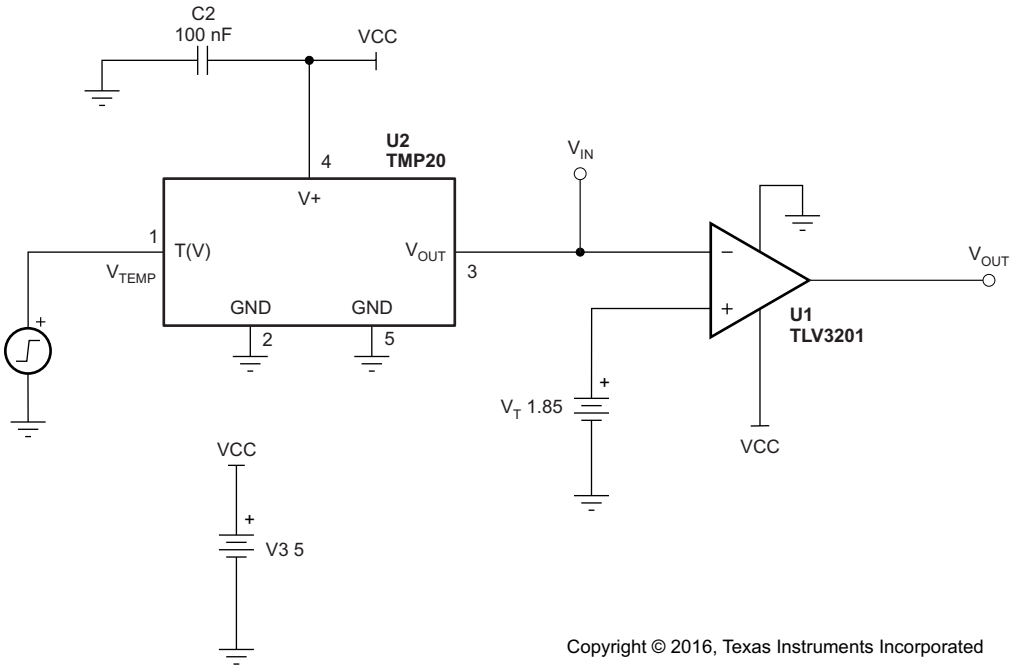


Figure 33. TLV3201 and TMP20 Configured as a Precision Analog Temperature Switch

10 Power Supply Recommendations

The TLV3201 and TLV3202 comparators are specified for use on a single supply from 2.7 V to 5.5 V (or a dual supply from ±1.35 V to ±2.75 V) over a temperature range of −40°C to 125°C. The device continues to function below this range, but performance is not specified. Place bypass capacitors close to the power-supply pins to reduce noise coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout Guidelines*.

11 Layout

11.1 Layout Guidelines

The TLV3201 and TLV3202 are fast-switching, high-speed comparators and require high-speed layout considerations. For best results, maintain the following layout guidelines.

- Use a printed-circuit board (PCB) with a good, unbroken low-inductance ground plane.
- Place a decoupling capacitor (0.1-µF ceramic, surface-mount capacitor) as close as possible to V_{CC}.
- On the inputs and the output, keep lead lengths as short as possible to avoid unwanted parasitic feedback around the comparator. Keep inputs away from the output.
- Solder the device directly to the PCB rather than using a socket.
- For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000 pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes some degradation to propagation delay when the impedance is low. The topside ground plane runs between the output and inputs.
- The ground pin ground trace runs under the device up to the bypass capacitor, shielding the inputs from the outputs.

11.2 Layout Example

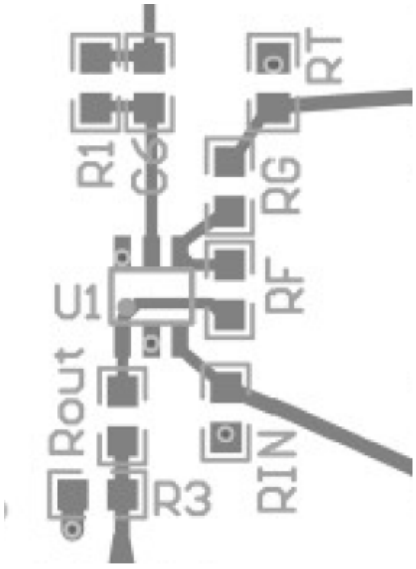


Figure 34. TLV320x Board Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 TINA-TI™ (Free Software Download)

TINA-TI™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

12.1.1.2 Universal Op Amp EVM

The Universal Op Amp EVM is a series of general-purpose, blank circuit boards that simplify prototyping circuits for a variety of IC package types. The evaluation module board design allows many different circuits to be constructed easily and quickly. Five models are offered, with each model intended for a specific package type. PDIP, SOIC, MSOP, TSSOP and SOT23 packages are all supported.

NOTE

These boards are unpopulated, so users must provide their own ICs. TI recommends requesting several op amp device samples when ordering the Universal Op Amp EVM.

12.1.1.3 TI Precision Designs

TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits. TI Precision Designs are available online at http://www.ti.com/ww/en/analog/precision-designs/.

12.1.1.4 WEBENCH® Filter Designer

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web-based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

12.2 Documentation Support

12.2.1 Related Documentation

The following documents are relevant to using the TLV320x, and recommended for reference. All are available for download at www.ti.com unless otherwise noted.

- *Frequency Dithering With the UCC28950 and TLV3201* (SLUA646)
- *Frequency Dithering with the UCC28180 and TLV3201* (SLUA704)
- *Comparator with Hysteresis Reference Design* (TIDU020)

12.3 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV3201	Click here	Click here	Click here	Click here	Click here
TLV3202	Click here	Click here	Click here	Click here	Click here

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
DesignSoft is a trademark of DesignSoft, Inc.
TINA-TI is a trademark of Texas Insturments and DesignSoft, Inc..
All other trademarks are the property of their respective owners.

12.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3201AIDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAI	Samples
TLV3201AIDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAI	Samples
TLV3201AIDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SDP	Samples
TLV3201AIDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SDP	Samples
TLV3202AID	ACTIVE	SOIC	D	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3202	Samples
TLV3202AIDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VUDC	Samples
TLV3202AIDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	VUDC	Samples
TLV3202AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL3202	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

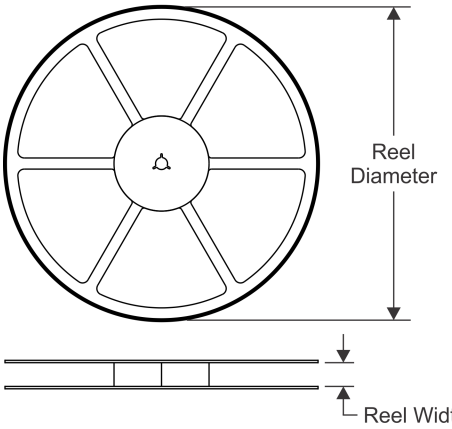
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

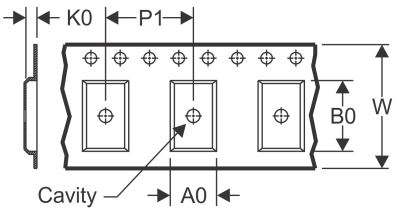
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

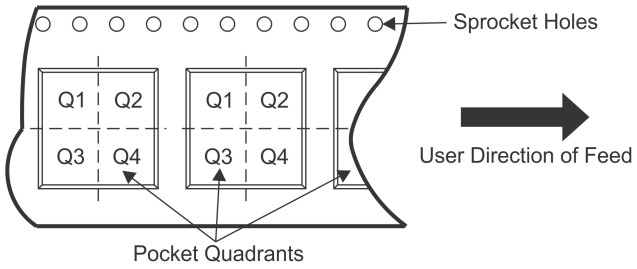


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

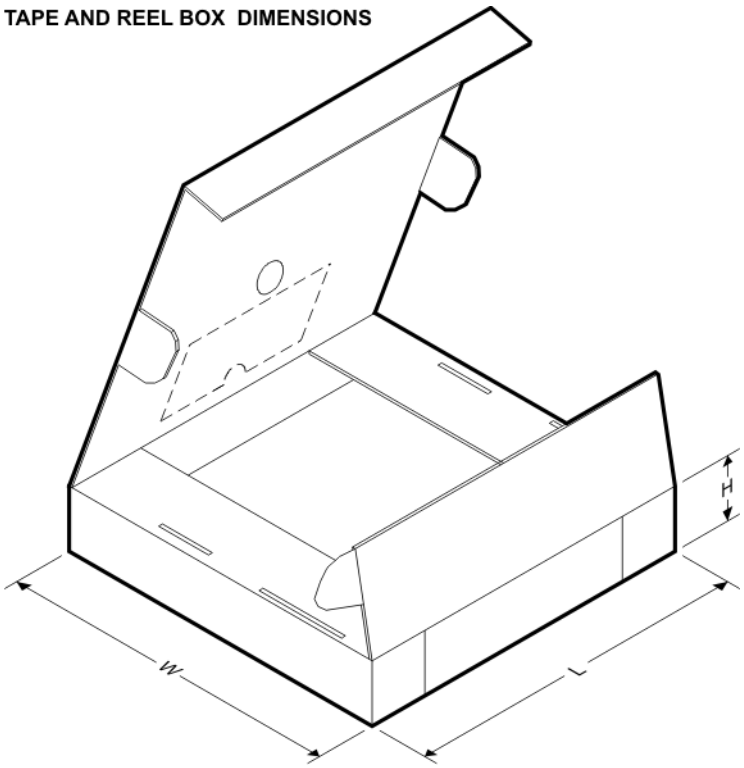
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3201AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV3201AIDBVT	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
TLV3201AIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV3201AIDCKT	SC70	DCK	5	250	178.0	8.4	2.4	2.5	1.2	4.0	8.0	Q3
TLV3202AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV3202AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

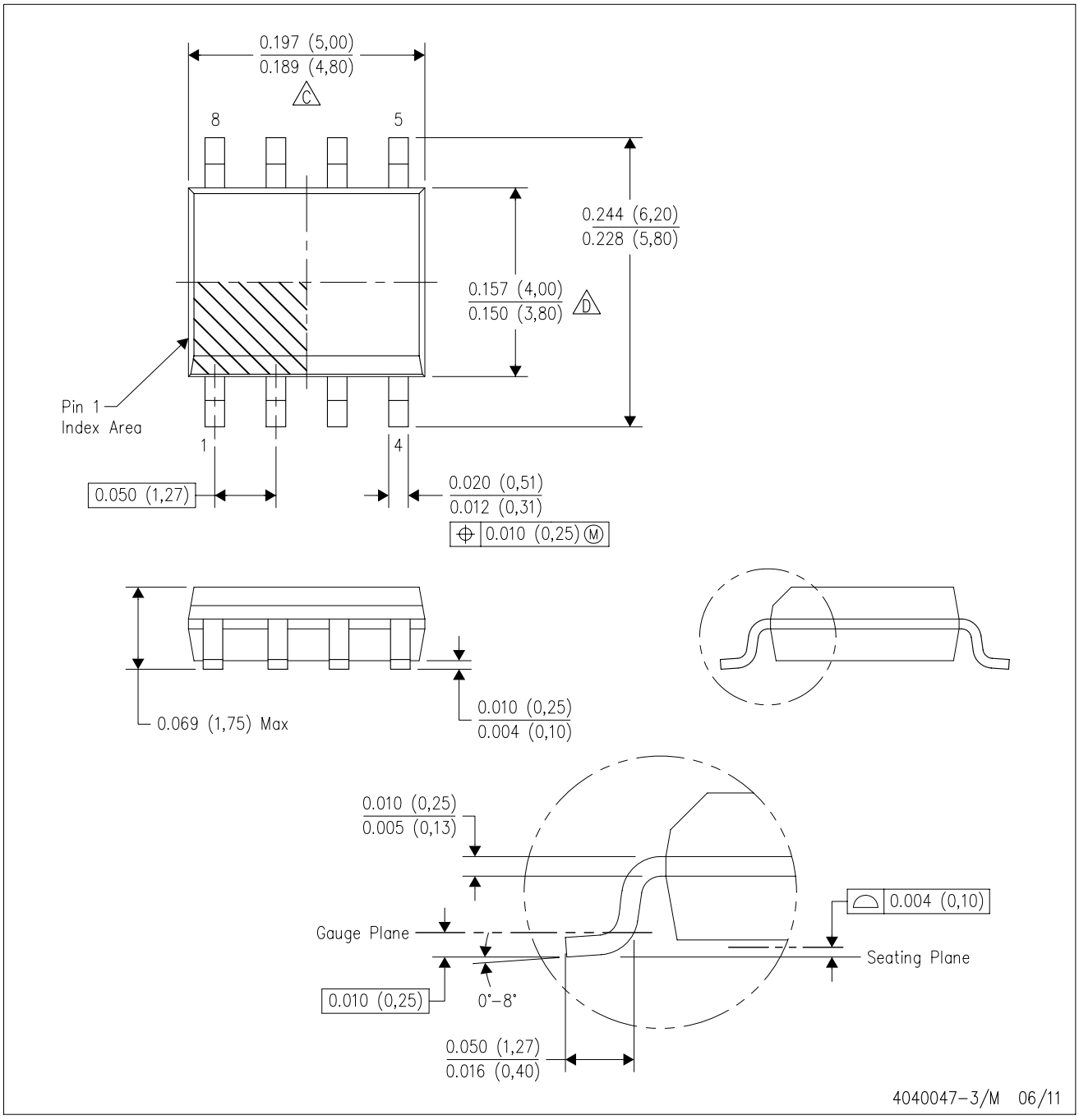
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

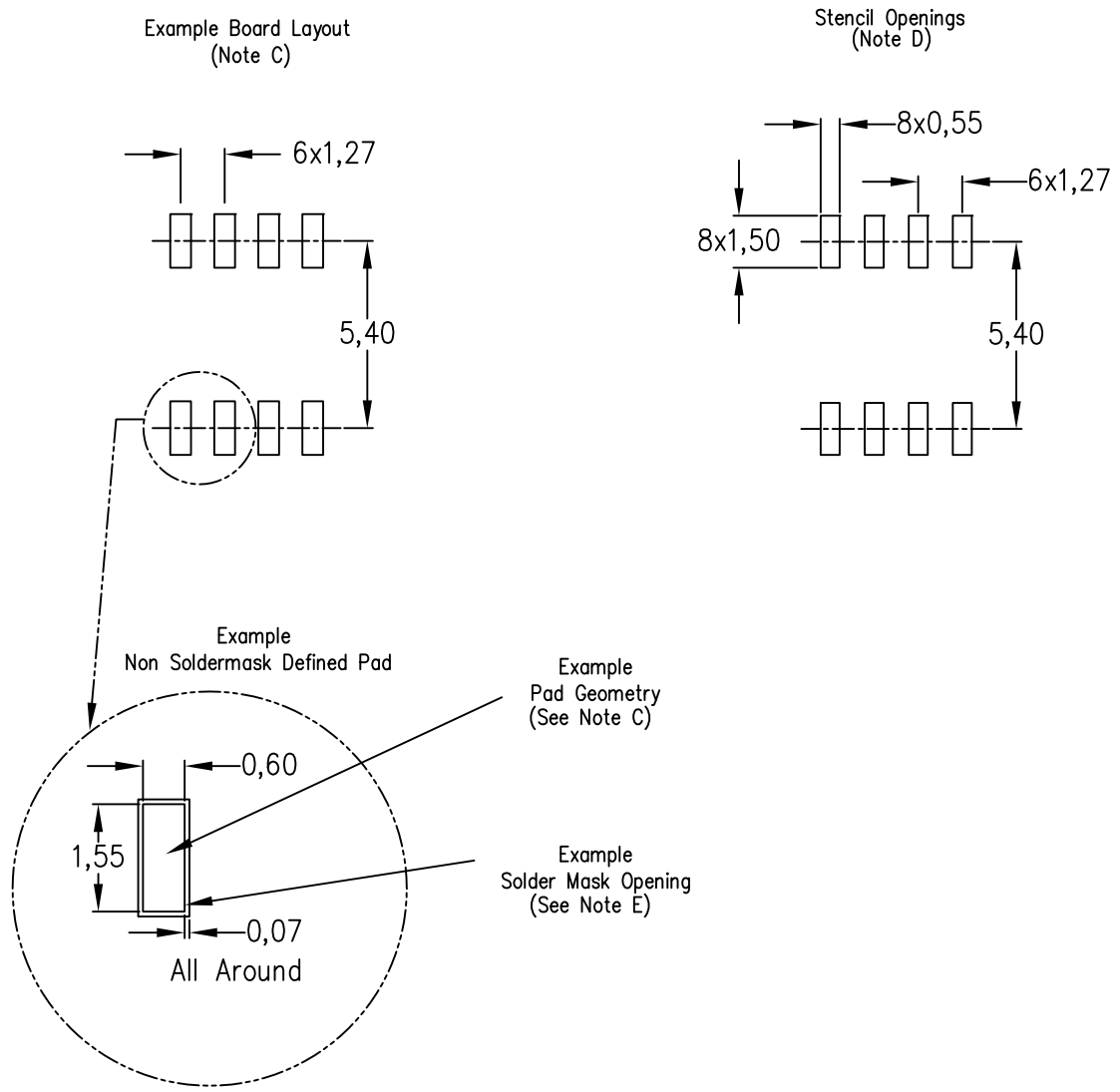
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3201AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV3201AIDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV3201AIDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TLV3201AIDCKT	SC70	DCK	5	250	190.0	190.0	30.0
TLV3202AIDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV3202AIDR	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



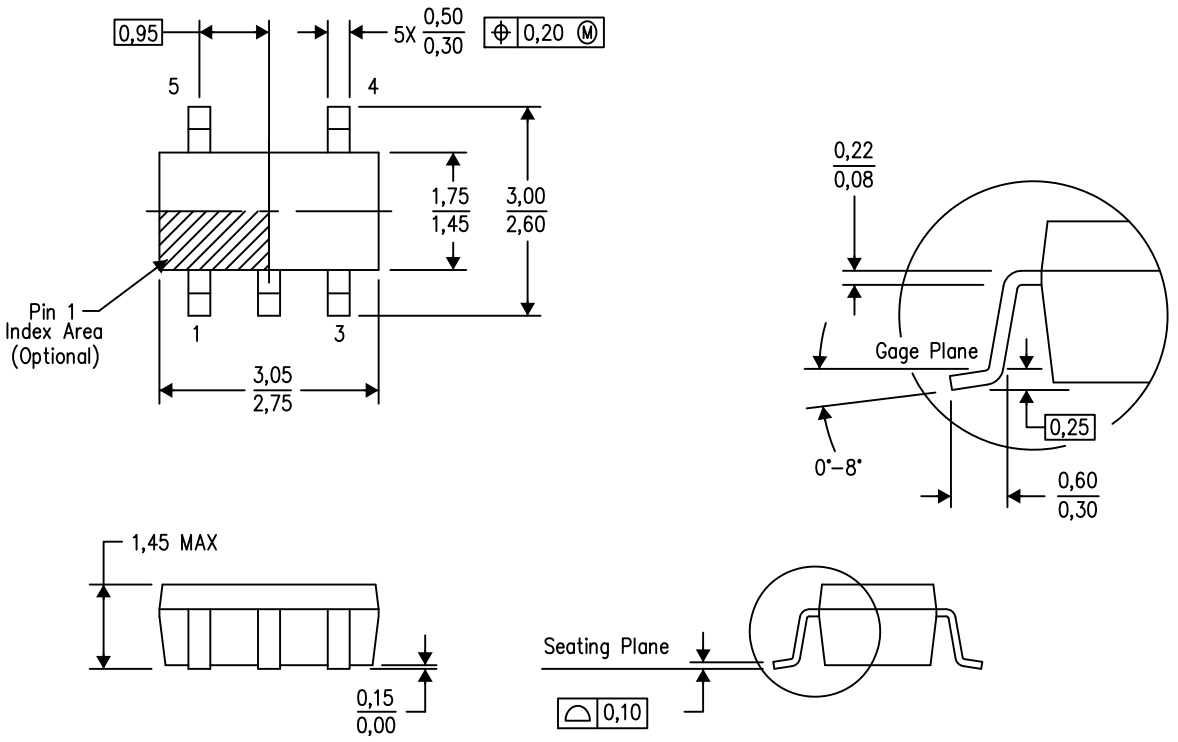
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

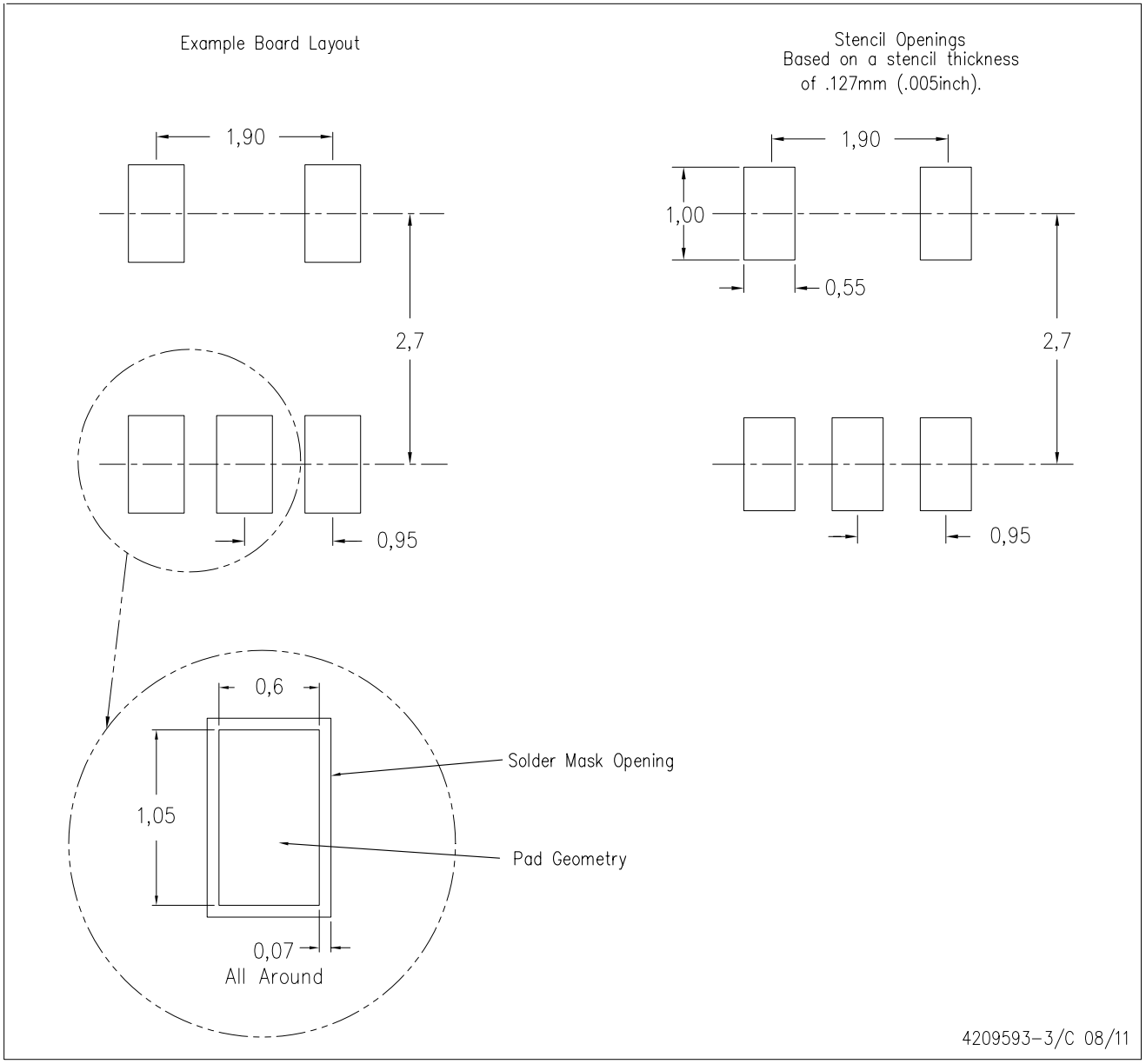
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

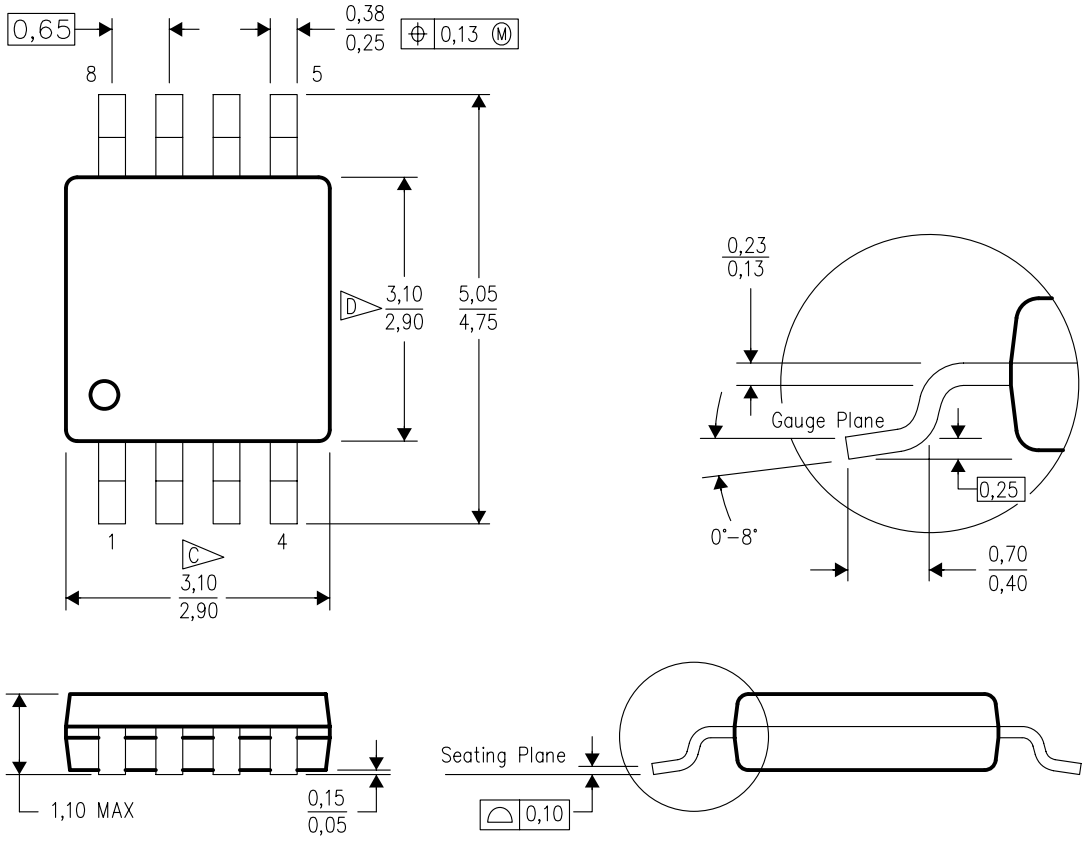
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

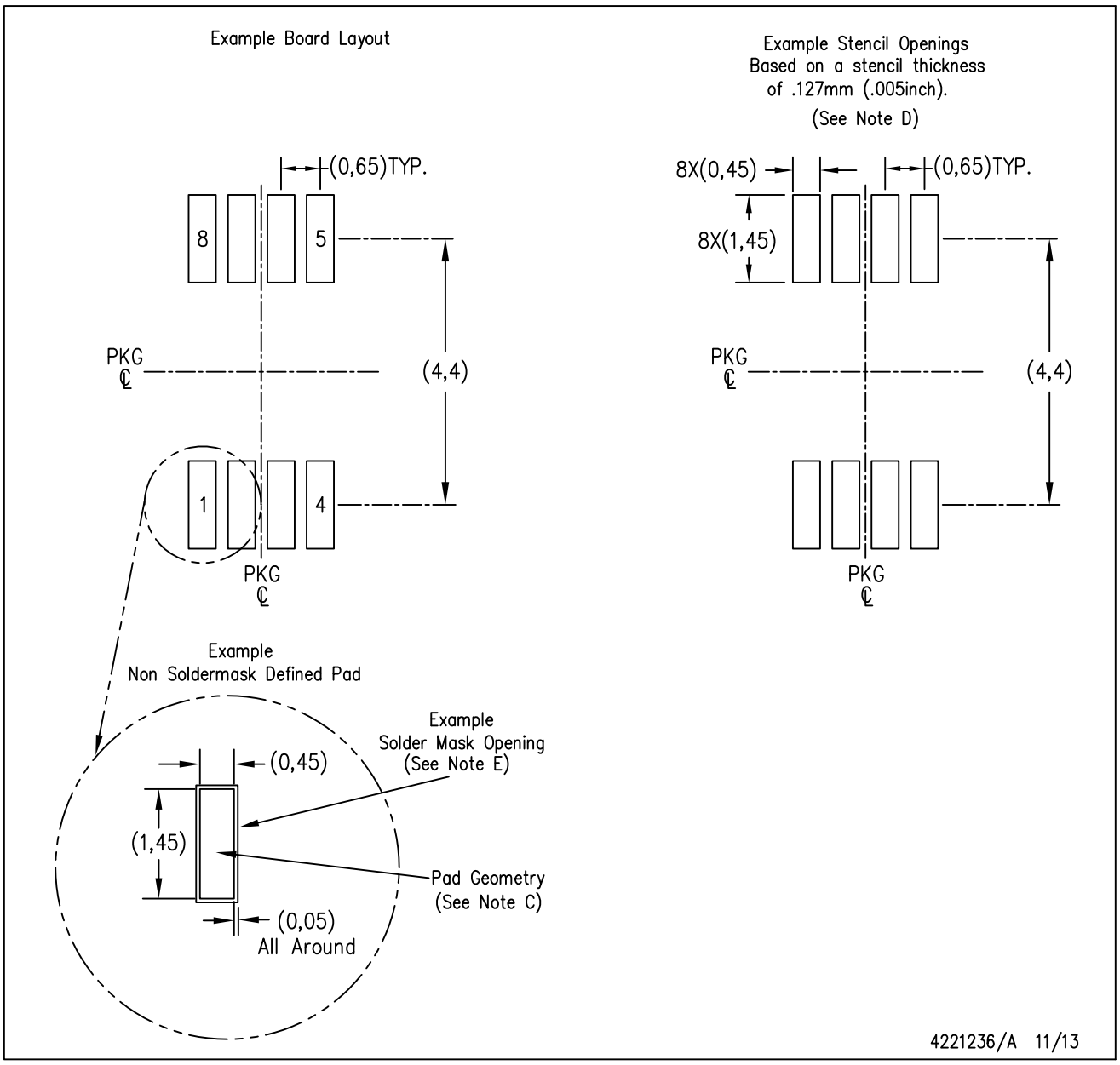
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

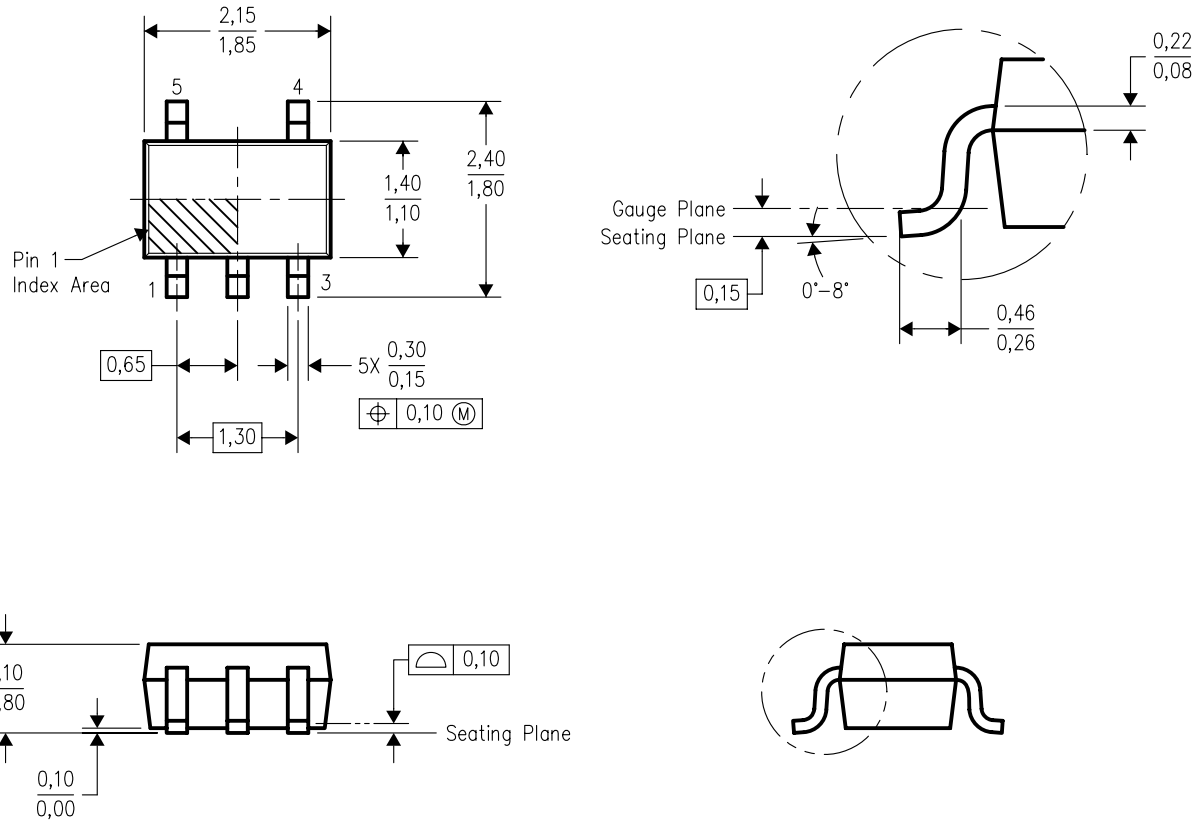
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

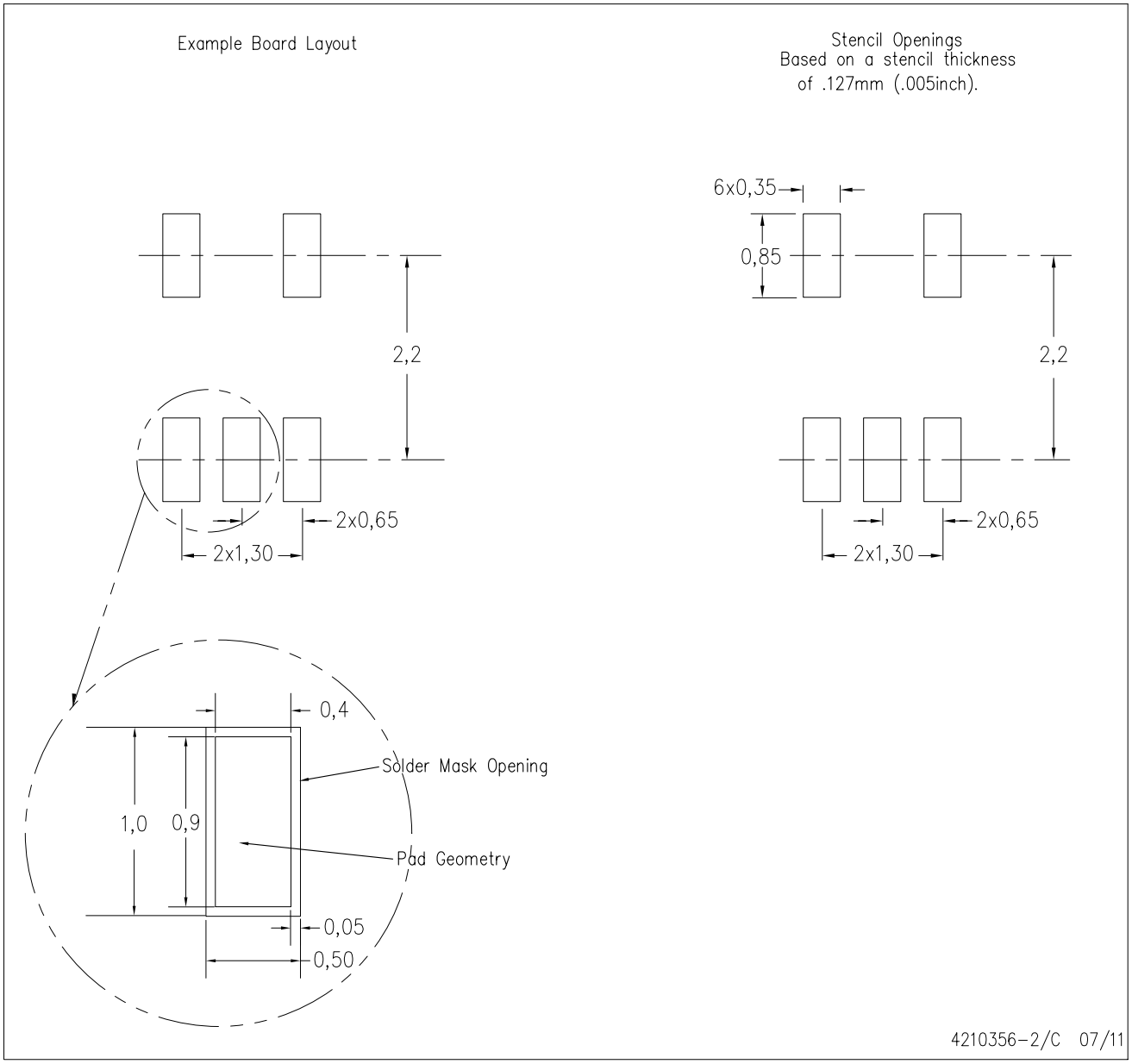
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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