TLVx316
10MHz、轨到轨输入/输出、低电压、1.8V CMOS 运算放大器

1 特性

- 单位增益带宽：10MHz
- 低 I_Q：每通道 400μA
  - 出色的功率带宽比
  - 在温度和电源电压范围内保持稳定的 I_Q
- 宽电源电压范围：1.8V 至 5.5V
- 低噪声：1kHz 时为 12nV/√Hz
- 低输入偏置电流：±10pA
- 偏移电压：±0.75mV
- 单位增益稳定
- 内部射频干扰 (RFI)/电磁干扰 (EMI) 滤波器
- 扩展温度范围：-40°C 至 +125°C

2 应用范围

- 电池供电仪器：
  - 消费类应用、工业应用、医疗应用
  - 笔记本电脑、便携式媒体播放器
- 传感器信号调节
- 条形码扫描器
- 有源滤波器
- 音频

3 说明

TLV316（单路）、TLV2316（双路）和 TLV4316（四路）器件构成了低功耗、通用运算放大器系列。该系列器件将轨到轨输入 和输出摆幅以及低静态电流（典型值为 400μA/通道）与 10MHz 高带宽和极低噪声（1kHz 时为 12nV/√Hz）相结合，广泛应用于 需要在成本与性能之间实现平衡 的应用。低输入偏置电流支持在 源阻抗高达兆欧级的 应用中使用此类运算放大器。

TLV316 器件采用稳健耐用的设计，方便电路设计人员使用。该器件具有单位增益稳定的集成 RFI/EMI 抑制滤波器，在过驱条件下不会出现反相并且具有高静电放电 (ESD) 保护（4kV 人体模型 (HBM)）。

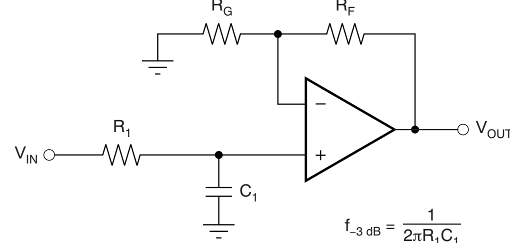
此类器件经过优化，适合在 1.8V (±0.9V) 至 5.5V (±2.75V) 的低电压状态下工作。这些最新补充的低电压互补金属氧化物半导体 (CMOS) 运算放大器与 TLVx313 和 TLVx314 搭配，为用户提供了广泛的带宽、噪声和功率选择，可以满足各种 应用的需要。

器件信息(1)

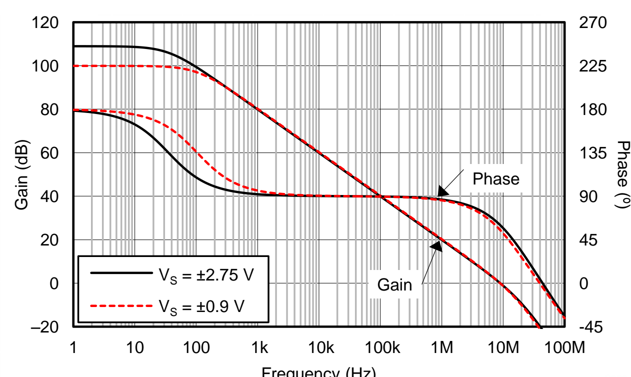
器件型号	封装	封装尺寸（标称值）
TLV316	SC70 (5)	1.25mm x 2.00mm
	SOT-23 (5)	1.60mm x 2.90mm
TLV2316	VSSOP (8)	3.00mm x 3.00mm
	SOIC (8)	3.91mm x 4.90mm
TLV4316	TSSOP (14)	4.40mm x 5.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

单极低通滤波器



10MHz 带宽下的低电源电流（400μA/通道）



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4 修订历史记录

日期	修订版本	注释
2016 年2 月	*	最初发布。

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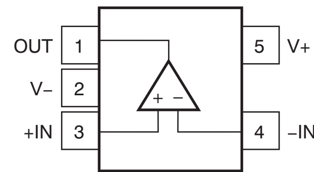
5 Device Comparison Table

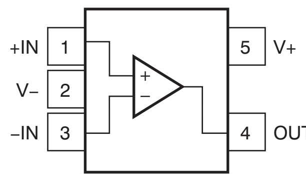
DEVICE	NO. OF CHANNELS	PACKAGE-LEADS				
		DBV	DCK	D	DGK	PW
TLV316	1	5	5	—	—	—
TLV2316	2	—	—	8	8	—
TLV4316	4	—	—	—	—	14

6 Pin Configuration and Functions

DBV Package: TLV316
5-Pin SOT-23
Top View



DCK Package: TLV316
5-Pin SC70
Top View



Pin Functions: TLV316

PIN			I/O	DESCRIPTION
NAME	DBV (SOT-23)	DCK (SC70)		
–IN	4	3	I	Inverting input
+IN	3	1	I	Noninverting input
OUT	1	4	O	Output
V–	2	2	—	Negative (lowest) supply or ground (for single-supply operation)
V+	5	5	—	Positive (highest) supply

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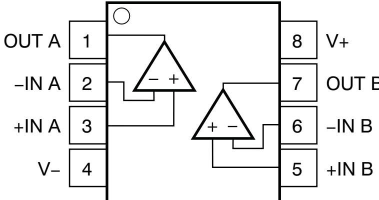
D, DGK Packages: TLV2316
8-Pin SOIC, VSSOP
Top View



Pin Functions: TLV2316

PIN		I/O	DESCRIPTION
NAME	D (SOIC), DGK (VSSOP)		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply

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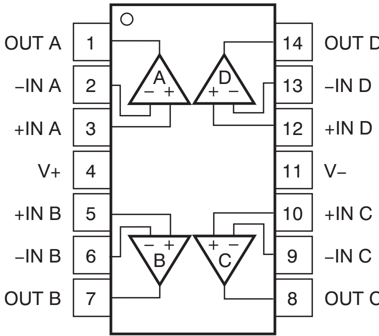
PW Package: TLV4316
14-Pin TSSOP
Top View



Pin Functions: TLV4316

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Inverting input, channel A
+IN A	3	I	Noninverting input, channel A
–IN B	6	I	Inverting input, channel B
+IN B	5	I	Noninverting input, channel B
–IN C	9	I	Inverting input, channel C
+IN C	10	I	Noninverting input, channel C
–IN D	13	I	Inverting input, channel D
+IN D	12	I	Noninverting input, channel D
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
OUT C	8	O	Output, channel C
OUT D	14	O	Output, channel D
V–	11	—	Negative (lowest) supply or ground (for single-supply operation)
V+	4	—	Positive (highest) supply

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)[1]

			MIN	MAX	UNIT
Supply voltage				7	V
Signal input pins	Voltage[2]	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	
	Current[2]		–10	10	mA
Output short-circuit[3]			Continuous		mA
Temperature	Specified, T_A		–40	125	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage	1.8		5.5	V
	Specified temperature range	–40		125	°C

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7.4 Thermal Information: TLV316

THERMAL METRIC[1]		TLV316		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	221.7	263.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	144.7	75.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	51.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	26.1	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.0	50.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Thermal Information: TLV2316

THERMAL METRIC[1]		TLV2316		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	127.2	186.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	71.6	78.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	68.2	107.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.0	15.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	67.6	106.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.6 Thermal Information: TLV4316

THERMAL METRIC[1]		TLV4316	UNIT
		PW (TSSOP)	
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	117.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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7.7 Electrical Characteristics

at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted); V_S (total supply voltage) = (V+) – (V–) = 1.8 V to 5.5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±0.75	±3	mV
		V_S = 5 V, T_A = –40°C to +125°C			±4.5	
dV_{OS}/dT	Drift	V_S = 5 V, T_A = –40°C to +125°C		±2		μV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 V – 5.5 V, V_{CM} = (V–)		±30	±175	μV/V
	Channel separation, dc	At dc		100		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	V_S = 5.5 V	(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, (V–) – 0.2 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to +125°C	72	90		dB
		V_S = 5.5 V, V_{CM} = –0.2 V to 5.7 V, T_A = –40°C to +125°C		75		
INPUT BIAS CURRENT						
I_B	Input bias current			±10		pA
I_{OS}	Input offset current			±10		pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	V_S = 5 V, f = 0.1 Hz to 10 Hz		5		$μV_{PP}$
e_n	Input voltage noise density	V_S = 5 V, f = 1 kHz		12		nV/√Hz
i_n	Input current noise density	f = 1 kHz		1.3		fA/√Hz
INPUT IMPEDANCE						
Z_{ID}	Differential			2 || 2		10^{16}Ω || pF
Z_{IC}	Common-mode			2 || 4		10^{11}Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 5.5 V, (V–) + 0.05 V < V_O < (V+) – 0.05 V, R_L = 10 kΩ	100	104		dB
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ		104		
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	V_S = 5 V, G = +1		10		MHz
$φ_m$	Phase margin	V_S = 5 V, G = +1		60		Degrees
SR	Slew rate	V_S = 5 V, G = +1		6		V/μs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step , G = +1, C_L = 100 pF		1		μs
t_{OR}	Overload recovery time	V_S = 5 V, V_{IN} × gain = V_S		0.8		μs
THD + N	Total harmonic distortion + noise(1)	V_S = 5 V, V_O = 0.5 V_{RMS}, G = +1, f = 1 kHz		0.008%		
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 1.8 V to 5.5 V, R_L = 10 kΩ,			35	mV
		V_S = 1.8 to 5.5 V, R_L = 2 kΩ,			125	
I_{SC}	Short-circuit current	V_S = 5 V		±50		mA
Z_O	Open-loop output impedance	V_S = 5 V, f = 10 MHz		250		Ω
POWER SUPPLY						
V_S	Specified voltage range		1.8		5.5	V
I_Q	Quiescent current per amplifier	V_S = 5 V, I_O = 0 mA, T_A = –40°C to 125°C		400	575	μA
TEMPERATURE						
T_A	Specified		–40		125	°C
T_{stg}	Storage		–65		150	°C

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.

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7.8 Typical Characteristics

Table 1. Table of Graphs

TITLE	FIGURE
Offset Voltage Production Distribution	Figure 1
Offset Voltage vs Common-Mode Voltage	Figure 2
Open-Loop Gain and Phase vs Frequency	Figure 3
Input Bias and Offset Current vs Temperature	Figure 4
Input Voltage Noise Spectral Density vs Frequency	Figure 5
Quiescent Current vs Supply Voltage	Figure 6
Small-Signal Overshoot vs Load Capacitance	Figure 7
No Phase Reversal	Figure 8
Small-Signal Step Response	Figure 9
Large-Signal Step Response	Figure 10
Short-Circuit Current vs Temperature	Figure 11
Electromagnetic Interference Rejection Ratio Referred to Noninverting Input vs Frequency	Figure 12
Channel Separation vs Frequency	Figure 13

7.9 Typical Characteristics

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

Distribution taken from 12551 amplifiers

Figure 1. Offset Voltage Production Distribution

V+ = 2.75 V, V– = –2.75 V, 9 typical units shown

Figure 2. Offset Voltage vs Common-Mode Voltage

V_{CM} < (V+) – 1.4 V

Figure 3. Open-Loop Gain and Phase vs Frequency

Figure 4. Input Bias and Offset Current vs Temperature

Figure 5. Input Voltage Noise Spectral Density vs Frequency

Figure 6. Quiescent Current vs Supply Voltage

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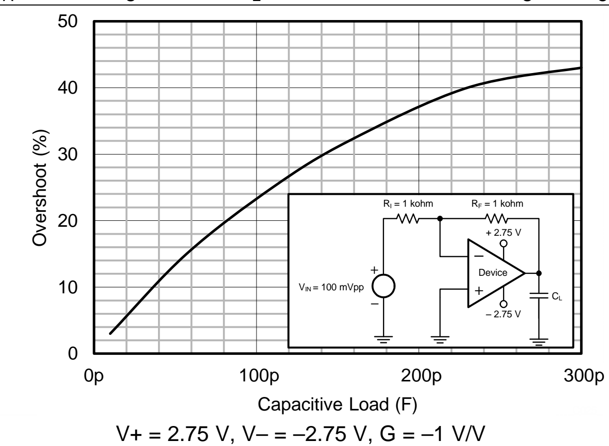
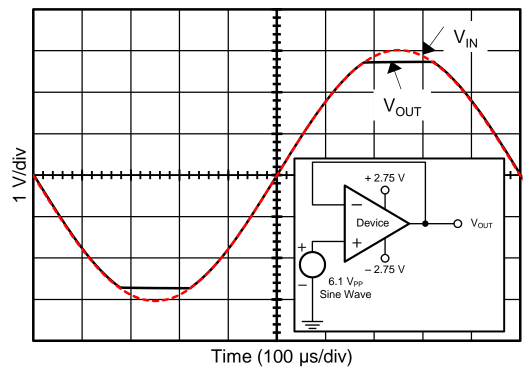
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



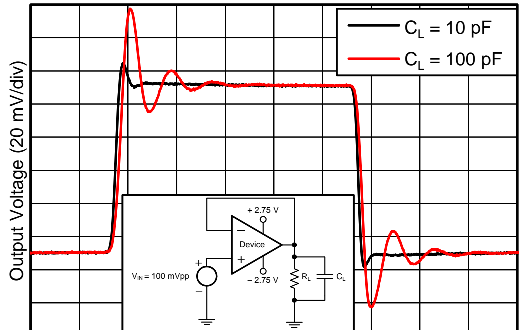
V+ = 2.75 V, V– = –2.75 V, G = –1 V/V

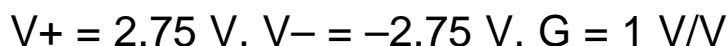
Figure 7. Small-Signal Overshoot vs Load Capacitance



V+ = 2.75 V, V– = –2.75 V

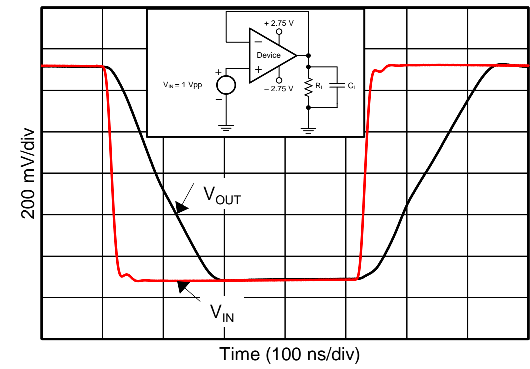
Figure 8. No Phase Reversal





V+ = 2.75 V, V– = –2.75 V, G = 1 V/V

Figure 9. Small-Signal Step Response



V+ = 2.75 V, V– = –2.75 V, C_L = 100 pF, G = 1 V/V

Figure 10. Large-Signal Step Response

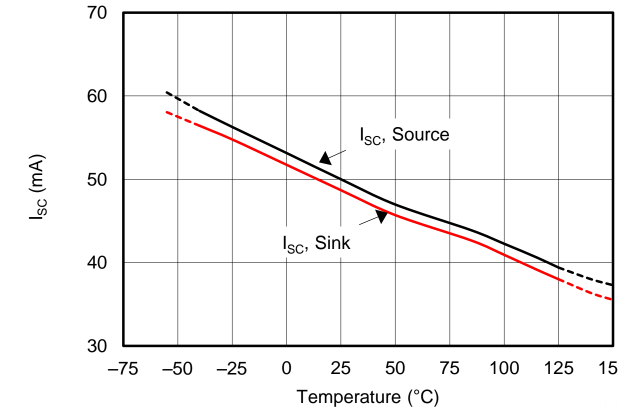
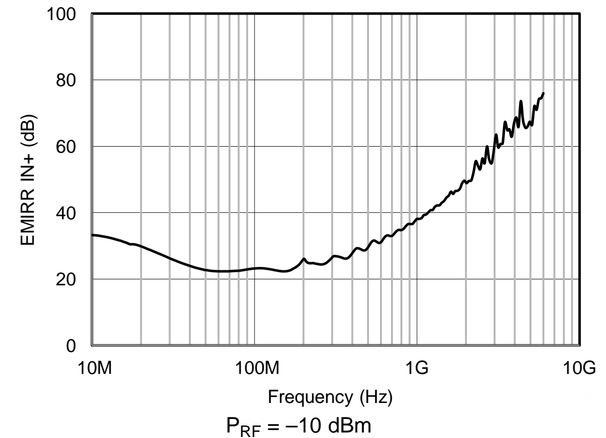


Figure 11. Short-Circuit Current vs Temperature



P_{RF} = –10 dBm

Figure 12. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input vs Frequency

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

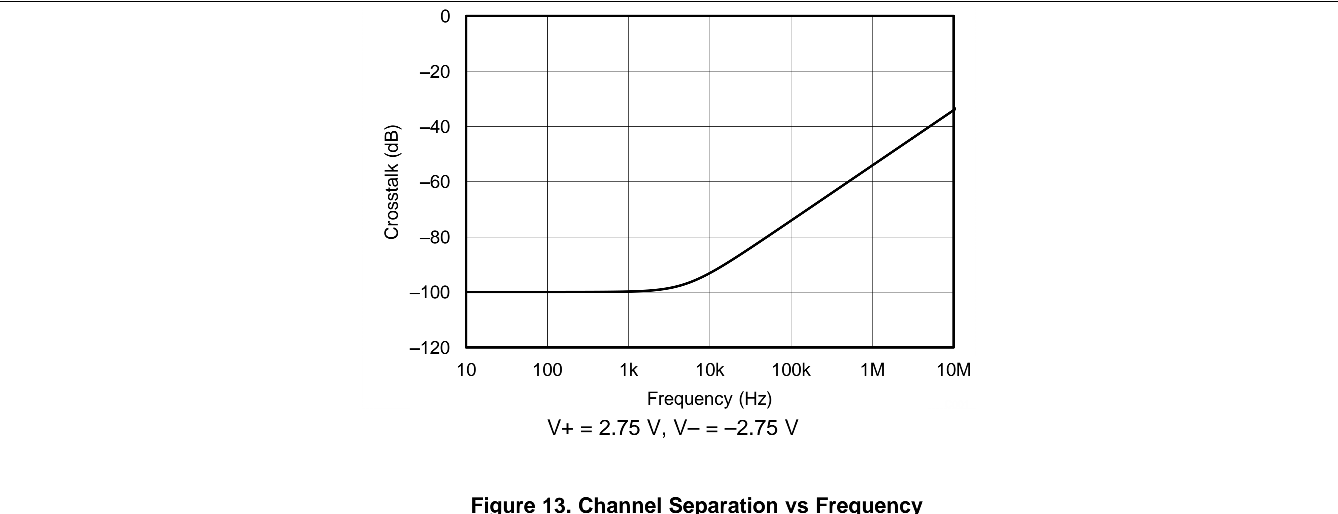

Figure 13. Channel Separation vs Frequency

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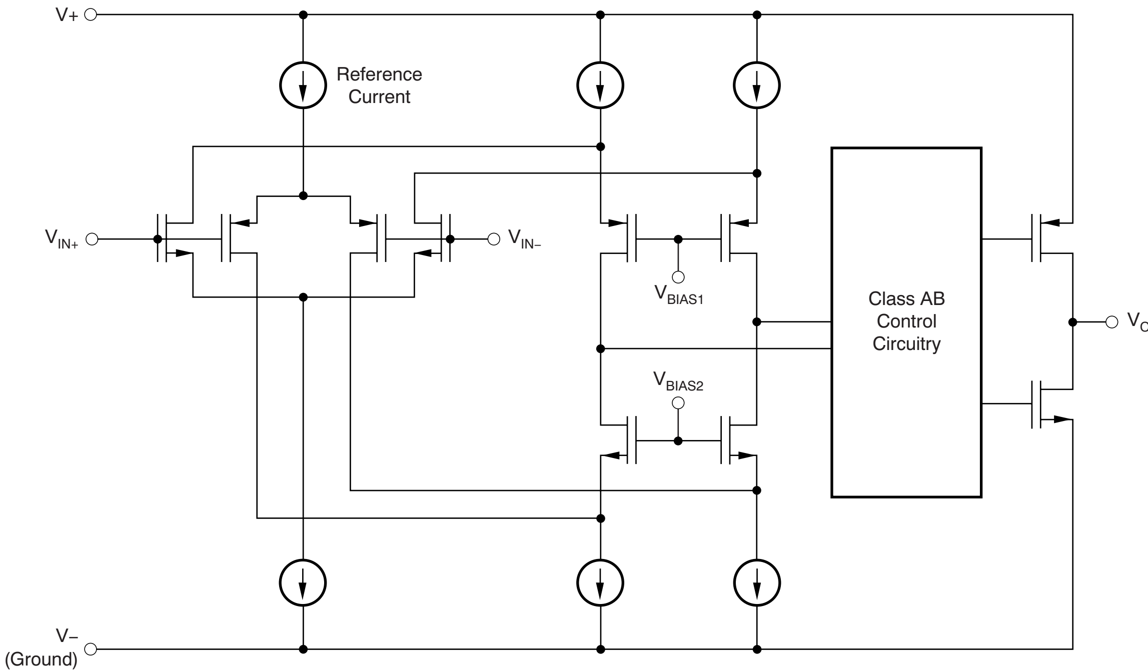
8 Detailed Description

8.1 Overview

The TLV316 is a family of low-power, rail-to-rail input and output operational amplifiers. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤ 10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails and allows the TLV316 series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them ideal for driving sampling analog-to-digital converters (ADCs).

The TLV316 features 10-MHz bandwidth and 6-V/μs slew rate with only 400-μA supply current per channel, providing good ac performance at very-low power consumption. DC applications are also well served with a very-low input noise voltage of 12 nV/√Hz at 1 kHz, low input bias current (5 pA), and an input offset voltage of 0.5 mV (typical).

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Operating Voltage

The TLV316 series operational amplifiers are fully specified and ensured for operation from 1.8 V to 5.5 V. In addition, many specifications apply from –40°C to +125°C. Parameters that vary significantly with operating voltages or temperature are illustrated in the *Typical Characteristics* section.

8.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLV316 series extends 200 mV beyond the supply rails for supply voltages greater than 2.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair; see the *Functional Block Diagram* section. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4 V to 200 mV above the positive supply, whereas the P-channel pair is active for inputs from 200 mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.2 V to (V+) – 1 V, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (both stages on) can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, up to (V+) – 1 V to (V+) – 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can be degraded compared to device operation outside this region.

8.3.3 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TLV316 delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads of 10 kΩ, the output swings typically to within 30 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails; see typical characteristic graph *Output Voltage Swing vs Output Current* ().

8.3.4 Common-Mode Rejection Ratio (CMRR)

CMRR for the TLV316 is specified in two ways so the best match for a given application can be selected. First, the *Electrical Characteristics* table provides the CMRR of the device in the common-mode range below the transition region [V_{CM} < (V+) – 1.4 V]. This specification is the best indicator of device capability when the application requires using one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at V_{CM} = –0.2 V to 5.7 V for V_S = 5.5 V. This last value includes the variations through the transition region.

8.3.5 Capacitive Load and Stability

The TLV316 is designed to be used in applications where driving a capacitive load is required. As with all operational amplifiers, there may be specific instances where the TLV316 can become unstable. The particular operational amplifier circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An operational amplifier in the unity-gain (1 V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the operational amplifier output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases when the capacitive loading increases. For a conservative best practice, designing for 25% overshoot (40° phase margin) provides improved stability over process variations. The equivalent series resistance (ESR) of some very-large capacitors (C_L greater than 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains. See typical characteristic graph, *Small-Signal Overshoot vs Capacitive Load* (Figure 7, G = –1 V/V).

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Feature Description (continued)

One technique for increasing the capacitive load drive capability of the amplifier operating in a unity-gain configuration is to insert a small resistor (typically 10 Ω to 20 Ω) in series with the output, as shown in Figure 14. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique, however, is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

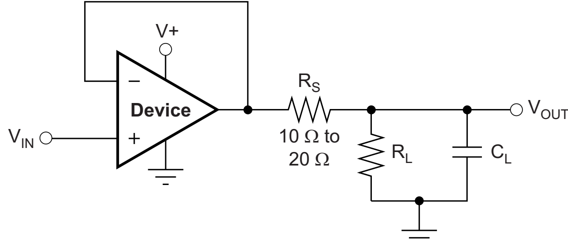

Figure 14. Improving Capacitive Load Drive

8.3.6 EMI Susceptibility and Input Filtering

Operational amplifiers vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the dc offset measured at the amplifier output can shift from its nominal value when EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. Although all operational amplifier pin functions can be affected by EMI, the signal input pins are likely to be the most susceptible. The TLV316 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifier response to EMI. This filter provides both common-mode and differential-mode filtering. The filter is designed for a cutoff frequency of approximately 80 MHz (–3 dB), with a roll-off of 20 dB per decade.

The immunity of an operational amplifier can be accurately measured and quantified over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows operational amplifiers to be directly compared by the EMI immunity. Figure 12 illustrates the results of this testing on the TLV316. Detailed information can also be found in application report, *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download from www.ti.com.

8.3.7 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, either because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV316 is approximately 300 ns.

8.4 Device Functional Modes

The TLVx316 devices have a single functional mode. These devices are powered on as long as the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

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9 Application and Implementation

NOTE

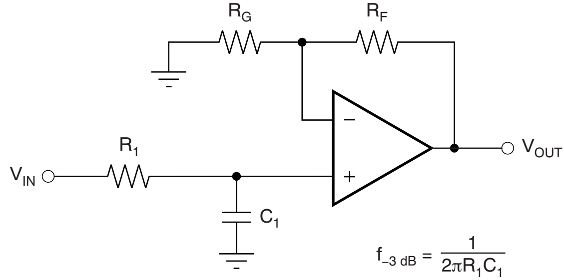
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV316, TLV2316, and TLV4316 are powered on when the supply is connected. The devices can be operated as a single-supply operational amplifier or a dual-supply amplifier, depending on the application.

9.2 System Examples

When receiving low-level signals, the device often requires limiting the bandwidth of the incoming signals into the system. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting pin of the amplifier, as shown in Figure 15.



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

Figure 15. Single-Pole, Low-Pass Filter

If even more attenuation is needed, the device requires a multiple-pole filter. The Sallen-Key filter can be used for this task, as shown in Figure 16. For best results, the amplifier must have a bandwidth that is eight to ten times the filter frequency bandwidth. Failure to follow this guideline can result in a phase shift of the amplifier.

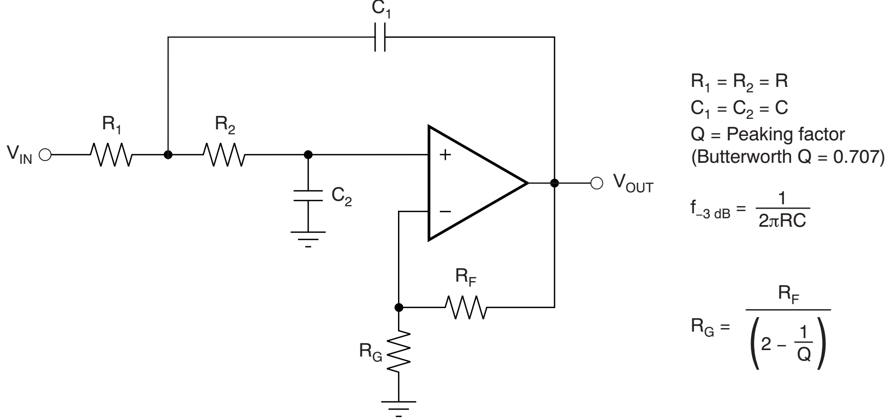


Figure 16. Two-Pole, Low-Pass, Sallen-Key Filter

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10 Power Supply Recommendations

The TLV316 is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout Guidelines* section.

10.1 Input and ESD Protection

The TLV316 family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings* table. Figure 17 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value must be kept to a minimum in noise-sensitive applications.

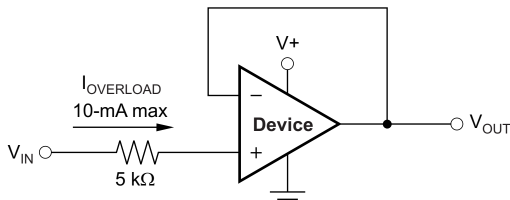

Figure 17. Input Current Protection

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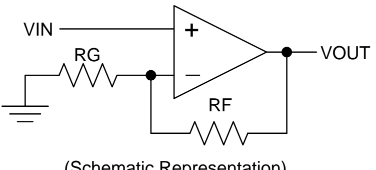
11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*, SLOA089.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example



(Schematic Representation)

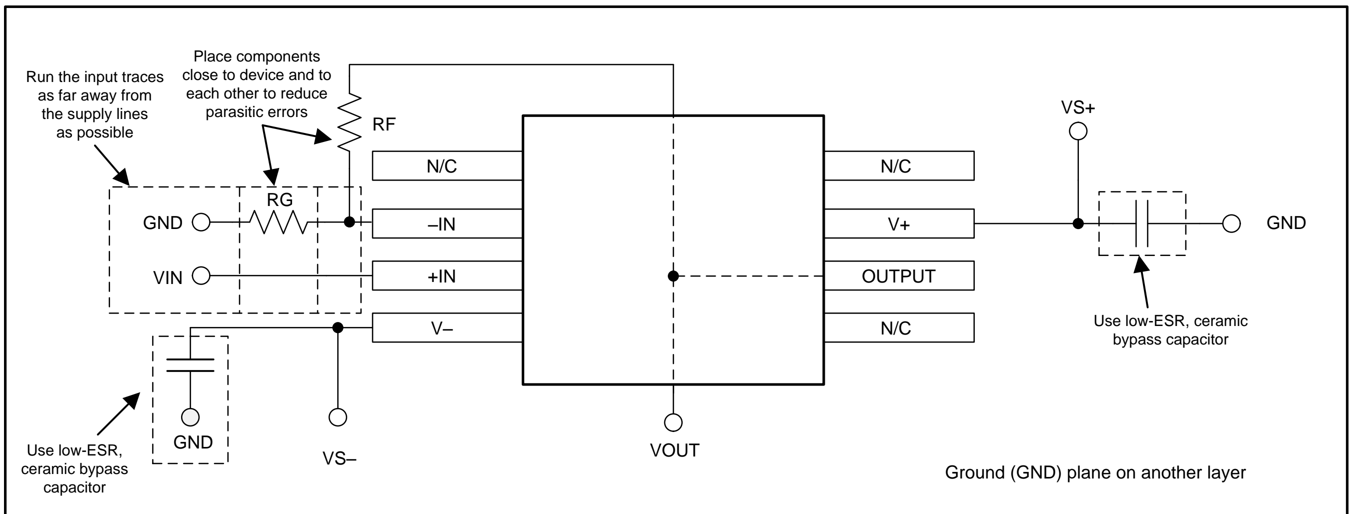


Figure 18. Operational Amplifier Board Layout for a Noninverting Configuration

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12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

《TLVx313 数据表》，SBOS753

《TLVx314 数据表》，SBOS754

《运算放大器的电磁干扰 (EMI) 抑制比》，SBOA128

《QFN/SON PCB 连接》，SLUA271

《四方扁平无引线逻辑器件封装》，SCBA017

《电路板布局布线技巧》，SLOA089

《单端输入至差动输出转换电路参考设计》，TIPD131

12.2 相关链接

表 2 列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **2.** 相关链接

器件	产品文件夹	样片与购买	技术文章	工具与软件	支持与社区
TLV316	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV2316	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TLV4316	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 社区资源

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
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RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2316IDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	12X6	Samples
TLV2316IDGKT	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	12X6	Samples
TLV2316IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	V2316	Samples
TLV316IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12C	Samples
TLV316IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12C	Samples
TLV316IDCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12D	Samples
TLV316IDCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	12D	Samples
TLV4316IDR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T4316D	Samples
TLV4316IPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV4316	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE

0,95
5X 0,50/0,30
0,20 Ⓜ
5 4
1 3
Pin 1 Index Area (Optional)
1,75/1,45
3,00/2,60
3,05/2,75
0,22/0,08
Gage Plane
0,25
0°–8°
0,60/0,30
1,45 MAX
0,15/0,00
Seating Plane
0,10

4073253-4/N 12/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE

Example Board Layout

1,90

2,7

0,95

0,6

1,05

Solder Mask Opening

Pad Geometry

0,07
All Around

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

1,90

1,00

0,55

2,7

0,95

4209593–3/C 08/11

NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.

D. Publication IPC–7351 is recommended for alternate designs.

E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE

4093553-3/G 01/2007

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

6x0,35
0,85
2,2
2,2
2x0,65
2x1,30
2x0,65
2x1,30
0,4
Solder Mask Opening
1,0
0,9
Pad Geometry
0,05
0,50

4210356–2/C 07/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE

4073329/E 05/06

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE

Example Board Layout

(0,65)TYP.

8 5

PKG ℄ (4,4)

1 4

PKG ℄

Example Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).
(See Note D)

8X(0,45) (0,65)TYP.

8X(1,45)

PKG ℄ (4,4)

PKG ℄

Example
Non Soldermask Defined Pad

(0,45)

Example
Solder Mask Opening
(See Note E)

(1,45)

Pad Geometry
(See Note C)

(0,05)
All Around

4221236/A 11/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE

0.344 (8,75)
0.337 (8,55)
C
14
8
0.244 (6,20)
0.228 (5,80)
0.157 (4,00)
0.150 (3,80)
D
1
7
Pin 1
Index Area
0.050 (1,27)
0.020 (0,51)
0.012 (0,31)
0.010 (0,25) M
0.069 (1,75) Max
0.010 (0,25)
0.004 (0,10)
0.010 (0,25)
0.005 (0,13)
Gauge Plane
0.004 (0,10)
Seating Plane
0.010 (0,25)
0°–8°
0.050 (1,27)
0.016 (0,40)

4040047-5/M 06/11

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

12x1,27

5,40

Stencil Openings
(Note D)

14x0,55

12x1,27

14x1,50

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

Example
Solder Mask Opening
(See Note E)

0.07
All Around

4211283-3/E 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

0,65
0,30
0,19
0,10 M
14
8
4,50
4,30
6,60
6,20
D
1
7
5,10
4,90
C
0,15 NOM
Gage Plane
0,25
0°–8°
0,75
0,50
1,20 MAX
0,15
0,05
Seating Plane
0,10

4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

12x0,65

5,60

Stencil Openings
(Note D)

14x0,30

12x0,65

14x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,35

1,60

Example
Solder Mask Opening
(See Note E)

0,07
All Around

4211284–2/G 08/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE

0.197 (5,00)
0.189 (4,80) C

8 5

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80) D

Pin 1 Index Area

1 4

0.050 (1,27)

0.020 (0,51)
0.012 (0,31)
⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max

0.010 (0,25)
0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane

0.004 (0,10)

Seating Plane

0.010 (0,25)

0°–8°

0.050 (1,27)
0.016 (0,40)

4040047–3/M 06/11

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

6x1,27

5,40

Stencil Openings
(Note D)

8x0,55

6x1,27

8x1,50

5,40

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,60

1,55

0,07
All Around

Example
Solder Mask Opening
(See Note E)

4211283-2/E 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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