FlatLink™ RECEIVER

**Check for Samples: SN75LVDS82**

FEATURES

- **4:28 Data Channel Expansion at up to 238 Mbytes/s Throughput**
- **Suited for SVGA, XGA, or SXGA Display Data Transmission From Controller to Display With Very Low EMI**
- **Four Data Channels and Clock Low-Voltage Differential Channels In and 28 Data and Clock Low-Voltage TTL Channels Out**
- **Operates From a Single 3.3-V Supply With 250 mW (Typ)**
- **5-V Tolerant $\overline{\text{SHTDN}}$ Input**
- **Falling Clock-Edge-Triggered Outputs**
- **Packaged in Thin Shrink Small-Outline Package (TSSOP) With 20-Mil Terminal Pitch**
- **Consumes Less Than 1 mW When Disabled**
- **Wide Phase-Lock Input Frequency Range . . . 31 MHz to 68 MHz**
- **No External Components Required for PLL**
- **Inputs Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
- **Improved Replacement for the National™ DS90C582**

DESCRIPTION

The SN75LVDS82 FlatLink™ receiver contains four serial-in, 7-bit parallel-out shift registers, a 7× clock synthesizer, and five low-voltage differential signaling (LVDS) line receivers in a single integrated circuit.

DGG PACKAGE
(TOP VIEW)

D22	1	56	V_{CC}
D23	2	55	D21
D24	3	54	D20
GND	4	53	D19
D25	5	52	GND
D26	6	51	D18
D27	7	50	D17
LVDSGND	8	49	D16
A0M	9	48	V_{CC}
A0P	10	47	D15
A1M	11	46	D14
A1P	12	45	D13
LVDSV$_{CC}$	13	44	GND
LVDSGND	14	43	D12
A2M	15	42	D11
A2P	16	41	D10
CLKINM	17	40	V_{CC}
CLKINP	18	39	D9
A3M	19	38	D8
A3P	20	37	D7
LVDSGND	21	36	GND
PLLGND	22	35	D6
PLLV$_{CC}$	23	34	D5
PLLGND	24	33	D4
$\overline{\text{SHTDN}}$	25	32	D3
CLKOUT	26	31	V_{CC}
D0	27	30	D2
GND	28	29	D1

These functions allow receipt of synchronous data from a compatible transmitter, such as the SN75LVDS81, over five balanced-pair conductors, and expansion to 28 bits of single-ended low-voltage TTL (LVTTL) synchronous data at a lower transfer rate. The SN75LVDS82 can also be used with the SN75LVDS84 or SN75LVDS85 for 21-bit transfers.

When receiving, the high-speed LVDS data is received and loaded into registers at the rate of seven times (7×) the LVDS input clock (CLKIN). The data is then unloaded to a 28-bit-wide LVTTL parallel bus at the CLKIN rate. A phase-locked loop (PLL) clock synthesizer circuit generates a 7× clock for internal clocking and an output clock for the expanded data. The SN75LVDS82 presents valid data on the falling edge of the output clock (CLKOUT).
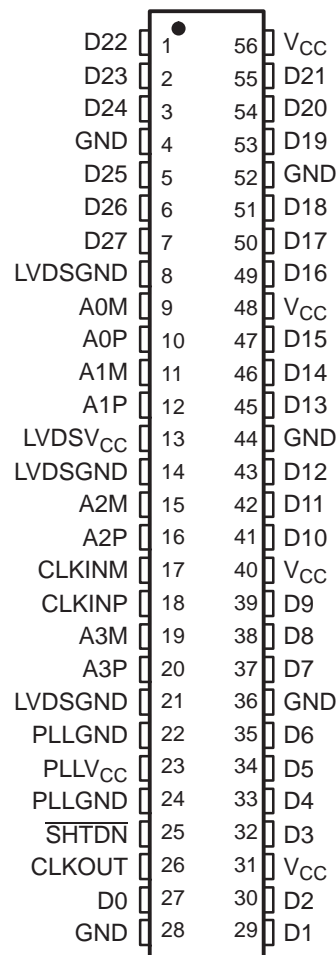
SN75LVDS82

The SN75LVDS82 requires only five line-termination resistors for the differential inputs and little or no control. The data bus appears the same at the input to the transmitter and output of the receiver with the data transmission transparent to the user. The only possible user intervention is the use of the shutdown/clear (SHTDN) active-low input to inhibit the clock and shut off the LVDS receivers for lower power consumption. A low-level on SHTDN clears all internal registers to a low level and places the CMOS outputs in a high-impedance state.

The SN75LVDS82 is characterized for operation over ambient air temperatures of 0°C to 70°C.
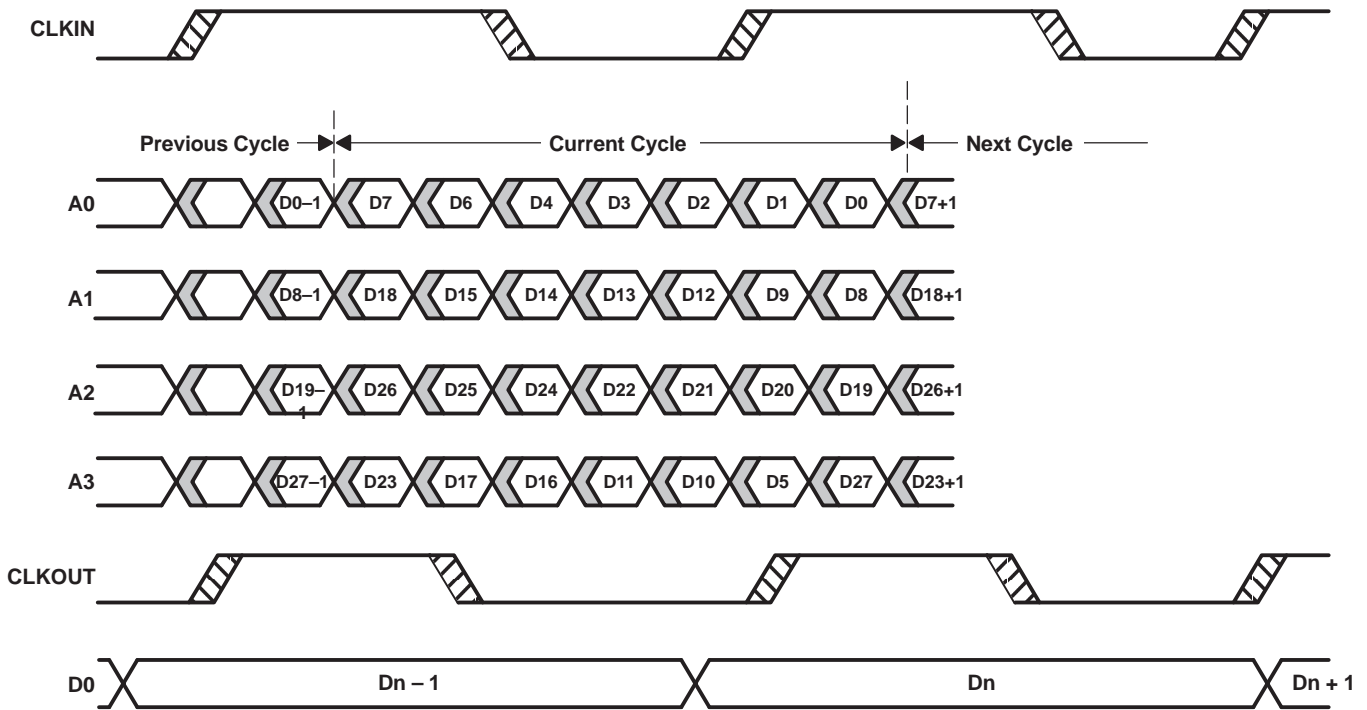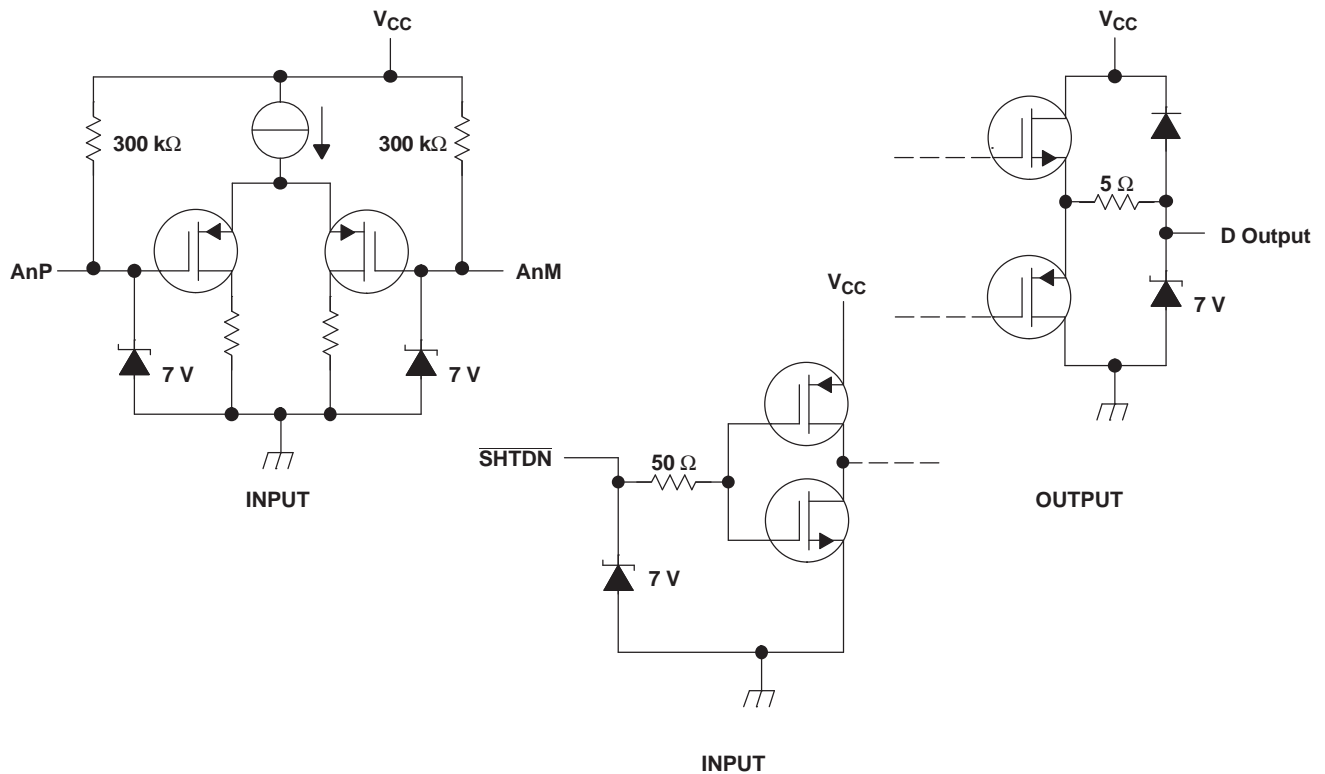
FUNCTIONAL BLOCK DIAGRAM
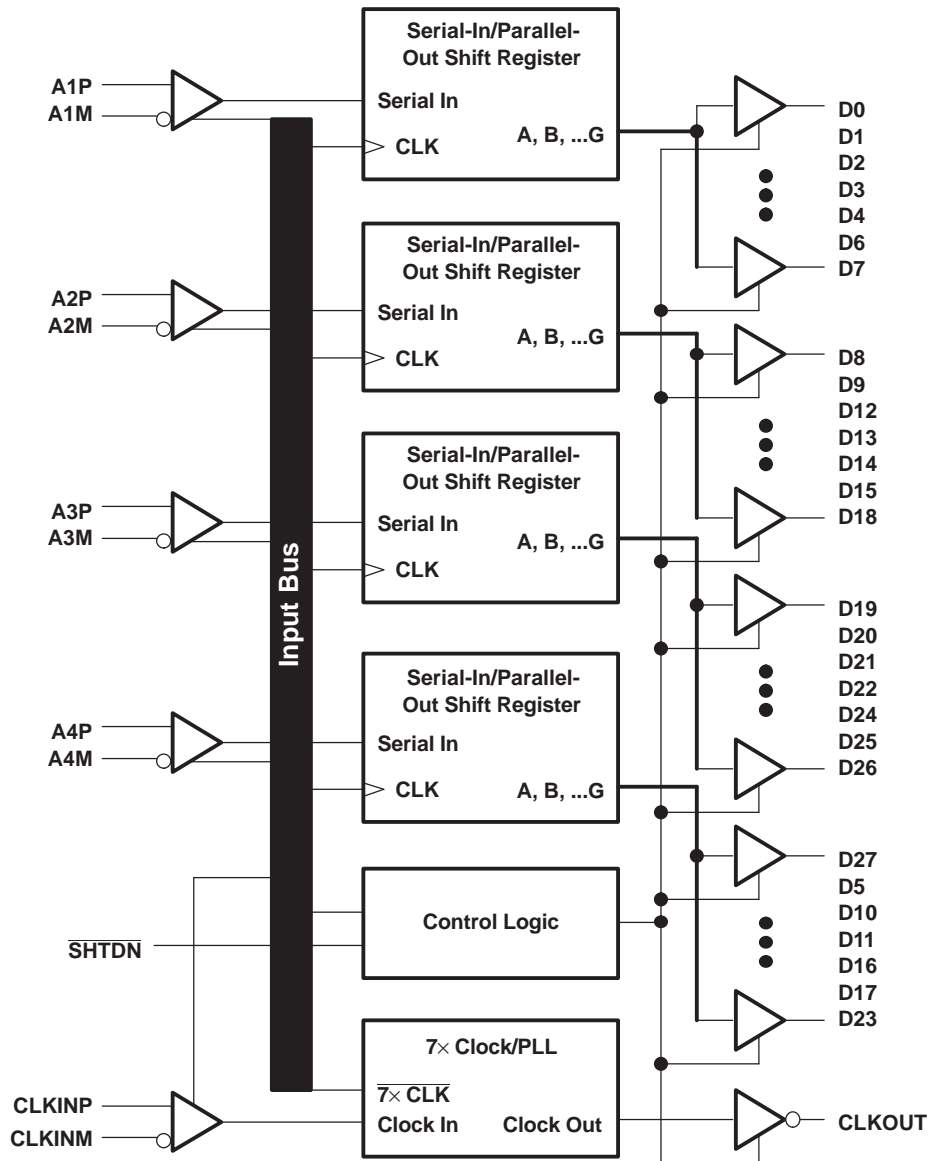
Figure 1. SN75LVDS82 Load and Shift Timing Sequences

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

ABSOLUTE MAXIMUM RATINGS[(1)]

over operating free-air temperature range (unless otherwise noted)

			UNIT
V_{CC}	Supply voltage range[(2)]		–0.5 V to 4 V
V_O	Output voltage range (Dxx terminals)		–0.5 V to V_{CC} + 0.5 V
V_I	Input voltage range	Any terminal except $\overline{\text{SHTDN}}$	–0.5 V to V_{CC} + 0.5 V
		$\overline{\text{SHTDN}}$	–0.5 V to 5.5 V
	Continuous total power dissipation		See Dissipation Rating Table
T_A	Operating temperature range		0°C to 70°C
T_{stg}	Storage temperature range		–65°C to 150°C
	Lead temperature 1,6 mm (1/16 in) from case for 10 s		260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND, unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR[(1)] ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
DGG	1377 mW	11.0 mW/°C	822 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage ($\overline{\text{SHTDN}}$)	2			V
V_{IL}	Low-level input voltage ($\overline{\text{SHTDN}}$)			0.8	V
$|V_{ID}|$	Differential input voltage	0.1		0.6	V
V_{IC}	Common-mode input voltage (see Figure 2 and Figure 3)	$\dfrac{|V_{ID}|}{2}$		$2.4 - \dfrac{|V_{ID}|}{2}$ $V_{CC} - 0.8$	V
T_A	Operating free-air temperature	0		70	°C

TIMING REQUIREMENTS

		MIN	MAX	UNIT
t_c	Cycle time, input clock[(1)]	14.7	32.3	ns
t_{su1}	Setup time, input (see Figure 7)	600		ps
t_{h1}	Hold time, input (see Figure 7)	600		ps

(1) Parameter t_c is defined as the mean duration of a minimum of 32000 clock cycles.

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage				100	mV
V_{IT-}	Negative-going differential input threshold voltage[2]		−100			mV
V_{OH}	High-level output voltage	I_{OH} = −4 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	V
I_{CC}	Quiescent current (average)	Disabled, All inputs open			280	µA
		Enabled, AnP = 1 V, AnM = 1.4 V, t_c = 15.38 ns		60	74	mA
		Enabled, C_L = 8 pF, Grayscale pattern (see Figure 4), t_c = 15.38 ns		74		
		Enabled, C_L = 8 pF, Worst-case pattern (see Figure 5), t_c = 15.38 ns		107		
I_{IH}	High-level input current ($\overline{SHTDN}$)	V_{IH} = V_{CC}			±20	µA
I_{IL}	Low-level input current ($\overline{SHTDN}$)	V_{IL} = 0			±20	µA
I_{IN}	Input current (LVDS input terminals A and CLKIN)	0 ≤ V_I ≤ 2.4 V			±20	µA
I_{OZ}	High-impedance output current	V_O = 0 or V_{CC}			±10	µA

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) The algebraic convention, in which the less-positive (more-negative) limit is designed minimum, is used in this data sheet for the negative-going input voltage threshold only.

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
t_{su2}	Setup time, D0–D27 valid to CLKOUT↓	C_L = 8 pF, See Figure 6	5			ns
t_{h2}	Hold time, CLKOUT↓ to D0–D27 valid	C_L = 8 pF, See Figure 6	5			ns
t_{RSKM}	Receiver input skew margin[2] (see Figure 7)	t_c = 15.38 ns (± 0.2%), |Input clock jitter| < 50 ps[3]	490			ps
t_d	Delay time, CLKIN↑ to CLKOUT↓ (see Figure 7)	t_c = 15.38 ns (± 0.2%), C_L = 8 pF		3.7		ns
$\Delta t_{c(o)}$	Cycle time, change in output clock period[4]	t_c = 15.38 + 0.75 sin (2π500E3t) ± 0.05 ns, See Figure 8		±80		ps
		t_c = 15.38 + 0.75 sin (2π3E6t) ± 0.05 ns, See Figure 8		±300		
t_{en}	Enable time, $\overline{SHTDN}$↑ to Dn valid	See Figure 9		1		ms
t_{dis}	Disable time, $\overline{SHTDN}$↓ to off state	See Figure 10		400		ns
t_t	Transition time, output (10% to 90% t_r or t_f)	C_L = 8 pF		3		ns
t_w	Pulse duration, output clock			0.43 t_c		ns

(1) All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
(2) The parameter $t_{(RSKM)}$ is the timing margin available to the transmitter and interconnection skews and clock jitter. It is defined by $t_c/14 − t_{su1}/t_{h1}$.
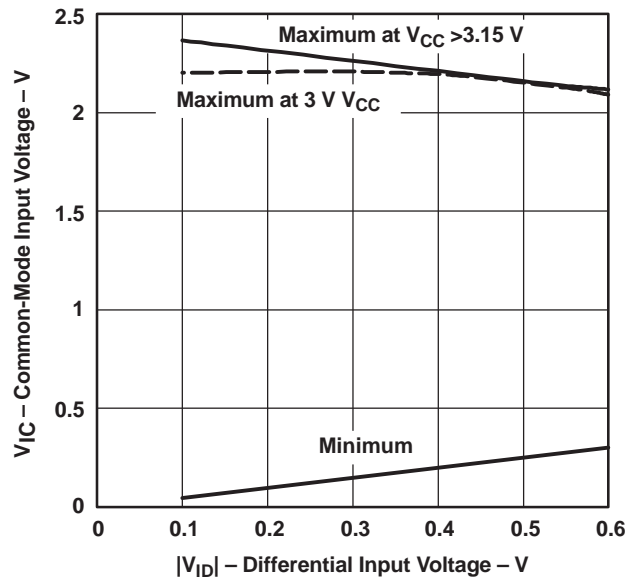(3) \|Input clock jitter\| is the magnitude of the change in input clock period.
(4) $\Delta t_{c(o)}$ is the change in the output clock period from one cycle to the next cycle observed over 15000 cycles.

PARAMETER MEASUREMENT INFORMATION
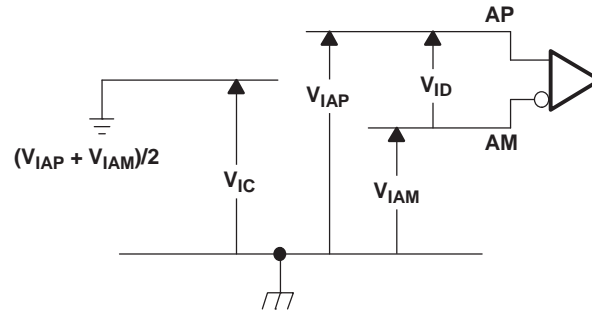
Figure 2. Voltage Definitions

Figure 3. Common-Mode Input Voltage vs Differential Input Voltage
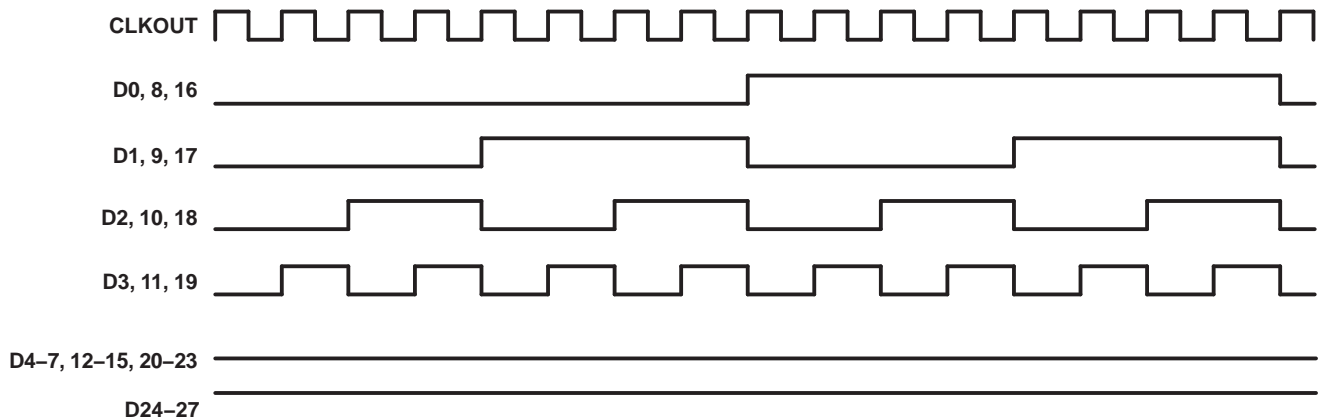
NOTE A: The 16-grayscale test-pattern tests device power consumption for a typical display pattern.

Figure 4. 16-Grayscale Test-Pattern Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)
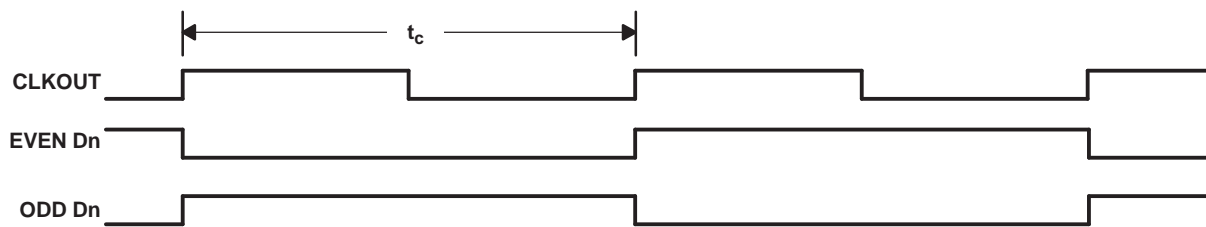
NOTE A: The worst-case test pattern produces the maximum switching frequency for all of the outputs.

Figure 5. Worst-Case Test-Pattern Waveforms
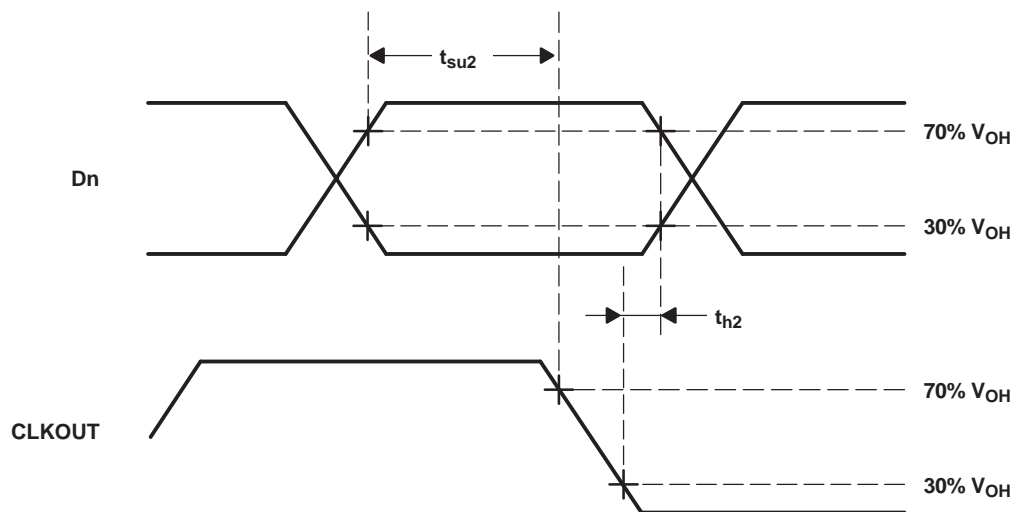
Figure 6. Setup and Hold Time Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)
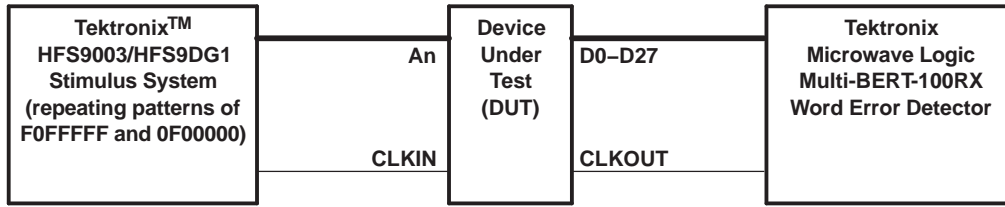
A. CLKIN is advanced or delayed with respect to data until errors are observed at the receiver outputs. The magnitude of the advance or delay is $t_{(RSKM)}$.
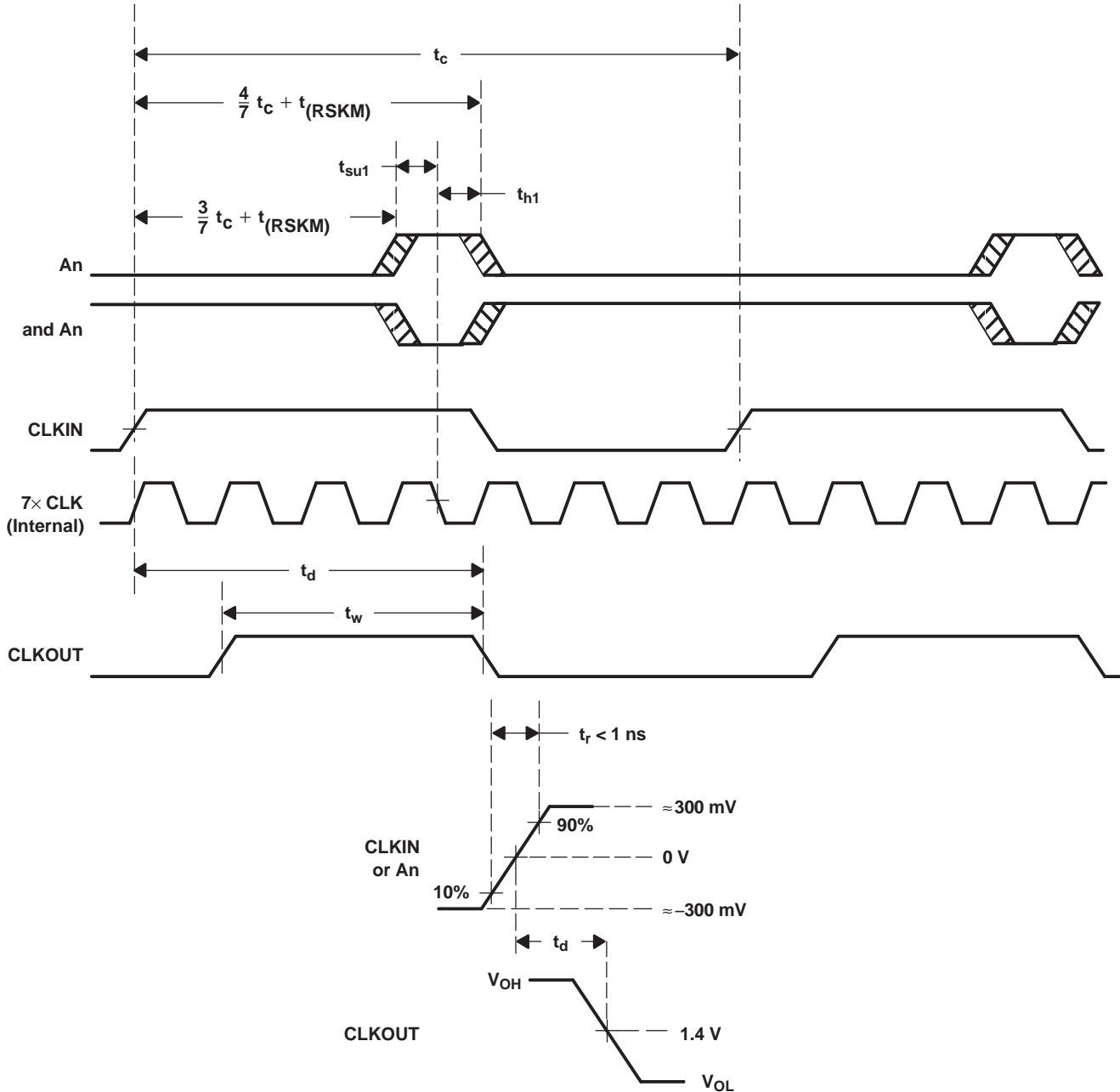
Figure 7. Receiver Input Skew Margin and Delay Timing Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

$$V(t) = A \sin (2 \pi f_{(mod)} t)$$

Figure 8. Input Clock Jitter Test

Figure 9. Enable Time Waveforms

Figure 10. Disable Time Waveforms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
CLOCK FREQUENCY

Figure 11.

ZERO-TO-PEAK OUTPUT JITTER
vs
MODULATION FREQUENCY

Figure 12.

APPLICATION INFORMATION

Host	Cable	Flat Panel Display

SN75LVDS81

Host pin		Display pin	
Y0M	48	9	A0M
Y0P	47	10	A0P
Y1M	46	11	A1M
Y1P	45	12	A1P
Y2M	42	15	A2M
Y2P	41	16	A2P
Y3M	38	19	A3M
Y3P	37	20	A3P
CLKOUTM	40	17	CLKINM
CLKOUTP	39	18	CLKINP

100 Ω terminating resistors (five)

SN75LVDS82

Graphic Controller

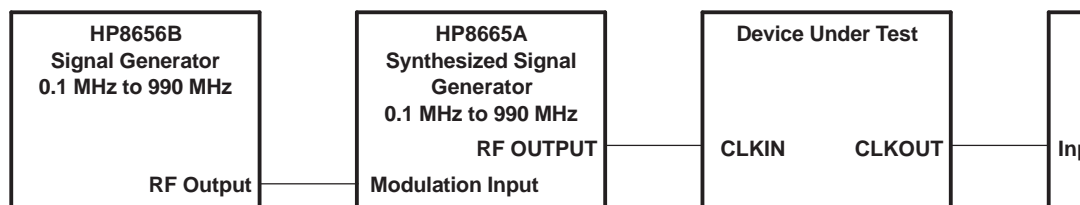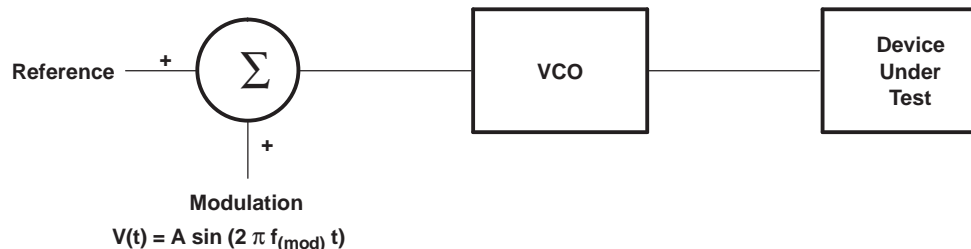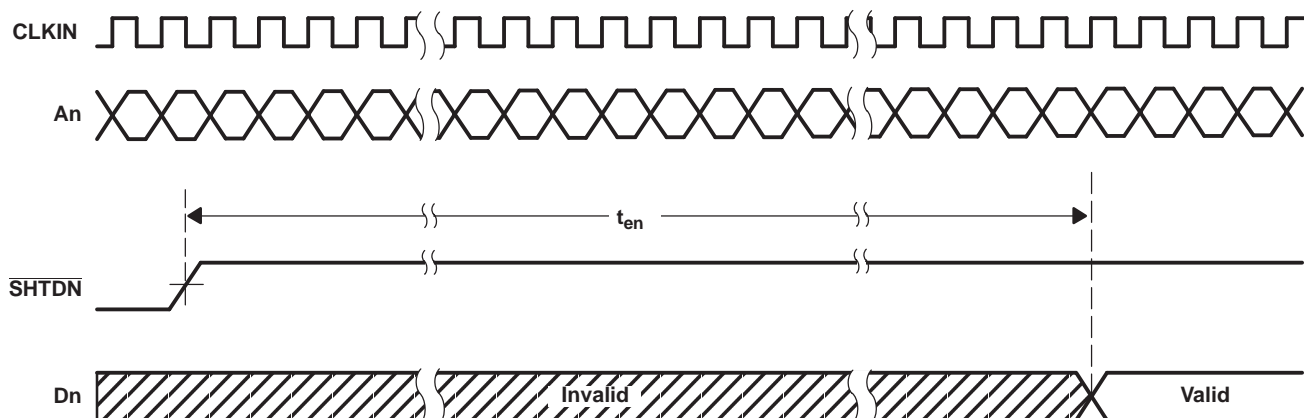|	Pin	12-BIT	18-BIT	24-BIT
D0	27	RED0	RED0	RED0
D1	29	RED1	RED1	RED1
D2	30	RED2	RED2	RED2
D3	32	RED3	RED3	RED3
D4	33	RSVD	RED4	RED4
D6	35	RSVD	RED5	RED5
D27	7	NA	NA	RED6
D5	34	NA	NA	RED7
D7	37	GREEN0	GREEN0	GREEN0
D8	38	GREEN1	GREEN1	GREEN1
D9	39	GREEN2	GREEN2	GREEN2
D12	43	GREEN3	GREEN3	GREEN3
D13	45	RSVD	GREEN4	GREEN4
D14	46	RSVD	GREEN5	GREEN5
D10	41	NA	NA	GREEN6
D11	42	NA	NA	GREEN7
D15	47	BLUE0	BLUE0	BLUE0
D18	51	BLUE1	BLUE1	BLUE1
D19	53	BLUE2	BLUE2	BLUE2
D20	54	BLUE3	BLUE3	BLUE3
D21	55	RSVD	BLUE4	BLUE4
D22	1	RSVD	BLUE5	BLUE5
D16	49	NA	NA	BLUE6
D17	50	NA	NA	BLUE7
D24	3	H_SYNC	H_SYNC	H_SYNC
D25	5	V_SYNC	V_SYNC	V_SYNC
D26	6	ENABLE	ENABLE	ENABLE
D23	2	NA	NA	RSVD
CLKOUT	26	CLOCK	CLOCK	CLOCK

A. The five 100-Ω terminating resistors are recommended to be 0603 types.

B. NA — not applicable, these unused inputs should be left open.

Figure 13. 24-Bit Color Host to 24-Bit LCD Flat Panel Display Application

Host	Cable	Flat Panel Display		Graphic Controller		

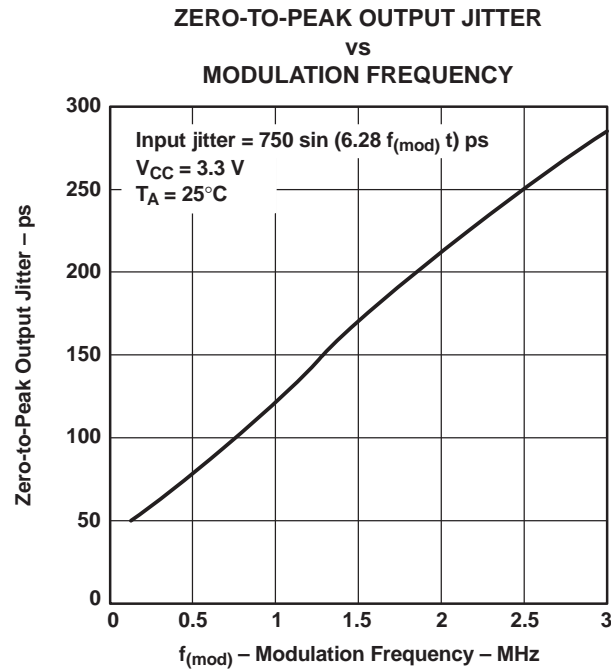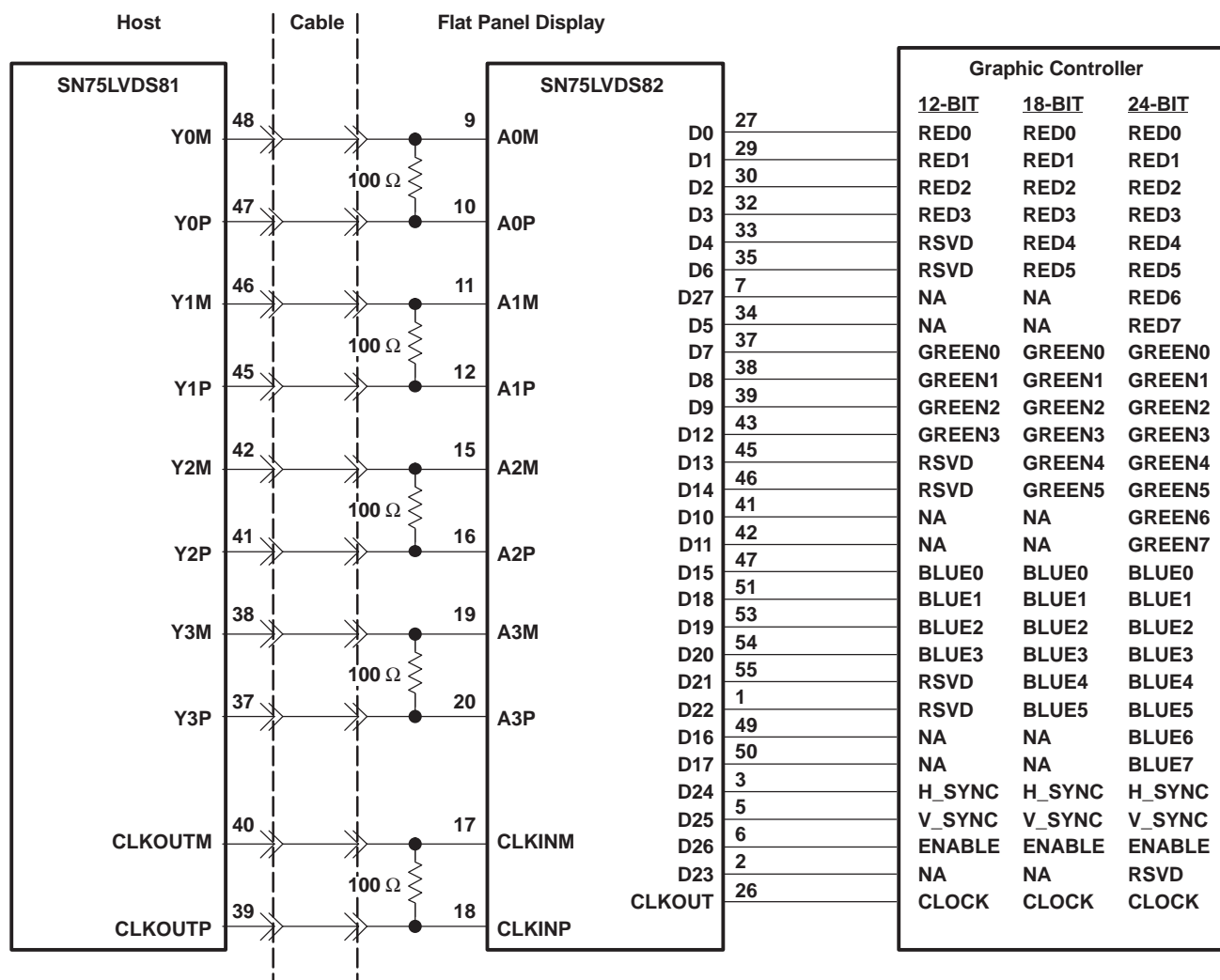| SN75LVDS84/85				SN75LVDS82			12-BIT	18-BIT	24-BIT
Y0M	41	9	A0M	D0	27		RED0	RED0	RED0
				D1	29		RED1	RED1	RED1
		100 Ω		D2	30		RED2	RED2	RED2
Y0P	40	10	A0P	D3	32		RED3	RED3	RED3
				D4	33		RSVD	RED4	RED4
				D6	35		RSVD	RED5	RED5
Y1M	39	11	A1M	D27	7		NA	NA	RED6
				D5	34		NA	NA	RED7
		100 Ω		D7	37		GREEN0	GREEN0	GREEN0
Y1P	38	12	A1P	D8	38		GREEN1	GREEN1	GREEN1
				D9	39		GREEN2	GREEN2	GREEN2
				D12	43		GREEN3	GREEN3	GREEN3
Y2M	35	15	A2M	D13	45		RSVD	GREEN4	GREEN4
				D14	46		RSVD	GREEN5	GREEN5
		100 Ω		D10	41		NA	NA	GREEN6
Y2P	34	16	A2P	D11	42		NA	NA	GREEN7
				D15	47		BLUE0	BLUE0	BLUE0
		19	A3M	D18	51		BLUE1	BLUE1	BLUE1
				D19	53		BLUE2	BLUE2	BLUE2
				D20	54		BLUE3	BLUE3	BLUE3
		20	A3P	D21	55		RSVD	BLUE4	BLUE4
				D22	1		RSVD	BLUE5	BLUE5
				D16	49		NA	NA	BLUE6
				D17	50		NA	NA	BLUE7
CLKOUTM	40	17	CLKINM	D24	3		H_SYNC	H_SYNC	H_SYNC
				D25	5		V_SYNC	V_SYNC	V_SYNC
		100 Ω		D26	6		ENABLE	ENABLE	ENABLE
CLKOUTP	39	18	CLKINP	D23	2		NA	NA	RSVD
				CLKOUT	26		CLOCK	CLOCK	CLOCK

A. The four 100-Ω terminating resistors are recommended to be 0603 types.

B. NA — not applicable, these unused inputs should be left open.

Figure 14. 18-Bit Color Host to 24-Bit Color LCD Panel Display Application

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN75LVDS82DGG	ACTIVE	TSSOP	DGG	56	35	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS82	Samples
SN75LVDS82DGGG4	ACTIVE	TSSOP	DGG	56	35	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS82	Samples
SN75LVDS82DGGR	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS82	Samples
SN75LVDS82DGGRG4	ACTIVE	TSSOP	DGG	56	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	SN75LVDS82	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LVDS82DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LVDS82DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0

8.3
7.9 TYP

PIN 1 ID
AREA

A

1

54X ⌴0.5⌴

56

C

SEATING PLANE

⌓ 0.1 C

14.1
13.9
NOTE 3

2X
13.5

28

29

B

6.2
6.0

56X 0.27
0.17

⊕ 0.08Ⓜ C AⓈ BⓈ

1.2 MAX

(0.15) TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

0.75
0.50

0.15
0.05

DETAIL A
TYPICAL
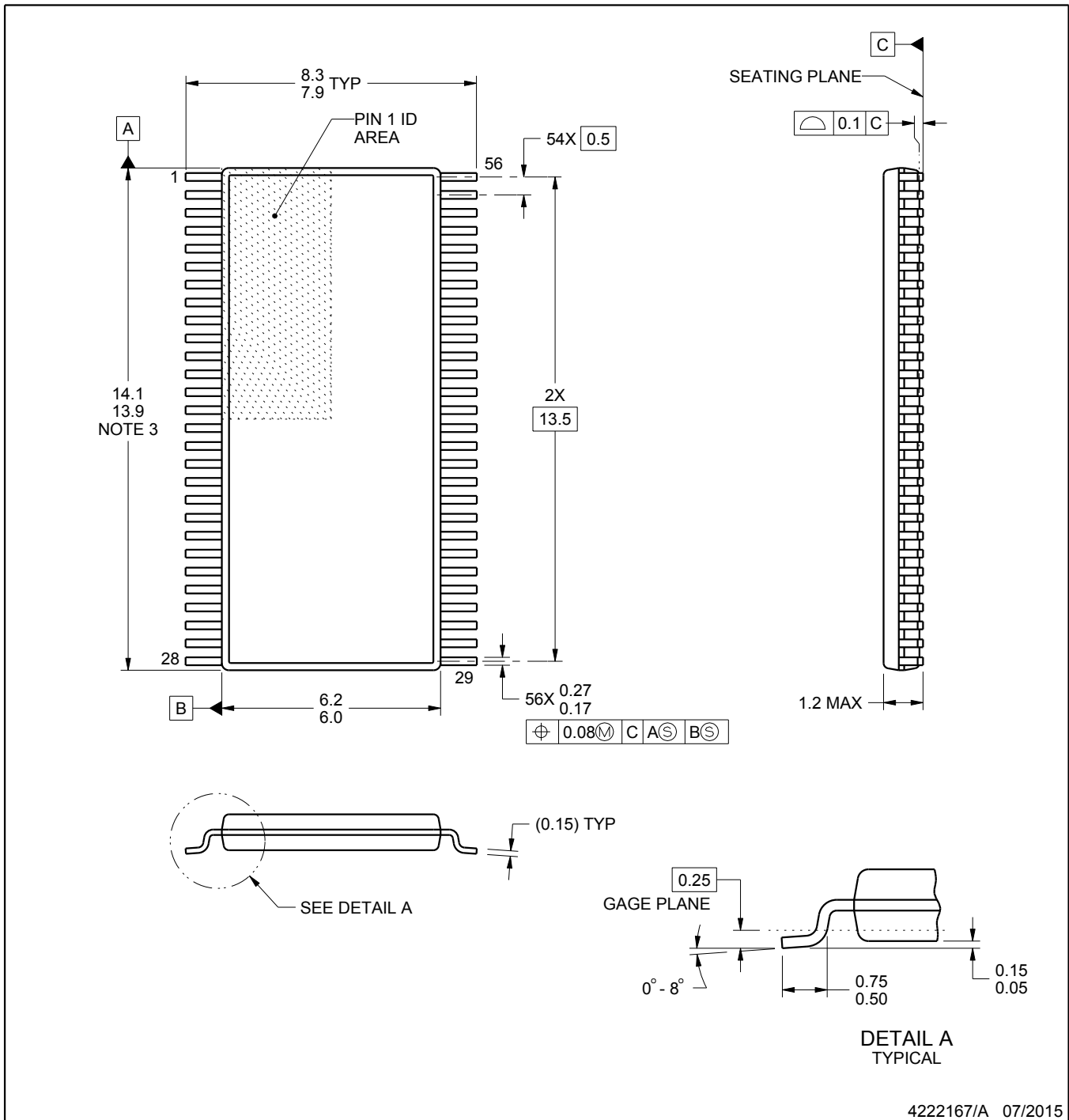
4222167/A 07/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

56X (1.5)

1

56X (0.3)

SYMM

56

54X (0.5)

(R0.05)
TYP

SYMM

28

29

(7.5)
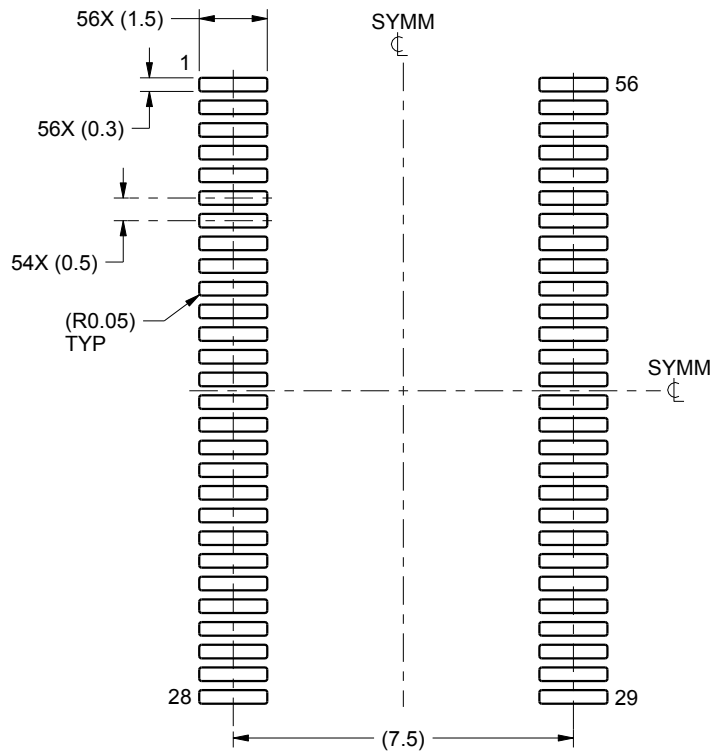
LAND PATTERN EXAMPLE
SCALE:6X

SOLDER MASK
OPENING

METAL

0.05 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED
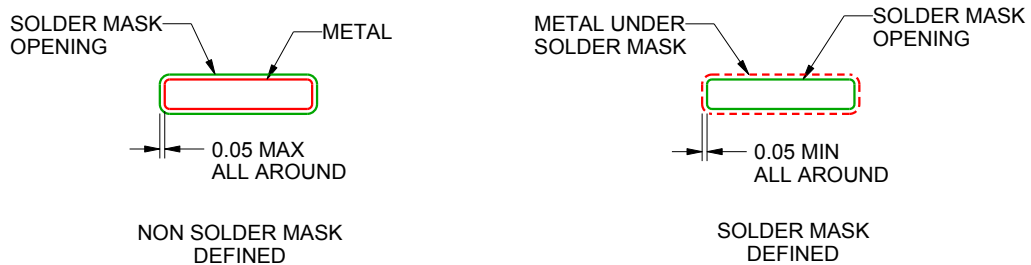
SOLDER MASK DETAILS

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NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DGG0056A

56X (1.5)

1

SYMM

56

56X (0.3)

54X (0.5)

(R0.05) TYP

SYMM

28

29

(7.5)
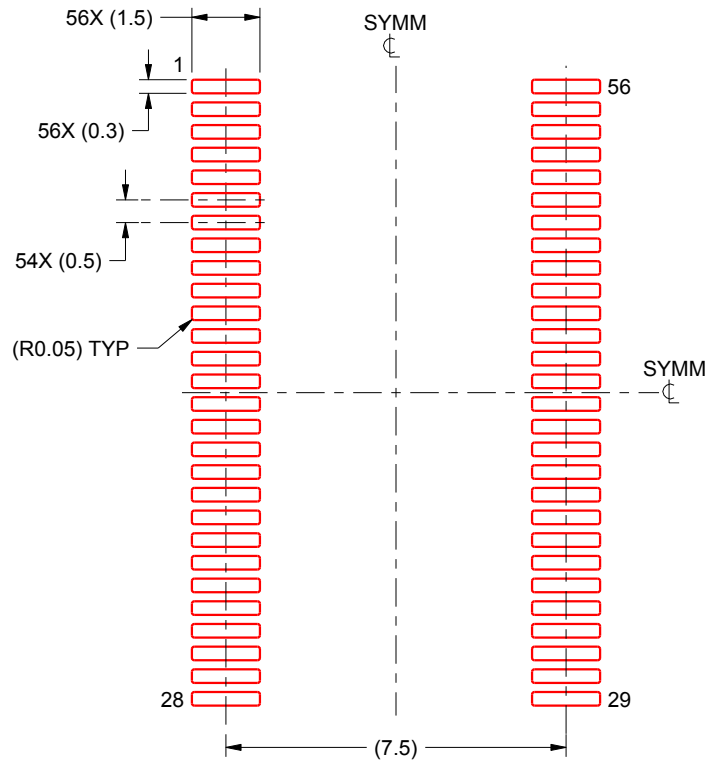
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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