

SN54HC259, SN74HC259 8-BIT ADDRESSABLE LATCHES

SCLS134B – DECEMBER 1982 – REVISED MAY 1997

- **8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion With Storage**
- **Asynchronous Parallel Clear**
- **Active-High Decoder**
- **Enable Input Simplifies Expansion**
- **Expandable for n-Bit Applications**
- **Four Distinct Functional Modes**
- **Package Options Include Plastic Small-Outline (D), Thin Shrink Small-Outline (PW), and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

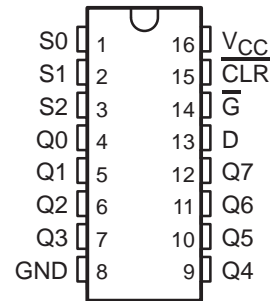
description

These 8-bit addressable latches are designed for general-purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

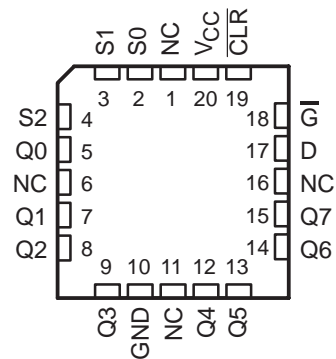
Four distinct modes of operation are selectable by controlling the clear ($\overline{\text{CLR}}$) and enable ($\overline{\text{G}}$) inputs. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch follows the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, $\overline{\text{G}}$ should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output follows the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

The SN54HC259 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74HC259 is characterized for operation from -40°C to 85°C .

SN54HC259 . . . J OR W PACKAGE
SN74HC259 . . . D, N, OR PW PACKAGE
(TOP VIEW)



SN54HC259 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1997, Texas Instruments Incorporated

SN54HC259, SN74HC259 8-BIT ADDRESSABLE LATCHES

SCLS134B – DECEMBER 1982 – REVISED MAY 1997

Function Tables

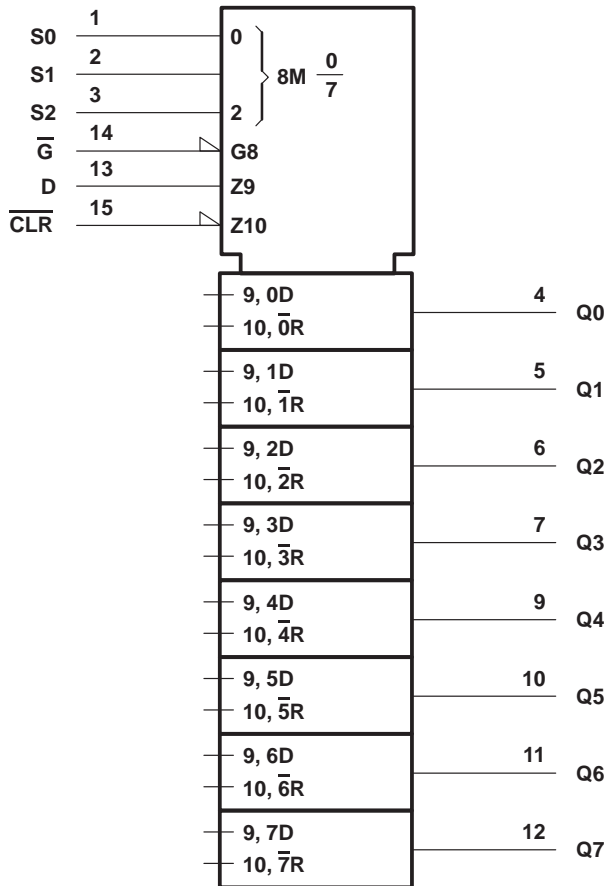
FUNCTION

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
$\overline{\text{CLR}}$	$\overline{\text{G}}$			
H	L	D	Q_iO	Addressable latch
H	H	Q_iO	Q_iO	Memory
L	L	D	L	8-line demultiplexer
L	H	L	L	Clear

LATCH SELECTION

SELECT INPUTS			LATCH ADDRESSED
S2	S1	S0	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

logic symbol†

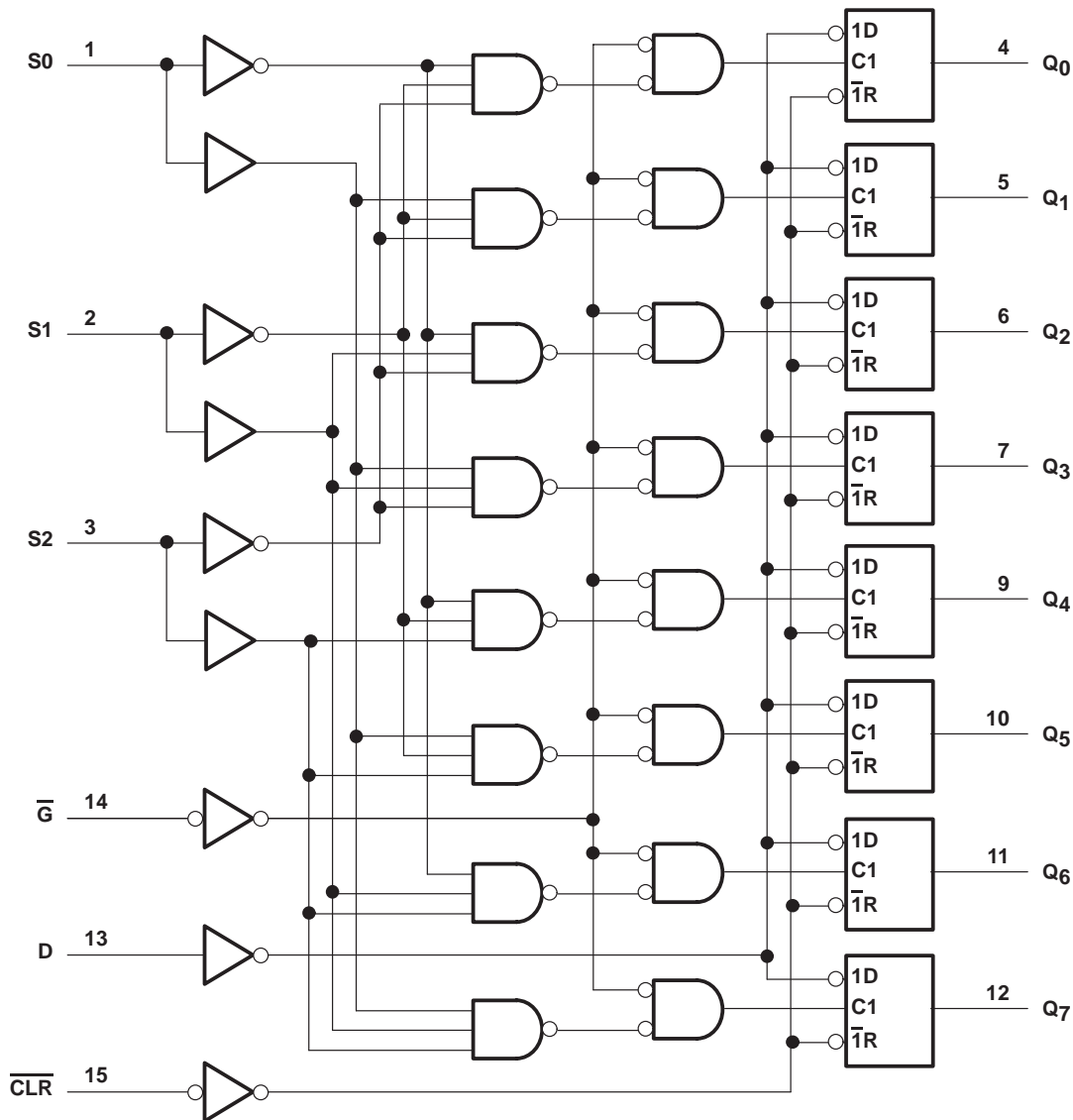


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, PW, and W packages.

SN54HC259, SN74HC259 8-BIT ADDRESSABLE LATCHES

SCLS134B – DECEMBER 1982 – REVISED MAY 1997

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, PW, and W packages.

SN54HC259, SN74HC259 8-BIT ADDRESSABLE LATCHES

SCLS134B – DECEMBER 1982 – REVISED MAY 1997

recommended operating conditions

		SN54HC259			SN74HC259			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	2	5	6	2	5	6	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5		1.5		V	
		$V_{CC} = 4.5\text{ V}$	3.15		3.15			
		$V_{CC} = 6\text{ V}$	4.2		4.2			
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$	0	0.5	0	0.5	V	
		$V_{CC} = 4.5\text{ V}$	0	1.35	0	1.35		
		$V_{CC} = 6\text{ V}$	0	1.8	0	1.8		
V_I	Input voltage	0	V_{CC}		0	V_{CC}		V
V_O	Output voltage	0	V_{CC}		0	V_{CC}		V
t_t	Input transition (rise and fall) time	$V_{CC} = 2\text{ V}$	0	1000	0	1000	ns	
		$V_{CC} = 4.5\text{ V}$	0	500	0	500		
		$V_{CC} = 6\text{ V}$	0	400	0	400		
T_A	Operating free-air temperature	-55	125		-40	85		°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	$T_A = 25^\circ\text{C}$			SN54HC259		SN74HC259		UNIT	
				MIN	TYP	MAX	MIN	MAX	MIN	MAX		
V_{OH}	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20\ \mu\text{A}$	2 V	1.9	1.998		1.9		1.9	V		
			4.5 V	4.4	4.499		4.4		4.4			
			6 V	5.9	5.999		5.9		5.9			
		$I_{OH} = -4\text{ mA}$	4.5 V	3.98	4.3		3.7		3.84			
		$I_{OH} = -5.2\text{ mA}$	6 V	5.48	5.8		5.2		5.34			
V_{OL}	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20\ \mu\text{A}$	2 V		0.002	0.1		0.1		V		
			4.5 V		0.001	0.1		0.1			0.1	
			6 V		0.001	0.1		0.1			0.1	
		$I_{OL} = 4\text{ mA}$	4.5 V		0.17	0.26		0.4			0.33	
		$I_{OL} = 5.2\text{ mA}$	6 V		0.15	0.26		0.4			0.33	
I_I	$V_I = V_{CC}$ or 0		6 V		± 0.1	± 100		± 1000		± 1000	nA	
I_{CC}	$V_I = V_{CC}$ or 0, $I_O = 0$		6 V				8		160		80	μA
C_i			2 V to 6 V		3	10		10			10	pF



SN54HC259, SN74HC259 8-BIT ADDRESSABLE LATCHES

SCLS134B – DECEMBER 1982 – REVISED MAY 1997

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V _{CC}	T _A = 25°C		SN54HC259		SN74HC259		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	$\overline{\text{CLR}}$ low	2 V	80	120	100	ns		
			4.5 V	16	24	20			
			6 V	14	20	17			
	$\overline{\text{G}}$ low	2 V	80	120	100				
		4.5 V	16	24	20				
		6 V	14	20	17				
t _{su}	Setup time, data or address before $\overline{\text{G}}\uparrow$	2 V	75	115	95	ns			
		4.5 V	15	23	19				
		6 V	13	20	16				
t _h	Hold time, data or address after $\overline{\text{G}}\uparrow$	2 V	5	5	5	ns			
		4.5 V	5	5	5				
		6 V	5	5	5				

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC}	T _A = 25°C			SN54HC259		SN74HC259		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PHL}	$\overline{\text{CLR}}$	Any Q	2 V	60	150	225	190	ns			
			4.5 V	18	30	45	38				
			6 V	14	26	38	32				
t _{pd}	Data	Any Q	2 V	56	130	195	165	ns			
			4.5 V	17	26	39	33				
			6 V	13	22	33	28				
	Address	Any Q	2 V	74	200	300	250				
			4.5 V	21	40	60	50				
			6 V	17	34	51	43				
	$\overline{\text{G}}$	Any Q	2 V	66	170	255	215				
			4.5 V	20	34	51	43				
			6 V	16	29	43	37				
t _t		Any	2 V	28	75	110	95	ns			
			4.5 V	8	15	22	19				
			6 V	6	13	19	16				

operating characteristics, T_A = 25°C

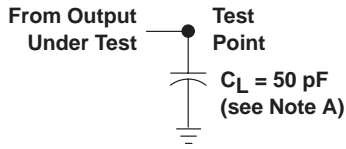
PARAMETER	TEST CONDITIONS	TYP	UNIT
C _{pd} Power dissipation capacitance per latch	No load	33	pF



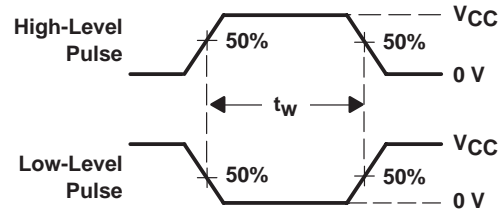
SN54HC259, SN74HC259 8-BIT ADDRESSABLE LATCHES

SCLS134B – DECEMBER 1982 – REVISED MAY 1997

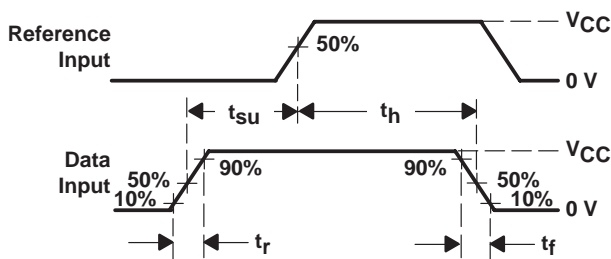
PARAMETER MEASUREMENT INFORMATION



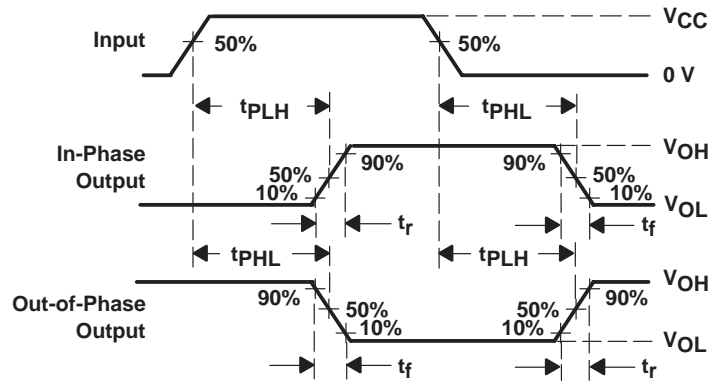
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

- NOTES:
- C_L includes probe and test-fixture capacitance.
 - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r = 6 \text{ ns}$, $t_f = 6 \text{ ns}$.
 - The outputs are measured one at a time with one input transition per measurement.
 - t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.