具有关断功能的 OPAx357 250MHz、轨至轨 I/O、CMOS 运算放大器

1 特性

- 单位增益带宽：250MHz
- 带宽：100MHz GBW
- 高转换率：150V/µs
- 低噪声：$6.5nV/\sqrt{Hz}$
- 轨至轨 I/O
- 高输出电流：> 100mA
- 出色的视频性能：
  - 差分增益：0.02%，差分相位：0.09°
  - 0.1dB 增益平坦度：40MHz
- 低输入偏置电流：3pA
- 静态电流：4.9mA
- 热关断
- 电源范围：2.5V 至 5.5V
- 关断 $I_Q < 6\mu A$
- *微型*封装
- 使用 OPA357 并借助 WEBENCH® 电源设计器创建定制设计方案

2 应用

- 视频处理
- 超声波
- 光网络、可调激光器
- 光电二极管互阻放大器
- 有源滤波器
- 高速积分器
- 模数 (A/D) 转换器输入缓冲器
- 数模 (D/A) 转换器输出放大器
- 条形码扫描器
- 通信

3 说明

OPA357 系列高速电压反馈 CMOS 运算放大器专为视频应用和其他需要宽带宽的 应用 而设计。这些器件具有单位增益稳定性，可以驱动大型输出电流。差分增益为 0.02%，而差分相位为 0.09°。静态电流仅为每通道 4.9mA。

OPA357 系列运算放大器针对低至 2.5V (±1.25V) 和高达 5.5V (±2.75V) 的单电源或双电源供电运行进行了优化。共模输入范围超出电源供电范围。电源轨的输出摆幅在 100mV 以内，从而支持宽动态范围。

单电源版本 (OPA357) 采用小型 SOT23-6 封装。双电源版本 (OPA2357) 采用 VSSOP-10 封装。

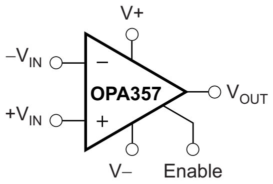
双电源版本 具有 完全独立的电路，可将串扰降到最低并彻底消除相互干扰。两个版本的额定扩展工作温度范围为 –40°C 至 +125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA357	SOT23 (6)	2.90mm × 1.60mm
OPA2357	VSSOP (10)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



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4 修订历史记录

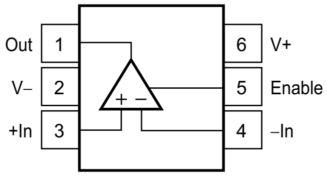
注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (May 2009) to Revision F **Page**

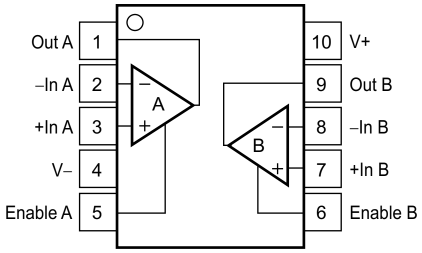
- 已添加 添加了*器件信息* 表、*引脚功能* 表、*ESD 额定值* 表、*建议运行条件* 表、*热性能信息* 表、*概述* 部分、*功能块图* 部分、*特性 说明* 部分，*器件功能模式* 部分，*应用和实施* 部分，*电源相关建议* 部分，*布局* 部分，*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1
- 已更改 在整篇文档中将*MSOP* 更改为 *VSSOP* 1
- 已删除 在文档中删除了 DDA 封装 (SO-8 PowerPAD) 1
- 已更改 在整篇文档中将*MSOP* 更改为 *VSSOP* 1
- 已添加 WEBENCH *特性*特性项目符号中添加了器件 HBM 和 CDM 分类子项目符号 1
- Deleted OADI from DBV pin drawing 3
- Deleted *Package/Ordering Information* table 4
- Deleted footnote from *Signal input pins* parameter in *Absolute Maximum Ratings* table 4
- Changed *Temperature Range* section of *Electrical Characteristics* table: changed θ_{JA} to $R_{\theta JA}$ and deleted *Specified range*, *Operating range*, and *Storage range* parameters 6
- Added *OPAx357 Comparison* section and moved *OPAx357 Related Products* table to this section from page 1 14
- Deleted first paragraph of *Power Dissipation* section 26
- Changed *PCB Layout* title to *Layout Guidelines* 26
- Deleted *PowerPAD Thermall Enhanced Package* and *PowerPAD Assembly Process* sections 26
- 已添加 添加了*借助 WEBENCH® 工具定制设计方案* 部分 27

5 Pin Configuration and Functions

OPA357: DBV Package
6-Pin SOT-23
Top View



OPA2357: DGS Package
10-Pin VSSOP
Top View



(1) Pin 1 of the SOT23-6 is determined by orienting the package marking as indicated in the diagram.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	DBV (SOT-23)	DGS (VSSOP)		
Enable	5	—	—	Amplifier power down. Low = disabled, high = normal operation (pin must be driven).
Enable A	—	5	—	Amplifier power down, channel A. Low = disabled, high = normal operation (pin must be driven).
Enable B	—	6	—	Amplifier power down, channel B. Low = disabled, high = normal operation (pin must be driven).
–In	4	—	I	Inverting input pin
–In A	—	2	I	Inverting input pin, channel A
–In B	—	8	I	Inverting input pin, channel B
+In	3	—	I	Noninverting input pin
+In A	—	3	I	Noninverting input pin, channel A
+In B	—	7	I	Noninverting input pin, channel B
Out	1	—	O	Output pin
Out A	—	1	O	Output pin, channel A
Out B	—	9	O	Output pin, channel B
V–	2	4	—	Negative power supply
V+	6	10	—	Positive power supply

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Supply voltage, V+ to V−			7.5	V
Signal input pins	Voltage	(V–) – 0.5	(V+) + 0.5	V
	Current		10	mA
Enable input		(V–) – 0.5	(V+) + 0.5	V
Output short-circuit(2)		Continuous		
Operating temperature		–55	150	°C
Junction temperature			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage			5.5	V
T_A	Ambient temperature	–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		OPA357	OPA2357	UNIT
		DBV (SOT-23)	DGS (VSSOP)	
		6 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	166.4	171.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	104.6	58.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.9	93.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.6	6.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.7	91.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: V_S = +2.7-V to +5.5-V Single-Supply

at T_A = 25°C, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = +5 V		±2	±8	mV
		Specified temperature range, T_A = –40°C to +125°C			±10	
dV_{OS}/dT	V_{OS} vs temperature	Specified temperature range, T_A = –40°C to +125°C		±4		µV/°C
PSRR	Power-supply rejection ratio	V_S = +2.7 V to +5.5 V, V_{CM} = (V_S / 2) – 0.55 V		±200	±800	µV/V
		Specified temperature range, T_A = –40°C to +125°C			±900	
INPUT BIAS CURRENT						
I_B	Input bias current			3	±50	pA
I_{OS}	Input offset current			±1	±50	pA
NOISE						
e_n	Input voltage noise density	f = 1 MHz		6.5		nV/√Hz
i_n	Current noise density	f = 1 MHz		50		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = +5.5 V, –0.1 V < V_{CM} < +3.5 V	66	80		dB
		Specified temperature range, T_A = –40°C to +125°C	64			
		V_S = +5.5 V, –0.1 V < V_{CM} < +5.6 V	56	68		
		Specified temperature range, T_A = –40°C to +125°C	55			
INPUT IMPEDANCE						
	Differential			10^{13} || 2		Ω || pF
	Common-mode			10^{13} || 2		Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop gain	V_S = +5 V, +0.3 V < V_O < +4.7 V	94	110		dB
		Specified temperature range, T_A = –40°C to +125°C, V_S = +5 V, +0.4 V < V_O < +4.6 V	90			
FREQUENCY RESPONSE						
$f_{–3dB}$	Small-signal bandwidth	G = +1, V_O = 100 mV_{PP}, R_F = 25 Ω		250		MHz
		G = +2, V_O = 100 mV_{PP}		90		
GBP	Gain-bandwidth product	G = +10		100		MHz
$f_{0.1dB}$	Bandwidth for 0.1-dB gain flatness	G = +2, V_O = 100 mV_{PP}		40		MHz
SR	Slew rate	V_S = +5 V, G = +1, 4-V step		150		V/µs
		V_S = +5 V, G = +1, 2-V step		130		
		V_S = +3 V, G = +1, 2-V step		110		
	Rise-and-fall time	G = +1, V_O = 100 mV_{PP}, 10% to 90%		2		ns
		G = +1, V_O = 2 V_{PP}, 10% to 90%		11		
	Settling time, 0.1%	V_S = +5 V, G = +1, 2-V output step		30		ns
	Settling time, 0.01%			60		ns
	Overload recovery time	V_{IN} × gain = V_S		5		ns
HD2	2nd-order harmonic distortion	G = +1, f = 1 MHz, V_O = 2 V_{PP}, R_L = 200 Ω, V_{CM} = 1.5 V		–75		dBc
HD3	3rd-order harmonic distortion	G = +1, f = 1 MHz, V_O = 2 V_{PP}, R_L = 200 Ω, V_{CM} = 1.5 V		–83		dBc

Electrical Characteristics: V_S = +2.7-V to +5.5-V Single-Supply (continued)

at T_A = 25°C, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FREQUENCY RESPONSE (continued)						
	Differential gain error	NTSC, R_L = 150 Ω		0.02%		
	Differential phase error	NTSC, R_L = 150 Ω		0.09		Degrees
	Channel-to-channel crosstalk, OPA2357	f = 5 MHz		–100		dB
OUTPUT						
	Voltage output swing from rail	V_S = +5 V, R_L = 1 kΩ, A_{OL} > 94 dB		0.1	0.3	V
		Specified temperature range, T_A = –40°C to +125°C, V_S = +5 V, R_L = 1 kΩ, A_{OL} > 90 dB			0.4	
I_O	Output current(1)(2)	V_S = +5 V, single	100			mA
		V_S = +3 V, dual		50		
	Closed-loop output impedance			0.05		Ω
R_O	Open-loop output resistance			35		Ω
POWER SUPPLY						
V_S	Specified voltage range		2.7		5.5	V
	Operating voltage range			2.5 to 5.5		V
I_Q	Quiescent current (per amplifier)	V_S = +5 V, enabled, I_O = 0 V		4.9	6	mA
		Specified temperature range, T_A = –40°C to +125°C			7.5	
ENABLE, SHUTDOWN FUNCTION						
	Disabled (logic−low threshold)				0.8	V
	Enabled (logic−high threshold)		2			V
	Logic input current	Logic low		200		nA
	Turn-on time			100		ns
	Turn-off time			30		ns
	Off isolation	G = +1, 5 MHz, R_L = 10 Ω		74		dB
	Quiescent current (per amplifier)			3.4	6	µA
THERMAL SHUTDOWN						
T_J	Junction temperature	Shutdown		160		°C
		Reset from shutdown		140		
TEMPERATURE RANGE						
$R_{\theta JA}$	Thermal resistance	SOT23-6		150		°C/W
		VSSOP-10		150		

(1) See Figure 21 and Figure 23.
(2) Specified by design.

6.6 Typical Characteristics

at T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2 (unless otherwise noted)

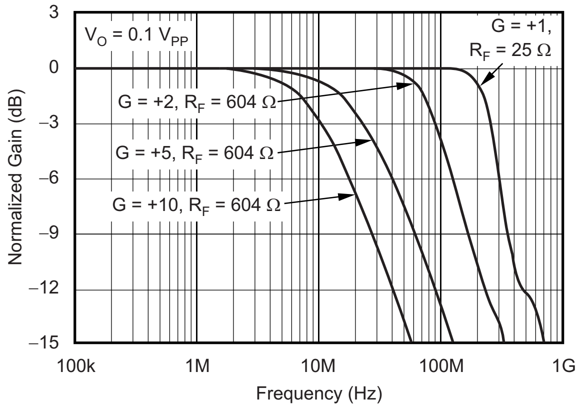


Figure 1. Noninverting Small-Signal Frequency Response

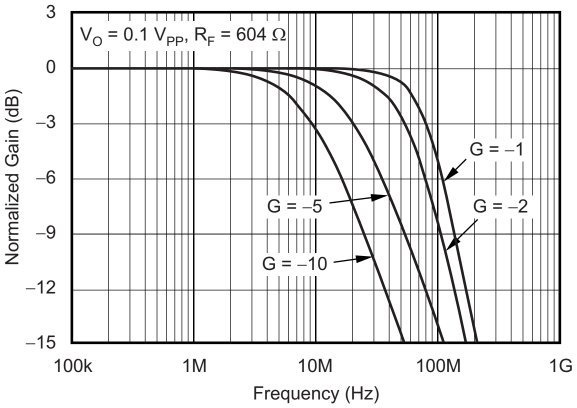


Figure 2. Inverting Small-Signal Frequency Response

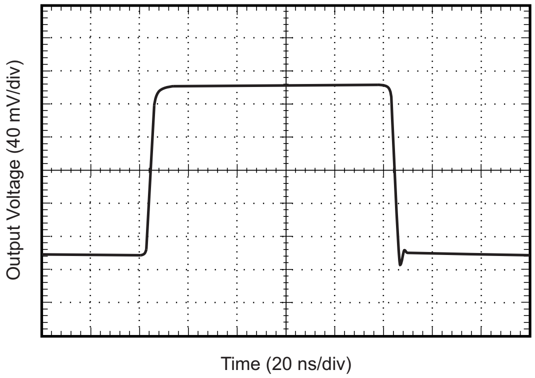


Figure 3. Noninverting Small-Signal Step Response

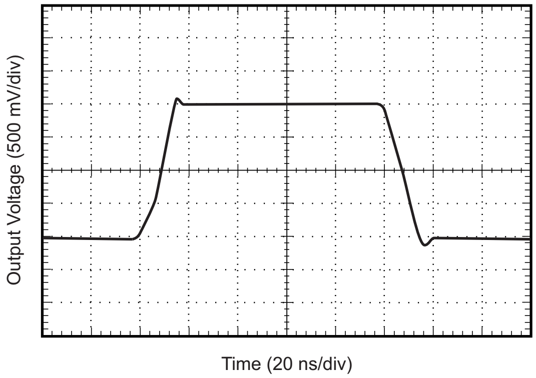


Figure 4. Noninverting Large-Signal Step Response

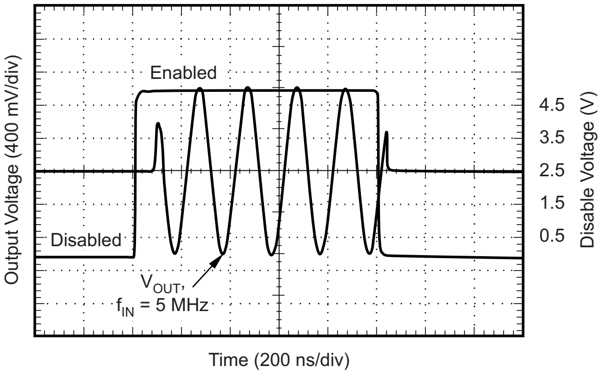


Figure 5. Large-Signal Disable, Enable Response

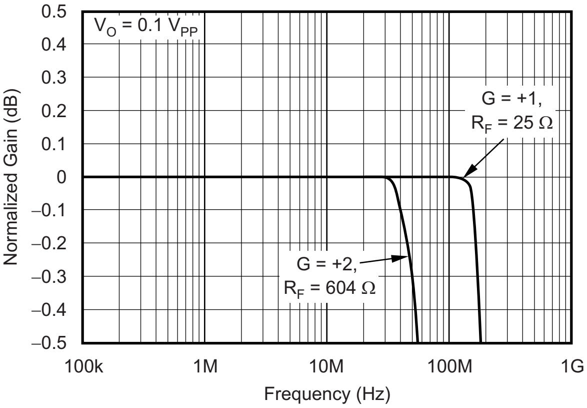


Figure 6. 0.1-dB Gain Flatness

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2 (unless otherwise noted)

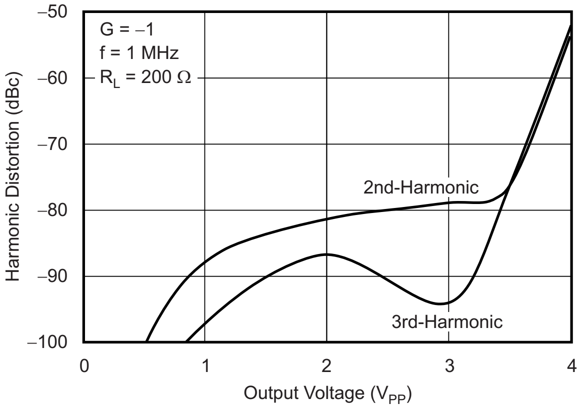


Figure 7. Harmonic Distortion vs Output Voltage

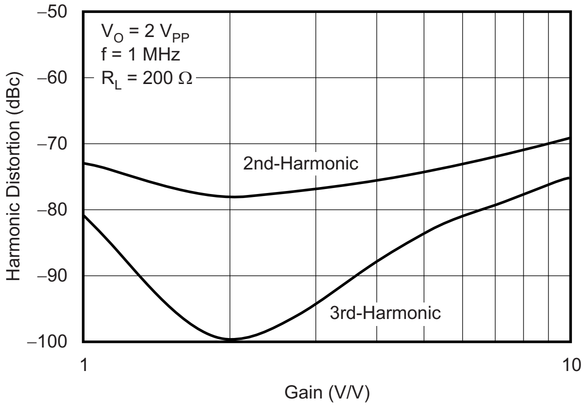


Figure 8. Harmonic Distortion vs Noninverting Gain

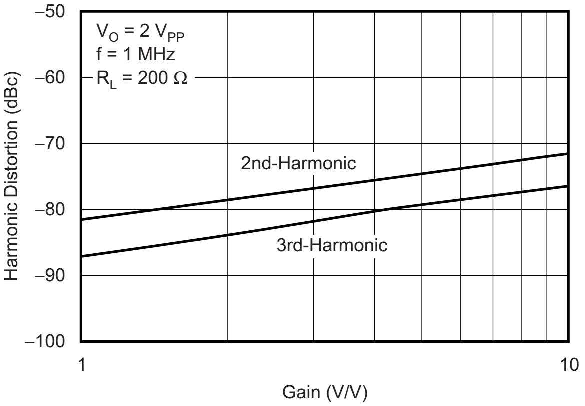


Figure 9. Harmonic Distortion vs Inverting Gain

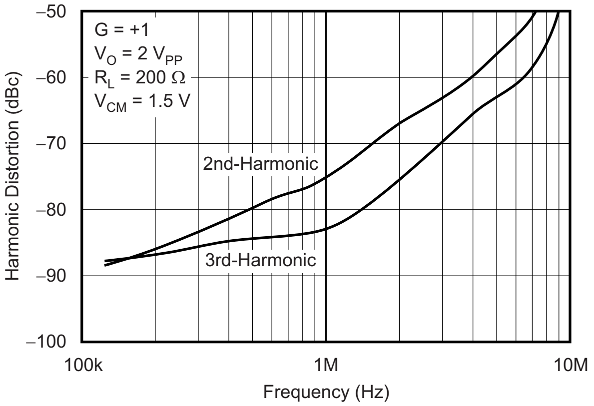


Figure 10. Harmonic Distortion vs Frequency

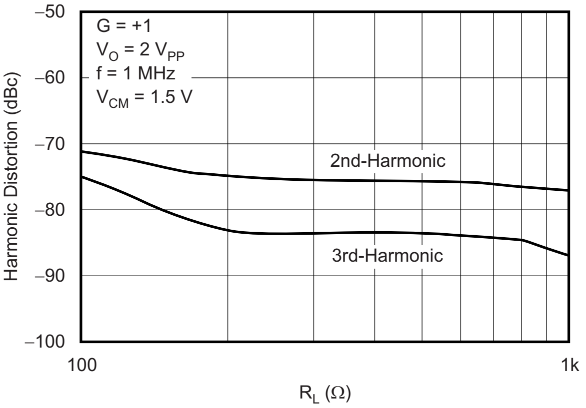


Figure 11. Harmonic Distortion vs Load Resistance

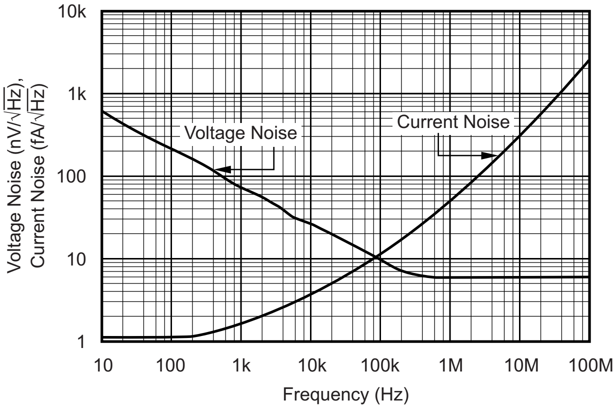


Figure 12. Input Voltage and Current Noise Spectral Density vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2 (unless otherwise noted)

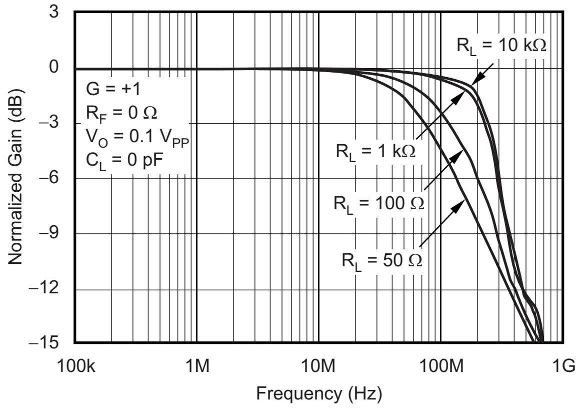


Figure 13. Frequency Response for Various R_L

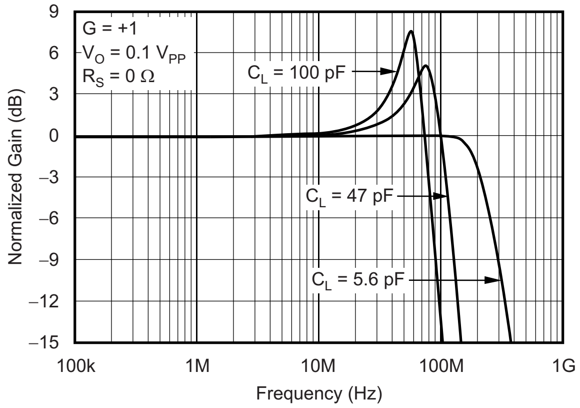


Figure 14. Frequency Response for Various C_L

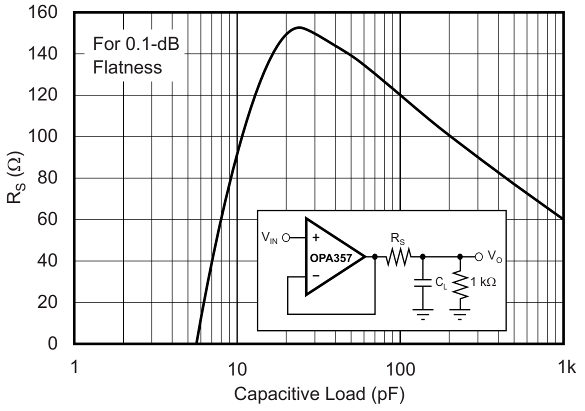


Figure 15. Recommended R_S vs Capacitive Load

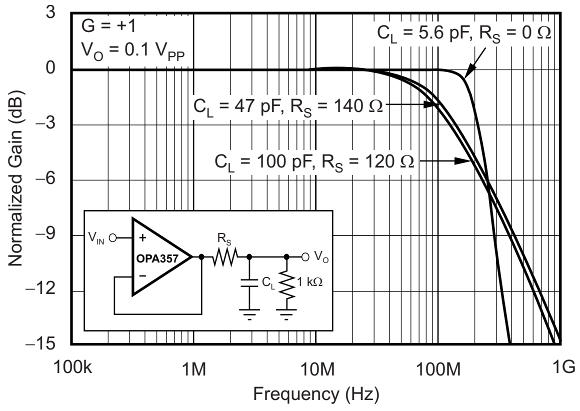


Figure 16. Frequency Response vs Capacitive Load

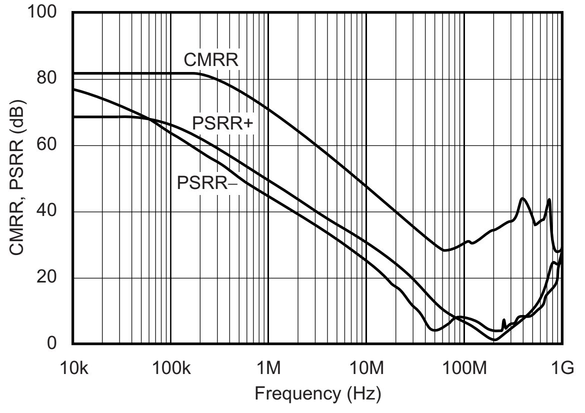


Figure 17. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Frequency

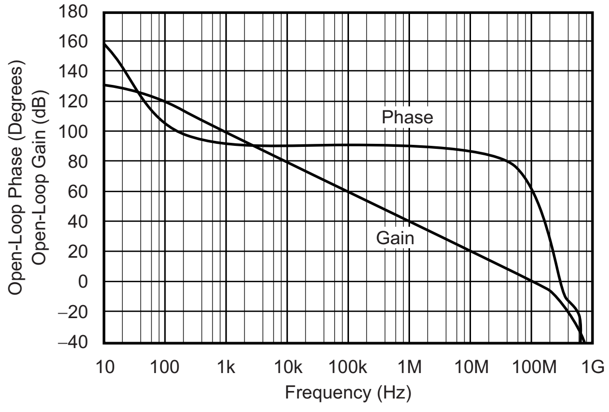


Figure 18. Open-Loop Gain and Phase

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2 (unless otherwise noted)

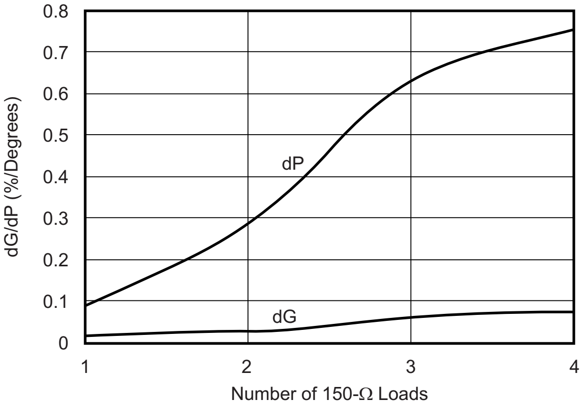


Figure 19. Composite Video differential Gain and Phase

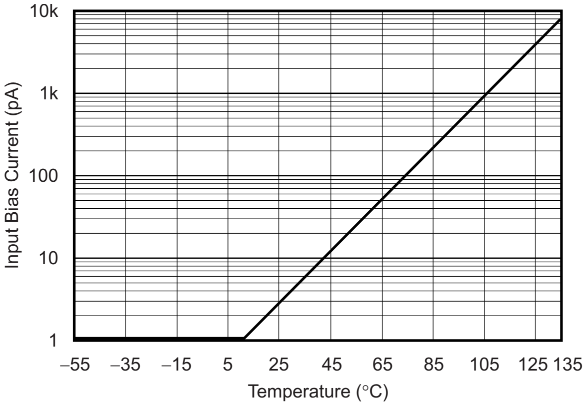


Figure 20. Input Bias Current vs Temperature

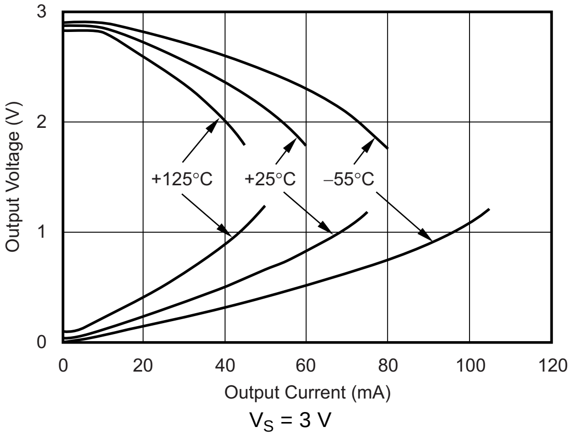


Figure 21. Output Voltage Swing vs Output Current

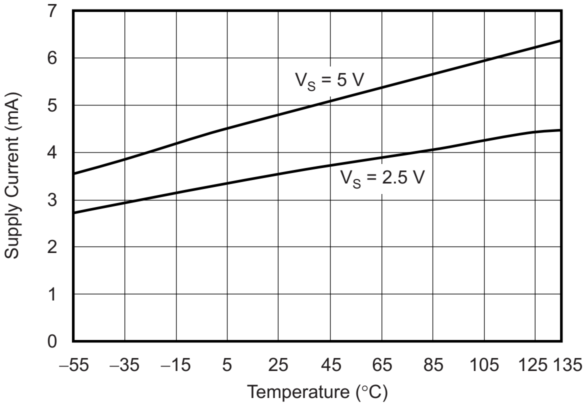


Figure 22. Supply Current vs Temperature

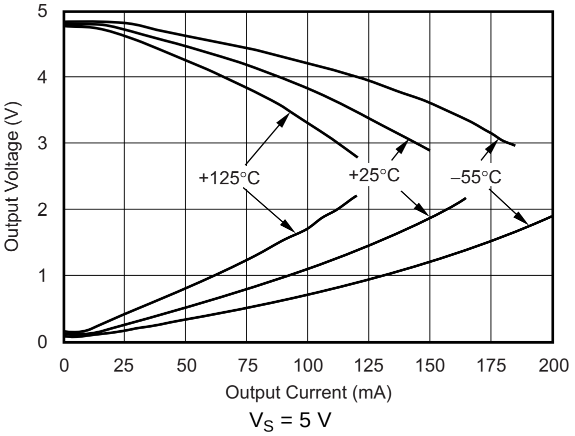


Figure 23. Output Voltage Swing vs Output Current

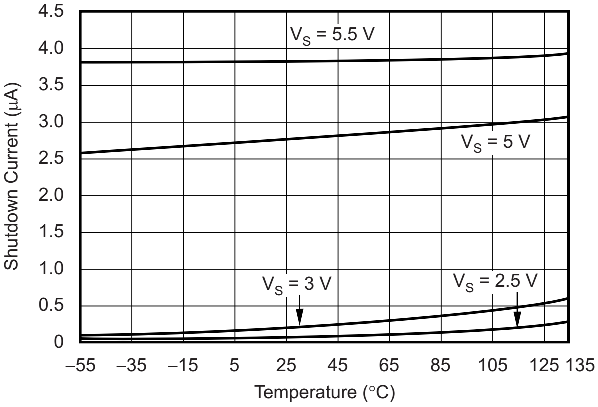


Figure 24. Shutdown Current vs Temperature

Typical Characteristics (continued)

at $T_A = 25°C$, $V_S = 5$ V, G = +1, $R_F = 0\ \Omega$, $R_L = 1\ k\Omega$, and connected to V_S / 2 (unless otherwise noted)

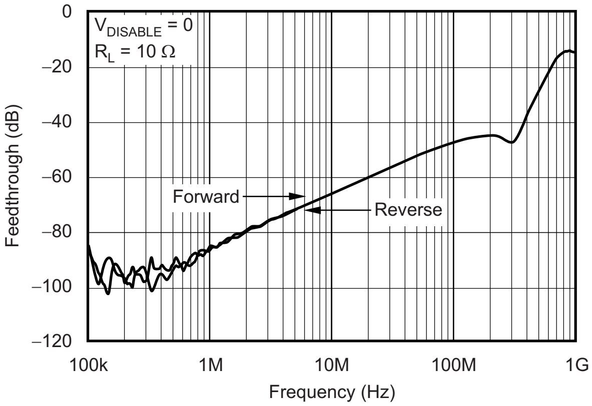


Figure 25. Disable Feedthrough vs Frequency

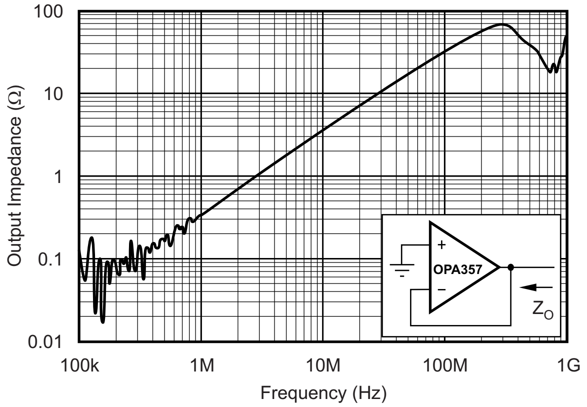


Figure 26. Closed-Loop Output Impedance vs Frequency

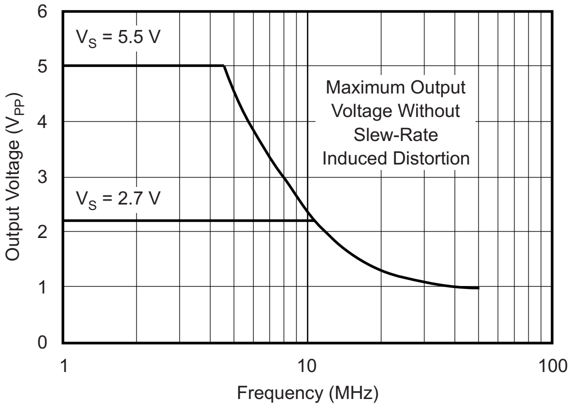


Figure 27. Maximum Output Voltage vs Frequency

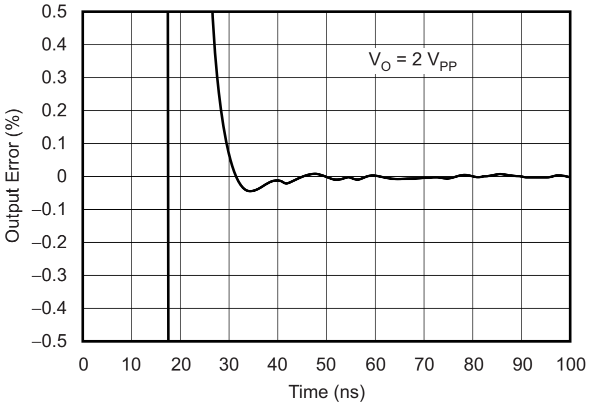


Figure 28. Output Settling Time to 0.1%

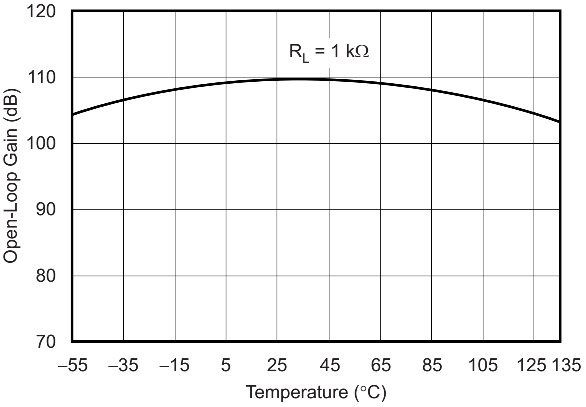


Figure 29. Open-Loop Gain vs Temperature

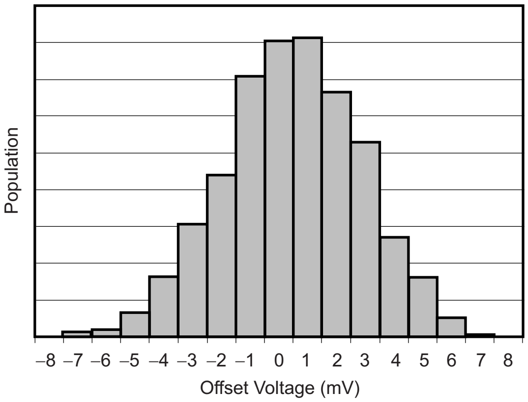


Figure 30. Offset Voltage Production Distribution

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, G = +1, R_F = 0 Ω, R_L = 1 kΩ, and connected to V_S / 2 (unless otherwise noted)

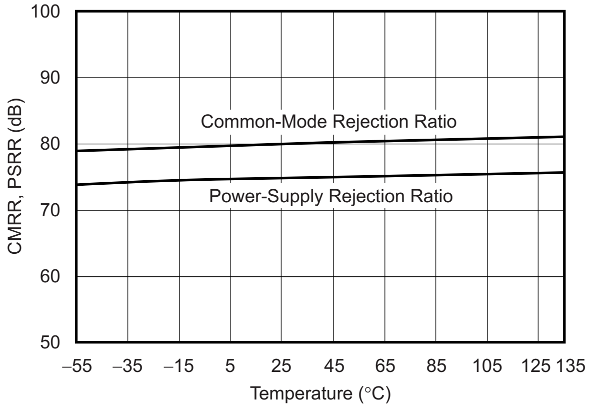


Figure 31. Common-Mode Rejection Ratio and Power-Supply Rejection Ratio vs Temperature

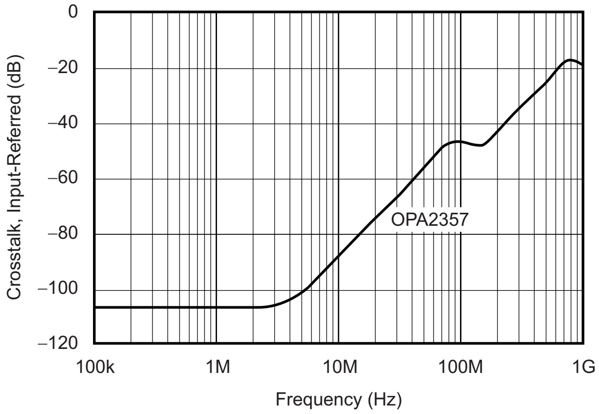


Figure 32. Channel-to-Channel Crosstalk

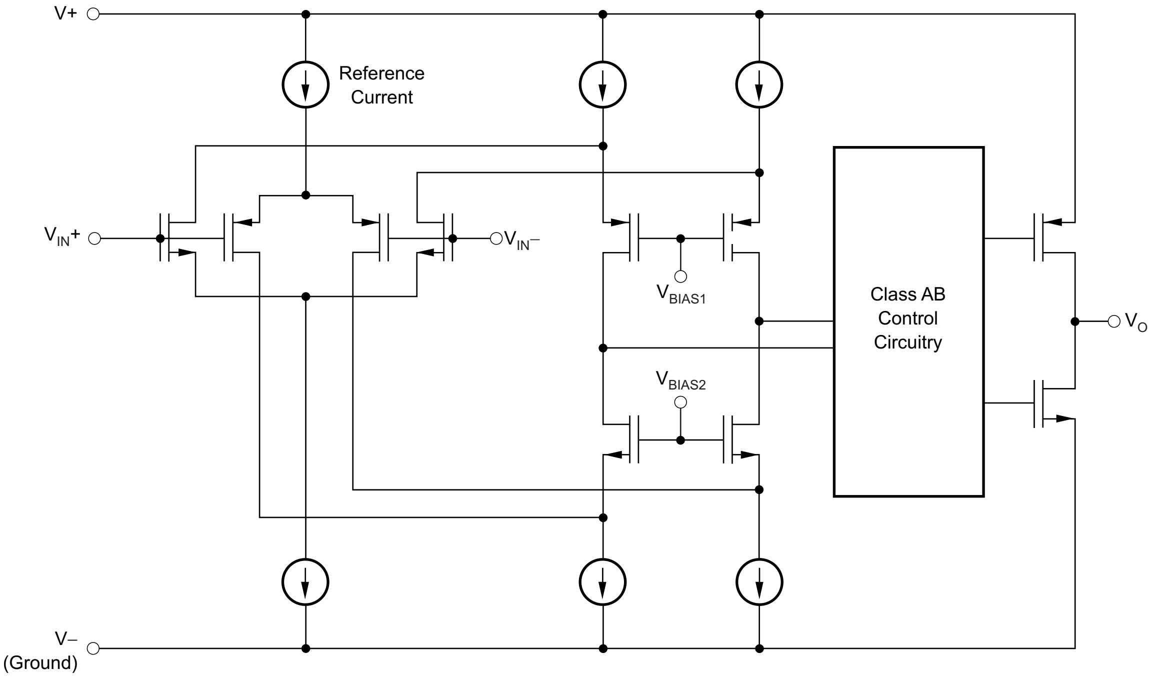
7 Detailed Description

7.1 Overview

The OPA357 is a CMOS, rail-to-rail I/O, high-speed, voltage-feedback operational amplifier designed for video, high-speed, and other applications. The device is available as a single or dual op amp.

The amplifier features a 100-MHz gain bandwidth, and 150-V/µs slew rate, but is unity-gain stable and can be operated as a +1-V/V voltage follower.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 OPAx357 Comparison

Table 1 lists several members of the device family that includes the OPAx357.

Table 1. OPAx357 Related Products

PART NUMBER	FEATURED
OPAx354	Non-shutdown version of OPA357 family
OPAx355	200-MHz GBW, rail-to-rail output, CMOS, shutdown
OPAx356	200-MHz GBW, rail-to-rail output, CMOS
OPAx350, OPAx353	38-MHz GBW, rail-to-rail input/output, CMOS
OPAx631	75-MHz BW G = 2, rail-to-rail output
OPAx634	150-MHz BW G = 2, rail-to-rail output
THS412x	100-MHz BW, differential input/output, 3.3-V supply

7.3.2 Operating Voltage

The OPA357 is specified over a power-supply range of +2.7 V to +5.5 V (±1.35 V to ±2.75 V). However, the supply voltage can range from +2.5 V to +5.5 V (±1.25 V to ±2.75 V). Supply voltages higher than 7.5 V (absolute maximum) can permanently damage the amplifier.

Parameters that vary over supply voltage or temperature are shown in the *Typical Characteristics* section.

7.3.3 Enable Function

The OPA357 enable function is implemented using a Schmitt trigger. The amplifier is enabled by applying a TTL high voltage level (referenced to V−) to the Enable pin. Conversely, a TTL low voltage level (referenced to V−) disables the amplifier, reducing its supply current from 4.9 mA to only 3.4 µA per amplifier. Independent Enable pins are available for each channel (dual version), providing maximum design flexibility. For portable battery-operated applications, this feature can be used to greatly reduce the average current and thereby extend battery life.

The Enable input can be modeled as a CMOS input gate with a 100-kΩ pull-up resistor to V+. Connect this pin to a valid high or low voltage or driven, not left open circuit.

The enable time is 100 ns and the disable time is only 30 ns. This time allows the OPA357 to be operated as a gated amplifier, or to have its output multiplexed onto a common output bus. When disabled, the output assumes a high-impedance state.

7.3.4 Rail-to-Rail Input

The specified input common-mode voltage range of the OPA357 extends 100 mV beyond the supply rails. This range is achieved with a complementary input stage—an N-channel input differential pair in parallel with a P-channel differential pair; see the *Functional Block Diagram* section. The N-channel pair is active for input voltages close to the positive rail, typically (V+) − 1.2 V to 100 mV above the positive supply, whereas the P-channel pair is on for inputs from 100 mV below the negative supply to approximately (V+) − 1.2 V. There is a small transition region, typically (V+) − 1.5 V to (V+) − 0.9 V, in which both pairs are on. This 600-mV transition region can vary ±500 mV with process variation. Thus, the transition region (both input stages on) can range from (V+) − 2.0 V to (V+) − 1.5 V on the low end, up to (V+) − 0.9 V to (V+) − 0.4 V on the high end.

A double-folded cascode adds the signal from the two input pairs and presents a differential signal to the class AB output stage.

7.3.5 Rail-to-Rail Output

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For high-impedance loads (> 200 Ω), the output voltage swing is typically 100 mV from the supply rails. With 10-Ω loads, a useful output swing can be achieved while maintaining high open-loop gain; see Figure 21 and Figure 23.

7.3.6 Output Drive

The OPA357 output stage can supply a continuous output current of ±100 mA and still provide approximately 2.7 V of output swing on a 5-V supply, as shown in Figure 33. For maximum reliability, TI recommends running a continuous DC current in excess of ±100 mA; see Figure 21 and Figure 23. For supplying continuous output currents greater than ±100 mA, the OPA357 can be operated in parallel as shown in Figure 34.

The OPA357 provides peak currents up to 200 mA, which corresponds to the typical short-circuit current. Therefore, an on-chip thermal shutdown circuit is provided to protect the OPA357 from dangerously high junction temperatures. At 160°C, the protection circuit shuts down the amplifier. Normal operation resumes when the junction temperature cools to below 140°C.

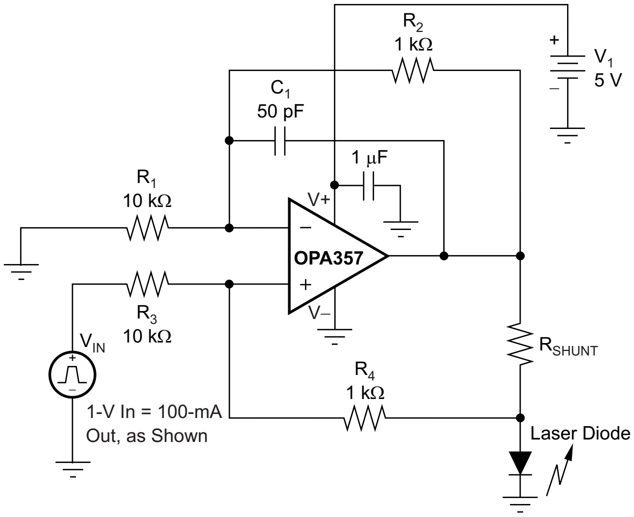


Figure 33. Laser Diode Driver

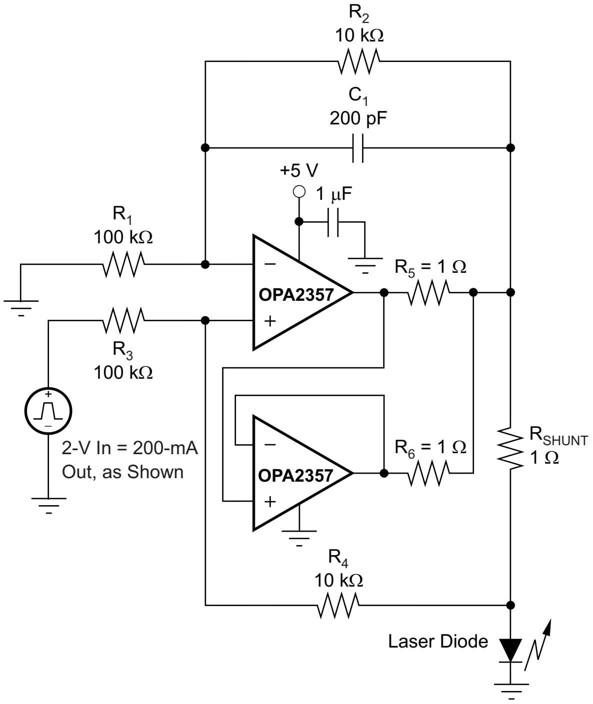


Figure 34. Parallel Operation

7.3.7 Video

The OPA357 output stage is capable of driving standard back-terminated 75-Ω video cables, as shown in Figure 35. By back-terminating a transmission line, the cable does not exhibit a capacitive load to its driver. A properly back-terminated 75-Ω cable does not appear as capacitance; this cable presents only a 150-Ω resistive load to the OPA357 output.

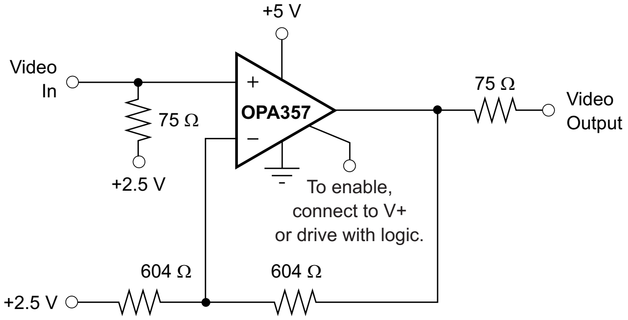
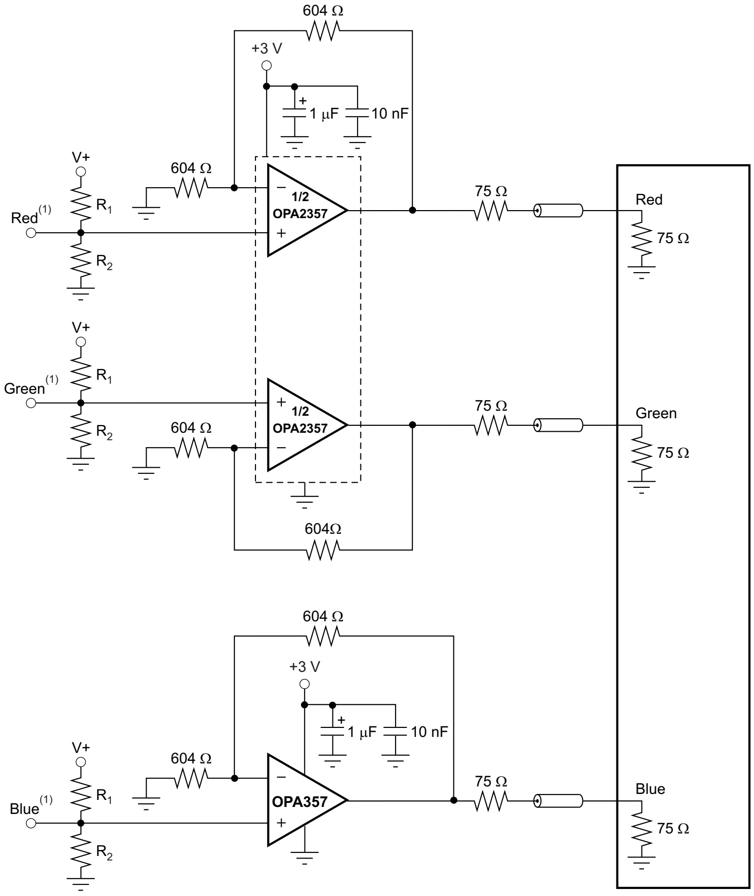


Figure 35. Single-Supply Video Line Driver

The OPA357 can be used as an amplifier for RGB graphic signals, which have a voltage of zero at the video black level, by offsetting and AC-coupling the signal, as shown in Figure 36.



(1) The source video signal offset is 300 mV above ground to accommodate the op amp swing-to-ground capability.

Figure 36. RGB Cable Driver

7.3.8 Wideband Video Multiplexing

One common application for video speed amplifiers that include an Enable pin is to wire multiple amplifier outputs together, then select which one of several possible video inputs to source onto a single line. This simple wired-OR video multiplexer can be easily implemented using the OPA357, as shown in Figure 37.

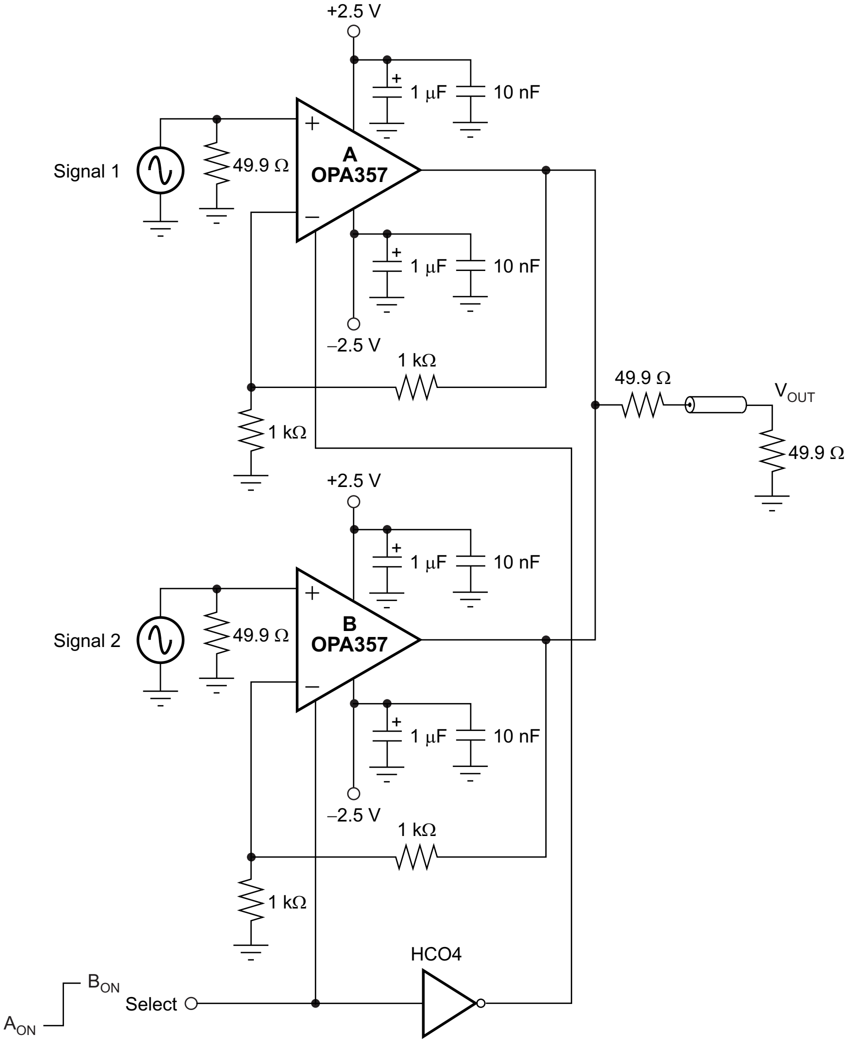
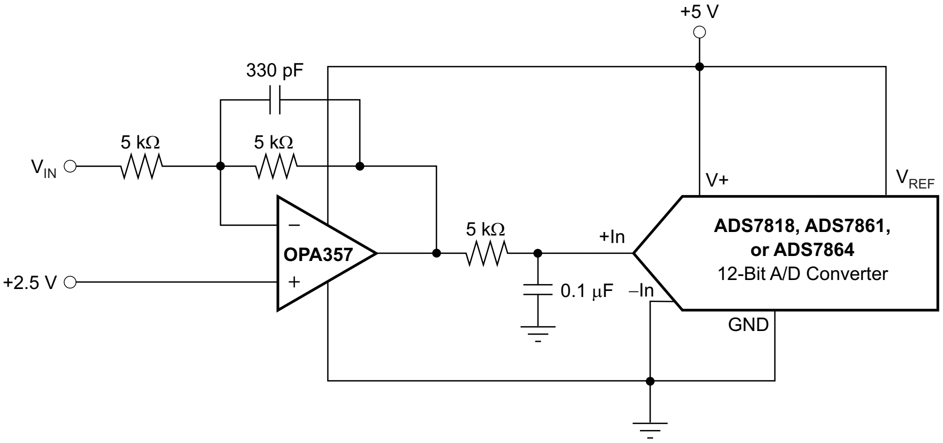


Figure 37. Multiplexed Output

7.3.9 Driving Analog-to-Digital Converters

The OPA357 series op amps offer 60 ns of settling time to 0.01%, making the series a good choice for driving high- and medium-speed sampling A/D converters and reference circuits. The OPA357 series provides an effective means of buffering the A/D converter input capacitance and resulting charge injection while providing signal gain.

Figure 38 shows the OPA357 driving an A/D converter. With the OPA357 in an inverting configuration, a capacitor across the feedback resistor can be used to filter high-frequency noise in the signal, as shown in Figure 38.



NOTE: A/D converter input = 0 V to V_{REF}.

NOTE: V_{IN} = 0 V to –5 V for a 0-V to 5-V output.

Figure 38. The OPA357 in Inverting Configuration Driving an A/D Converter

7.3.10 Capacitive Load and Stability

The OPA357 series of op amps can drive a wide range of capacitive loads. However, all op amps under certain conditions may become unstable. Op amp configuration, gain, and load value are just a few factors to consider when determining stability. An op amp in unity-gain configuration is most susceptible to the effects of capacitive loading. The capacitive load reacts with the op amp output resistance, along with any additional load resistance, to create a pole in the small-signal response that degrades the phase margin; see Figure 14 for details.

The OPA357 topology enhances its ability to drive capacitive loads. In unity gain, these op amps perform well with large capacitive loads. See Figure 15 for details.

One method of improving capacitive load drive in the unity-gain configuration is to insert a 10-Ω to 20-Ω resistor in series with the output, as shown in Figure 39. This method significantly reduces ringing with large capacitive loads; see Figure 14. However, if there is a resistive load in parallel with the capacitive load, R_S creates a voltage divider. This process introduces a DC error at the output and slightly reduces output swing. This error can be insignificant. For instance, with R_L = 10 kΩ and R_S = 20 Ω, there is only about a 0.2% error at the output.

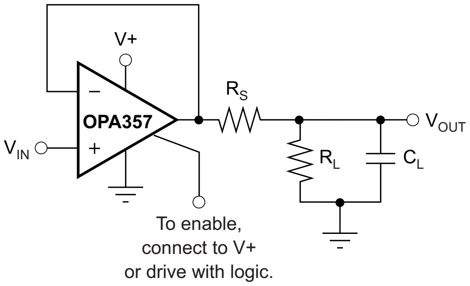


Figure 39. Series Resistor in Unity-Gain Configuration Improves Capacitive Load Drive

7.3.11 Wideband Transimpedance Amplifier

Wide bandwidth, low input bias current, and low input voltage and current noise make the OPA357 an ideal wideband photodiode transimpedance amplifier for low-voltage single-supply applications. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in Figure 40, are the expected diode capacitance (including the parasitic input common-mode and differential-mode input capacitance (2 + 2)pF for the OPA357), the desired transimpedance gain (R_F), and the gain bandwidth product (GBP) for the OPA357 (100 MHz). With these three variables set, the feedback capacitor value (C_F) can be set to control the frequency response.

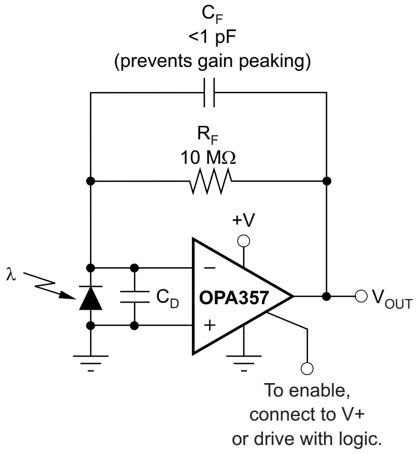


Figure 40. Transimpedance Amplifier

To achieve a maximally flat 2nd-order Butterworth frequency response, set the feedback pole to:

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \quad (1)$$

Typical surface-mount resistors have a parasitic capacitance of approximately 0.2 pF that must be deducted from the calculated feedback capacitance value.

Bandwidth is calculated by:

$$f_{-3dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}}\ \text{Hz} \quad (2)$$

For even higher transimpedance bandwidth, the high-speed CMOS OPA355 (200-MHz GBW) or the OPA655 (400-MHz GBW) can be used.

7.4 Device Functional Modes

The OPAx357 family of devices is powered on when the supply is connected. The devices can be operated as single-supply operational amplifiers or dual-supply amplifiers depending on the application. The devices can also be used with asymmetrical supplies as long as the differential voltage (V– to V+) is at least 1.8 V and no greater than 5.5 V (for example, when V– is set to –3.5 V and V+ is set to 1.5 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx357 family of devices is a CMOS, rail-to-rail I/O, high-speed, voltage-feedback operational amplifier designed for video, high-speed, and other applications. The OPAx357 family of devices is available as a single or dual op-amp.

The amplifier features a 100-MHz gain bandwidth, and 150-V/µs slew rate, but the device is unity-gain stable and operates as a 1-V/V voltage follower.

8.2 Typical Applications

8.2.1 Transimpedance Amplifier

Wide gain bandwidth, low input bias current, low input voltage, and current noise make the OPAx357 family of devices an ideal wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency. The key elements to a transimpedance design, as shown in Figure 41, are the expected diode capacitance, (which include the parasitic input common-mode and differential-mode input capacitance) the desired transimpedance gain, and the gain-bandwidth (GBW) for the OPAx357 family of devices (20 MHz). With these three variables set, the feedback capacitor value is set to control the frequency response. Feedback capacitance includes the stray capacitance, which is 0.2 pF for a typical surface-mount resistor.

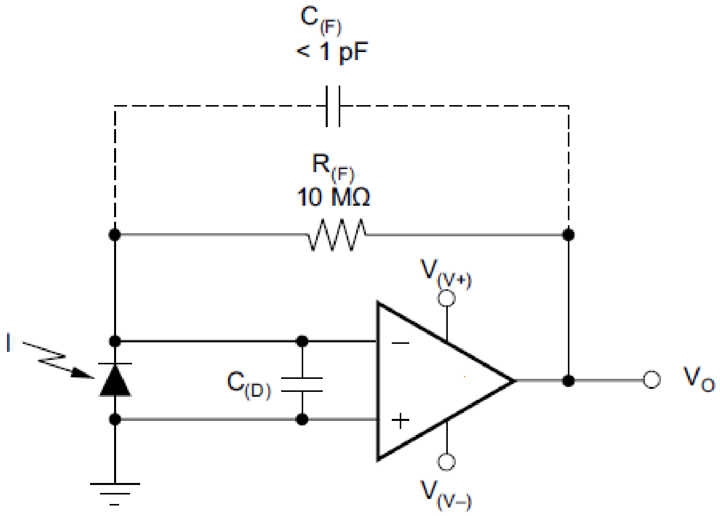


Figure 41. Dual-Supply Transimpedance Amplifier

Typical Applications (continued)

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

PARAMETER	EXAMPLE VALUE
Supply voltage, $V_{(V+)}$	2.5 V
Supply voltage, $V_{(V-)}$	–2.5 V

$C_{(F)}$ is optional to prevent gain peaking. $C_{(F)}$ includes the stray capacitance of $R_{(F)}$.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the OPA357 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 OPAx357 Design Procedure

To achieve a maximally-flat, second-order Butterworth frequency response, set the feedback pole using Equation 3.

$$\frac{1}{2 \times \pi \times R_{(F)} \times C_{(F)}} = \sqrt{\frac{GBW}{4 \times \pi \times R_{(F)} \times C_{(D)}}} \tag{3}$$

Calculate the bandwidth using Equation 4.

$$f_{(-3\ dB)} = \sqrt{\frac{GBW}{2 \times \pi \times R_{(F)} \times C_{(D)}}} \tag{4}$$

For other transimpedance bandwidths, consider the high-speed CMOS OPA380 (90-MHz GBW), OPA354 (100-MHz GBW), OPA300 (180-MHz GBW), OPA355 (200-MHz GBW), or OPA656 and OPA657 (400-MHz GBW).

For single-supply applications, the +INx input can be biased with a positive DC voltage to allow the output to reach true zero when the photodiode is not exposed to any light, and respond without the added delay that results from coming out of the negative rail; Figure 42 shows this configuration. This bias voltage appears across the photodiode, providing a reverse bias for faster operation.

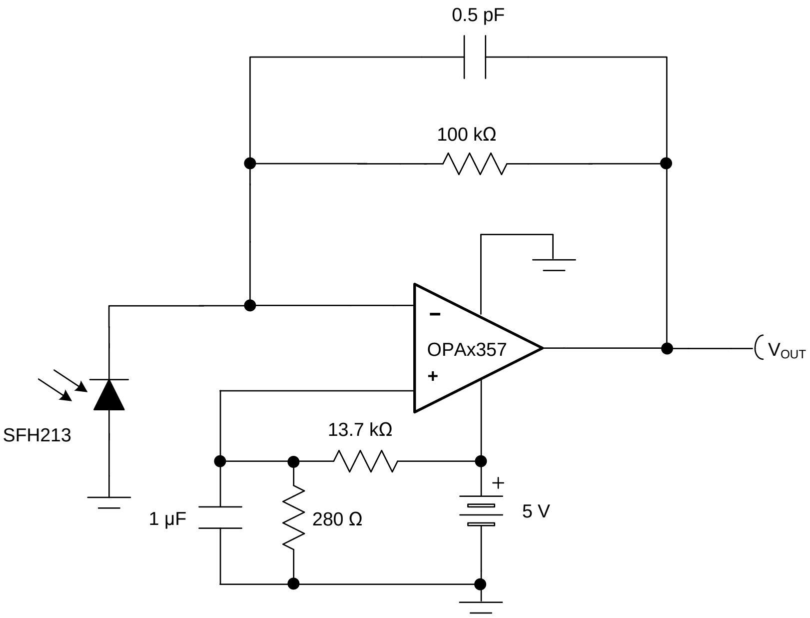


Figure 42. Single-Supply Transimpedance Amplifier

For additional information, see the *Compensate Transimpedance Amplifiers Intuitively* application bulletin.

8.2.1.2.2.1 Optimizing the Transimpedance Circuit

To achieve the best performance, components must be selected according to the following guidelines:

1. For lowest noise, select $R_{(F)}$ to create the total required gain. Using a lower value for $R_{(F)}$ and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by $R_{(F)}$ increases with the square-root of $R_{(F)}$, whereas the signal increases linearly. Therefore, signal-to-noise ratio improves when all the required gain is placed in the transimpedance stage.
2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to amplify (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode reduce the capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.
3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only the required bandwidth. Use a capacitor across the $R_{(F)}$ to limit bandwidth, even if a capacitor not required for stability.
4. Circuit board leakage degrades the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage helps control leakage.

8.2.1.3 Application Curve

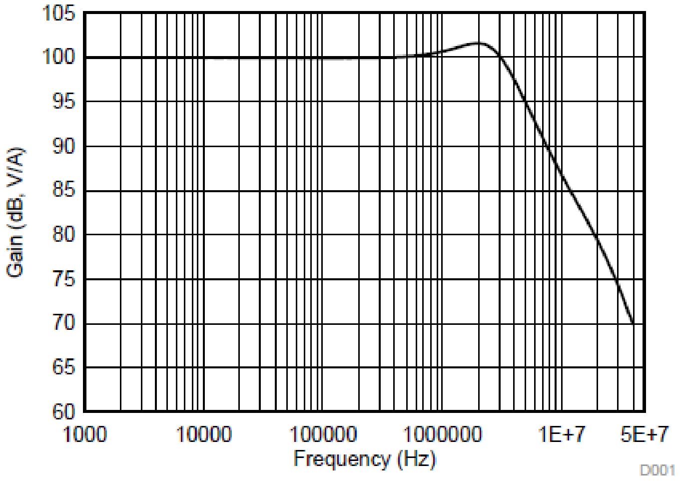


Figure 43. AC Transfer Function

8.2.2 High-Impedance Sensor Interface

Many sensors have high source impedances that can range up to 10 MΩ, or even higher. The output signal of sensors often must be amplified or otherwise conditioned by an amplifier. The input bias current of this amplifier can load the sensor output and cause a voltage drop across the source resistance, as shown in Figure 44, where ($V_{(+INx)} = V_S – I_{(BIAS)} \times R_{(S)}$). The last term, $I_{(BIAS)} \times R_{(S)}$, shows the voltage drop across $R_{(S)}$. To prevent errors introduced to the system as a result of this voltage, use an op amp with low input bias current and high-impedance sensors. This low current keeps the error contribution by $I_{(BIAS)} \times R_{(S)}$ less than the input voltage noise of the amplifier, so that the amplifier does not become the dominant noise factor. The OPAx357 family of devices series of op amps feature low input bias current (typically 200 fA), and are therefore designed for such applications.

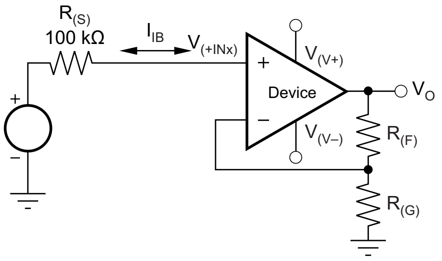
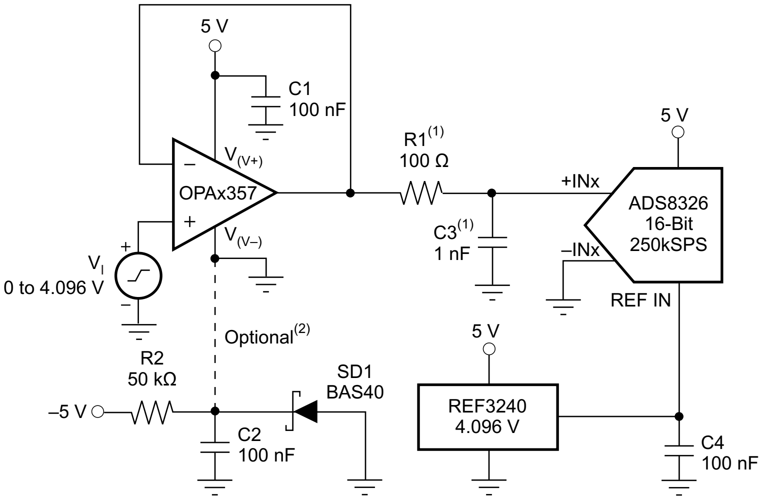


Figure 44. Noise as a Result of $I_{(BIAS)}$

8.2.3 Driving ADCs

The OPAx357 op amps are designed for driving sampling analog-to-digital (A/D) converters with sampling speeds up to 1 MSPS. The zero-crossover distortion input stage topology allows the OPAx357 family of devices to drive A/D converters without degradation of differential linearity and THD.

The OPAx357 family of devices can be used to buffer the A/D converter switched input capacitance and resulting charge injection while providing signal gain. Figure 45 shows the OPAx357 family of devices configured to drive the ADS8326.



(1) Suggested value; may require adjustment based on specific application.

(2) Single-supply applications lose a small number of A/D converter codes near ground as a result of op amp output swing limitation. If a negative power supply is available, this simple circuit creates a –0.3-V supply to allow output swing to true ground potential.

Figure 45. Driving the ADS8326

8.2.4 Active Filter

The OPAx357 family of devices is designed for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 46 shows a 500-kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components are selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is –40 dB/dec. The Butterworth response is designed for applications requiring predictable gain characteristics, such as the antialiasing filter used in front of an A/D converter.

One point to note when considering the MFB filter is that the output is inverted relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of the following options:

1. Adding an inverting amplifier
2. Adding an additional second-order MFB stage
3. Using a noninverting filter topology, such as the Sallen-Key (see Figure 47).

MFB and Sallen-Key, low-pass and high-pass filter synthesis is accomplished using TI's FilterPro™ program. This software is available as a free download on www.ti.com.

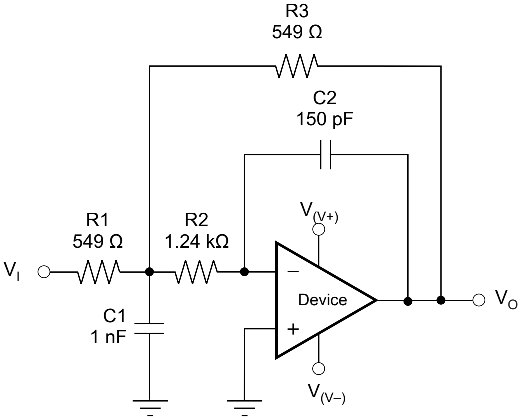


Figure 46. Second-Order, Butterworth, 500-kHz, Low-Pass Filter

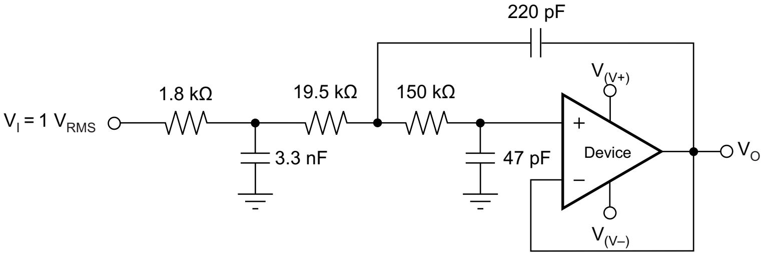


Figure 47. OPAx357 Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

9 Power Supply Recommendations

9.1 Power Dissipation

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power-supply voltage. Dissipation with AC signals is lower. The *Power Amplifier Stress and Power Handling Limitations* application note explains how to calculate or measure power dissipation with unusual signals and loads, and can be found at www.ti.com. Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 150°C, maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered at 160°C. The thermal protection should trigger more than 35°C above the maximum expected ambient condition of your application.

10 Layout

10.1 Layout Guidelines

Use good high-frequency printed circuit board (PCB) layout techniques for the OPA357. Generous use of ground planes, short and direct signal traces, and a suitable bypass capacitor located at the V+ pin assures clean, stable operation. Large areas of copper also provide a means of dissipating heat that is generated in normal operation.

Sockets are definitely not recommended for use with any high-speed amplifier.

A 10-nF ceramic bypass capacitor is the minimum recommended value; adding a 1-µF or larger tantalum capacitor in parallel can be beneficial when driving a low-resistance load. Providing adequate bypass capacitance is essential to achieving very low harmonic and intermodulation distortion.

10.2 Layout Example

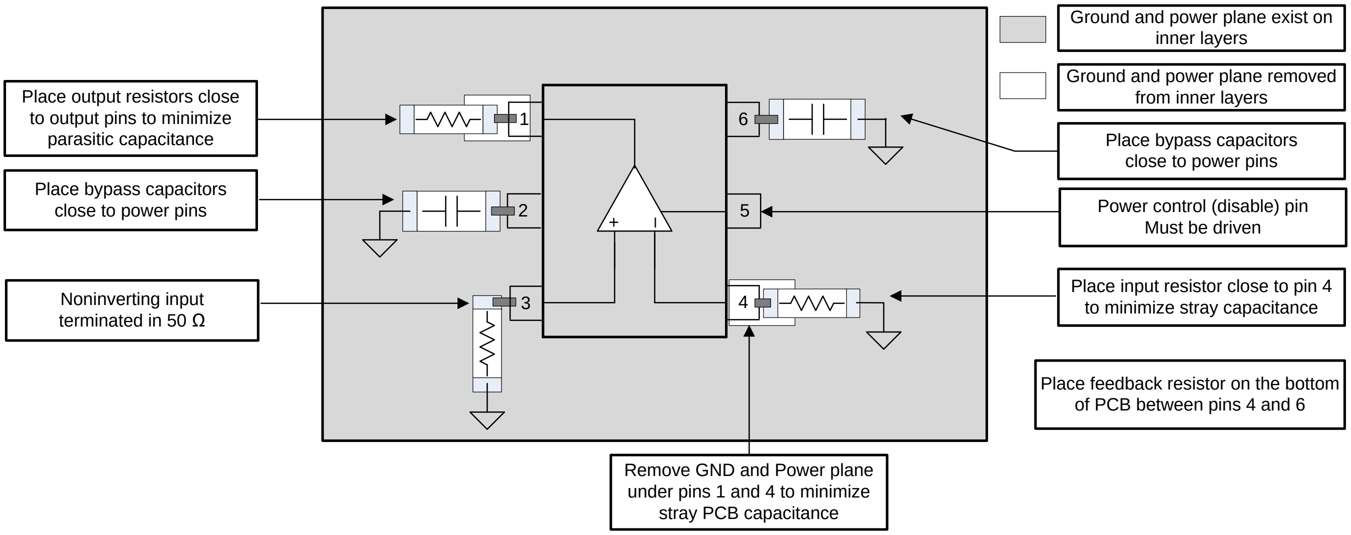


Figure 48. Example Layout

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 使用 WEBENCH® 工具创建定制设计

单击此处，使用 OPA357 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 首先键入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化关键参数设计，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：
- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

11.2 文档支持

11.2.1 相关文档

如需相关文档，请参阅：
- *《OPAx380 精密高速跨阻放大器》*
- *《OPAx354 250MHz、轨至轨 I/O CMOS 运算放大器》*
- *《OPAx300 低噪声高速 16 位精确 CMOS 运算放大器》*
- *《具有关断功能的 OPAx355 200MHz CMOS 运算放大器》*
- *《OPA656 宽带单位增益稳定 FET 输入运算放大器》*
- *《OPA657 1.6GHz、低噪声、FET 输入运算放大器》*
- *《ADS8326 16 位、2.7V 至 5.5V 高速微功耗采样模数转换器》*
- FilterPro™
- *《用直观方式补偿跨阻放大器》*
- *《功率放大器应力和功率处理限制》*

11.3 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即购买的快速链接。

表 **3.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
OPA357	单击此处	单击此处	单击此处	单击此处	单击此处
OPA2357	单击此处	单击此处	单击此处	单击此处	单击此处

11.4 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

社区资源 (接下页)

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.6 商标

FilterPro, E2E are trademarks of Texas Instruments.
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11.7 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请参阅左侧的导航栏。

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2357AIDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BBG	Samples
OPA2357AIDGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BBG	Samples
OPA2357AIDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BBG	Samples
OPA2357AIDGSTG4	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BBG	Samples
OPA357AIDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OADI	Samples
OPA357AIDBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OADI	Samples
OPA357AIDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OADI	Samples
OPA357AIDBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OADI	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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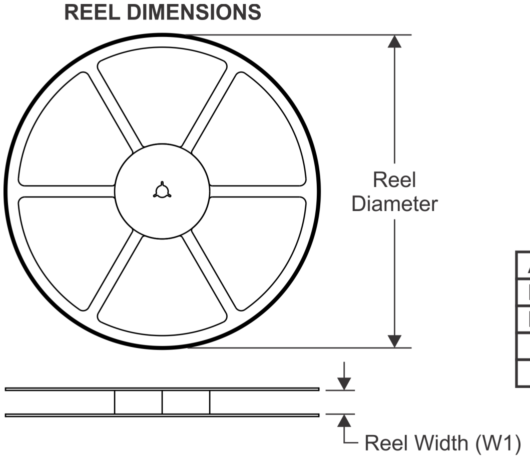
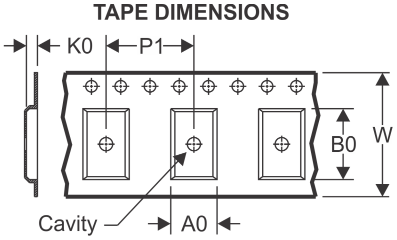
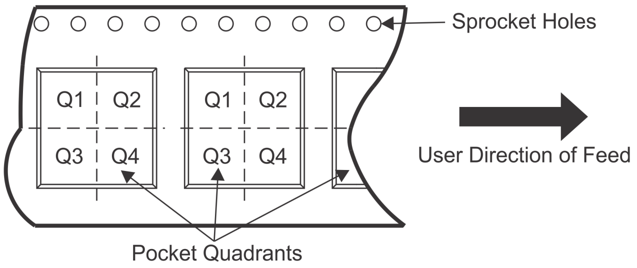
TAPE AND REEL INFORMATION


REEL DIMENSIONS


TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

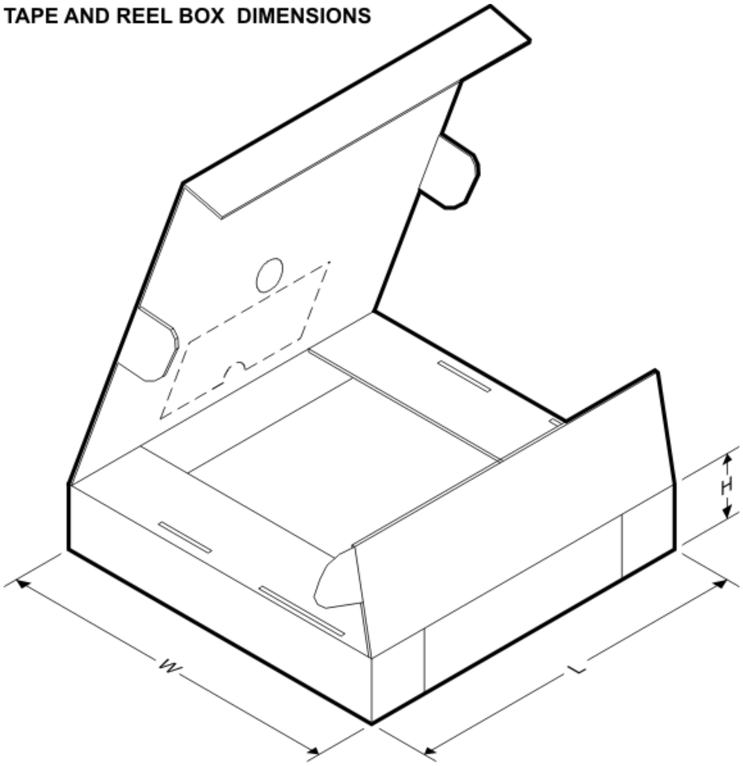
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2357AIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2357AIDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA357AIDBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

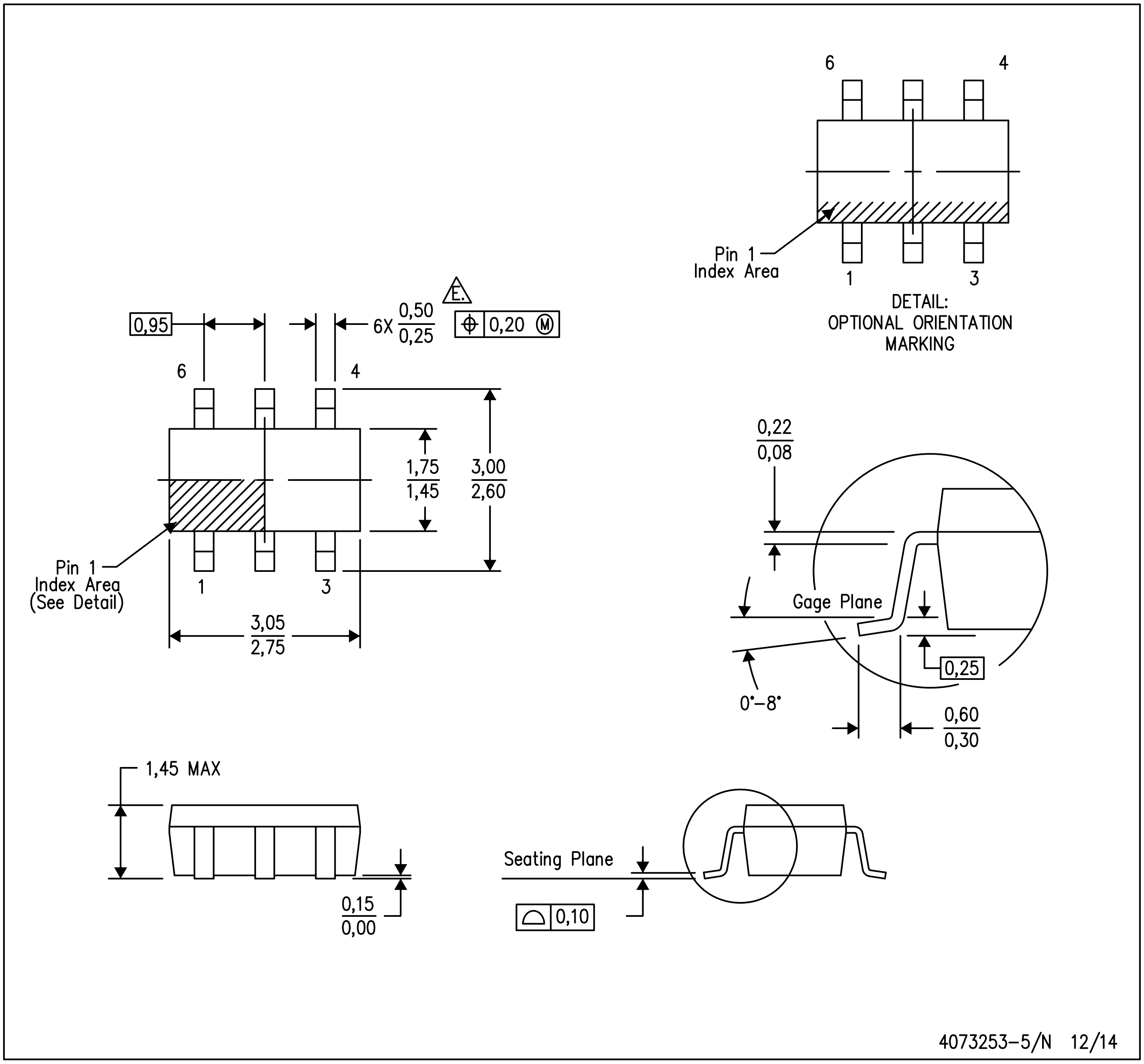
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

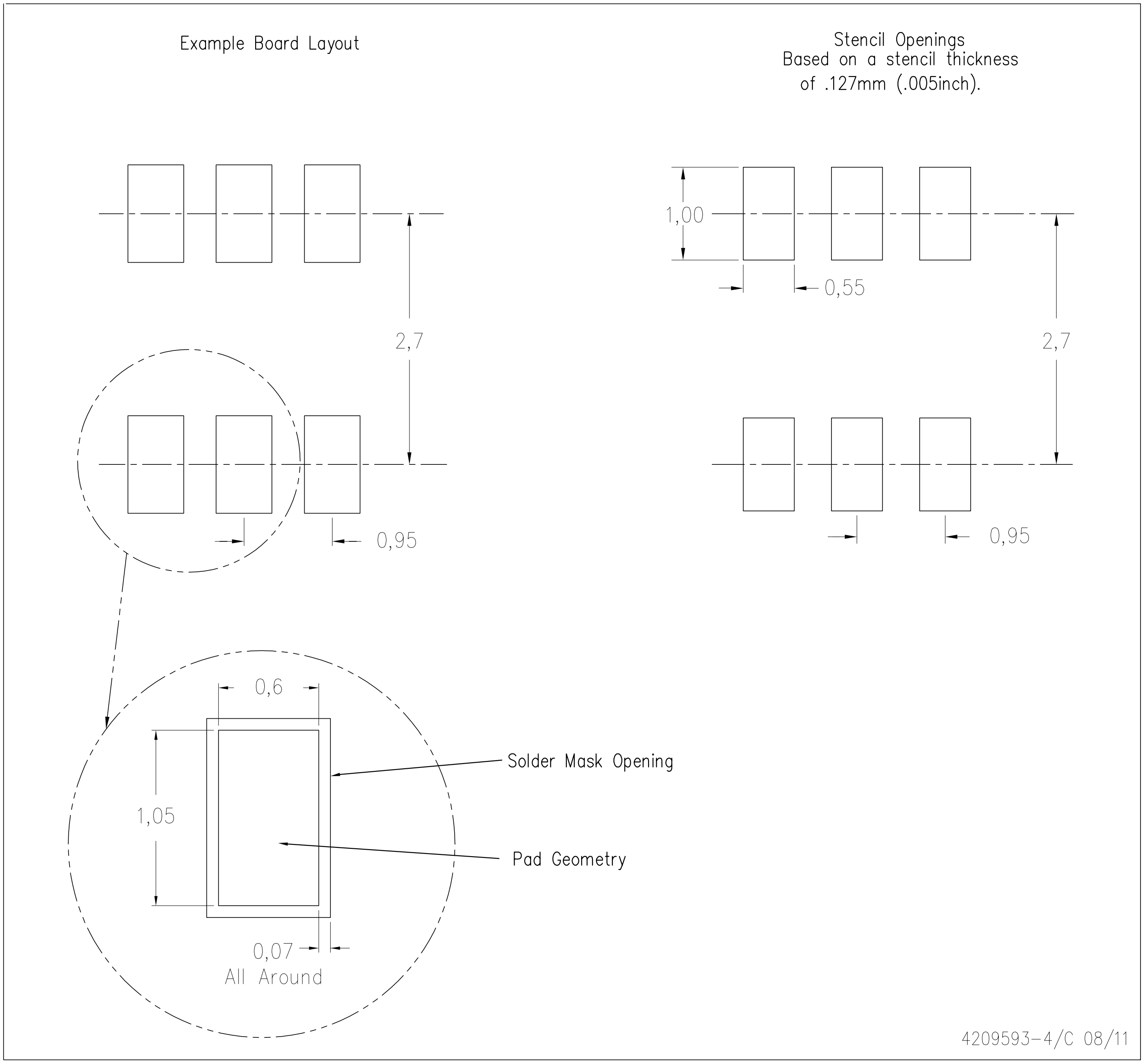
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2357AIDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
OPA2357AIDGST	VSSOP	DGS	10	250	210.0	185.0	35.0
OPA357AIDBVT	SOT-23	DBV	6	250	195.0	200.0	45.0

DBV (R-PDSO-G6) PLASTIC SMALL-OUTLINE PACKAGE



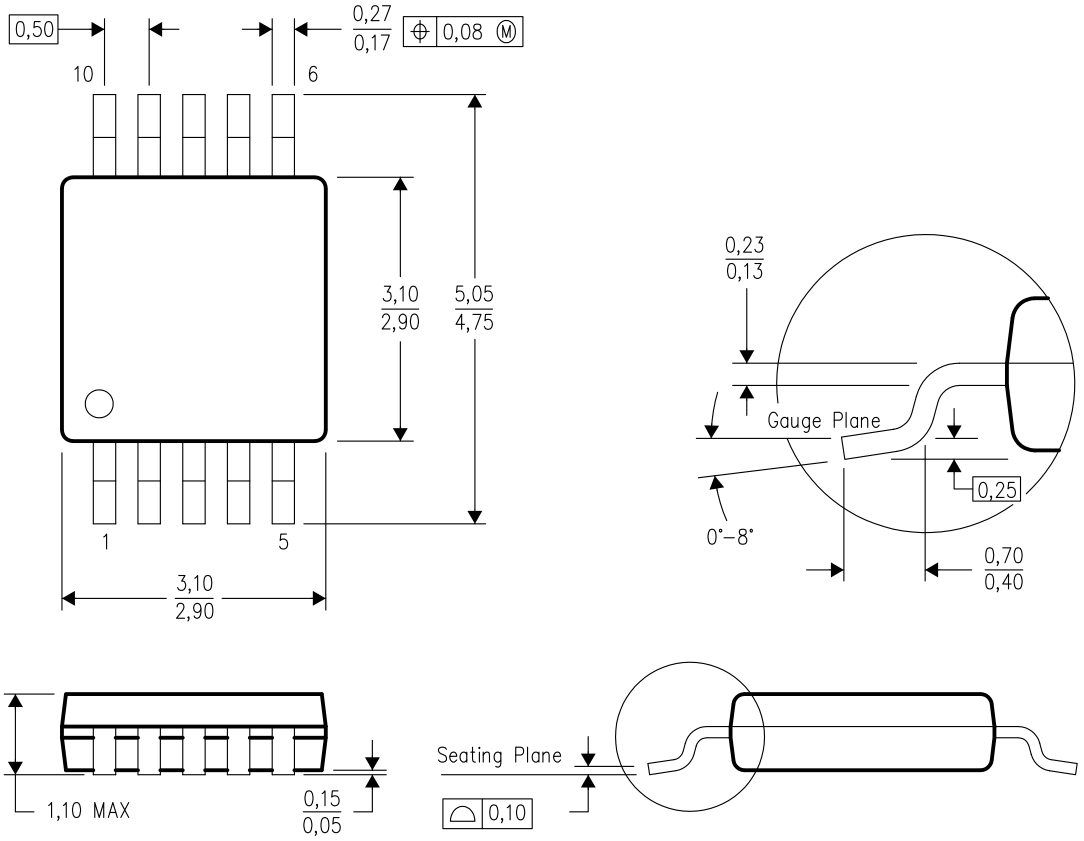
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGS (S-PDSO-G10) PLASTIC SMALL-OUTLINE PACKAGE



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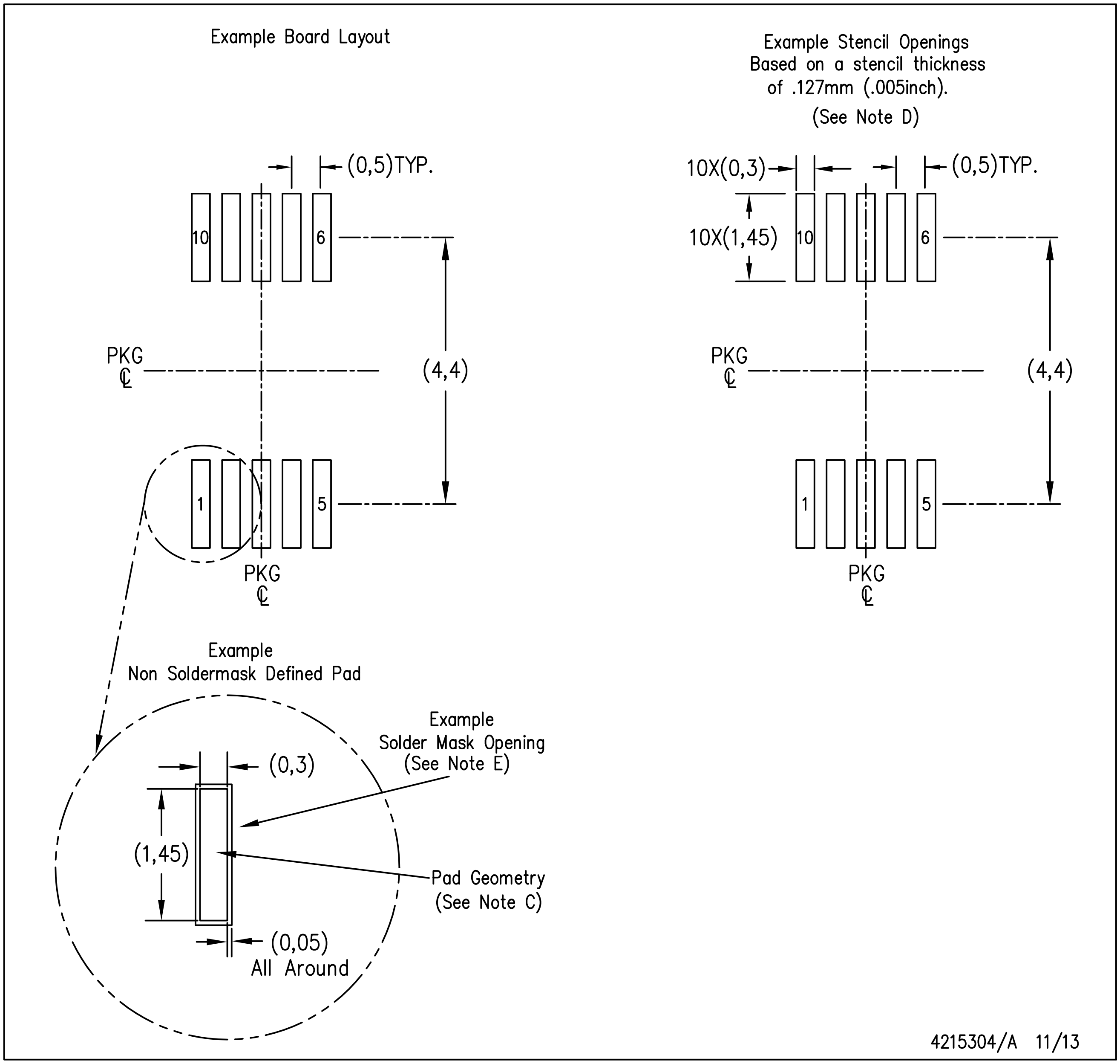
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. Falls within JEDEC MO–187 variation BA.

DGS (S–PDSO–G10) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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