

LMV7219 7-ns 2.7-V to 5-V Comparator with Rail-to-Rail Output

1 Features

- ($V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Typical Values Unless Specified)
- Propagation Delay 7 ns
- Low Supply Current 1.1 mA
- Input Common Mode Voltage Range Extends 200 mV Below Ground
- Ideal for 2.7-V and 5-V Single Supply Applications
- Internal Hysteresis Ensures Clean Switching
- Fast Rise and Fall Time 1.3 ns
- Available in Space-saving Packages: SC-70 and SOT-23
- Supports 105°C PCB Temperature

2 Applications

- Portable and Battery-powered Systems
- Scanners
- Set Top Boxes
- High Speed Differential Line Receiver
- Window Comparators
- Zero-crossing Detectors
- High-speed Sampling Circuits

3 Description

The LMV7219 is a low-power, high-speed comparator with internal hysteresis. The LMV7219 operating voltage ranges from 2.7 V to 5 V with push-pull rail-to-rail output. This device achieves a 7-ns propagation delay while consuming only 1.1 mA of supply current at 5 V.

The LMV7219 inputs have a common mode voltage range that extends 200 mV below ground, allowing ground sensing. The internal hysteresis ensures clean output transitions even with slow-moving inputs signals.

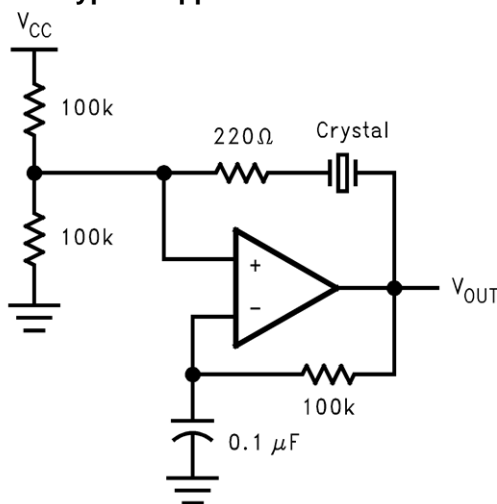
The LMV7219 is available in the SC-70 and SOT-23 packages, which are ideal for systems where small size and low power are critical.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMV7219	SC-70 (5)	2.00 mm x 1.25 mm
	SOT-23 (5)	2.88 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



Copyright © 2016, Texas Instruments Incorporated



Table of Contents

1 Features	1	7.3 Feature Description.....	11
2 Applications	1	7.4 Device Functional Modes.....	11
3 Description	1	8 Application and Implementation	12
4 Revision History	2	8.1 Application Information.....	12
5 Pin Configuration and Functions	3	8.2 Typical Application	12
6 Specifications	4	9 Power Supply Recommendations	16
6.1 Absolute Maximum Ratings	4	10 Layout	16
6.2 ESD Ratings.....	4	10.1 Layout Guidelines	16
6.3 Recommended Operating Conditions.....	4	10.2 Layout Example	17
6.4 Thermal Information	4	11 Device and Documentation Support	18
6.5 Electrical Characteristics 2.7 V	5	11.1 Documentation Support	18
6.6 Electrical Characteristics 5 V	6	11.2 Receiving Notification of Documentation Updates	18
6.7 Typical Performance Characteristics	8	11.3 Community Resources.....	18
7 Detailed Description	11	11.4 Trademarks	18
7.1 Overview	11	11.5 Electrostatic Discharge Caution.....	18
7.2 Functional Block Diagram	11	12 Mechanical, Packaging, and Orderable Information	18

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (April 2016) to Revision I	Page
• Added Supports 105°C PCB Temperature to Features List.....	1
• Changed Operating Temperature to Ambient Temperature	4
• Added Junction Temperature of 125 °C	4
• Added PCB Temperature of 105 °C	4
• Added $T_{PCB} \leq 105^{\circ}\text{C}$ throughout Electrical Tables	5

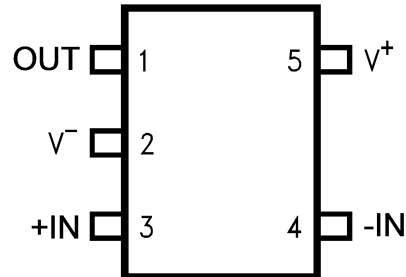
Changes from Revision G (January 2015) to Revision H	Page
• Changed "Infrared or Convection (20 sec)" from 235 °C	4
• Added thermal data for SOT23 and SC70 packages	4

Changes from Revision F (April 2013) to Revision G	Page
• Added, updated, or renamed the following sections: Device Information Table, <i>Pin Configurations and Functions</i> ; <i>Specifications</i> ; <i>Application and Implementation</i> ; <i>Power Supply Recommendations</i> ; <i>Layout</i> ; <i>Device and Documentation Support</i> ; <i>Mechanical, Packaging, and Ordering Information</i>	1
• Changed from "transient response" to "eliminate possible output chatter" in <i>Circuit Layout and Bypassing</i>	16

Changes from Revision E (March 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	1

5 Pin Configuration and Functions

5-Pin SC-70 and SOT-23
Packages DCK and DBV
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	OUT	O	Output
2	V ⁻	I	Negative Supply
3	+IN	I	Non-inverting input
4	-IN	I	Inverting input
5	V ⁺	I	Positive Supply

6 Specifications

6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted) ⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
Differential input voltage		± Supply Voltage		
Output short circuit duration		See ⁽³⁾		
Supply voltage (V ⁺ - V ⁻)		5.5		V
Soldering information	Infrared or Convection (20 sec)	260		°C
	Wave Soldering (10 sec)	260 (lead temp)		°C
Voltage at input/output pins		(V ⁺) + 0.4 (V ⁻) - 0.4		V
Current at input pin ⁽⁴⁾		±10		mA
Maximum junction temperature		150		°C
Storage temperature		-65	150	°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and the test conditions, see the Electrical characteristics.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of ±30mA over long term may adversely affect reliability.
- (4) Limiting input pin current is only necessary for input voltages that exceed absolute maximum input voltage ratings.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±150

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±150 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltages (V ⁺ - V ⁻)	2.7	5	V
Ambient Temperature ⁽¹⁾	-40	+85	°C
Junction Temperature		125	°C
PCB Temperature		105	°C

- (1) The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A)/R_{θJA}. All numbers apply for packages soldered directly into a PC board.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LMV7219	LMV7219	UNIT
		DBV (SOT23)	DCK (SC70)	
		5 PINS	5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	209	296	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	170	132	°C/W
R _{θJB}	Junction-to-board thermal resistance	68	76	°C/W
ψ _{JT}	Junction-to-top characterization parameter	52	8.6	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com/lit/zip/Spra953).

Thermal Information (continued)

THERMAL METRIC ⁽¹⁾		LMV7219	LMV7219	UNIT
		DBV (SOT23)	DCK (SC70)	
		5 PINS	5 PINS	
ψ_{JB}	Junction-to-board characterization parameter	68	75	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

6.5 Electrical Characteristics 2.7 V

Unless otherwise specified, all limits ensured for $T_J = 25^\circ\text{C}$, $V_{CM} = V^+/2$, $V^+ = 2.7\text{ V}$, $V^- = 0\text{ V}$, $C_L = 10\text{ pF}$ and $R_L > 1\text{ M}\Omega$ to V^- .

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX ⁽²⁾	UNIT	
V_{OS}	Input offset voltage			1	6	mV	
		$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$			8		
I_B	Input bias current			450	950	nA	
		$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$			2000		
I_{OS}	Input offset current			50	200	nA	
		$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$			400		
CMRR	Common mode rejection ratio	$0\text{ V} < V_{CM} < 1.50\text{ V}$		62	85	dB	
			$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$		55		
PSRR	Power supply rejection ratio	$V^+ = 2.7\text{ V}$ to 5 V		65	85	dB	
			$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$		55		
V_{CM}	Input common-voltage range	CMRR > 50 dB		$V_{CC} - 1.2$	$V_{CC} - 1$	V	
			$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$		$V_{CC} - 1.3$		
					-0.2		-0.1
			$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$				0
V_O	Output swing high	$I_L = 4\text{ mA}$, $V_{ID} = 500\text{ mV}$		$V_{CC} - 0.3$	$V_{CC} - 0.22$	V	
			$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$		$V_{CC} - 0.4$		
					$V_{CC} - 0.05$		$V_{CC} - 0.02$
	Output swing low	$I_L = 0.4\text{ mA}$, $V_{ID} = 500\text{ mV}$		$V_{CC} - 0.05$	$V_{CC} - 0.02$	mV	
			$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$		$V_{CC} - 0.15$		
I_{SC}	Output short circuit current	Sourcing, $V_O = 0\text{ V}$ ⁽³⁾			20	mA	
			$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$				300
					15		50
			$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$				150
I_S	Supply current	No Load		0.9	1.6	mA	
			$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$				2.2
V_{HYST}	Input hysteresis voltage	See ⁽⁴⁾		7		mV	
V_{TRIP}^*	Input referred positive trip point	(see Figure 19)		3	8	mV	

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

(3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C . Output currents in excess of $\pm 30\text{ mA}$ over long term may adversely affect reliability.

(4) The LMV7219 comparator has internal hysteresis. The trip points are the input voltage needed to change the output state in each direction. The offset voltage is defined as the average of V_{trip}^+ and V_{trip}^- , while the hysteresis voltage is the difference of these two.

Electrical Characteristics 2.7 V (continued)

Unless otherwise specified, all limits ensured for $T_J = 25^\circ\text{C}$, $V_{CM} = V^+/2$, $V^+ = 2.7\text{ V}$, $V^- = 0\text{ V}$, $C_L = 10\text{ pF}$ and $R_L > 1\text{ M}\Omega$ to V^- .

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX ⁽²⁾	UNIT
V_{TRIP^-}	Input referred negative trip point (see Figure 19)	-8	-4		mV
t_{PD}	Propagation delay	Overdrive = 5 mV, $V_{CM} = 0\text{ V}$ ⁽⁵⁾		12	ns
		Overdrive = 15 mV, $V_{CM} = 0\text{ V}$ ⁽⁵⁾		11	
		Overdrive = 50 mV, $V_{CM} = 0\text{ V}$ ⁽⁵⁾		10 20	
t_{SKEW}	Propagation delay skew	See ⁽⁶⁾		1	ns
t_r	Output rise time	10% to 90%		2.5	ns
t_f	Output fall time	90% to 10%		2	ns

(5) Propagation delay measurements made with 100 mV steps. Overdrive is measured relative to V_{TRIP^-} .

(6) Propagation Delay Skew is defined as absolute value of the difference between $t_{PD\text{LH}}$ and $t_{PD\text{HL}}$.

6.6 Electrical Characteristics 5 V

Unless otherwise specified, all limits ensured for $T_J = 25^\circ\text{C}$, $V_{CM} = V^+/2$, $V^+ = 5\text{ V}$, $V^- = 0\text{ V}$, $C_L = 10\text{ pF}$ and $R_L > 1\text{ M}\Omega$ to V^- .

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX ⁽²⁾	UNIT	
V_{OS}	Input offset voltage			1 6	mV	
		$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$		8		
I_B	Input bias current			500 950	nA	
		$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$		2000		
I_{OS}	Input offset current			50 200	nA	
		$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$		400		
CMRR	Common mode rejection ratio	$0\text{ V} < V_{CM} < 3.8\text{ V}$			65 85	dB
			$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$		55	
PSRR	Power supply rejection ratio	$V^+ = 2.7\text{ V}$ to 5 V			65 85	dB
			$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$		55	
V_{CM}	Input common-mode voltage range	CMRR > 50 dB	$V_{CC} - 1.2$ $V_{CC} - 1$		V	
			$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$			$V_{CC} - 1.3$
					-0.2 -0.1	V
			$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$		0	
V_O	Output swing high	$I_L = 4\text{ mA}$, $V_{ID} = 500\text{ mV}$	$V_{CC} - 0.2$ $V_{CC} - 0.13$		V	
			$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$			$V_{CC} - 0.3$
		$I_L = 0.4\text{ mA}$, $V_{ID} = 500\text{ mV}$	$V_{CC} - 0.05$ $V_{CC} - 0.02$		V	
			$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$			$V_{CC} - 0.15$
Output swing low		$I_L = -4\text{ mA}$, $V_{ID} = -500\text{ mV}$	80 180		mV	
			$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$			280
						10 50
		$I_L = -0.4\text{ mA}$, $V_{ID} = -500\text{ mV}$	$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$		150	

(1) Typical Values represent the most likely parametric norm.

(2) All limits are specified by testing or statistical analysis.

Electrical Characteristics 5 V (continued)

Unless otherwise specified, all limits ensured for $T_J = 25^\circ\text{C}$, $V_{CM} = V^+/2$, $V^+ = 5\text{ V}$, $V^- = 0\text{ V}$, $C_L = 10\text{ pF}$ and $R_L > 1\text{ M}\Omega$ to V^- .

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX ⁽²⁾	UNIT
I_{SC} Output short circuit current	Sourcing, $V_O = 0\text{ V}$ ⁽³⁾		30	68	mA
		$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$	20		
	Sinking, $V_O = 5\text{ V}$ ⁽³⁾		30	65	
		$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$	20		
I_S Supply current	No Load		1.1	1.8	mA
		$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$ and $T_{PCB} \leq 105^\circ\text{C}$		2.4	
V_{HYST} Input hysteresis voltage	See ⁽⁴⁾		7.5		mV
V_{Trip}^+ Input referred positive trip point	(See Figure 19)		3.5	8	mV
V_{Trip}^- Input referred negative trip point	(See Figure 19)	-8	-4		mV
t_{PD} Propagation delay	Overdrive = 5 mV, $V_{CM} = 0\text{ V}$ ⁽⁵⁾		9		ns
	Overdrive = 15 mV, $V_{CM} = 0\text{ V}$ ⁽⁵⁾		8	20	
	Overdrive = 50 mV, $V_{CM} = 0\text{ V}$ ⁽⁵⁾		7	19	
t_{SKEW} Propagation delay skew	See ⁽⁶⁾		0.4		ns
t_r Output rise time	10% to 90%		1.3		ns
t_f Output fall time	90% to 10%		1.25		ns

- (3) Applies to both single-supply and split-supply operation. Continuous short circuit operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C . Output currents in excess of $\pm 30\text{ mA}$ over long term may adversely affect reliability.
- (4) The LMV7219 comparator has internal hysteresis. The trip points are the input voltage needed to change the output state in each direction. The offset voltage is defined as the average of V_{Trip}^+ and V_{Trip}^- , while the hysteresis voltage is the difference of these two.
- (5) Propagation delay measurements made with 100 mV steps. Overdrive is measured relative to V_{Trip} .
- (6) Propagation Delay Skew is defined as absolute value of the difference between t_{PDH} and t_{PDHL} .

6.7 Typical Performance Characteristics

Unless otherwise specified, $V_S = 5\text{ V}$, $C_L = 10\text{ pF}$, $T_A = 25^\circ\text{C}$

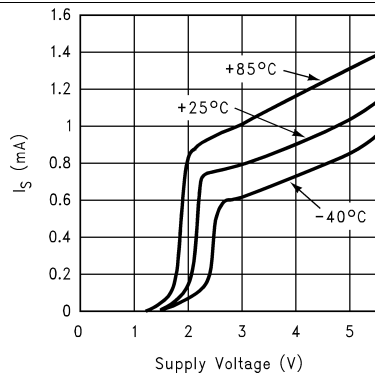


Figure 1. Supply Current vs. Supply Voltage

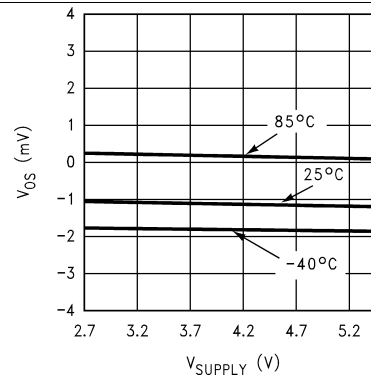


Figure 2. V_{OS} vs. Supply Voltage

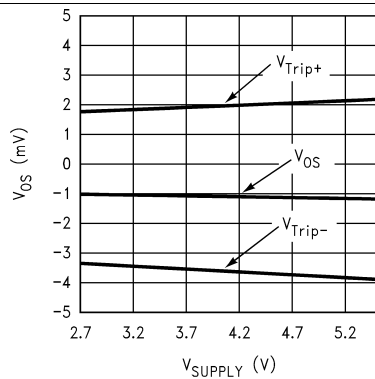


Figure 3. Input Offset and Trip Voltage vs. Supply Voltage

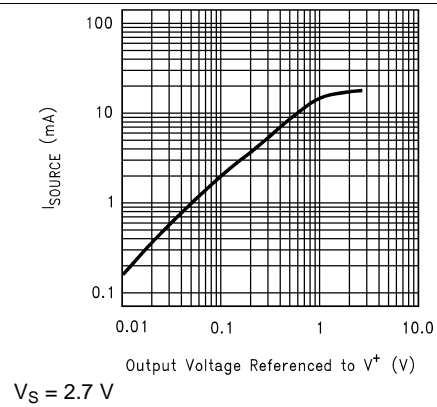


Figure 4. Sourcing Current vs. Output Voltage

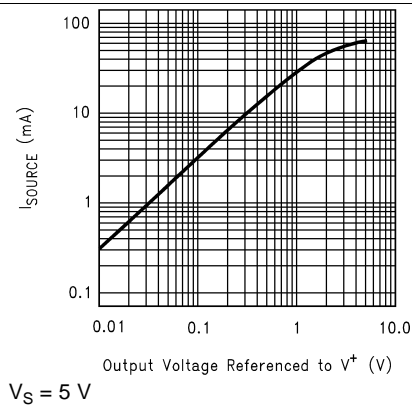


Figure 5. Sourcing Current vs. Output Voltage

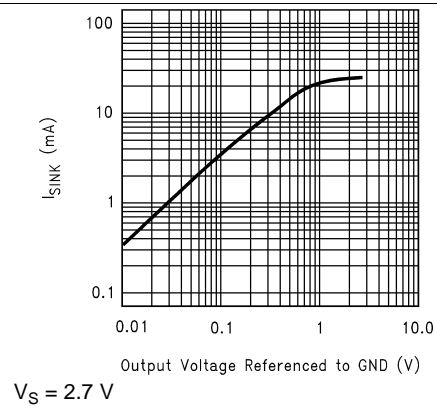


Figure 6. Sinking Current vs. Output Voltage

Typical Performance Characteristics (continued)

Unless otherwise specified, $V_S = 5\text{ V}$, $C_L = 10\text{ pF}$, $T_A = 25^\circ\text{C}$

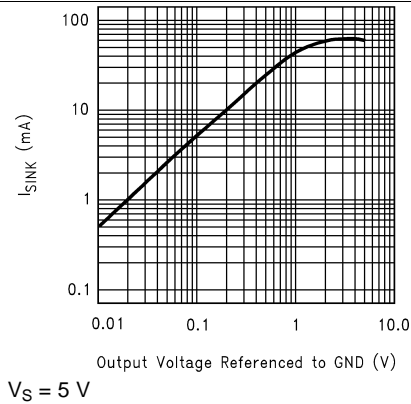


Figure 7. Sinking Current vs. Output Voltage

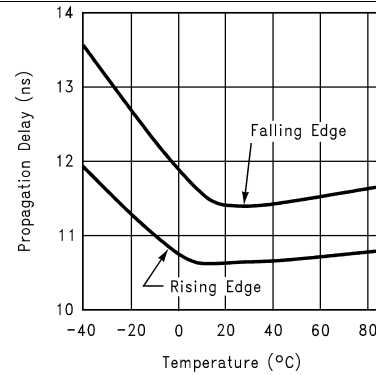


Figure 8. Propagation Delay vs. Temperature

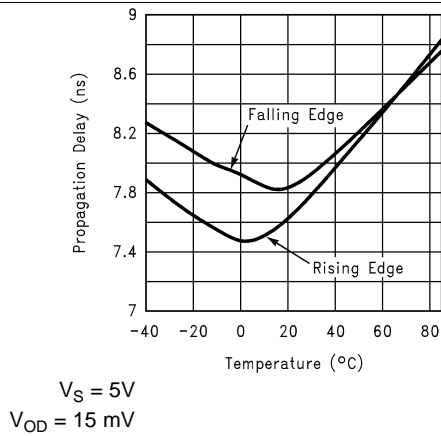


Figure 9. Propagation Delay vs. Temperature

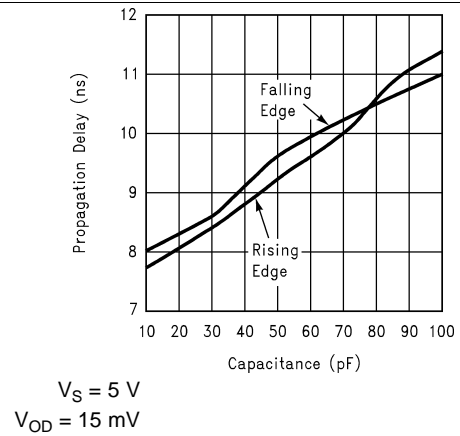


Figure 10. Propagation Delay vs. Capacitive Load

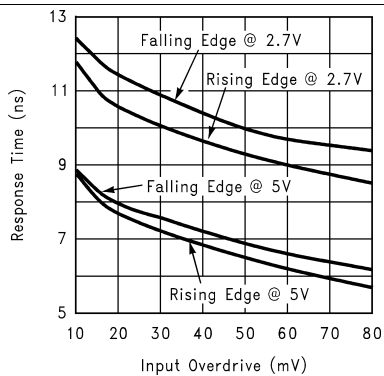


Figure 11. Propagation Delay vs. Input Overdrive

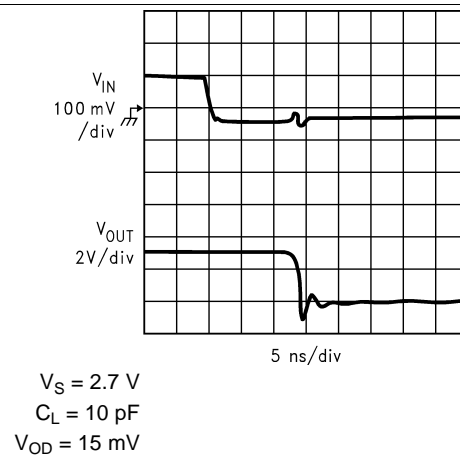
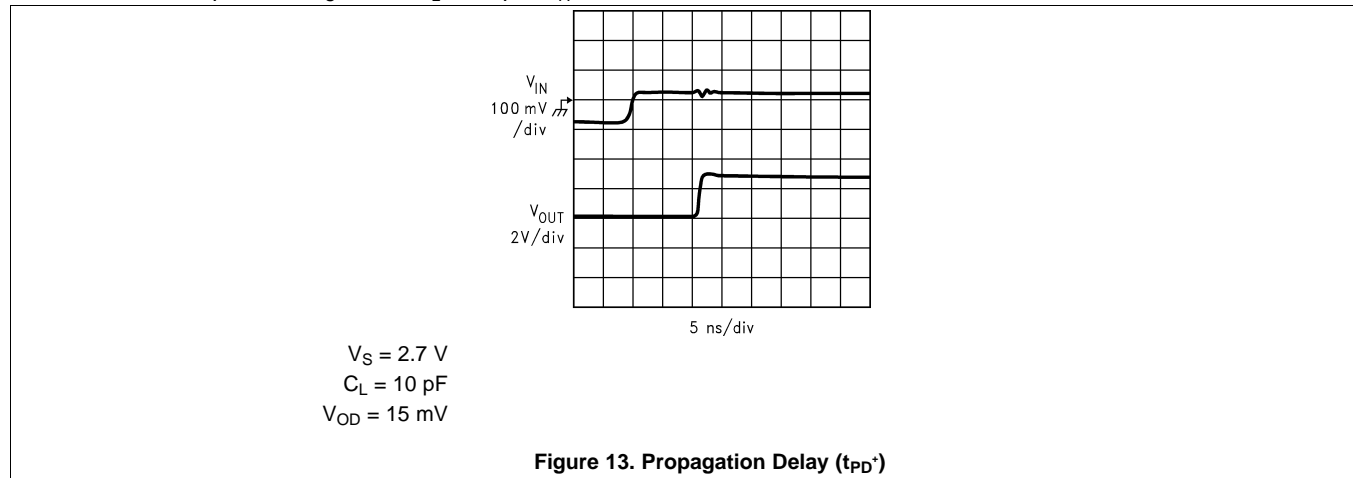


Figure 12. Propagation Delay (t_{PD})

Typical Performance Characteristics (continued)

Unless otherwise specified, $V_S = 5\text{ V}$, $C_L = 10\text{ pF}$, $T_A = 25^\circ\text{C}$



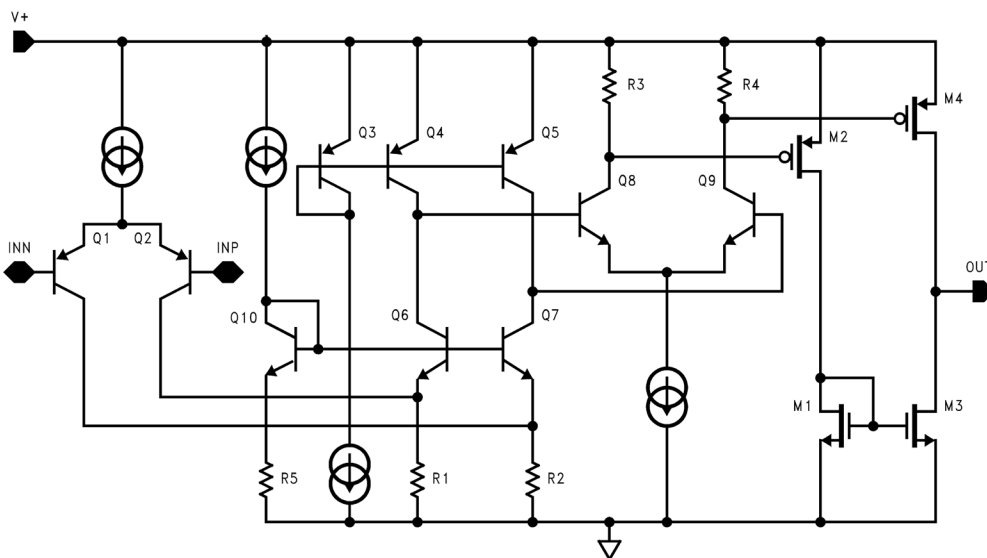
7 Detailed Description

7.1 Overview

LMV7219 is a single supply comparator with internal hysteresis, 7 ns of propagation delay and only 1.1 mA of supply current.

The LMV7219 has a typical input common mode voltage range of -0.2 V below the ground to 1 V below V_{CC} . The differential input stage is a pair of PNP transistors, therefore, the input bias current flows out of the device. If either of the input signals falls below the negative common mode limit, the parasitic PN junction formed by the substrate and the base of the PNP will turn on, resulting in an increase of input bias current.

7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

7.3 Feature Description

If one of the inputs goes above the positive common mode limit, the output will still maintain the correct logic level as long as the other input stays within the common mode range. However, the propagation delay will increase. When both inputs are outside the common mode voltage range, current saturation occurs in the input stage, and the output becomes unpredictable.

7.4 Device Functional Modes

The propagation delay does not increase significantly with large differential input voltages. However, large differential voltages greater than the supply voltage should be avoided to prevent damages to the input stage.

The LMV7219 has a push-pull output. When the output switches, there is a direct path between V_{CC} and ground, causing high output sinking or sourcing current during the transition. After the transition, the output current decreases and the supply current settles back to about 1.1 mA at 5 V, thus conserving power consumption.

Most high-speed comparators oscillate when the voltage of one of the inputs is close to or equal to the voltage on the other input due to noise or undesirable feedback. The LMV7219 has 7 mV of internal hysteresis to counter parasitic effects and noise. The hysteresis does not change significantly with the supply voltages and the common mode input voltages as reflected in the specification table.

8 Application and Implementation

NOTE

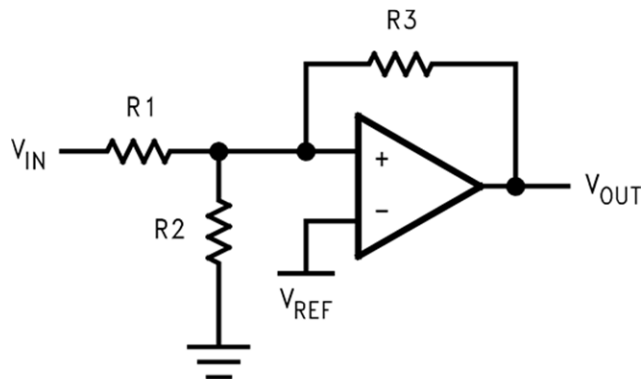
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following section explains in detail how to manipulate the hysteresis voltage of the LMV7219. Detailed expressions are provided along with practical considerations for designing hysteresis.

8.2 Typical Application

Figure 14 shows the typical method of adding external hysteresis to a comparator. The positive feedback is responsible for shifting the comparator trip point depending on the state of the output.



Copyright © 2016, Texas Instruments Incorporated

Figure 14. Additional Hysteresis

8.2.1 Design Requirements

The internal hysteresis creates two trip points, one for the rising input voltage and one for the falling input voltage, as shown in Figure 19. The difference between the trip points is the hysteresis. With internal hysteresis, when the comparator's input voltages are equal, the hysteresis effectively causes one comparator-input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. The fixed internal hysteresis eliminates these resistors.

8.2.2 Detailed Design Procedure

8.2.2.1 Additional Hysteresis

If additional hysteresis is desired, this can be done with the addition of three resistors using positive feedback, as shown in Figure 14. The positive feedback method slows the comparator response time. Calculate the resistor values as follows:

1. Select R3. The current through R3 should be greater than the input bias current to minimize errors. The current through R3 (I_F) at the trip point is $(V_{REF} - V_{OUT}) / R3$. Consider the two possible output states when solving for R3, and use the smaller of the two resulting resistor values. The two formulas are:

$$R3 = V_{REF} / I_F \quad (1)$$

When $V_{OUT} = 0$:

Typical Application (continued)

$$R3 = V_{CC} - V_{REF} / I_F \tag{2}$$

When $V_{OUT} = V_{CC}$:

2. Choose a hysteresis band required (V_{HB}).
3. Calculate R1, where $R1 = R3 \times (V_{HB}/V_{CC})$
4. Choose the trip point for V_{IN} rising. This is the threshold voltage (V_{THR}) at which the comparator switches from low to high as V_{IN} rises about the trip point.
5. Calculate R2 as follows:

$$R_2 = \frac{1}{\left(\frac{V_{THR}}{V_{REF} \times R_1}\right) - \frac{1}{R_1} - \frac{1}{R_3}} \tag{3}$$

6. Verify the trip voltage and hysteresis as follows:

$$V_{IN} \text{ rising: } V_{THR} = V_{REF} \times R_1 \times \left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right)$$

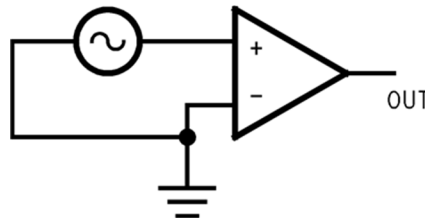
$$V_{IN} \text{ falling: } V_{THF} = V_{THR} - \left(\frac{R_1 \times V_{CC}}{R_3}\right)$$

$$\text{Hysteresis} = V_{THR} - V_{THF} \tag{4}$$

This method is recommended for additional hysteresis of up to a few hundred millivolts. Beyond that, the impedance of R3 is low enough to affect the bias string and adjustment of R1 may be also required.

8.2.2.2 Zero-Crossing Detector

The inverting input is connected to ground and the non-inverting input is connected to 100mVp-p signal. As the signal at the non-inverting input crosses 0 V, the comparator's output Changes State.

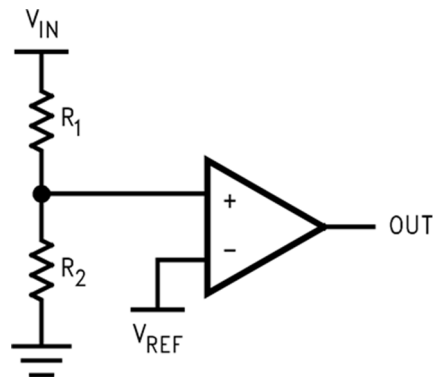


Copyright © 2016, Texas Instruments Incorporated

Figure 15. Zero-Crossing Detector

8.2.2.3 Threshold Detector

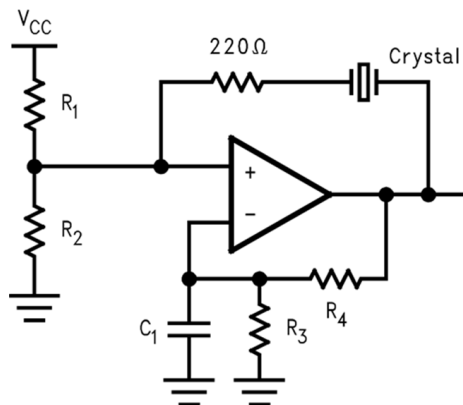
Instead of tying the inverting input to 0 V, the inverting input can be tied to a reference voltage. The non-inverting input is connected to the input. As the input passes the V_{REF} threshold, the comparator's output changes state.

Typical Application (continued)


Copyright © 2016, Texas Instruments Incorporated

Figure 16. Threshold Detector
8.2.2.4 Crystal Oscillator

A simple crystal oscillator using the LMV7219 is shown in [Figure 17](#). Resistors R1 and R2 set the bias point at the comparator's non-inverting input. Resistors R3, R4 and C1 sets the inverting input node at an appropriate DC average level based on the output. The crystal's path provides resonant positive feedback and stable oscillation occurs. The output duty cycle for this circuit is roughly 50%, but it is affected by resistor tolerances and to a lesser extent by the comparator offset.

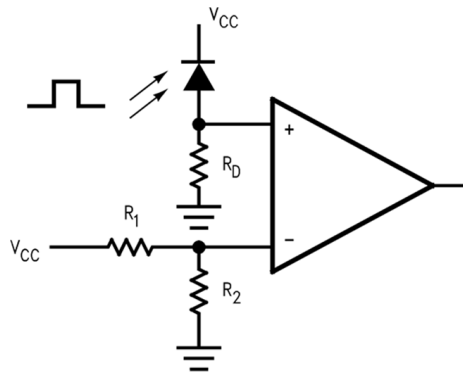


Copyright © 2016, Texas Instruments Incorporated

Figure 17. Crystal Oscillator
8.2.2.5 IR Receiver

The LMV7219 is an ideal candidate to be used as an infrared receiver. The infrared photo diode creates a current relative to the amount of infrared light present. The current creates a voltage across RD. When this voltage level cross the voltage applied by the voltage divider to the inverting input, the output transitions.

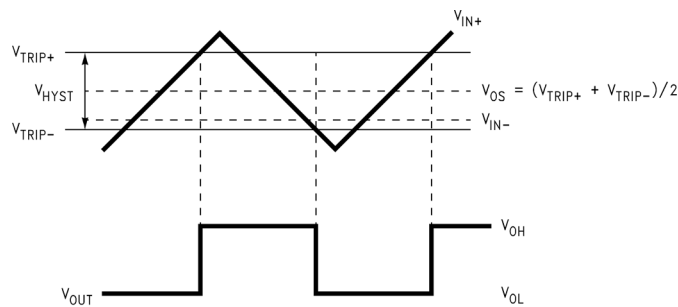
Typical Application (continued)



Copyright © 2016, Texas Instruments Incorporated

Figure 18. IR Receiver

8.2.3 Application Curve



Copyright © 2016, Texas Instruments Incorporated

Figure 19. Input and Output Waveforms, Non-Inverting Input Varied

9 Power Supply Recommendations

The LMV7219 can operate off a single supply or with dual supplies as long as the input CM voltage range (V_{CM}) has the required headroom to the positive rail $V+$. The input range extends to slightly below $V-$ voltage. Supplies should be decoupled with low inductance, often ceramic, capacitors to ground less than 0.5 inches from the device pins. The use of ground plane is recommended, and as in most high speed devices, it is advisable to remove ground plane close to device sensitive pins such as the inputs.

10 Layout

10.1 Layout Guidelines

10.1.1 Circuit Layout and Bypassing

The LMV7219 requires high-speed layout. Follow these layout guidelines:

1. Power supply bypassing is critical, and will improve stability and eliminate possible output chatter. A decoupling capacitor such as 0.1- μ F ceramic should be placed as close as possible to V^+ pin (and to $V-$ pin if used with dual supplies) as shown in [Figure 20](#). An additional 2.2- μ F tantalum capacitor may be required for extra noise reduction.
2. Keep all leads short to reduce stray capacitance and lead inductance. It will also minimize unwanted parasitic feedback around the comparator.
3. The device should be soldered directly to the PC board instead of using a socket.
4. Use a PC board with a good, unbroken low inductance ground plane as shown in [Figure 20](#). Make sure ground paths are low-impedance, especially where heavier currents are flowing.
5. Input traces should be kept away from output traces. This can be achieved by running a topside ground plane between the output and inputs.
6. Run the ground trace under the device up to the bypass capacitor to shield the inputs from the outputs.
7. To prevent parasitic feedback when input signals are slow-moving, a small capacitor of 1000 pF or less can be placed between the inputs. It can also help eliminate oscillations in the transition region. However, this capacitor can cause some degradation to t_{pd} when the source impedance is low.

10.2 Layout Example

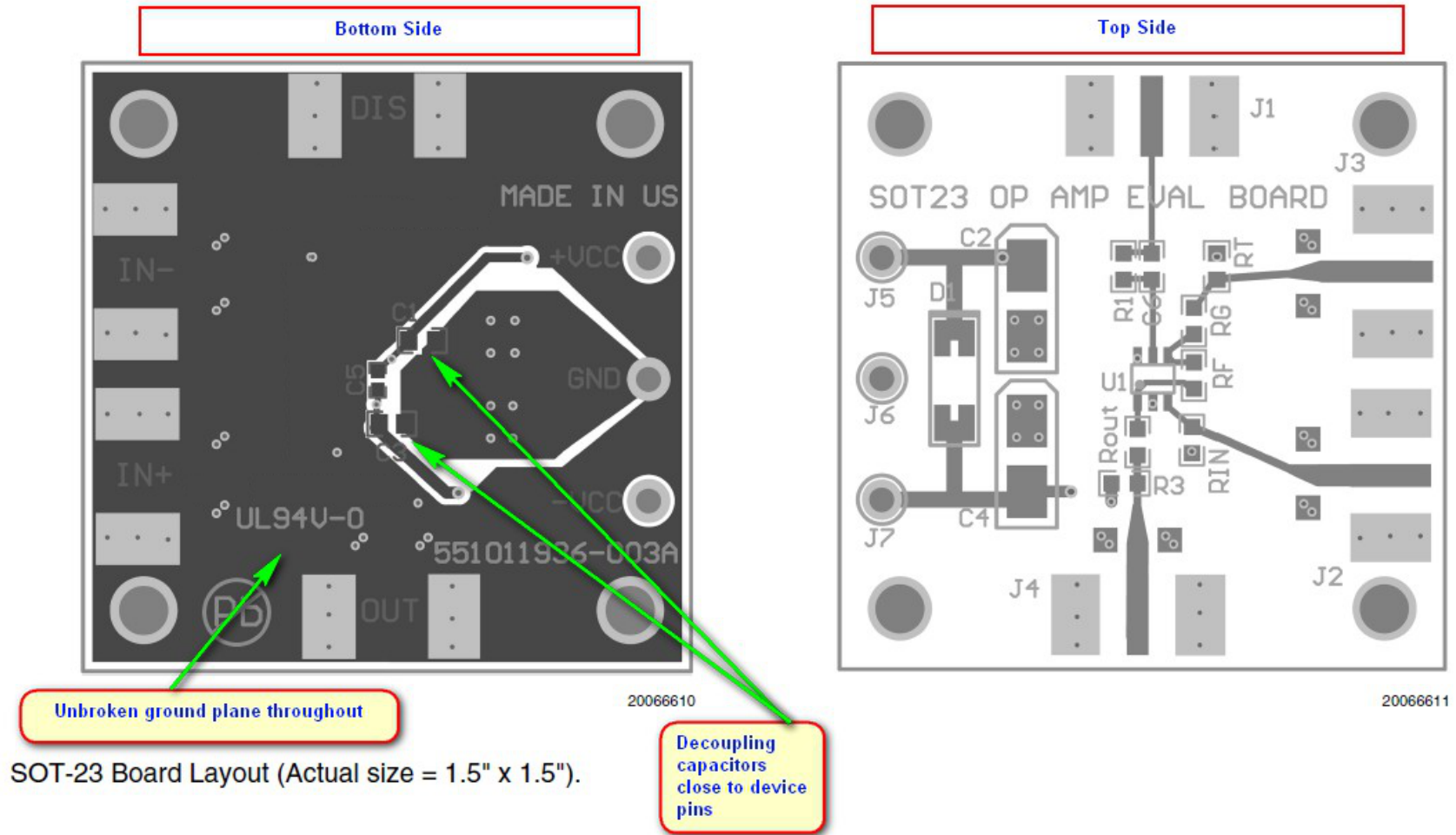


Figure 20. SOT-23 Board Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- [Absolute Maximum Ratings for Soldering \(SNOA549\)](#)
- [Semiconductor and IC Package Thermal Metrics \(SPRA953\)](#)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV7219M5	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 85	C14A	
LMV7219M5/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C14A	Samples
LMV7219M5X	NRND	SOT-23	DBV	5	3000	TBD	Call TI	Call TI	-40 to 85	C14A	
LMV7219M5X/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C14A	Samples
LMV7219M7	NRND	SC70	DCK	5	1000	TBD	Call TI	Call TI	-40 to 85	C15	
LMV7219M7/NOPB	ACTIVE	SC70	DCK	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C15	Samples
LMV7219M7X	NRND	SC70	DCK	5		TBD	Call TI	Call TI	-40 to 85	C15	
LMV7219M7X/NOPB	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	C15	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMV7219M5	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7219M5/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7219M5X	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7219M5X/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LMV7219M7	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7219M7/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
LMV7219M7X/NOPB	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

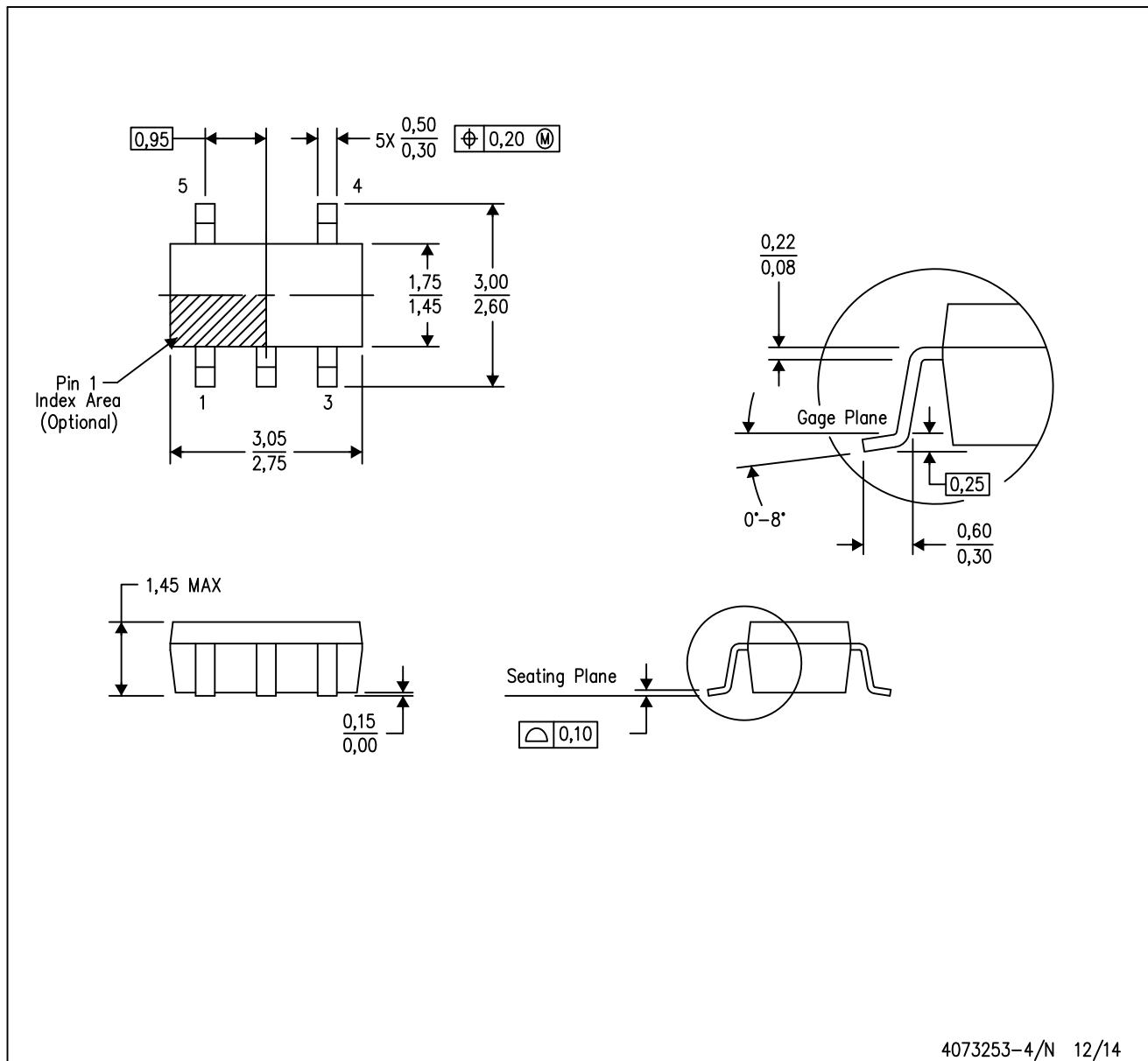
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMV7219M5	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7219M5/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LMV7219M5X	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7219M5X/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LMV7219M7	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7219M7/NOPB	SC70	DCK	5	1000	210.0	185.0	35.0
LMV7219M7X/NOPB	SC70	DCK	5	3000	210.0	185.0	35.0

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5)

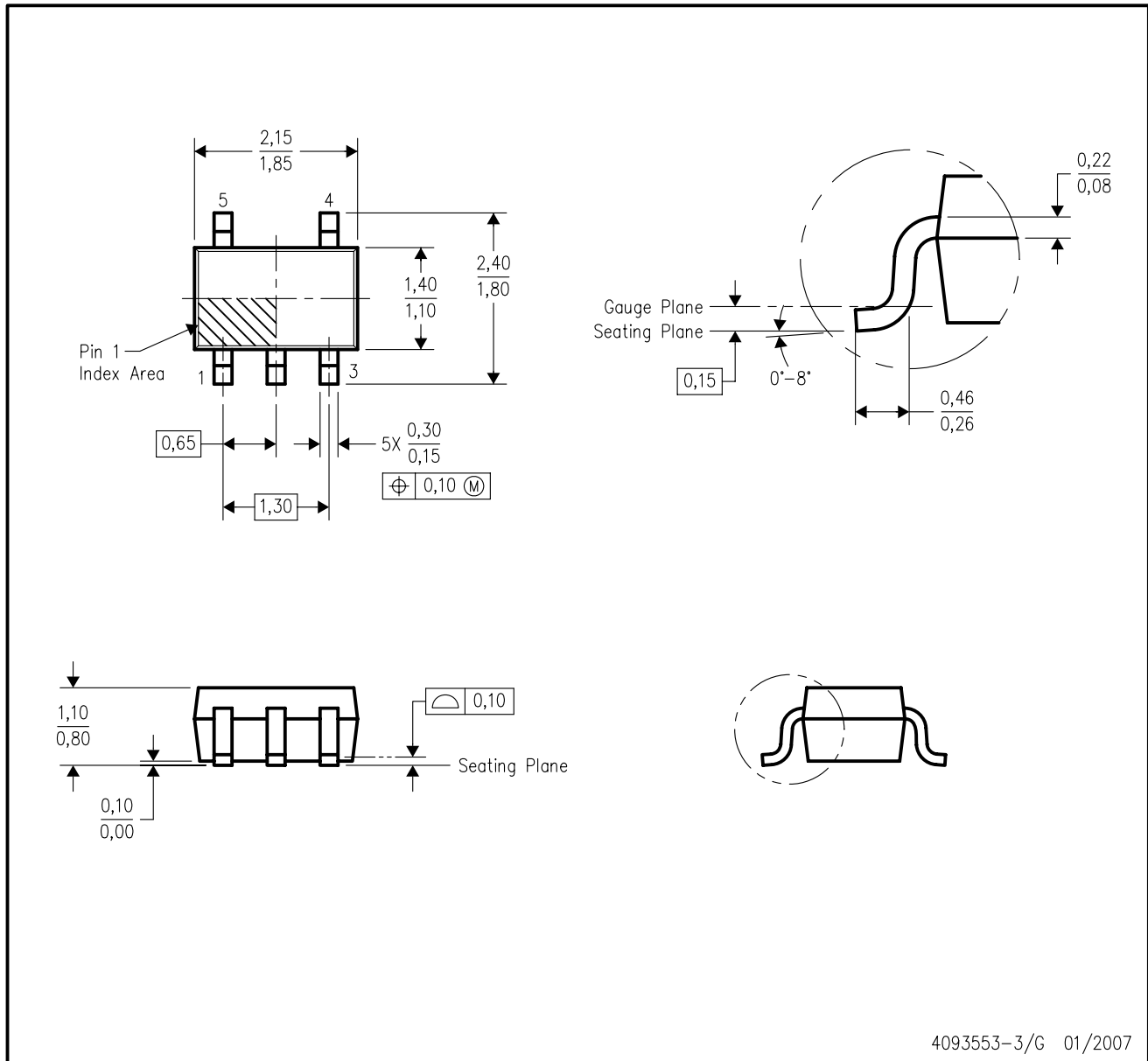
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G5)

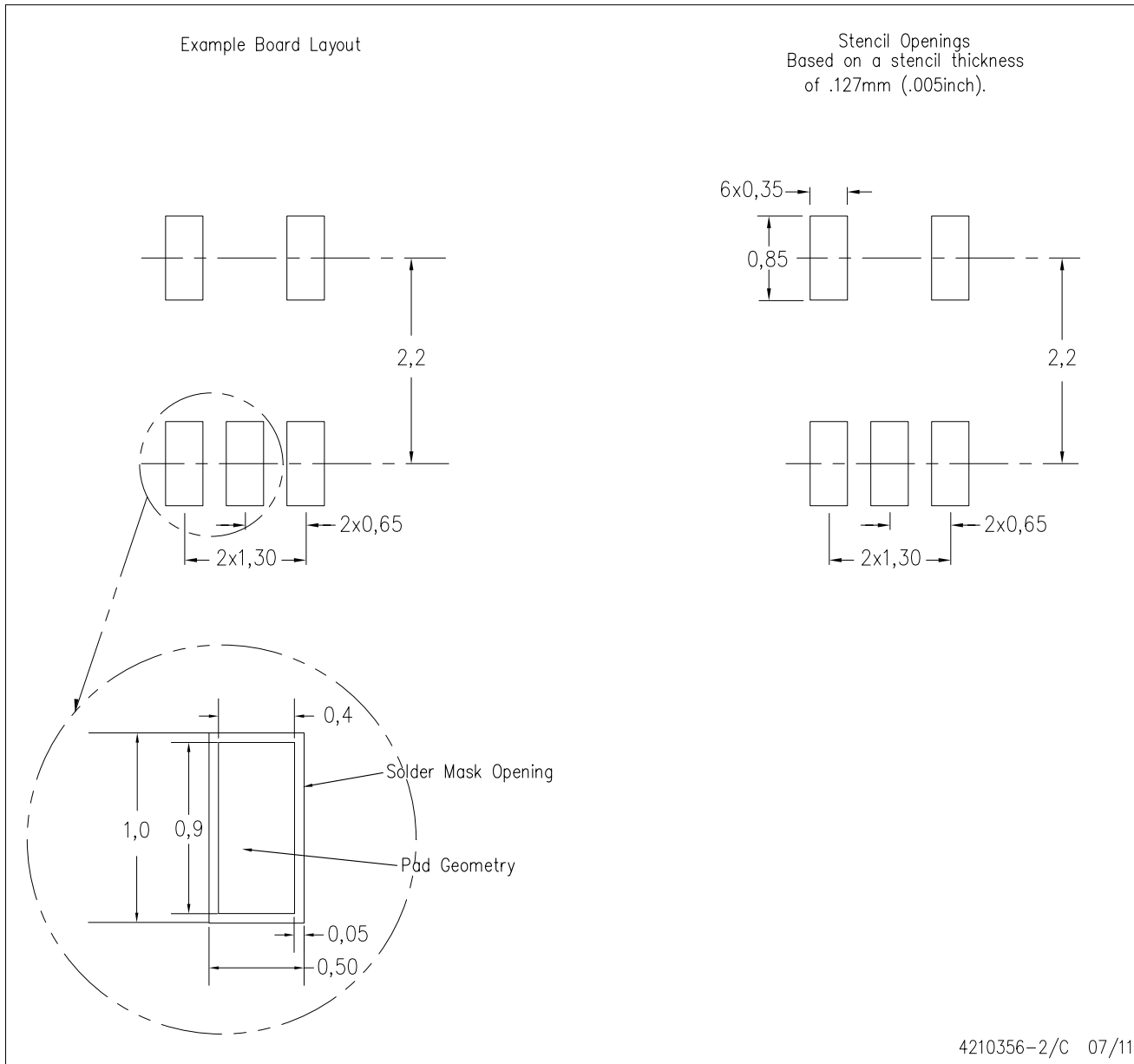
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.