Genesys Logic, Inc.

GL857L

USB 2.0 Hub Reader Controller

Datasheet

Revision 1.30
Oct. 26, 2016

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Revision History

Revision	Date	Description
1.00	05/22/2014	Formal release
1.10	09/19/2014	Updated CH3 Pin Assignment Description, p. 12
1.20	12/18/2014	Added CH6.5 Power Consumption, p. 23
1.30	10/26/2016	Modify T_A range, p. 21

Table of Contents

List of Figures

List of Tables

CHAPTER 1 GENERAL DESCRIPTION

GL857L is Genesys Logic's combo solution for USB2.0 hub (with 3 downstream ports) and SD card reader in single chip SSOP28 package. It is fully compliant with Universal Serial Bus Specification Revision 2.0, USB Storage Class Specification ver.1.0 and supports Secure Digital™ v1.0 / v1.1 / v2.0/ SDHC / SDXC (capacity up to 2TB). GL857L inherits Genesys Logic's cutting edge technology on cost and power efficient serial interface design. GL857L has proven compatibility, lower power consumption figure, and better cost structure above all USB2.0 hub-reader solutions worldwide.

GL857L provides multiple advantages to simplify board level design that helps achieve lowest BOM (Bill of Material) for system integrator by integrating both 5V to 3.3V with power MOSFETs and 3.3V to 1.8V low dropout voltage regulator into single chip, therefore no external LDO required. Also, it enables the function of on-chip clock source (OCCS) which indicates that no external 12MHz XTAL is needed.

GL857L embeds an 8-bit RISC processor to manipulate the control/status registers and respond to the requests from USB host. Another one high speed 8051 microprocessor and a high efficiency hardware engine are also embedded for the best data transfer performance between USB and flash card interfaces.

CHAPTER 2 FEATURES

2.1 General

- 3 downstream ports of USB2.0 Hub with SD Card Reader
- Integrated USB transceiver
- Built-in upstream 1.5KΩ pull-up and downstream 15KΩ pull-down
- Integrated 5-to-3.3 regulator and 3.3-to-1.8 regulator
- 0.152um CMOS technology
- On chip clock source and no external crystal needed.

2.2 USB 2.0 3-port Hub

- Compliant to USB specification Revision 2.0
  - Configurable 3/2/1 downstream ports
  - upstream port supports both high speed(HS) and full speed(FS) traffic
  - downstream ports support HS, FS, and low speed(LS) traffic
  - 1 control pipe(endpoint 0, 64-byte data payload) and 1 interrupt pipe(endpoint 1, 1-byte data payload)
  - backward compatible to USB specification Revision 1.1
- Support gang modes of power management and over-current detection for downstream ports.
- On-chip 8-bit micro-processor
  - RISC-like architecture
  - USB optimized instruction set
  - Single cycle instruction execution
  - Performance: 6 MIPS @ 12MHz
  - With 64-byte RAM and 2K mask ROM

2.3 SD2.0 Card Reader

- USB specification compliance
  - Comply with 480Mbps Universal Serial Bus specification rev. 2.0
  - Comply with USB Storage Class specification rev. 1.0
  - Support one device address and up to four endpoints: Control (0)/ Bulk Read (1)/ Bulk Write (2)/Interrupt(3)
- Secure DigitalTM (SD) and MultiMediaCardTM (MMC)
  - Supports SD specification v1.0 / v1.1 / v2.0 / SDHC (Up to 32GB)
  - Compatible with SDXC (Up to 2TB)
  - Supports MMC specification v3.x / v4.0 / v4.1 / v4.2
  - x1 / x4 bit data bus
- Support SD3.0 by 80MHz for better performance
- Embedded PMOS switch for power control of card interface

2.4 Available Packages

- SSOP-28 (150mil)

CHAPTER 3 PIN ASSIGNMENT

3.1 Pinouts

Figure 3.1 - GL857L SSOP 28 Pin Pin-out Diagram

3.2 Pin List

Table 3.1 - GL857L SSOP 28 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	RESETJ	I_5V	8	AVDD	P	15	V33	P	22	SD_D0	B,pu
2	GND	P	9	DM3	B	16	V5	P	23	SD_CLK	O
3	AVDD	P	10	DP3	B	17	PMOS	A	24	DVDD	P
4	DM0	B	11	RREF	A	18	GPIO4	O	25	SD_CMD	B,pu
5	DP0	B	12	AVDD1	P	19	SD_WPZ	I.pu	26	SD_D3	B,pu
6	DM2	B	13	DM4	B	20	SD_CDZ	I.pu	27	SD_D2	B,pu
7	DP2	B	14	DP4	B	21	SD_D1	B,pu	28	OCVUR1J	I_5V

Table 3.2 - Pin Descriptions

USB Interface			
Pin Name	**GL857L SSOP 28 Pin**	**I/O Type**	**Description**
DM0,DP0	4,5	B	USB signals for USPORT
DM2,DP2	6,7	B	USB signals for DSPORT1
DM3,DP3	9,10	B	USB signals for DSPORT2
DM4,DP4	13,14	B	USB signals for DSPORT3
RREF	11	A	A 680Ω resister must be connected between RREF and analog ground (AGND)

Note: USB signals must be carefully handled in PCB routing. For detailed information, please refer to **USB 2.0 Hub Design Guide**.

Hub/Reset Interface			
Pin Name	**GL857L SSOP 28 Pin**	**I/O Type**	**Description**
OVCUR1J	28	I_5V	Active low. Over current indicator for DSPORT1~3. *Over current flag On when OVCUR= low over 3ms. OVCUR1J the only over current flag for GANG mode.
RESETJ	1	I_5V	Active low. External reset input, default pull high 10KΩ When RESETJ = low, whole chip is reset to the initial state

Reader Interface			
Pin Name	**GL857L SSOP 28 Pin**	**I/O Type**	**Description**
SD_WPZ	19	I, pu	SD Write Protect, active low
SD_CDZ	20	I, pu	SD Card Detect, active low
SD_D[3:0]	26,27,21,22	B, pu	SD Data signals
SD_CLK	23	O	SD Clock signal
SD_CMD	25	B, pu	SD Command signal
GPIO4	18	O	Card Reader Power & Access LED

Power / Ground			
Pin Name	**GL857L SSOP 28 Pin**	**I/O Type**	**Description**
AVDD	3,8	P	3.3V analog power input for analog circuits
AVDD1	12	P	3.3V analog power input for analog PLL circuits
DVDD	24	P	3.3V digital power input for digital circuits
GND	2	P	Ground Exposed pad is connected to GND
V5	16	P	5V Power input. It need be NC if using external regulator
V33	15	P	5V-to-3.3V regulator Vout & 3.3 input
PMOS	17	A	PMOS 3.3V output to SD Card (current capacity 200mA)

Note: Analog circuits are quite sensitive to power and ground noise. PCB layout must takes care the power routing and the ground plane. For detailed information, please refer to **USB 2.0 Hub Design Guide.**

Notation:

Type	**O**	Output
	I	Input
	I_5V	5V tolerant input
	B	Bi-directional
	B/I	Bi-directional, default input
	B/O	Bi-directional, default output
	P	Power / Ground
	A	Analog
	SO	Automatic output low when suspend
	pu	Internal pull high
	pd	Internal pull down
	odpu	Open drain with internal pull high

CHAPTER 4 BLOCK DIAGRAM

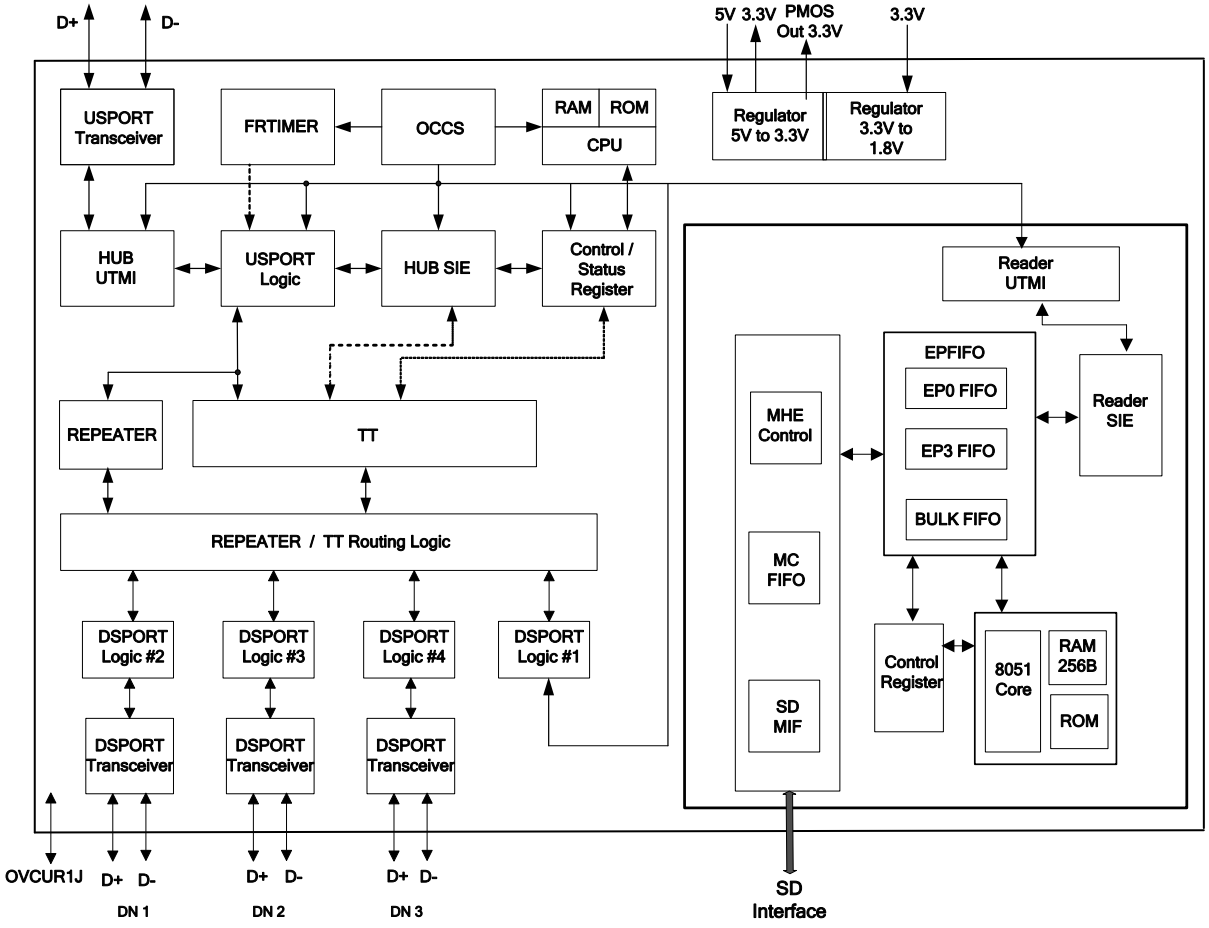


Figure 4.1- GL857L Block Diagram

CHAPTER 5 FUNCTION DESCRIPTION

5.1 General Description

5.1.1 USPORT Transceiver

USPORT (upstream port) transceiver is the analog circuit that supports both full-speed and high-speed electrical characteristics defined in chapter 7 of *USB specification Revision 2.0*. USPORT transceiver will operate in full-speed electrical signaling when GL857L is plugged into a 1.1 host/hub. USPORT transceiver will operate in high-speed electrical signaling when GL857L is plugged into a 2.0 host/hub.

5.1.2 FRTIMER

This module implements hub (micro) frame timer. The (micro) frame timer is derived from the hub's local clock and is synchronized to the host (micro) frame period by the host generated Start of (micro) frame (SOF). FRTIMER keeps tracking the host's SOF such that GL857L is always safely synchronized to the host. The functionality of FRTIMER is described in section 11.2 of *USB Specification Revision 2.0.*

5.1.3 OCCS USB PHY

The USB 2.0 Transceiver Macrocell is the analog circuitry that handles the low level USB protocol and signaling and shifts the clock domain of the data from the USB 2.0 rate to one that is compatible with the general logic. On chip clock source and no need of 12MHz Crystal Clock input.

5.1.4 µC

µC is the micro-processor unit of GL857L. It is an 8-bit RISC processor with 2K ROM and 64 bytes RAM. It operates at 6MIPS of 12MHz clock to decode the USB command issued from host and then prepares the data to respond to the host. In addition, µC can handle GPIO (general purpose I/O) settings and reading content of EEPROM to support high flexibility for customers of different configurations of hub. These configurations include self/bus power mode setting, individual/gang mode setting, downstream port number setting, device removable/non-removable setting, port electrical tuning and PID/VID setting.

5.1.5 UTMI (USB 2.0 Transceiver Microcell Interface)

UTMI handles the low level USB protocol and signaling. It's designed based on the Intel's UTMI specification 1.01. The major functions of UTMI logic are to handle the data and clock recovery, NRZI encoding/decoding, Bit stuffing /de-stuffing, supporting USB 2.0 test modes, and serial/parallel conversion.

5.1.6 USPORT Logic

USPORT implements the upstream port logic defined in section 11.6 of *USB specification Revision 2.0.* It mainly manipulates traffics in the upstream direction. The main functions include the state machines of Receiver and Transmitter, interfaces between UTMI and SIE, and traffic control to/from the REPEATER and TT.

5.1.7 SIE (Serial Interface Engine)

SIE handles the USB protocol defined in chapter 8 of *USB specification Revision 2.0.* It co-works with µC to play the role of the hub kernel. The main functions of SIE include the state machine of USB protocol flow, CRC check, PID error check, and timeout check. Unlike USB 1.1, bit stuffing/de-stuffing is implemented in UTMI, not in SIE.

5.1.8 Control/Status Register

Control/Status register is the interface register between hardware and firmware. This register contains the information necessary to control endpoint0 and endpoint1 pipes. Through the firmware based architecture, GL857L possesses higher flexibility to control the USB protocol easily and correctly.

5.1.9 REPEATER

Repeater logic implements the control logic defined in section 11.4 and section 11.7 of *USB specification Revision 2.0*. REPEATER controls the traffic flow when upstream port and downstream port are signaling in the same speed. In addition, REPEATER will generate internal resume signal whenever a wakeup event is issued under the situation that hub is globally suspended.

5.1.10 TT (Transaction Translator)

TT implements the control logic defined in section 11.14 ~ 11.22 of *USB specification Revision 2.0*. TT basically handles the unbalanced traffic speed between the USPORT (operating in HS) and DSPORTS (operating in FS/LS) of hub. GL857L adopts the single TT architecture to provide the most cost effective solution.

5.1.11 REPEATER/TT Routing Logic

REPEATER and TT are the major traffic control machines in the USB 2.0 hub. Under situation that USPORT and DSPORT are signaling in the same speed, REPEATER/TT routing logic switches the traffic channel to the REPEATER. Under situation that USPORT is in the high speed signaling and DSPORT is in the full/low speed signaling, REPEATER/TT routing logic switches the traffic channel to the TT.

5.1.11.1 Connected to USB 1.1 Host/Hub

If an USB 2.0 hub is connected to the downstream port of an USB 1.1 host/hub, it will operate in USB 1.1 mode. For an USB 1.1 hub, both upstream direction traffic and downstream direction traffic are passing through REPEATER. That is, the REPEATER/TT routing logic will route the traffic channel to the REPEATER.

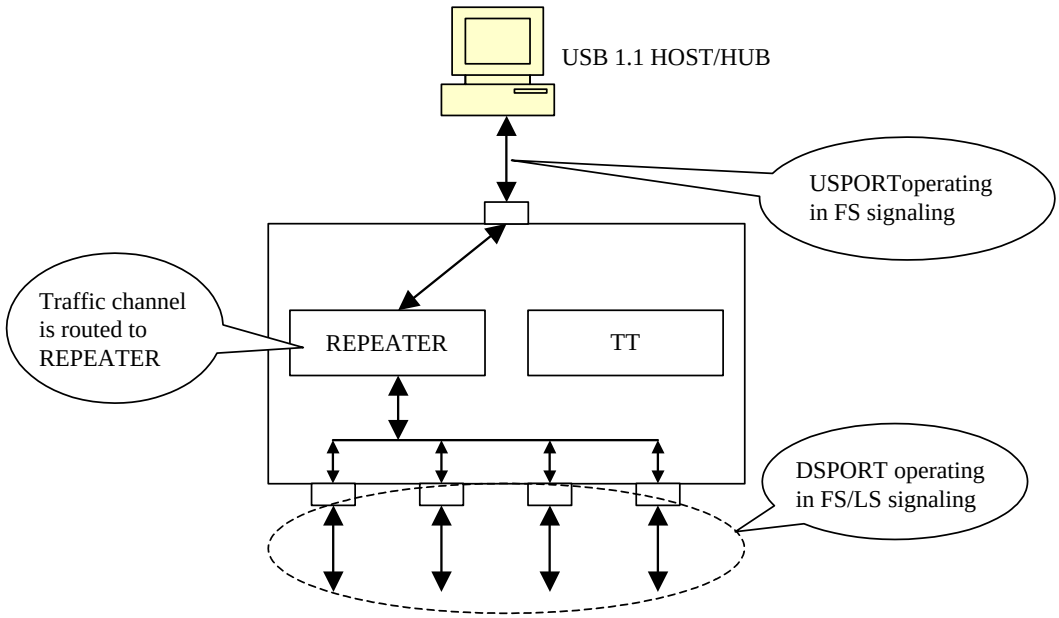


Figure 5.1 - Operating in USB 1.1 Scheme

5.1.11.2 Connected to USB 2.0 Host/Hub

If an USB 2.0 hub is connected to an USB 2.0 host/hub, it will operate in USB 2.0 mode. The upstream port signaling is in high speed with bandwidth of 480 Mbps under this environment. The traffic channel will then be routed to the REPEATER when the device connected to the downstream port is signaling also in high speed. On the other hand, the traffic channel will then be routed to TT when the device connected to the downstream port is signaling in full/low speed.

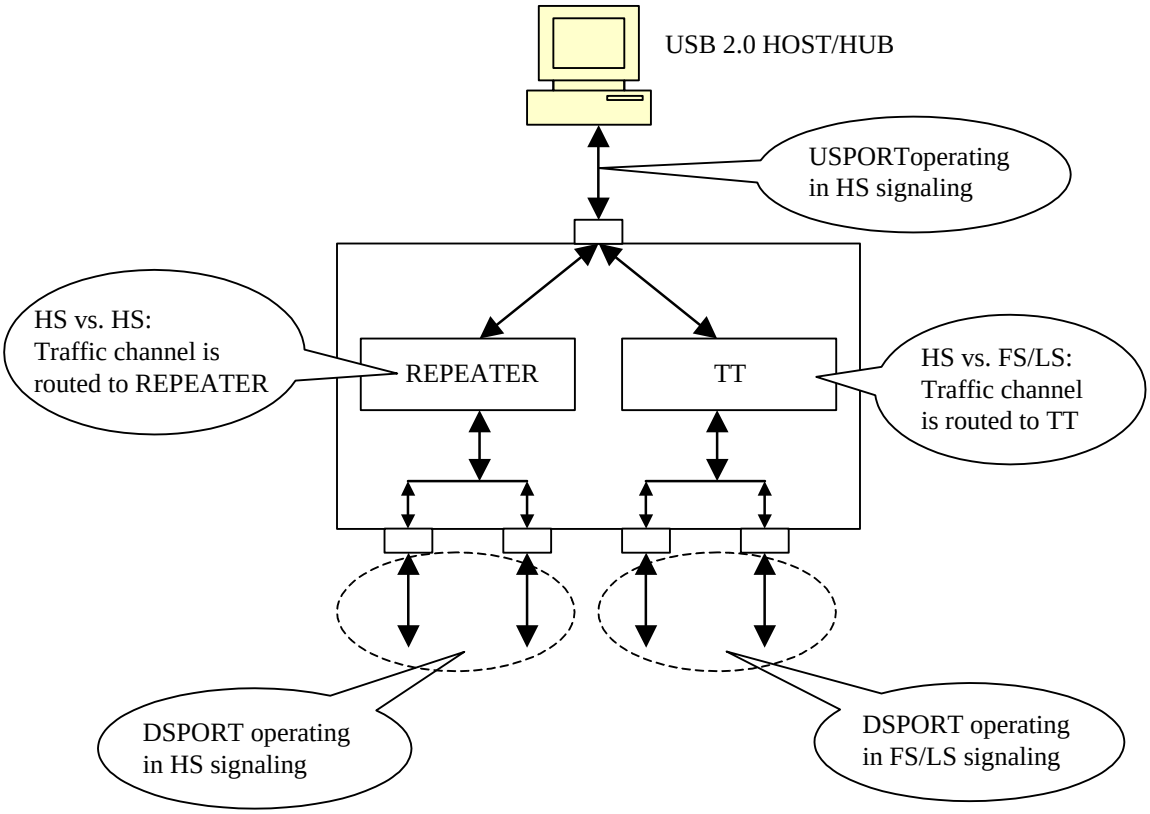


Figure 5.2 - Operating in USB 2.0 Scheme

5.1.12 DSPORT Logic

DSPORT (downstream port) logic implements the control logic defined in section 11.5 of *USB specification Revision 2.0.* It mainly manipulates the state machine, the connection/disconnection detection, over current detection and power enable control. Besides, it also output the control signals to the DSPORT transceiver.

5.1.13 DSPORT Transceiver

DSPORT transceiver is the analog circuit that supports high-speed, full-speed, and low-speed electrical characteristics defined in chapter 7 of *USB specification Revision 2.0.* In addition, each DSPORT transceiver accurately controls its own squelch level to detect the detachment and attachment of devices.

5.1.14 Regulator

GLI857L builds in two internal regulators as.

- **5V to 3.3V:** Band Gap Regulator for stable voltage supply for USB PHY, PMOS.
  When Power source is 3.3V, the 5V to 3.3V regulator will be disabled.
- **3.3V to 1.8V:** For core logic and internal memory.

5.1.15 EP0 FIFO for Card Reader

Endpoint 0 FIFO: The Control FIFO. It is composed of TX0FIFO and RX0FIFO, with 64-byte FIFO each, and it is used for endpoint 0 data transfer.

5.1.16 Bulk FIFO for Card Reader

It is composed of TXFIFO and RXFIFO for data transmission and receiving respectively, also with different modes support:

5.1.16.1 TXFIFO

- Supports MCU single byte access for SmartMedia ECC error correction.
- Supports transmit mode SIE won't transmit data filled in TXFIFO before MCU complete the data integrity checking.

5.1.16.2 RXFIFO

- Normally SME pops data, SIE pushes data for DATA A/B FIFOs, and redundant area is pushed by MCU and popped by SME.

5.1.17 MHE (Media Interface) for Card Reader

MIF Media Interface: SD
MCFIFO It can access by MCU for memory card short data packet.

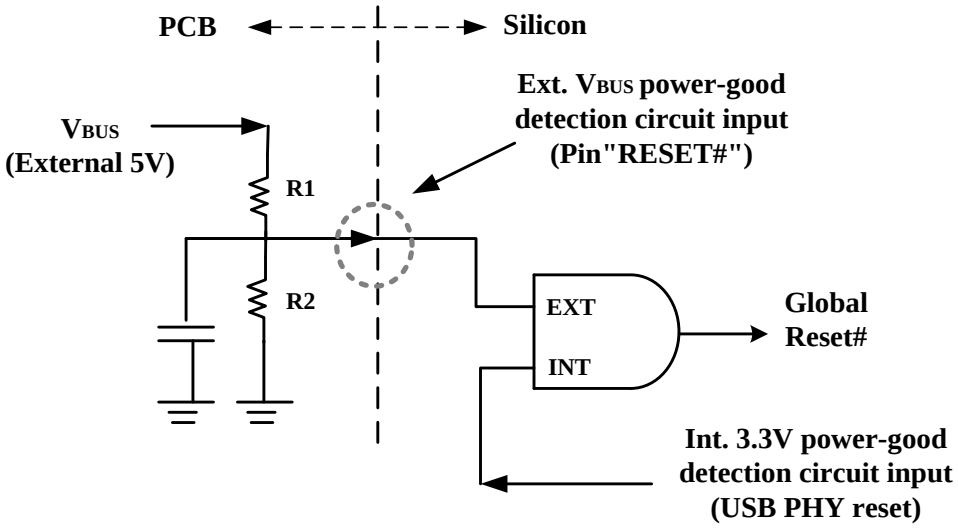
5.1.18 8051/MCU

The 8051/MCU is a super fast microprocessor . It includes 16K-byte ROM, 256-byte main memory SRAM. The frequency is 60 MHz at USB 2.0

5.2 Configuration and I/O Settings

5.2.1 RESET Setting

GL857L's power on reset can either be triggered by external reset or internal power good reset circuit. The external reset pin, RESETJ, is connected to upstream port Vbus (5V) to sense the USB plug / unplug or 5V voltage drop. The reset trigger voltage can be set by adjusting the value of resistor R1 and R2 (Suggested value refers to schematics) GL857L's internal reset is designed to monitor silicon's internal core power (3.3V) and initiate reset when unstable power event occurs. The power on sequence will start after the power good voltage has been met, and the reset will be released after approximately 2.7 uS after power good.



GL857L internally contains a power on reset circuit as depicted in the picture above

Figure 5.3 - Power on Reset Diagram

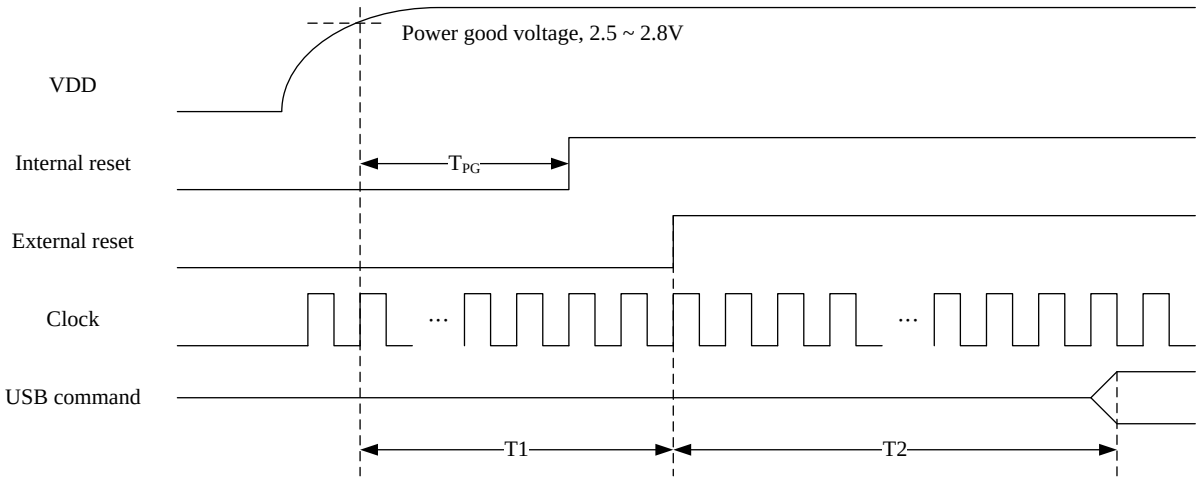


Figure 5.4 - Power on Sequence of GL857L

Table 5.1 - Reset Timing

Symbol	Parameter	Min.	Max.	Unit
T_{PG}	VDD power up to internal reset (power good) assert (12MHz)	-	2.7	µs
T1	VDD power up to external reset (RESETJ) assert	3	-	µs
T2	RESET assert to respond USB command ready	70	-	ms

To fully control the reset process of GL857L, we suggest the reset time applied in the external reset circuit should longer than that of the internal reset circuit.

5.2.2 Port Number Configuration

Number of downstream port can be configured by I/O Strapping. When DP and DM of a specific downstream port are pulled high externally with 1K resistor to 3.3V, the downstream port is disabled. Please refer to the following table for detailed setting information.

Table 5.2 - Port Number Configuration

Remaining Port Number	I/O Strapping
1	**DP3, DM3** Pull high
2	**DP4, DM4** Pull high

CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Maximum Ratings

Table 6.1 - Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_5	5V Power Supply	-0.5	+6.0	V
V_{DD}	3.3V Power Supply	-0.5	+3.6	V
V_{IN}	Input Voltage for digital I/O pins	-0.5	+3.6	V
V_{INOD}	Open-drain input pins(Ovcur1~4#,Pself,Reset)	-0.5	+5.5	V
V_{INUSB}	Input Voltage for USB signal (DP, DM) pins	-0.5	+3.6	V
T_S	Storage Temperature under bias	-55	+100	°C
	Operating Temperature	0	+70	°C
F_{OSC}	Frequency	12 MHz ± 0.05%		

6.2 Operating Ranges

Table 6.2 - Operating Ranges

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_5	5V Power Supply	4.75	5.0	5.25	V
V_{DD}	3.3V Power Supply	3.0	3.3	3.6	V
V_{IN}	Input Voltage for digital I/O pins	-0.5	-	3.6	V
V_{INOD}	Open-drain input pins(Ovcur1~4#,Pself,Reset)	-0.5	-	5.0	V
V_{INUSB}	Input Voltage for USB signal (DP, DM) pins	0.5	-	3.6	V
T_A	Ambient Temperature	0	-	70	°C
T_J	Absolute maximum junction temperature	0	-	125	°C
θ_{JA}	Thermal Characteristics 28 SSOP	-	65.65	-	°C/W

6.3 Memory Card Clock Frequency

Table 6.3 - SD/MMC Card Clock Frequency

Parameter	Description	Min.	Typ.	Max.	Unit
F_{ID}	Clock frequency Identification Mode	-	-	375	KHz
F_{DS}	Clock frequency Default Speed Mode	-	-	24	MHz
F_{HS}	Clock frequency High Speed Mode	-	-	48	MHz
F_{UHS}	Clock frequency Ultra High Speed Mode (SD only)	-	-	80	MHz

6.4 DC Characteristics

Table 6.4 - DC Characteristics except USB Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	LOW level input voltage	-	-	0.8	V
V_{IH}	HIGH level input voltage	2.0	-	-	V
V_{TLH}	LOW to HIGH threshold voltage	1.48	1.55	1.6	V
V_{THL}	HIGH to LOW threshold voltage	1.13	1.21	1.27	V
V_{OL}	LOW level output voltage when I_{OL}=8mA	-	-	0.4	V
V_{OH}	HIGH level output voltage when I_{OH}=8mA	2.4	-	-	V
R_{DN}	Pad internal pull down resister	230	275	565	KΩ
R_{UP}	Pad internal pull high resister	148	222	359	KΩ

Table 6.5 - DC Characteristics of USB Signals under FS/LS Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	DP/DM FS static output LOW(R_L of 1.5K to 3.6V)	0	-	0.3	V
V_{OH}	DP/DM FS static output HIGH (R_L of 15K to GND)	2.8	-	3.6	V
V_{DI}	Differential input sensitivity	0.2	-	-	V
V_{CM}	Differential common mode range	0.8	-	2.5	V
V_{SE}	Single-ended receiver threshold	0.2	-	-	V
C_{IN}	Transceiver capacitance	-	-	20	pf
I_{LO}	Hi-Z state data line leakage	-10	-	+10	μA
Z_{DRV}	Driver output resistance	28	-	44	Ω

Table 6.6 - DC Characteristics of USB Signals under HS Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	DP/DM HS static output LOW(R_L of 1.5K to 3.6V)	-	-	0.1	V
C_{IN}	Transceiver capacitance	4	4.5	5	pf
I_{LO}	Hi-Z state data line leakage	-5	0	+5	μA
Z_{DRV}	Driver output resistance for USB 2.0 HS	42	45	48	Ω

6.5 Power Consumption

Table 6.7 - GL857L power consumption

Symbol	Condition				Current	Unit
	Active ports	SD Card	Host	Device		
I_{SUSP}	Suspend				**1.14**	mA
I_{CC}	3	SD	H[*1]	H	**74.6**	mA
	3	-	H	H	**71.4**	mA
	2	-	H	H	**66.2**	mA
	1	-	H	H	**61.2**	mA
	-	SD	H	H	**56.4**	mA
	Upstream Port Config.	-	H	N/A	**53.1**	mA

[*1]: H: High-Speed

Note:

Test result was measured by 5V input (it will be lower by 3.3V input), and represents silicon level operating current, without considering additional power consumption contributed by external over-current protection circuit such as power switch or polyfuse.

6.6 On-Chip Power Regulator

GL857L requires 3.3V source power for normal operation of internal core logic and USB physical layer (PHY). The integrated low-drop power regulator converts 5V power input from USB cable (Vbus) to 3.3V voltage for silicon power source. The 3.3V power output is guaranteed by an internal voltage reference circuit to prevent unstable 5V power compromise USB data integrity. The regulator's maximum current loading is 200mA, which provides enough tolerance for normal GL857L operation (below 100mA).

On-chip Power Regulator Features:

- 5V to 3.3V low-drop power regulator
- 400mA maximum output driving capability
- Provide stable 3.3V output when Vin = 4.4V~5.5V
- Max. suspend current:266uA; typical suspend current 187uA

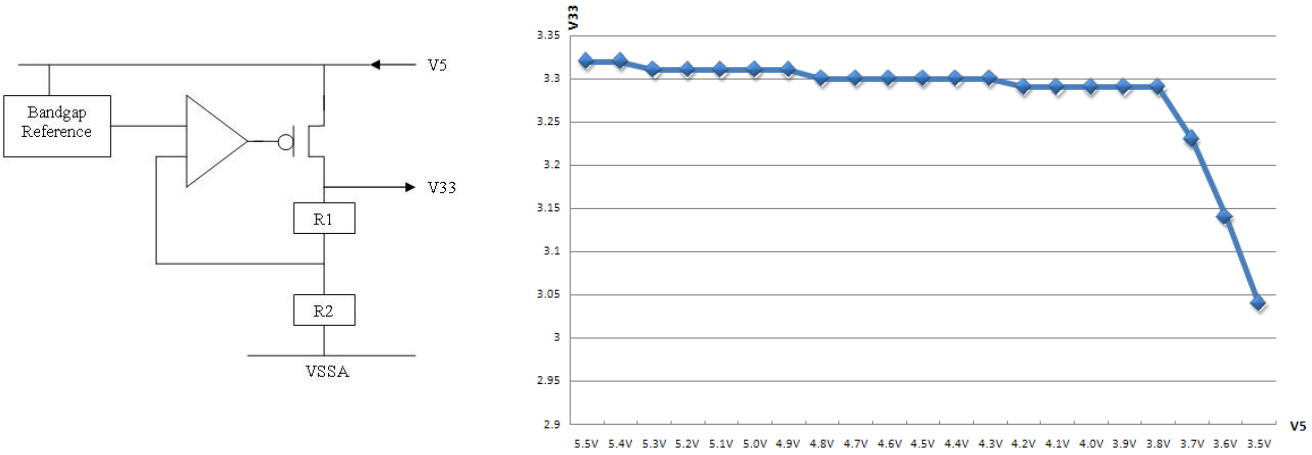
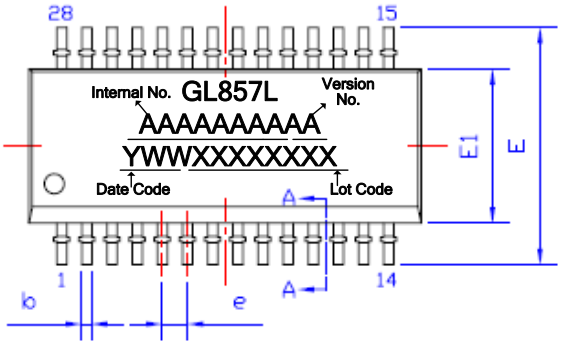


Figure 6.1 - Vin(V5) vs Vout(V33)*

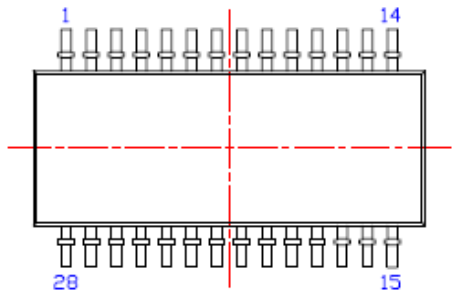
*Note: Measured environment: Ambient temperature = 25℃ / Current Loading = 200mA

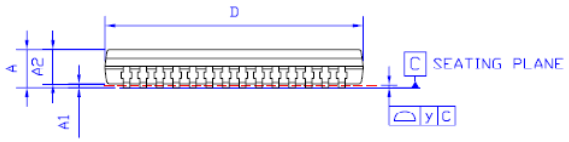
CHAPTER 7 PACKAGE DIMENSION

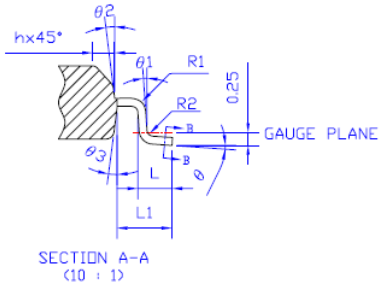


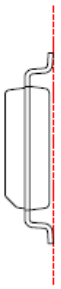
SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	---	---	1.75 (68.9)
A1	0.10 (3.9)	---	0.25 (9.8)
A2	1.30 (51.2)	1.40 (55.1)	1.50 (59.1)
b	0.20 (7.9)	---	0.30 (11.8)
b1	0.20 (7.9)	0.25 (9.8)	0.28 (11.0)
c	0.18 (7.1)	---	0.25 (9.8)
c1	0.18 (7.1)	---	0.23 (9.1)
D	9.90 (389.8) BSC		
e	0.635 (25.0) BSC		
E	6.00 (236.2) BSC		
E1	3.90 (153.5) BSC		
h	0.25 (9.8)	0.42 (16.5)	0.50 (19.7)
L	0.40 (15.7)	0.635 (25.0)	1.27 (50.0)
L1	1.05 (41.3) REF		
R1	0.15 (5.9)	0.20 (7.9)	0.25 (9.8)
R2	0.15 (5.9)	0.20 (7.9)	0.25 (9.8)
y	---	---	0.10 (3.9)
θ	0°	4°	8°
θ1	0°	---	---
θ2	7° TYP		
θ3	7° TYP		

NOTE: 1. REFER TO JEDEC MO-137
2. ALL DIMENSIONS IN MILLIMETERS.









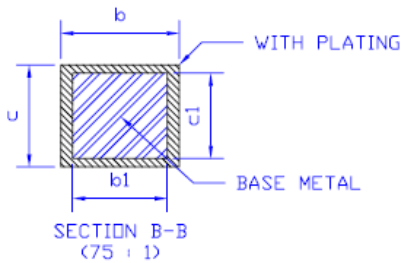


Figure 7.1 - GL857L 28 Pin SSOP Package (150 mil)

CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Package Type	Version	Status
GL857L-HHY10	SSOP 28	Green Package	10	Available