PAM8006A

15W Stereo Class-D Audio Power Amplifier with Power Limit

Key Features

- 15Wx2 into a 8Ω speaker
- Low Noise: -90dB
- Over 90% Efficiency
- With Shutdown/Mute Function
- Over Current ,OVP,UVLO,Thermal and Short-Circuit Protection
- Low THD+N
- Power Limit with Non-clip
- Low Quiescent Current
- Pop noise suppression
- Small Package Outlines: QFN5x5-32L
- Pb-Free Package (RoHS Compliant)

Applications

- Flat monitor /LCD TVS
- Multi-media speaker System
- DVD players, game machines
- Boom Box
- Music instruments

General Description

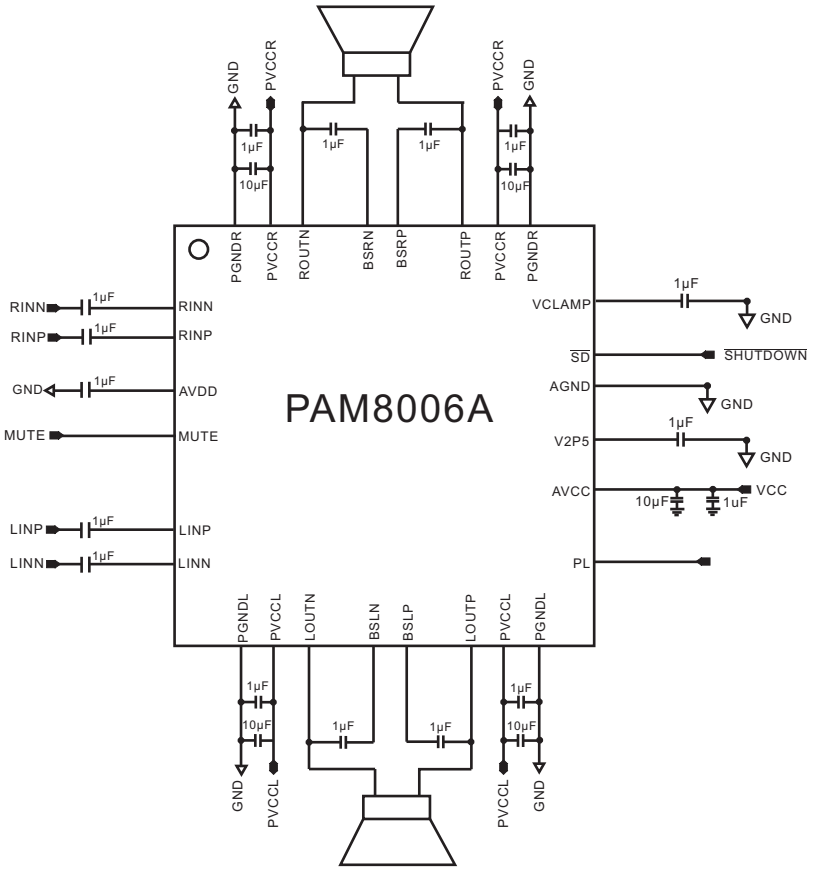
The PAM8006A is a 15W (per channel) stereo class-D audio amplifier which offers low THD+N (0.2%), low EMI, and good PSRR thus high-quality sound reproduction.

The PAM8006A runs off of a 8V to 18V supply at much higher efficiency than competitors' Ics.

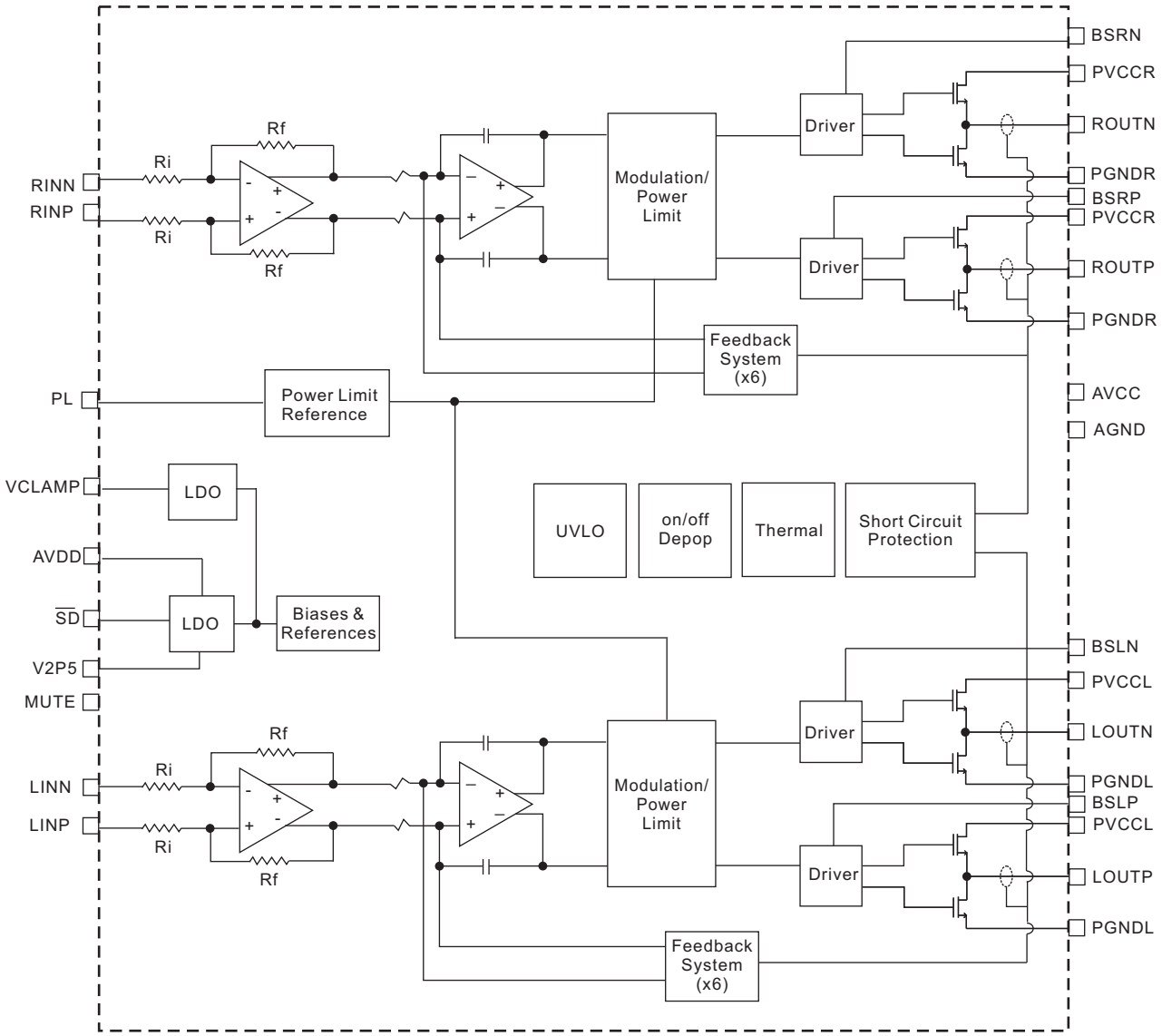
The PAM8006A only requires very few external components, significantly saving cost and board space.

The PAM8006A is available in a QFN5x5-32L package.

Typical Application



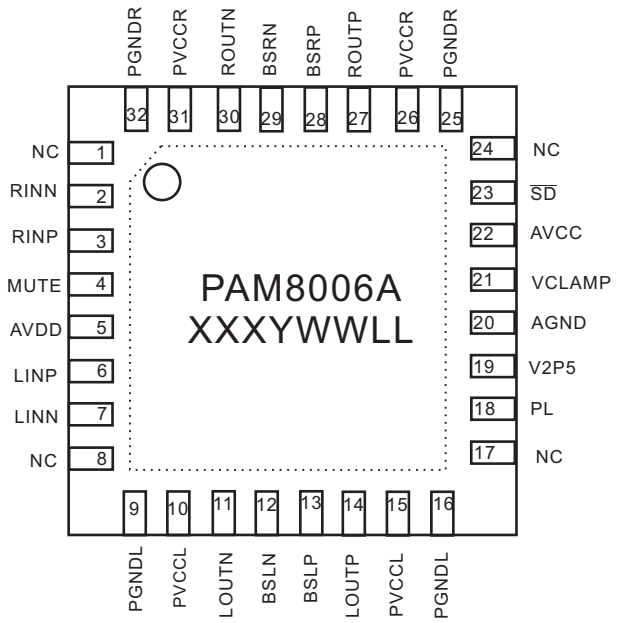
Block Diagram



Note:
Maximum Gain: Ri=12.5k, Rf=100k;
Power Limit Function: Ri and Rf are adjustable.

Pin Configuration & Marking Information

Top View
QFN5x5-32L



XXX: Internal Code
Y: Year
WW: Week
LL: Internal Code

Pin Descriptions

Pin No.	Name	Function
1,8,17,24	NC	No Connected
2	RINN	Negative differential audio input for right channel
3	RINP	Positive differential audio input for right channel
4	MUTE	A logic high on this pin disables the outputs and a logic low enables the outputs.
5	AVDD	5V Analog Supply
6	LINP	Positive differential audio input for left channel
7	LINN	Negative differential audio input for left channel
9,16	PGNDL	Power ground for left channel H-bridge
10,15	PVCCL	Power supply for left channel H-bridge, not connected to PVCCR or AVCC.
11	LOUTN	Class-D 1/2-H-bridge negative output for left channel
12	BSLN	Bootstrap I/O for left channel, negative high-side FET
13	BSLP	Bootstrap I/O for left channel, positive high-side FET
14	LOUTP	Class-D 1/2-H-bridge positive output for left channel
18	PL	Reference voltage for power limit function
19	V2P5	2.5V Reference for analog cells
20	AGND	Analog Ground
21	VCLAMP	Internally generated voltage supply for bootstrap capacitors.
22	AVCC	High-voltage analog power supply (8V to 26V)
23	$\overline{SD}$	Shutdown signal for IC (low= shutdown, high =operational). TTL logic levels with compliance to VCC.
25,32	PGNDR	Power ground for right channel H-bridge
26,31	PVCCR	Power supply for right channel H-bridge, not connected to PVCCL or AVCC.
27	ROUTP	Class-D 1/2-H-bridge positive output for right channel
28	BSRP	Bootstrap I/O for right channel, positive high-side FET
29	BSRN	Bootstrap I/O for right channel, negative high-side FET
30	ROUTN	Class-D 1/2-H-bridge negative output for right channel
33	Thermal Pad	Connect to ground. Thermal pad should be soldered down on all applications to secure the device properly to the printed wiring board.

Absolute Maximum Ratings

These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability. All voltages are with respect to ground.

Supply Voltage VCC.....-0.3V to 28V
Input Voltage Range V_I:
MUTE, PL.....0V to 6.0V
$\overline{SD}$.....-0.3V to VCC
RINN,RINP,LINN,LINP.....-0.3V to 6.0V

Junction Temperature Range,T_J.....-40°C to 125°C
Storage Temperature.....-65°C to150°C
Lead Temperature1,6mm(1/16 inch) from case for 5 seconds.....260°C

Recommended Operating Conditions

Supply Voltage (VCC)..... .....8V to 18V
Input Pin Voltage.....0V to 5.5V
High Level Input Voltage: $\overline{SD}$.....2.0V to VCC
MUTE. .....2.0V to 5.5V

Low Level Input Voltage: $\overline{SD}$.....0 to 0.3V
MUTE.....0 to 0.3V
Ambient Operating Temperature.....-20°C to 85°C

Thermal Information

Parameter	Package	Symbol	Maximum	Unit
Thermal Resistance (Junction to Case)	QFN5x5-32L	θ_{JC}	5.0	°C/W
Thermal Resistance (Junction to Ambient)	QFN5x5-32L	θ_{JA}	16.1	

The Exposed PAD must be soldered to a thermal land on the PCB.

Electrical Characteristic

T_A=25°C, VCC=12V,R_L=8Ω (unless otherwise noted)

Parameter	Symbol	Condition		MIN	TYP	MAX	Units
Continuous Output Power	Po	THD+N=0.12%,f=1kHz,R_L=8Ω			6		W
		THD+N=1%,f=1kHz,R_L=8Ω			8.5		
		THD+N=10%,f=1kHz,R_L=8Ω			10		
Quiescent Current	I_{DD}	(no load)			16.5	25	mA
Supply Quiescent Current in shutdown mode	I_{SD}	SHUTDOWN=0V			4	10	μA
Drain-source on-state resistance	$r_{ds(on)}$	I_O=0.5A T_J=25℃	High side		210		mΩ
			Low side		210		
			Total		420		
Power Supply Ripple Rejection Ratio	PSRR	$1V_{PP}$ ripple, f=1kHz, Inputs ac-coupled to ground			-65		dB
Oscillator Frequency	f_{OSC}				300		kHz
Output Integrated Noise Floor	Vn	20Hz to 22 kHz, A-weighting			-100		dB
Crosstalk	CS	P_O=3W, R_L=8Ω, f=1kHz			-95		dB
Signal to Noise Ratio	SNR	Maximum output at THD+N< 0.5%, f=1kHz			90		dB
Gain					32		dB
Output offset voltage (measured differentially)	$\|V_{OS}\|$	INN and INP connected together			30		mV
2.5V Bias voltage	V2P5	No Load			2.5		V
Internal Analog supply Voltage	AVDD	VCC=8V to 26V			5	5.5	V
Over Temperature Shutdown	OTS				160		°C
Thermal Hysteresis	OTH				50		°C

Electrical Characteristic

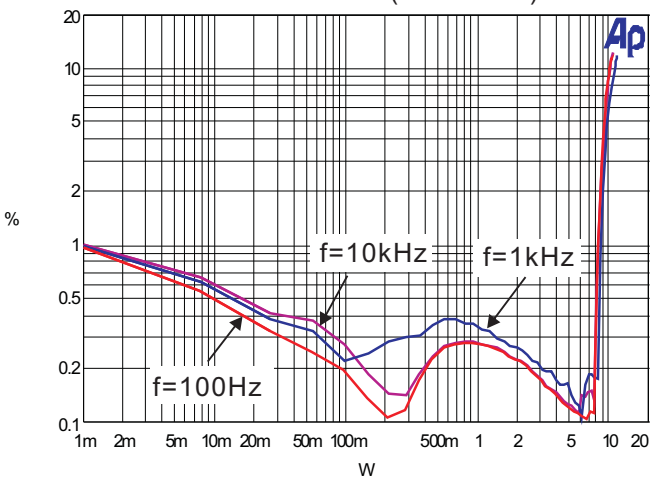
T_A=25°C, VCC=18V,R_L=8Ω (unless otherwise noted)

Parameter	Symbol	Condition		MIN	TYP	MAX	Units
Continuous Output Power	Po	THD+N=0.12%,f=1kHz,R_L=8Ω			2.2		W
		THD+N=0.18%,f=1kHz,R_L=8Ω			15		
Total Harmonic Distortion plus Noise	THD+N	P_O=10W,f=1kHz,R_L=8Ω,			0.28		%
Quiescent Current	I_{DD}	(no load)			18	25	mA
Supply Quiescent Current in shutdown mode	I_{SD}	SHUTDOWN=0V				50	μA
Drain-source on-state resistance	$r_{ds(on)}$	I_O=0.5A T_J=25℃	High side		210		mΩ
			Low side		210		
			Total		420		
Power Supply Ripple Rejection Ratio	PSRR	$1V_{PP}$ ripple, f=1kHz, Inputs ac-coupled to ground			-65		dB
Oscillator Frequency	f_{OSC}				300		kHz
Output Integrated Noise Floor	Vn	20Hz to 22 kHz, A-weighting			-100		dB
Crosstalk	CS	P_O=3W, R_L=8Ω, f=1kHz			-95		dB
Signal to Noise Ratio	SNR	Maximum output at THD+N< 0.5%, f=1kHz			90		dB
Gain					32		dB
Output offset voltage (measured differentially)	$\|V_{OS}\|$	INN and INP connected together			30		mV
2.5V Bias voltage	V2P5	No Load			2.5		V
Internal Analog supply Voltage	AVDD	VCC=8V to 26V			5	5.5	V
Over Temperature Shutdown	OTS				160		°C
Thermal Hysteresis	OTH				50		°C

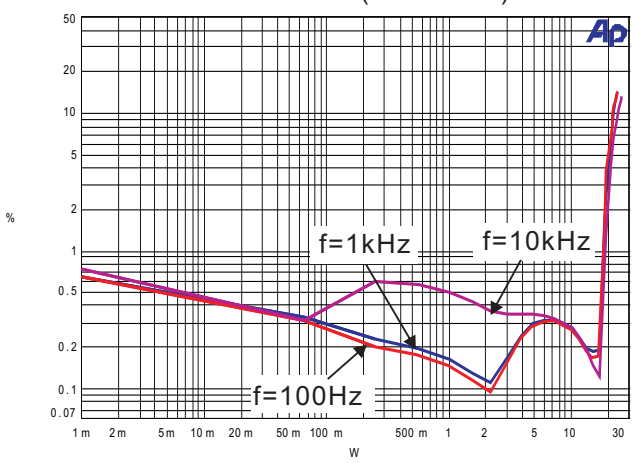
Typical Performance Characteristics

VCC=18V,R_L=8Ω, Gv=32dB,T_A=25°C, unless otherwise noted.

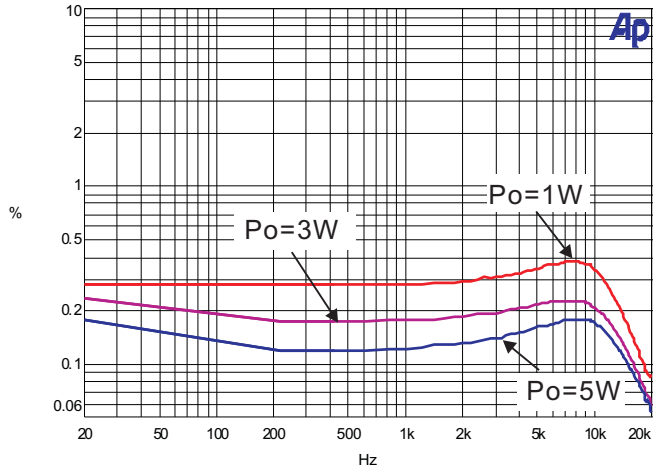
1. THD+N vs Power (VCC=12V)



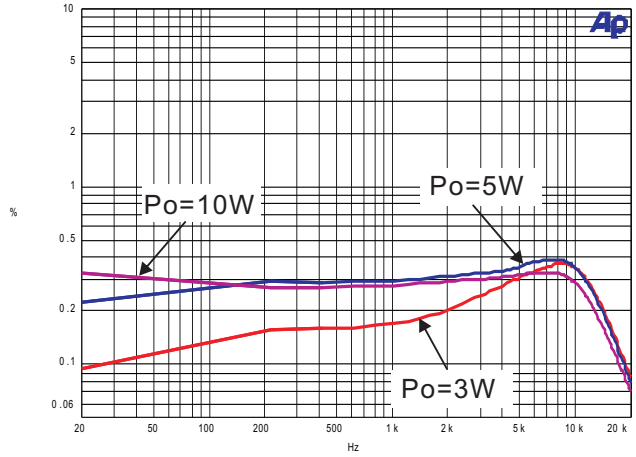
2. THD+N vs Power (VCC=18V)



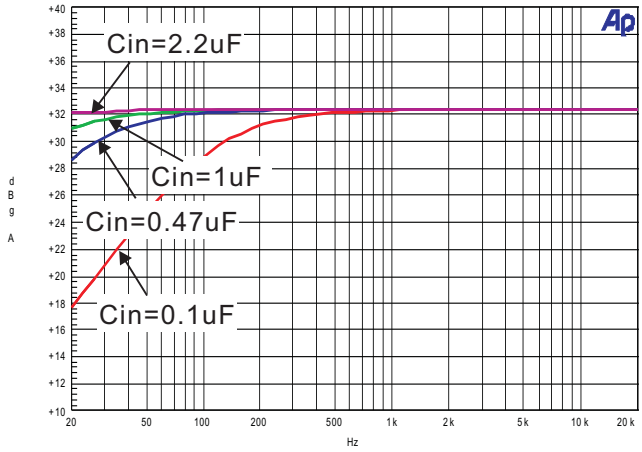
3. THD+N vs Frequency (VCC=12V)



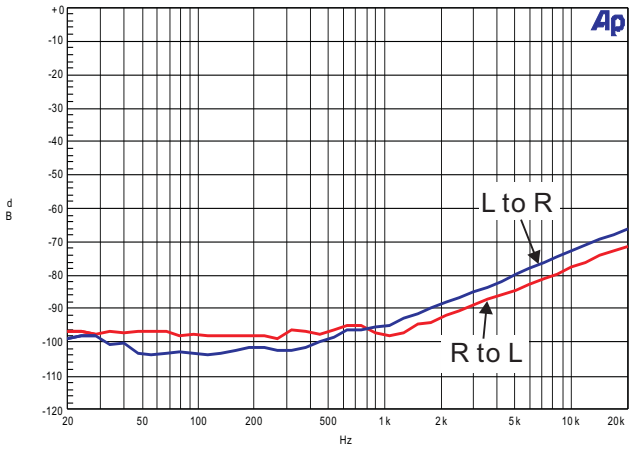
4. THD+N vs Frequency (VCC=18V)



5. Frequency Response



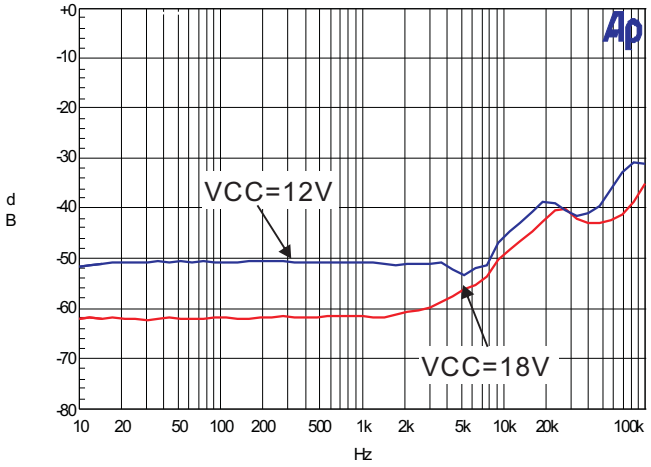
6. Crosstalk



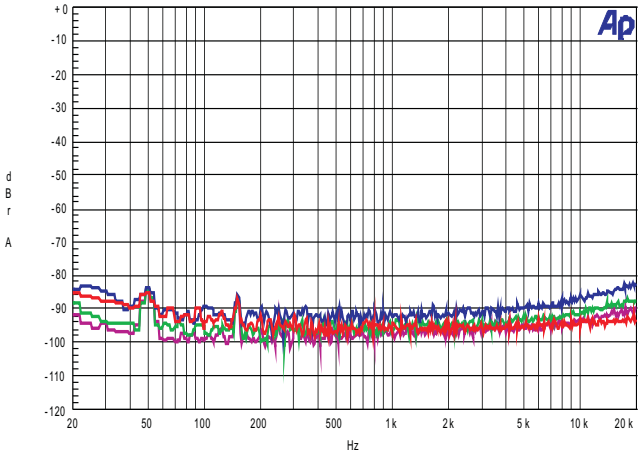
Typical Performance Characteristics

VCC=18V,R_L=8Ω, Gv=32dB,T_A=25°C, unless otherwise noted.

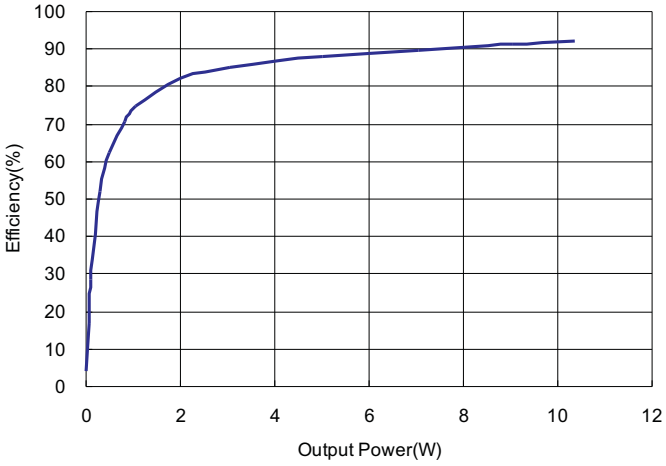
7. PSRR



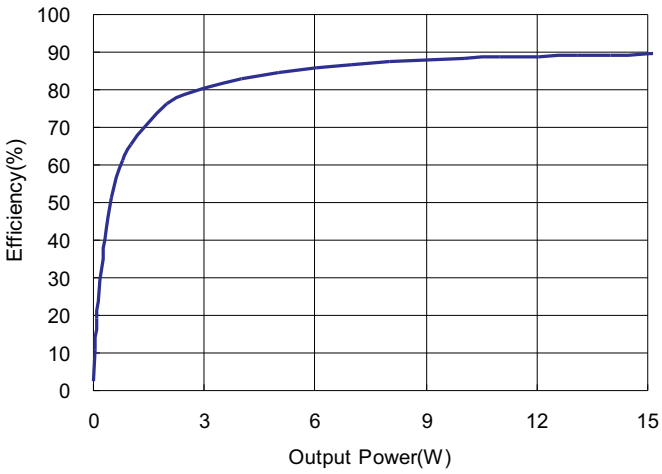
8. Noise Floor



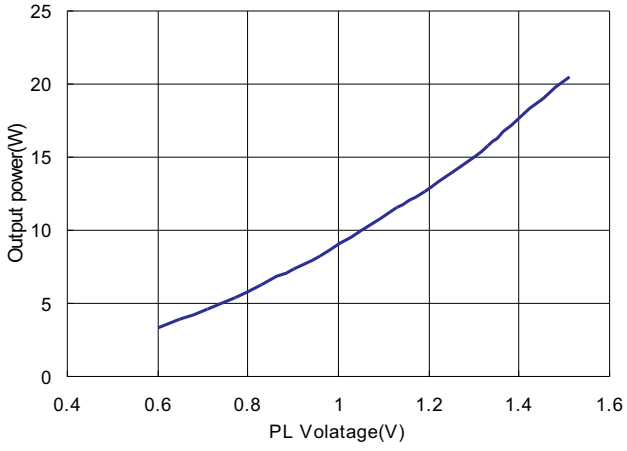
9. Efficiency vs Output Power (VCC=12V)



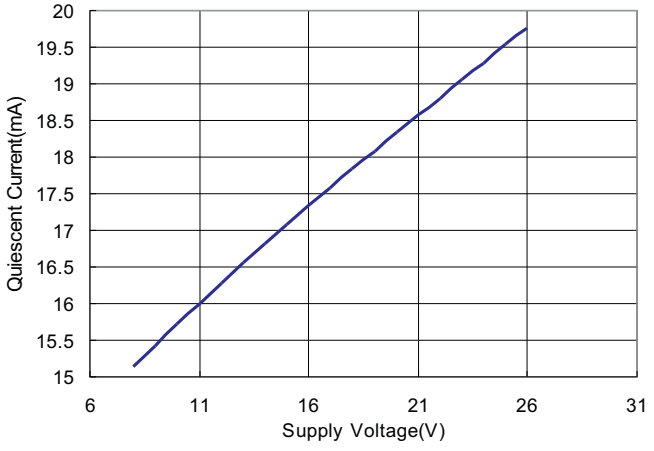
10. Efficiency vs Output Power (VCC=18V)



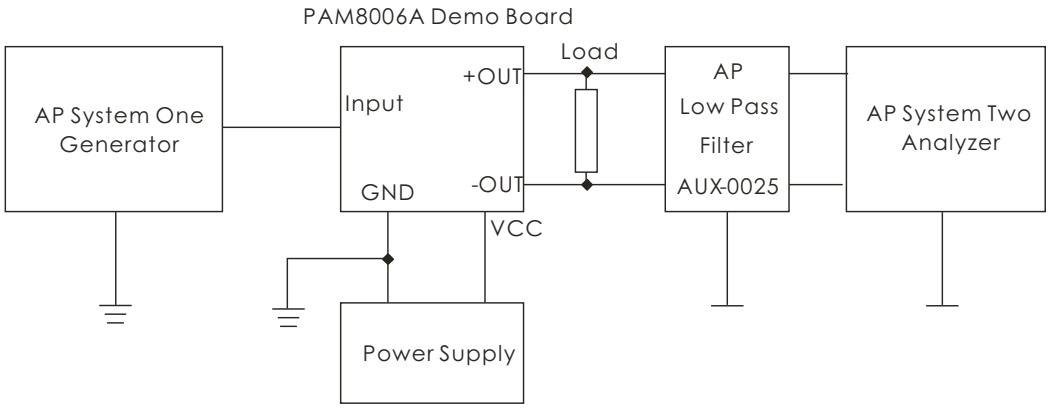
11. PL Voltage vs Output Power



12. Quiescent Current vs Supply Voltage



Test Setup for Performance Testing



Notes

1. The AP AUX-0025 low pass filter is necessary for class-D amplifier measurement with AP analyzer.
2. Two 22μH inductors are used in series with load resistor to emulate the small speaker for efficiency measurement.

Application Information

MUTE Operation

The MUTE pin is an input for controlling the output state of the PAM8006A. A logic high on this pin disables the outputs and low enables the outputs. This pin may be used as a quick disable or enable of the outputs without a volume fade.

Shutdown Operation

The PAM8006A employs a shutdown operation mode to reduce supply current to the absolute minimum level during periods of non-use to save power. The $\overline{SD}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{SD}$ low causes the outputs to mute and the amplifier to enter a low-current state. $\overline{SD}$ should never be left unconnected to prevent the amplifier from unpredictable operation.

For the best power-off pop performance, the amplifier should be set in shutdown mode prior to removing the power supply voltage.

Internal 2.5V Bias Generator Capacitor Selection

The internal 2.5V bias generator (V2P5) provides the internal bias for the preamplifier stage. The external input capacitors and this internal reference allow the inputs to be biased within the optimal common-mode range of the input preamplifiers.

The selection of the capacitor value on the V2P5 terminal is critical for achieving the best device performance. During startup or recovery from shutdown state, the V2P5 capacitor determines the rate at which the amplifier starts up. When the voltage on the V2P5 capacitor equals 0.75 x V2P5, or 75% of its final value, the device turns on and the class-D outputs start switching. The startup time is not critical for the best de-pop performance since any heard pop sound is the result of the class-D output switching-on other than that of the startup time. However, at least a 0.47µF capacitor is recommended for the V2P5 capacitor.
Another function of the V2P5 capacitor is to filter high frequency noise on the internal 2.5V bias generator.

Power Supply Decoupling, C_s

The PAM8006A is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible. Power supply decoupling also prevents oscillations caused by long lead between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1µF, is recommended, placing as close as possible to the device's VCC lead. To filter lower-frequency noises, a large aluminum electrolytic capacitor of 10µF or greater is recommended, placing near the audio power amplifier. The 10µF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs.

BSN and BSP Capacitors

The full H-bridge output stages use NMOS transistors only. They therefore require bootstrap capacitors for the high side of each output to turn on correctly. A at least 220nF ceramic capacitor, rated for at least 25V, must be connected from each output to its corresponding bootstrap input. Specifically, one 220nF capacitor must be connected from xOUTP to xBSP, and another 220nF capacitor from xOUTN to xBSN. It is recommended to use 1µF BST capacitor to replace 220nF or lower than 100Hz applications.

VCLAMP Capacitors

To ensure that the maximum gate-to-source voltage for the NMOS output transistors not exceeded, a internal regulators are used to clamp the gate voltage. A 1µF capacitors must be connected from VCLAMP to ground and must be rated for at least 25V. The voltages at the VCLAMP terminals vary with V_{CC} and may not be used to power any other circuitry.

Internal Regulated 5-V Supply (AVDD)

The AVDD terminal is the output of an internally-generated 5V supply, used for the oscillator, amplifier,power limit circuitry and logic control circuitry. It requires a 0.1µF to 1µF capacitor, placed very close to the pin to Ground to keep the regulator stable. The regulator may not be used to power any external circuitry.

Differential Input

The differential input stage of the amplifier eliminates noises that appear on the two input lines of the channel. To use the PAM8006A with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the PAM8006A with a single-ended source, ac-ground the INP input through a capacitor equal in value to the input capacitor on INN and apply the audio source to the INN input. In a single-ended input application, the INP input should be ac-grounded at the audio source other than at the device input for best noise performance.

Using low-ESR Capacitors

Low-ESR capacitors are recommended throughout this application section. A real (with respect to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves as an ideal capacitor.

Short-circuit Protection

The PAM8006A has short circuit protection circuitry on the outputs to prevent damage to the device when output-to-output shorts, output-to-GND shorts, or output-to-VCCshorts occur. Once a short-circuit is detected on the outputs, the output drive is immediately disabled. This is a latched fault and must be reset by cycling the voltage on the $\overline{SD}$ pin to a logic low and back to the logic high state for normal operation. This will clear the short-circuit flag and allow for normal operation if the short was removed. If the short was not removed, the protection circuitry will again activate.

Thermal Protection

Thermal protection on the PAM8006A prevents damage to the device when the internal die temperature exceeds 160°C. There is a ±15 degree tolerance on this trip point from device to device. Once the die temperature exceeds the set thermal point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 50°C. The device begins normal operation at this point without external system intervention.

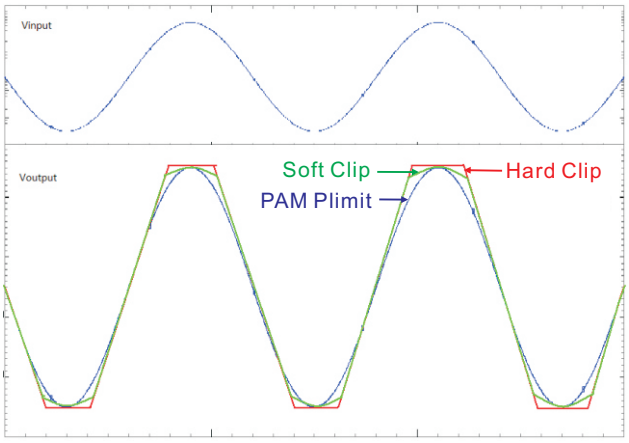
PLIMIT

The voltage at PL pin can used to limit the power to levels below that which is possible based on the supply rail. Add a resistor from PL to ground to set the voltage at the PLIMIT pin. An external reference may also be used if tighter tolerance is required. Also add a 1uF capacitor fromPL pin to ground. The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The gain of class D amplifier will automatic reduced if the output power higher than setting value to make output power less than limited value and also provide good sound quality.

The output power vs PL pin resistor value as below.

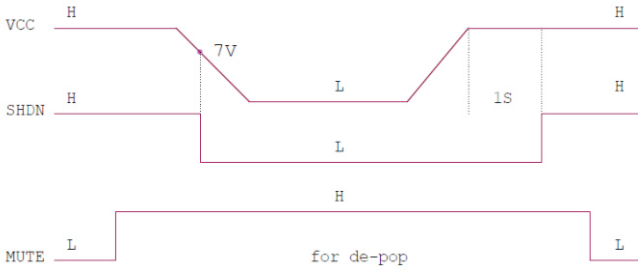
VCC=12V,Rload=8Ω

R(Ω)	PL (V)	PL(W)	R(Ω)	PL (V)	PL(W)
56K	0.61	3.1	100K	0.99	8.1
62K	0.67	3.7	110K	1.07	9.0
68K	0.73	4.3	120K	1.15	9.6
75K	0.79	5.1	130K	1.22	10.0
82K	0.85	6.0	140K	1.36	10.7
91K	0.92	7.0			



Power Up/Down Sequence

The PAM8006A employs a shutdown operation mode to reduce supply current to the absolute minimum level during periods of non-use to save power. The SD input terminal should be held high during normal operation when the amplifier is in use. Pulling SD low causes the outputs to mute and the amplifier to enter a low-current state. SD should never be left unconnected to prevent the amplifier from unpredictable operation. Suggest PL starting voltage is greater than 5V.



Start-up /power down sequencer recommended

Ordering Information

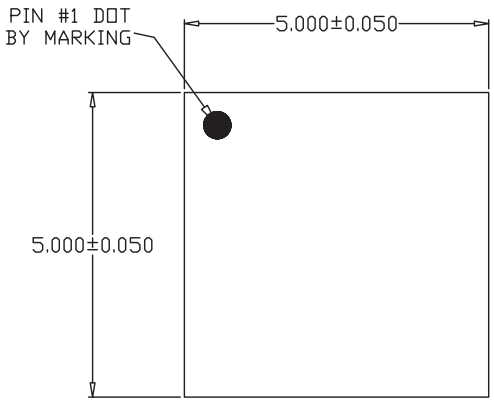
PAM8006A X X

Please consult PAM sales office or authorized distributors for more details.

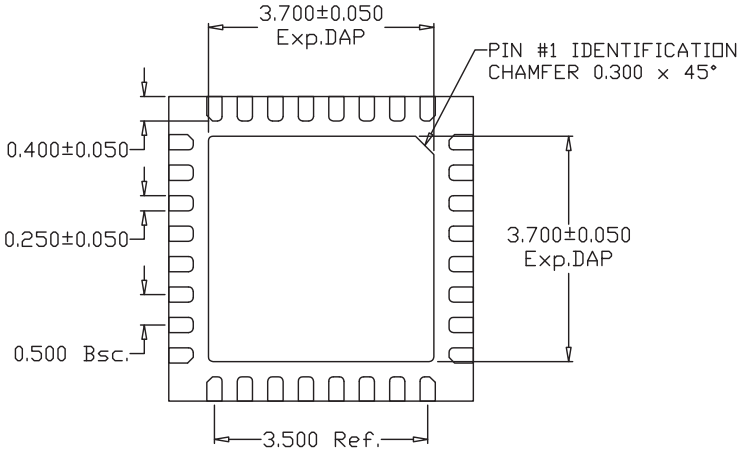
Part Number	Marking	Package Type	Standard Package
PAM8006ATR	PAM8006A XXXYWWLL	QFN 5x5-32L	3,000 units/Tape & Reel

Outline Dimension

QFN5x5-32L

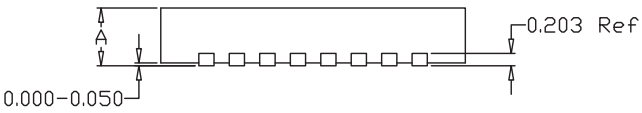


TOP VIEW



BOTTOM VIEW

A	MAX.	0.800
	NOM.	0.750
	MIN.	0.700



SIDE VIEW