

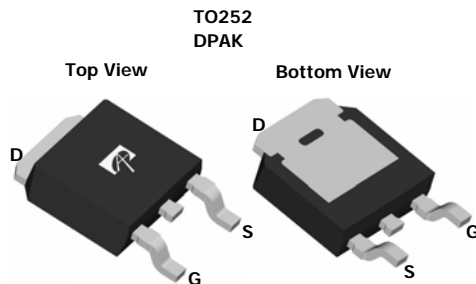
General Description

The AOD4184A combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is well suited for high current load applications.

Product Summary

V_{DS}	40V
I_D (at $V_{GS}=10V$)	50A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 7m Ω
$R_{DS(ON)}$ (at $V_{GS} = 4.5V$)	< 9.5m Ω

100% UIS Tested
100% Rg Tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	$T_C=25^\circ\text{C}$	50
		$T_C=100^\circ\text{C}$	40
Pulsed Drain Current ^C	I_{DM}	120	A
Continuous Drain Current	I_{DSM}	$T_A=25^\circ\text{C}$	13
		$T_A=70^\circ\text{C}$	10
Avalanche Current ^C	I_{AS}, I_{AR}	35	A
Avalanche energy $L=0.1\text{mH}$ ^C	E_{AS}, E_{AR}	61	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	50
		$T_C=100^\circ\text{C}$	25
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	2.3
		$T_A=70^\circ\text{C}$	1.5
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	18	22	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A D}		Steady-State	44	55
Maximum Junction-to-Case	$R_{\theta JC}$	2.4	3	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	40			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.7	2.1	2.6	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	120			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		5.8 9.6	7 12	mΩ
		V _{GS} =4.5V, I _D =15A		7.6	9.5	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =5A		37		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.7	1	V
I _S	Maximum Body-Diode Continuous Current				20	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =20V, f=1MHz	1200	1500	1800	pF
C _{oss}	Output Capacitance		150	215	280	pF
C _{rss}	Reverse Transfer Capacitance		80	135	190	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	2	3.5	5	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =20V, I _D =20A	21	27	33	nC
Q _g (4.5V)	Total Gate Charge		10	14	17	nC
Q _{gs}	Gate Source Charge		3	5	6	nC
Q _{gd}	Gate Drain Charge		3	6	9	nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =20V, R _L =1Ω, R _{GEN} =3Ω		6		ns
t _r	Turn-On Rise Time			17		ns
t _{D(off)}	Turn-Off DelayTime			30		ns
t _f	Turn-Off Fall Time			17		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=100A/μs	20	29	38	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=100A/μs	18	26	34	nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

THIS PRODUCT HAS BEEN DESIGNED AND QUALIFIED FOR THE CONSUMER MARKET. APPLICATIONS OR USES AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS ARE NOT AUTHORIZED. AOS DOES NOT ASSUME ANY LIABILITY ARISING OUT OF SUCH APPLICATIONS OR USES OF ITS PRODUCTS. AOS RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN, FUNCTIONS AND RELIABILITY WITHOUT NOTICE.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

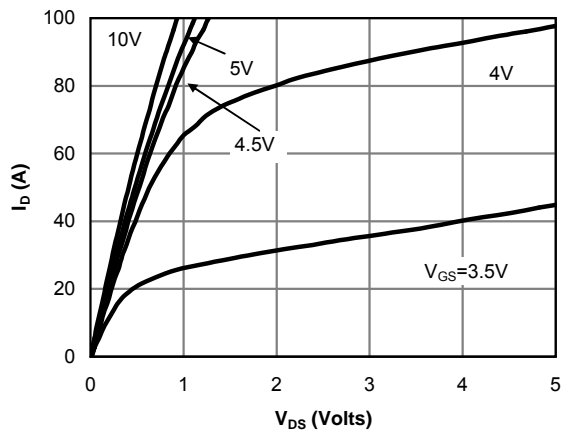


Fig 1: On-Region Characteristics (Note E)

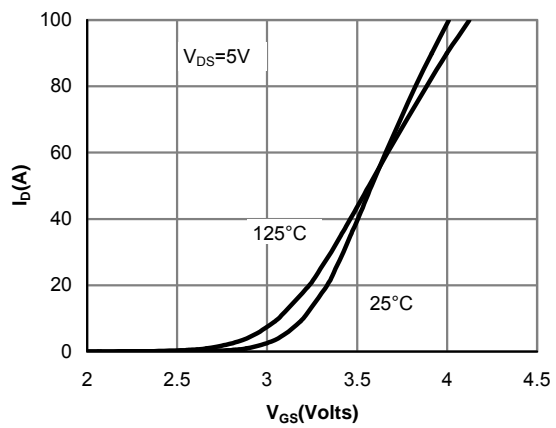


Figure 2: Transfer Characteristics (Note E)

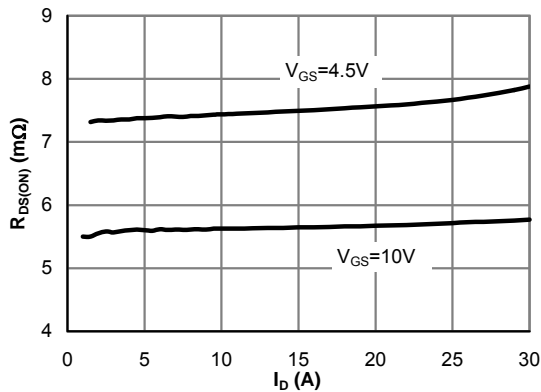


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

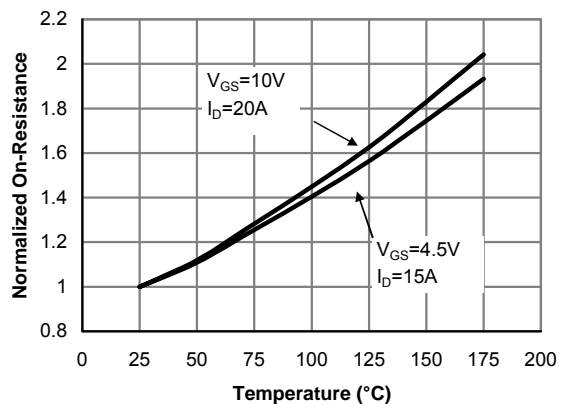


Figure 4: On-Resistance vs. Junction Temperature (Note E)

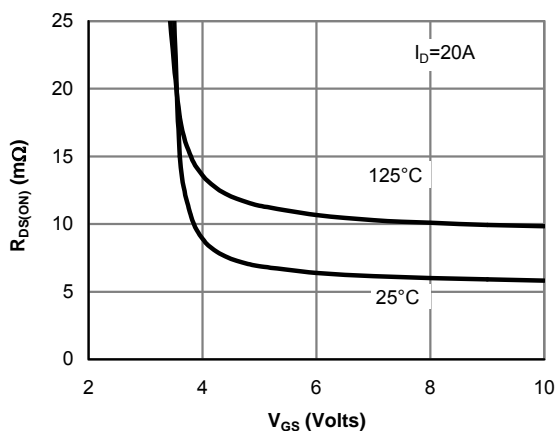


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

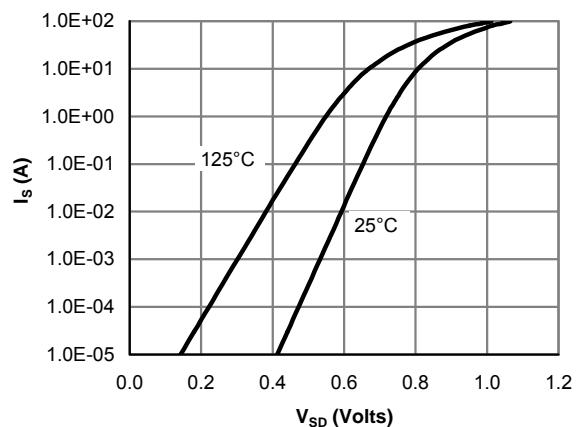


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

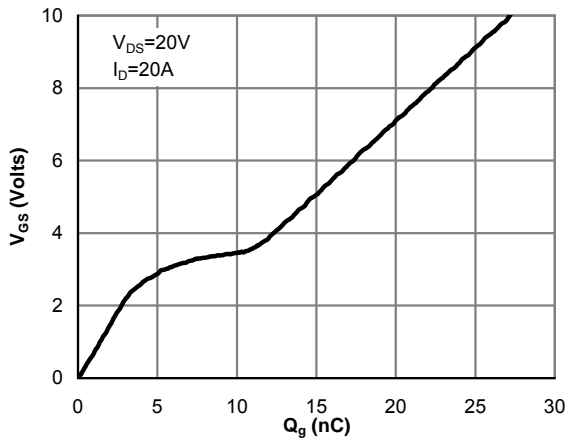


Figure 7: Gate-Charge Characteristics

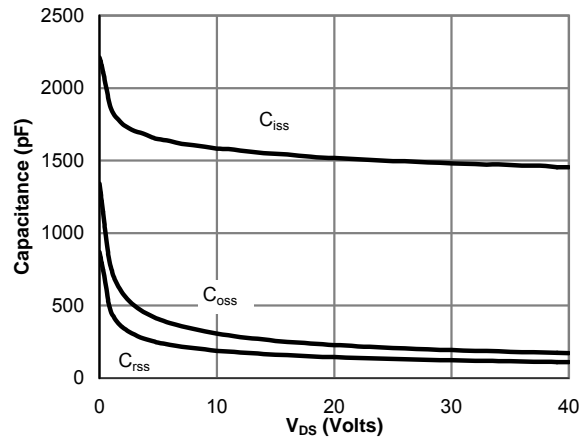


Figure 8: Capacitance Characteristics

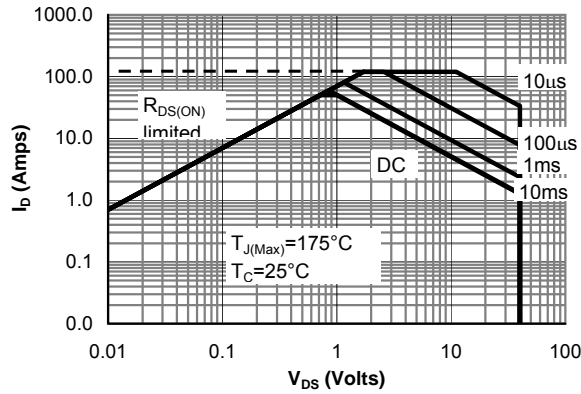


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

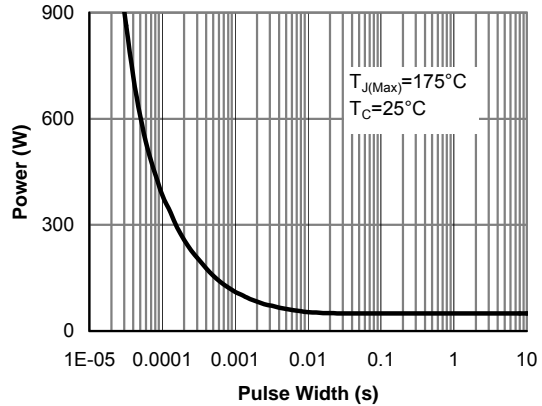


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

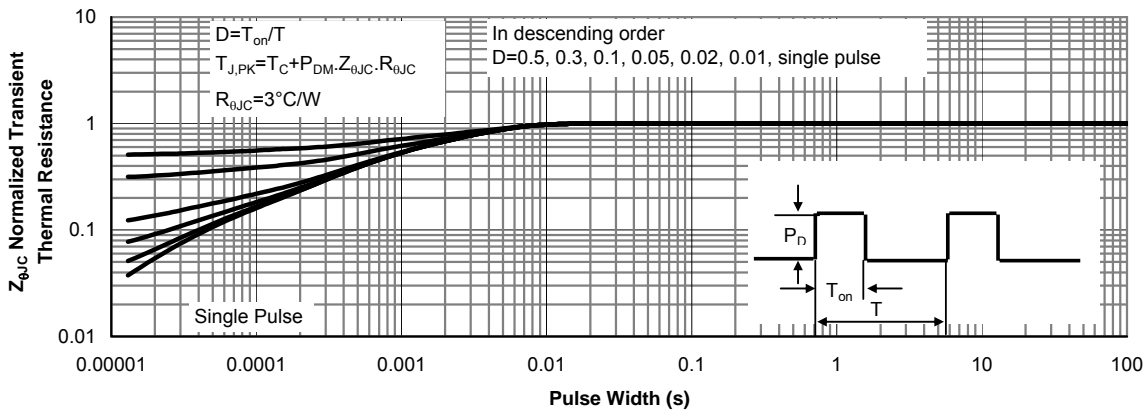


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

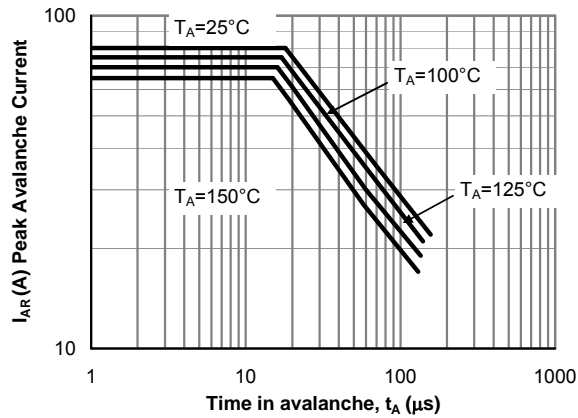


Figure 12: Single Pulse Avalanche capability (Note C)

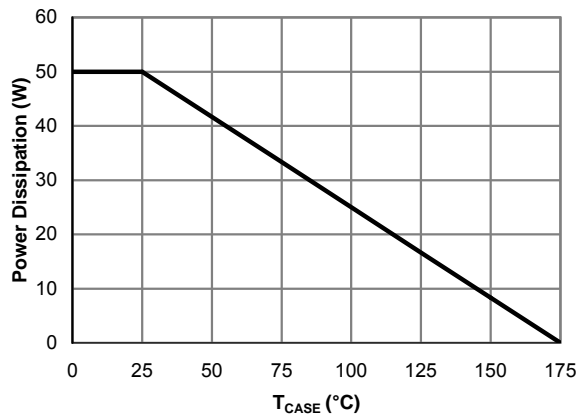


Figure 13: Power De-rating (Note F)

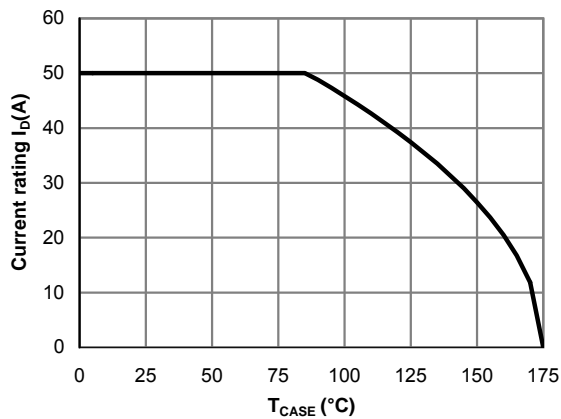


Figure 14: Current De-rating (Note F)

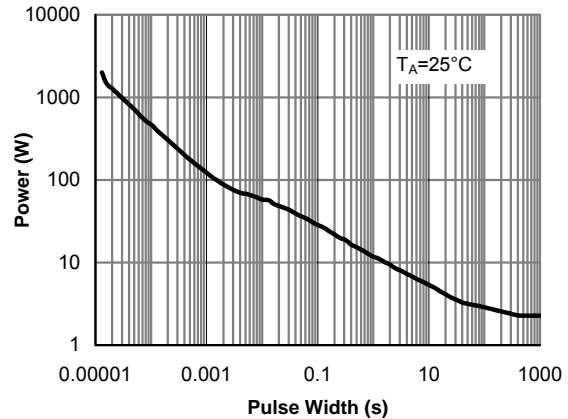


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

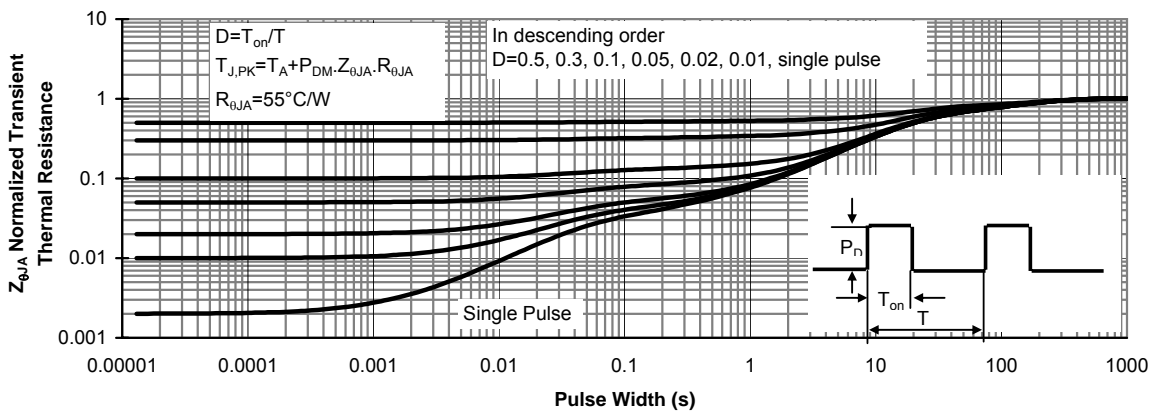
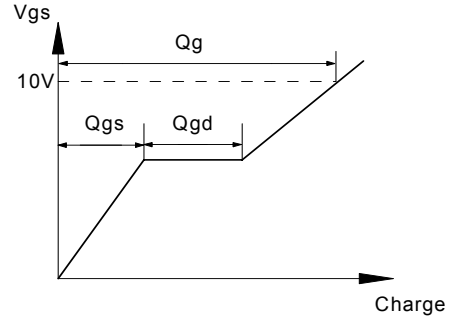
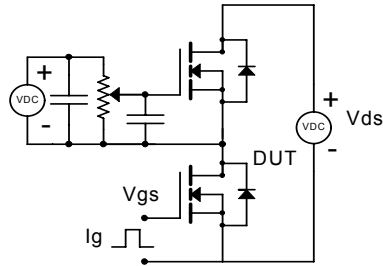
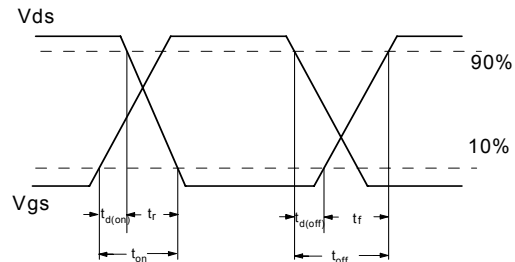
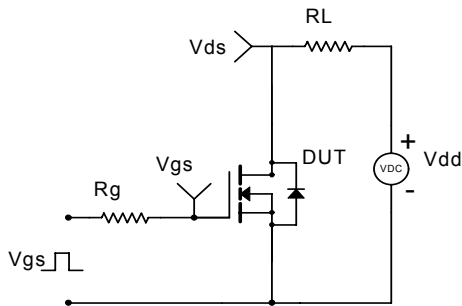


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

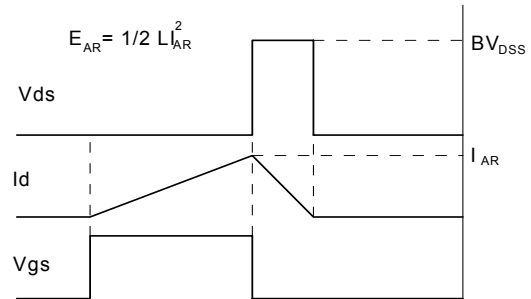
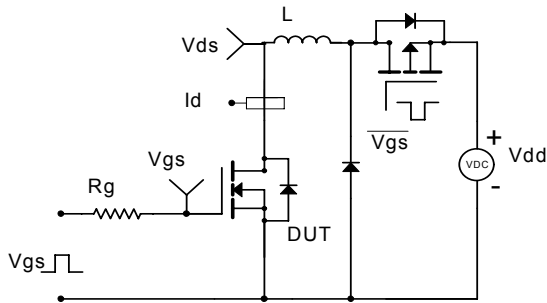
Gate Charge Test Circuit & Waveform



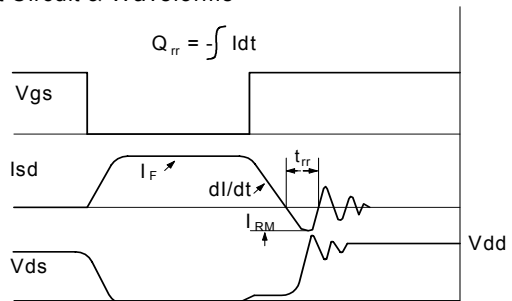
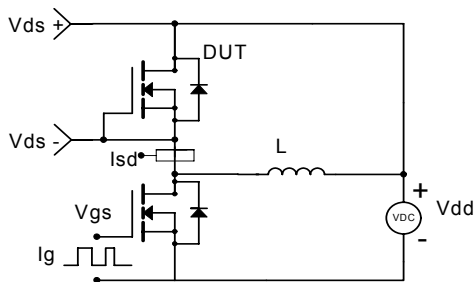
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



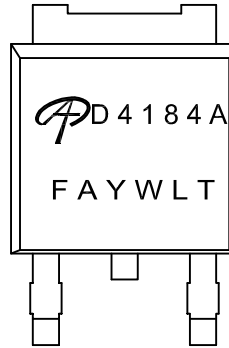
Diode Recovery Test Circuit & Waveforms





Document No.	PD-01139
Version	A
Title	AOD4184A Marking Description

DPAK (TO-252) PACKAGE MARKING DESCRIPTION



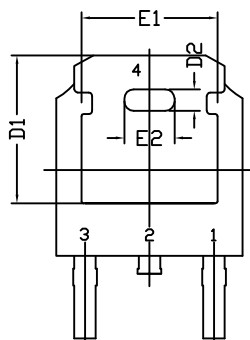
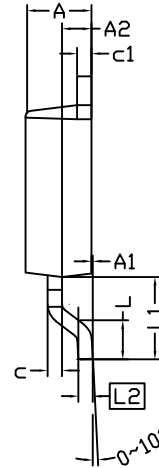
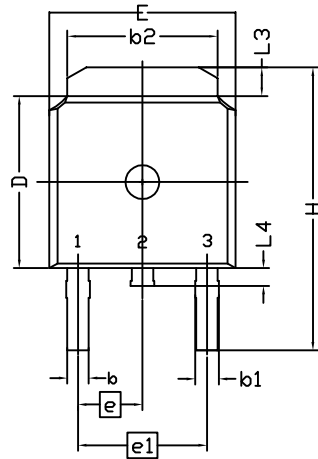
Green product

NOTE:	
LOGO	- AOS Logo
D4184A	- Part number code
F	- Fab code
A	- Assembly location code
Y	- Year code
W	- Week code
L&T	- Assembly lot code

PART NO.	DESCRIPTION	CODE
AOD4184A	Green product	D4184A
AOD4184AL	Green product	D4184A

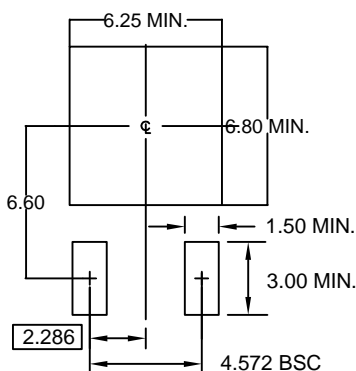


TO252(DPAK) PACKAGE OUTLINE



SYMBOL	DIMENSION IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	2.184	2.286	2.388	0.086	0.090	0.094
A1	0.000	-----	0.127	0.000	-----	0.005
A2	0.889	1.041	1.143	0.035	0.041	0.045
b	0.635	0.762	0.889	0.025	0.030	0.035
b1	0.762	0.840	1.143	0.030	0.033	0.045
b2	4.953	5.340	5.461	0.195	0.210	0.215
c	0.450	0.508	0.610	0.018	0.020	0.024
c1	0.450	0.508	0.610	0.018	0.020	0.024
D	5.969	6.096	6.223	0.235	0.240	0.245
D1	5.210	5.249	5.380	0.205	0.207	0.212
D2	0.662	0.762	0.862	0.026	0.030	0.034
E	6.350	6.604	6.731	0.250	0.260	0.265
E1	4.318	4.826	4.901	0.170	0.190	0.193
E2	1.678	1.778	1.878	0.066	0.070	0.074
e	2.286 BSC			0.090 BSC		
e1	4.572 BSC			0.180 BSC		
H	9.398	10.033	10.414	0.370	0.395	0.410
L	1.270	1.520	2.032	0.050	0.060	0.080
L1	2.921 REF.			0.115REF.		
L2	0.408	0.508	0.608	0.016	0.020	0.024
L3	0.889	1.016	1.270	0.035	0.040	0.050
L4	0.635	-----	1.016	0.025	-----	0.040

RECOMMENDED LAND PATTERN



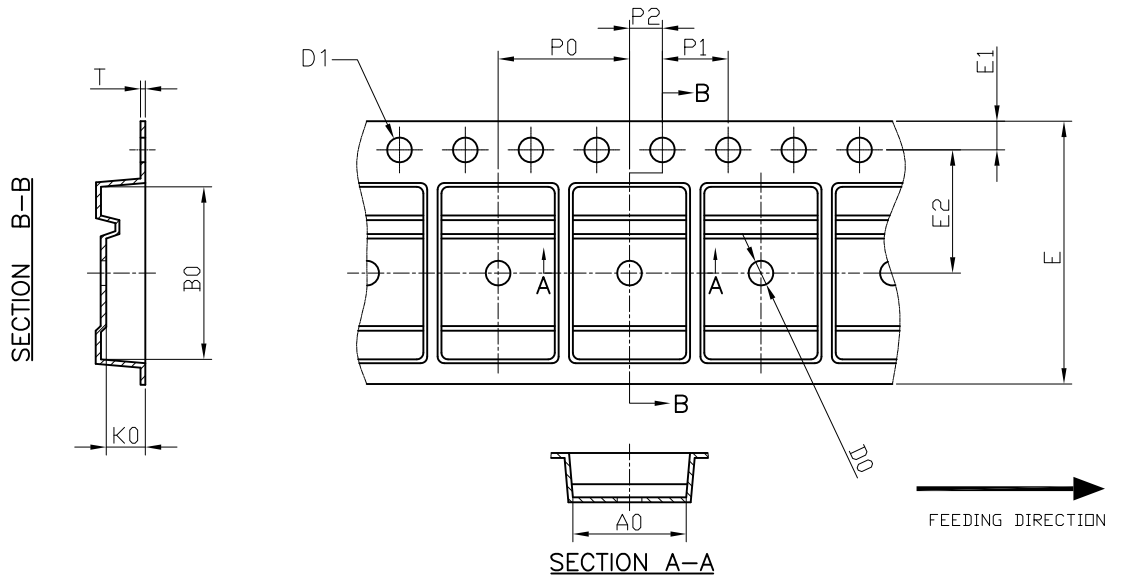
UNIT: mm

NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS. MOLD FLASH SHOULD BE LESS THAN 6 MILS.
2. DIMENSION L IS MEASURED IN GAUGE PLANE
3. TOLERANCE 0.10 mm UNLESS OTHERWISE SPECIFIED
4. CONTROLLING DIMENSION IS MILLIMETER. CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
5. REFER TO JEDEC TO-252 (AA)



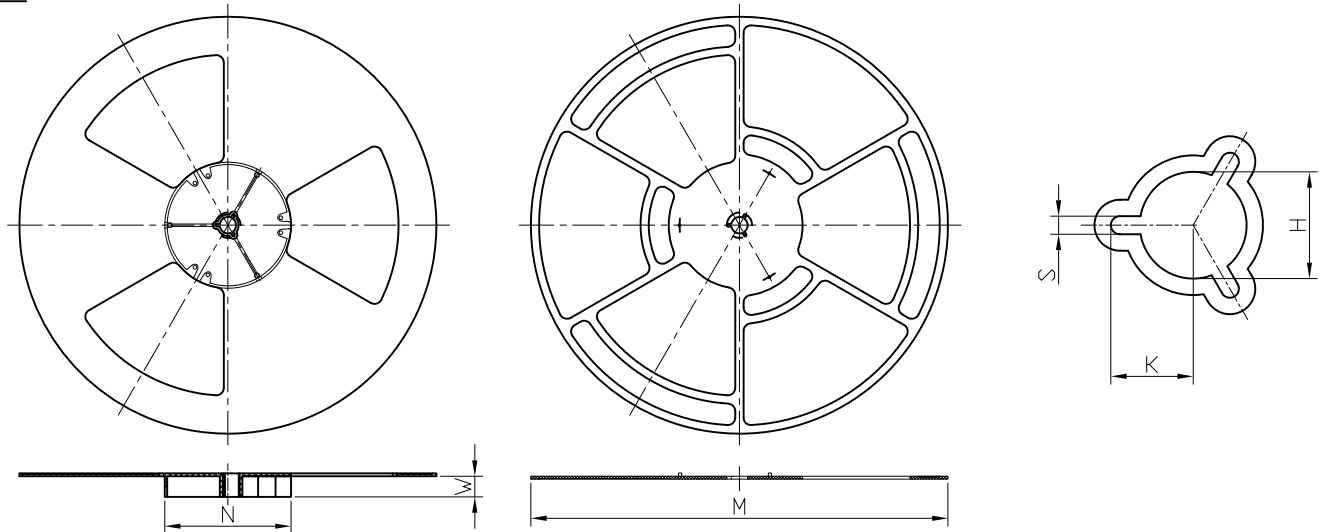
DPAK Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DPAK (16 mm)	6.90 ±0.10	10.50 ±0.10	2.50 ±0.10	1.50 +0.1 -0	1.50 +0.1 -0	16.00 ±0.30	1.75 ±0.10	7.50 ±0.10	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.30 ±0.05

DPAK Reel



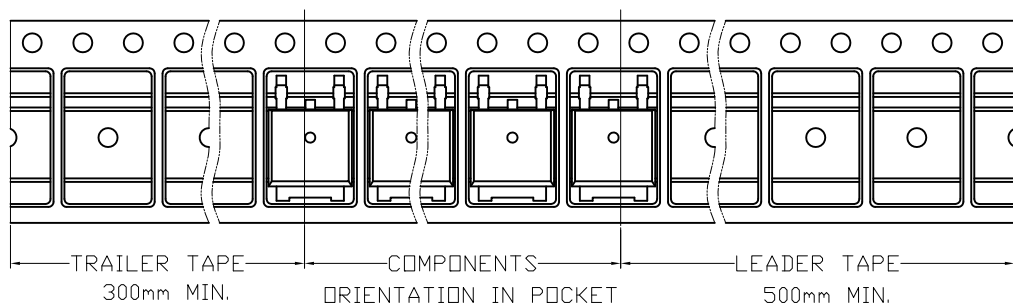
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	H	K	S
16 mm	ø330	ø330.00 +0.25 -4.00	ø100.00 ±0.2	16.4 +2.0 -0.0	ø13.00 +0.50 -0.20	10.5 ±0.25	2.2 ±0.25

DPAK Tape

Leader / Trailer
& Orientation

Unit Per Reel:
2500pcs





AOS Semiconductor Product Reliability Report

AOD4184A, rev B

Plastic Encapsulated Device

ALPHA & OMEGA Semiconductor, Inc

495 Mercury Drive
Sunnyvale, CA 94085
U.S.

Tel: (408) 830-9742

www.aosmd.com



This AOS product reliability report summarizes the qualification result for AOD4184A. Accelerated environmental tests are performed on a specific sample size, and then followed by electrical test at end point. Review of final electrical test result confirms that AOD4184A passes AOS quality and reliability requirements. The released product will be categorized by the process family and be monitored on a quarterly basis for continuously improving the product quality.

Table of Contents:

- I. Product Description
- II. Package and Die information
- III. Environmental Stress Test Summary and Result
- IV. Reliability Evaluation

I. Product Description:

The AOD4184A combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is well suited for high current load applications.

- RoHS Compliant
- Halogen Free

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted			
Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	$T_C=25^\circ\text{C}$	50
		$T_C=100^\circ\text{C}$	39
Pulsed Drain Current ^C	I_{DM}	120	A
Continuous Drain Current	I_{DSM}	$T_A=25^\circ\text{C}$	13
		$T_A=70^\circ\text{C}$	10
Avalanche Current ^C	I_{AS}, I_{AR}	35	A
Avalanche energy $L=0.1\text{mH}$ ^C	E_{AS}, E_{AR}	61	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	50
		$T_C=100^\circ\text{C}$	25
Power Dissipation ^A	P_{DSM}	$T_A=25^\circ\text{C}$	2.3
		$T_A=70^\circ\text{C}$	1.5
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics				
Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	18	22	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A D}				
Maximum Junction-to-Case	$R_{\theta JC}$	2.4	3	$^\circ\text{C/W}$



II. Die / Package Information:

Process	AOD4184A Standard sub-micron Low voltage N channel process
Package Type	3 leads TO252
Lead Frame	Bare Cu
Die Attach	Soft solder
Bond wire	G:1.3 mils Au; S: 20mils Al
Mold Material	Epoxy resin with silica filler
Flammability Rating	UL-94 V-0
Backside Metallization	Ti / Ni / Ag
Moisture Level	Up to Level 1 *
Note * based on info provided by assembler and mold compound supplier	

III. Result of Reliability Stress for AOD4184A

Test Item	Test Condition	Time Point	Lot Attribution	Total Sample size	Number of Failures
Solder Reflow Precondition	168hr 85°c /85%RH +3 cycle reflow @260c	-	9 lots	1210pcs	0
HTGB	Temp = 150°c , Vgs=100% of Vgsmax	168hrs 500 hrs 1000 hrs	1 lot (Note A*)	77pcs 77 pcs / lot	0
HTRB	Temp = 150°c , Vds=80% of Vdsmax	168hrs 500 hrs 1000 hrs	1 lot (Note A*)	77pcs 77 pcs / lot	0
HAST	130 +/- 2°c , 85%RH, 33.3 psi, Vgs = 80% of Vgs max	100 hrs	9 lots (Note B**)	495pcs 55 pcs / lot	0
Pressure Pot	121°c , 29.7psi, RH=100%	96 hrs	5 lots (Note B**)	275pcs 55 pcs / lot	0
Temperature Cycle	-65°c to 150°c , air to air,	250 / 500 cycles	8 lots (Note B**)	440pcs 55 pcs / lot	0

III. Result of Reliability Stress for AOD4184A

Continues

DPA	Internal Vision Cross-section X-ray	NA	5 5 5	5 5 5	0
CSAM		NA	5	5	0
Bond Integrity	Room Temp 150°c bake 150°c bake	0hr 250hr 500hr	40 40 40	40 wires 40 wires 40 wires	0
Solderability	245°c	5 sec	15	15 leads	0
Solder dunk	260°c	10secs 3 cycles	1	30 units	0

Note A: The HTGB and HTRB reliability data presents total of available AOD4184A burn-in data up to the published date.

Note B: The pressure pot, temperature cycle and HAST reliability data for AOD4184A comes from the AOS generic package qualification data.

IV. Reliability Evaluation

FIT rate (per billion): 46

MTTF = 2478 years

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size of the selected product (AOD4184A). Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

$$\text{Failure Rate} = \text{Chi}^2 \times 10^9 / [2 (N) (H) (Af)] = 1.83 \times 10^9 / [2 \times 2 \times 77 \times 500 \times 258] = 46$$

$$\text{MTTF} = 10^9 / \text{FIT} = 2.17 \times 10^7 \text{hrs} = 2478 \text{ years}$$

Chi² = Chi Squared Distribution, determined by the number of failures and confidence interval

N = Total Number of units from HTRB and HTGB tests

H = Duration of HTRB/HTGB testing

Af = Acceleration Factor from Test to Use Conditions (Ea = 0.7eV and Tuse = 55°C)

Acceleration Factor [Af] = $\text{Exp} [Ea / k (1/Tj u - 1/Tj s)]$

Acceleration Factor ratio list:

	55 deg C	70 deg C	85 deg C	100 deg C	115 deg C	130 deg C	150 deg C
Af	258	87	32	13	5.64	2.59	1

Tj s = Stressed junction temperature in degree (Kelvin), K = C+273.16

Tj u = The use junction temperature in degree (Kelvin), K = C+273.16

k = Boltzmann's constant, $8.617164 \times 10^{-5} \text{eV} / \text{K}$