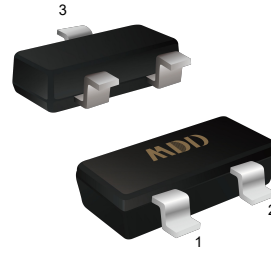


SOT-23



1. Gate
2. Source
3. Drain

$V_{(BR)DSS}$	$R_{DS(on)Typ}$	$I_D Max$
20V	19.4mΩ@4.5V	6.2A
	21.5mΩ@2.5V	

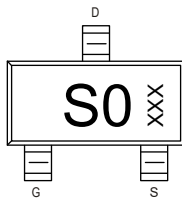
Features

- Advanced trench process technology
- High Density Cell Design For Ultra Low On-Resistance

Application

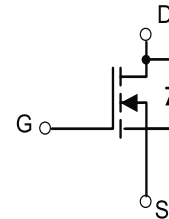
- Load Switch
- DC/DC Converter
- Switching Circuits
- Power Management

Marking



XXX:Date Code

Equivalent Circuit



Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	±12	V
Continuous Drain Current	I_D	6.2	A
Pulsed Drain Current (Note 1)	I_{DM}	24.8	A
Power Dissipation(Note 2)	P_D	1.56	W
Thermal Resistance from Junction to Ambient(Note 2)	$R_{\theta JA}$	80	$^\circ\text{C/W}$
Junction Temperature and Storage Temperature	T_J, T_{stg}	-50 ~150	$^\circ\text{C}$

Notes: Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Ta = 25°C unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20	--	--	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=20V, V_{GS}=0V$	--	--	1	μA
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 10V, V_{DS}=0V$	--	--	± 100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.45	0.6	1.0	V
$R_{DS(ON)}$	Drain-Source On-State Resistance(Note 3)	$V_{GS}=4.5V, I_D=4.5A$	--	19.4	25	m Ω
		$V_{GS}=2.5V, I_D=2A$	--	21.5	28	m Ω

Dynamic Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_{iss}	Input Capacitance	$V_{DS}=10V$ $V_{GS}=0V$ $f=1MHz$	--	457	--	pF
C_{oss}	Output Capacitance		--	71	--	pF
C_{rss}	Reverse Transfer Capacitance		--	66	--	pF
Q_g	Total Gate Charge	$V_{DS}=10V$ $V_{GS}=4.5V$ $I_D=4A$	--	6.6	--	nC
Q_{gs}	Gate Source Charge		--	0.4	--	nC
Q_{gd}	Gate Drain Charge		--	2	--	nC

Switching Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{d(on)}$	Turn on Delay Time	$V_{DS}=10V$ $V_{GS}=4.5V$ $I_D=1A$ $R_G=3.3\Omega$	--	4.1	--	ns
t_r	Turn on Rise Time		--	11.6	--	ns
$t_{d(off)}$	Turn Off Delay Time		--	24	--	ns
t_f	Turn Off Fall Time		--	7.6	--	ns

Source Drain Diode Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{SD}	Source drain current(Body Diode)	$T_A=25^\circ C$	--	--	0.2	A
V_{SD}	Drain-Source Diode Forward Voltage	$I_S=4A, V_{GS}=0V$	--	0.79	1.2	V

- Notes:**
- 1.Pulse width limited by maximum allowable junction temperature
 - 2.The value of P_D & $R_{\theta JA}$ is measured with the device mounted on 1 in² FR-4 board with 2oz.Copper, double sided, in a still air environment with $T_a=25^\circ C$.
 - 3.Pulse test ; Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

Typical Characteristics

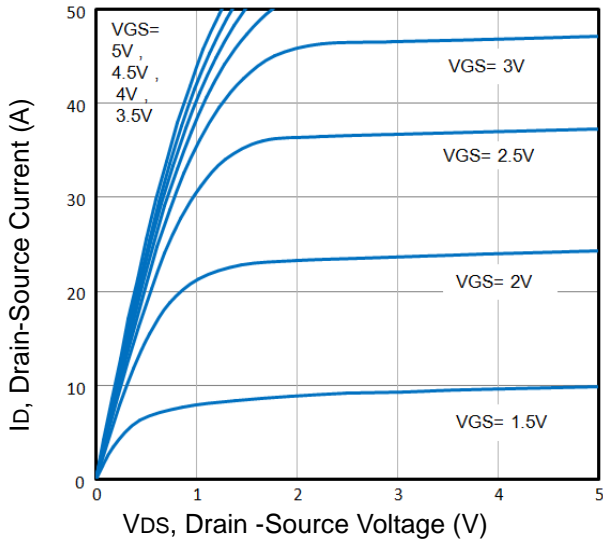


Fig1. Typical Output Characteristics

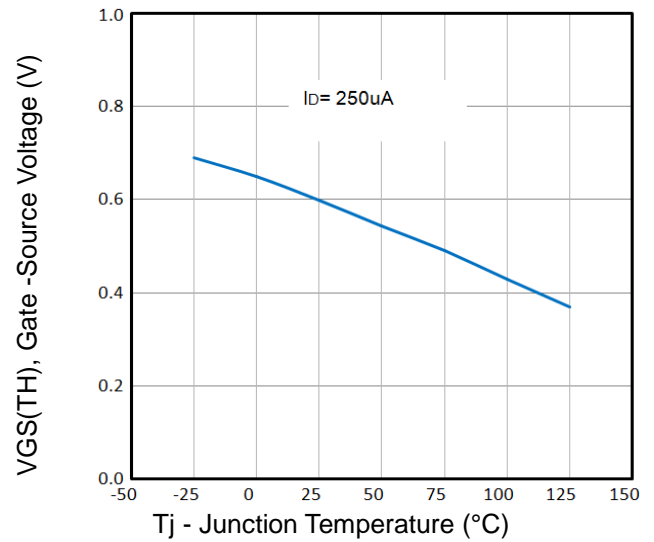


Fig2. VGS(TH) Voltage Vs. Temperature

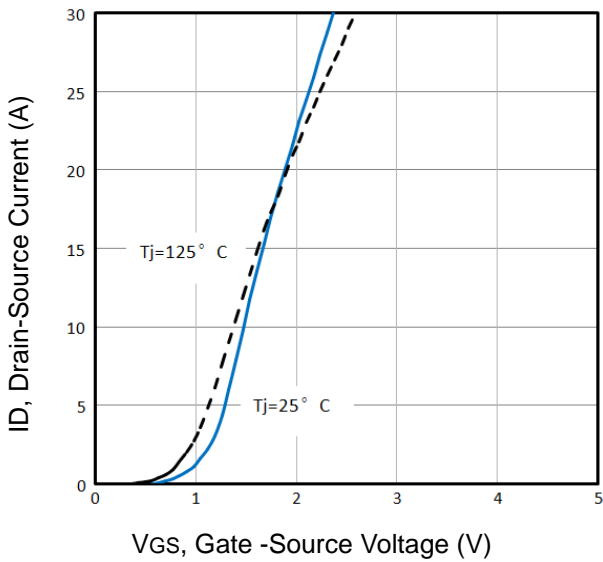


Fig3. Typical Transfer Characteristics

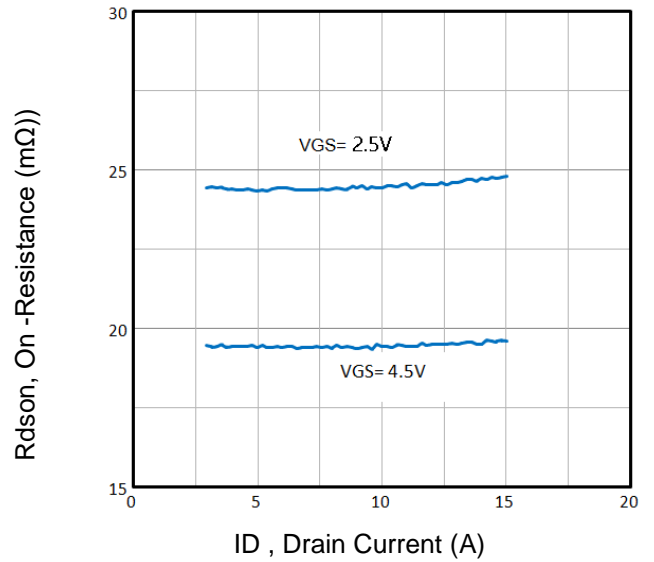


Fig4. On-Resistance vs. Drain Current and Gate

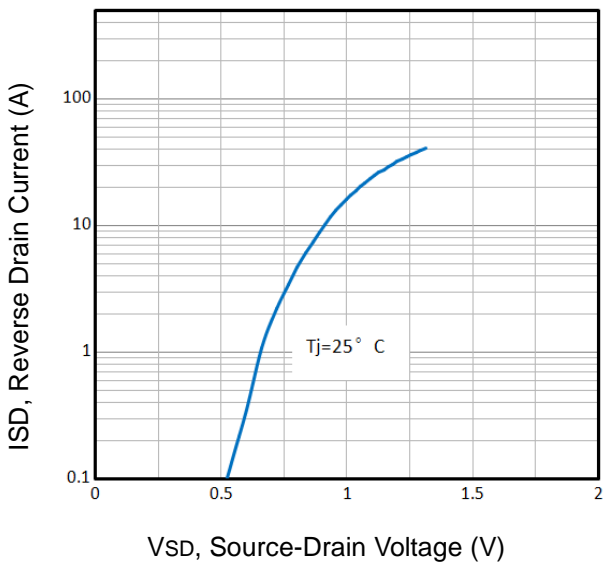


Fig5. Typical Source-Drain Diode Forward Voltage

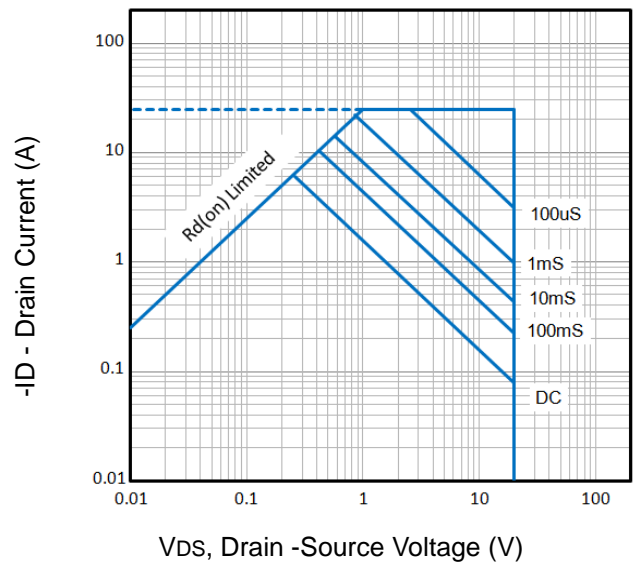


Fig6. Maximum Safe Operating Area

The curve above is for reference only.

Typical Characteristics

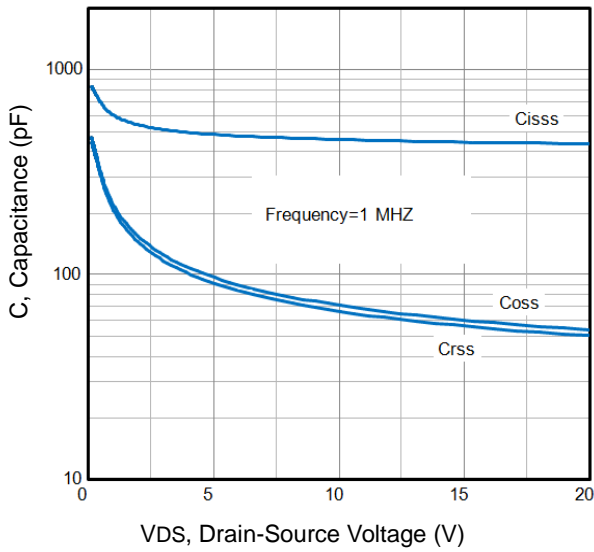


Fig7. Typical Capacitance Vs. Drain-Source Voltage

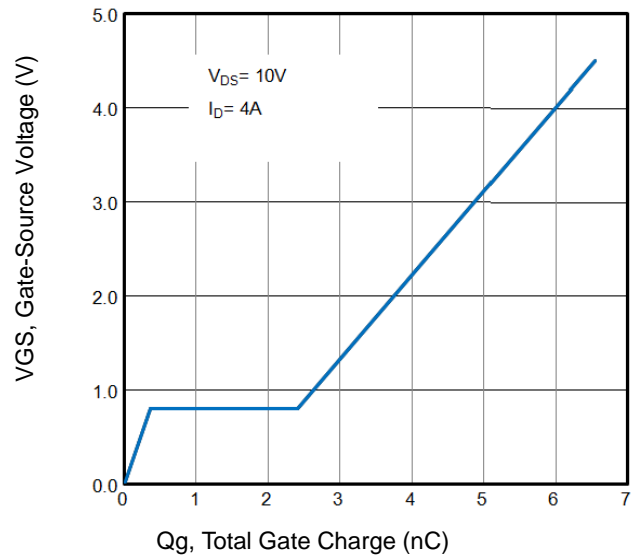


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

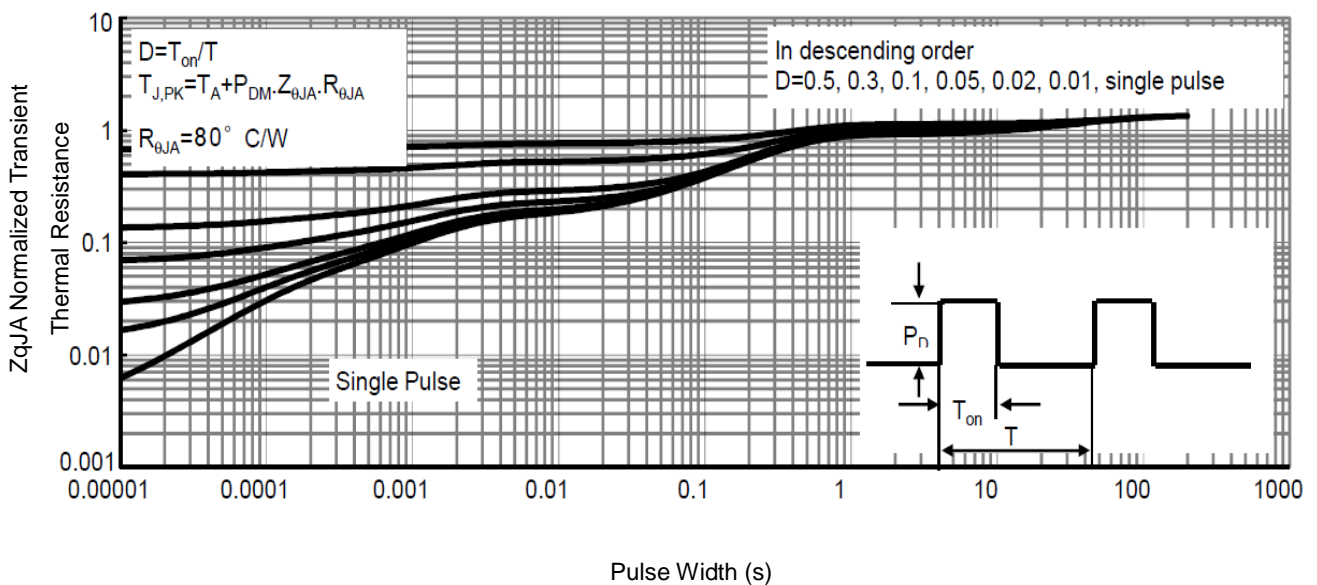


Fig9. Normalized Maximum Transient Thermal Impedance

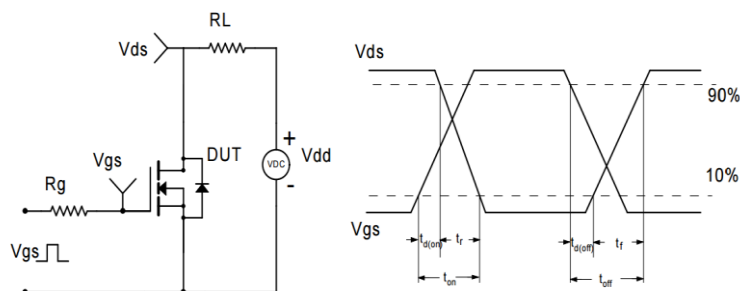
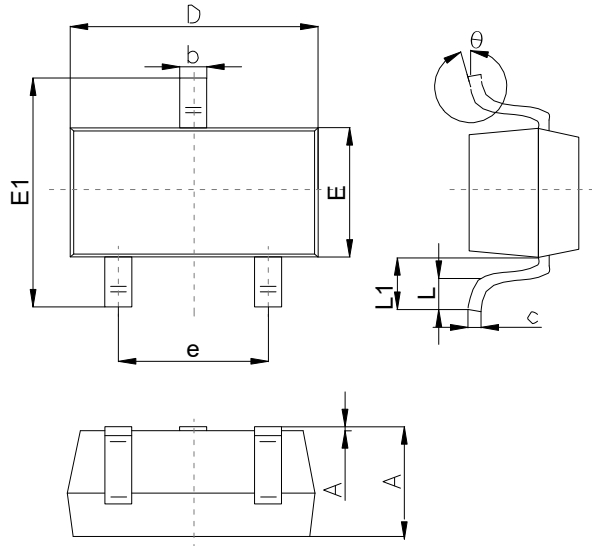


Fig10. Switching Time Test Circuit and waveforms

The curve above is for reference only.

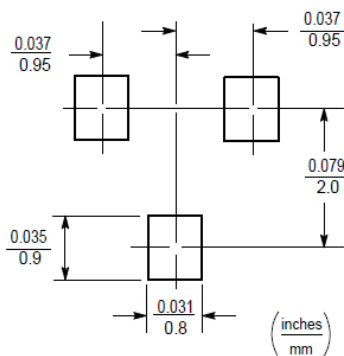
Outline Drawing

SOT-23 Package Outline Dimensions



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	0.90		1.40
A1	0.00		0.10
b	0.30		0.50
c	0.08		0.20
D	2.80	2.90	3.10
E	1.20		1.60
E1	2.25		2.80
e	1.80	1.90	2.00
L	0.10		0.50
L1	0.4		0.55
θ	0°		10°

Suggested Pad Layout



Note:

1. Controlling dimension: in/millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.