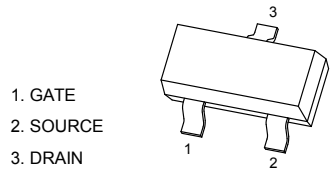
SI2301S

SOT-23 Plastic-Encapsulate MOSFETS

20V P-Channel MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$Typ	I_D Max
-20V	125mΩ@4.5V	-2.3A
	140mΩ@3.3V	

SOT-23



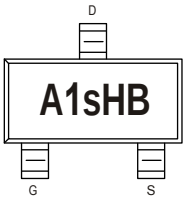
Features

Trench FET Power MOSFET

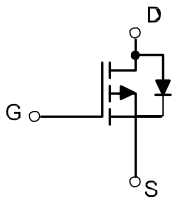
APPLICATION

- High-side Load Switch
- Switching Circuits
- High Speed line Driver

MARKING



Equivalent circuit



PACKAGE SPECIFICATIONS

Package	Reel Size	Reel DIA. (mm)	Q'TY/Reel (pcs)	Box Size (mm)	QTY/Box (pcs)	Carton Size (mm)	Q'TY/Carton (pcs)
SOT-23	7'	178	3000	203×203×195	45000	438×438×220	180000

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-20	V
Gate-Source Voltage		V_{GS}	±10	
Continuous Drain Current	T_A = 25°C	I_D	-2.3	A
	T_A = 70°C		-1.8	
Pulsed Drain Current [1]		I_{DM}	-9	A
Maximum Power Dissipation [2]	T_A = 25°C	P_D	1.0	W
	T_A = 70°C		0.8	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-50 to 150	°C
Junction-to-Ambient Thermal Resistance (PCB mounted) [2]		R_{thJA}	125	°C/W

Notes
1) Pulse width limited by maximum junction temperature.
2) Surface Mounted on FR4 Board, t ≤ 5 sec.

The above data are for reference only.

MOSFET ELECTRICAL CHARACTERISTICS

T_a=25℃ unless otherwise specified

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Static						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =-250μA	-20			V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =-250μA	-0.4	-0.6	-1	
Gate-source leakage	I_{GSS}	V_{DS} =0V, V_{GS} =±10V			±100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} =-20V, V_{GS} =0V			-1	μA
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} =-4.5V, I_D =-2A		125	140	mΩ
		V_{GS} =-3.3V, I_D =-1A		140	170	
Forward transconductance [a]	g_{fs}	V_{DS} =-5V, I_D =-2.8A		4.0		S
Dynamic[b]						
Input capacitance	C_{iss}	V_{DS} =-10V,V_{GS} =0V,f =1MHz		177		pF
Output capacitance	C_{oss}			30		
Reverse transfer capacitance	C_{rss}			25		
Total gate charge	Q_g	V_{DS} =-10V,V_{GS} =-4.5V,I_D =-2A		5.3		nC
Gate-source charge	Q_{gs}			0.7		
Gate-drain charge	Q_{gd}			1.4		
Turn-on delay time	$t_{d(on)}$	V_{DD}=-10V I_D =-2A, V_{GEN}=-4.5V,Rg=3.3Ω		11		ns
Rise time	t_r			32		
Turn-off delay time	$t_{d(off)}$			25		
Fall time	t_f			38		
Drain-source body diode characteristics						
Continuous source-drain diode current	I_S	T_C=25℃			-1.2	A
Body diode voltage	V_{SD}	Tj=25℃, ISD=-1A, VGS=0V		-0.83	-1.2	V

a) Pulse test: pulse width ≤ 300us, duty cycle≤ 2%

b) Guaranteed by design, not subject to production testing

Typical Characteristics

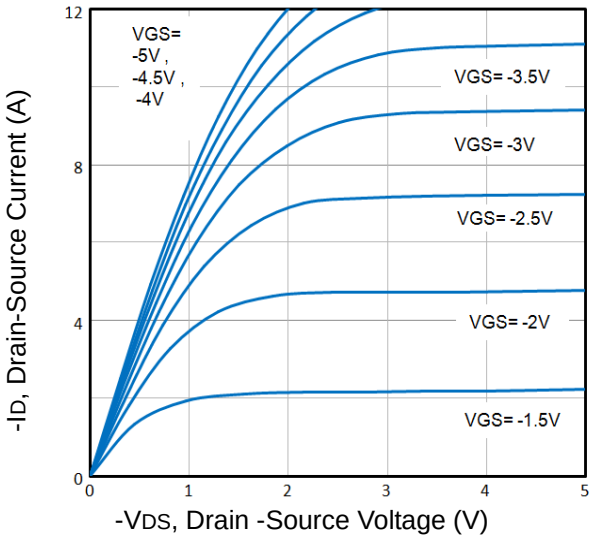


Fig1. Typical Output Characteristics

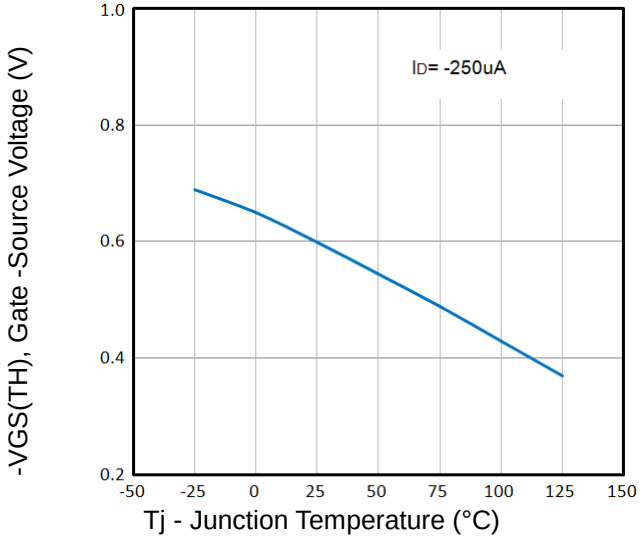


Fig2. Normalized Threshold Voltage Vs. Temperature

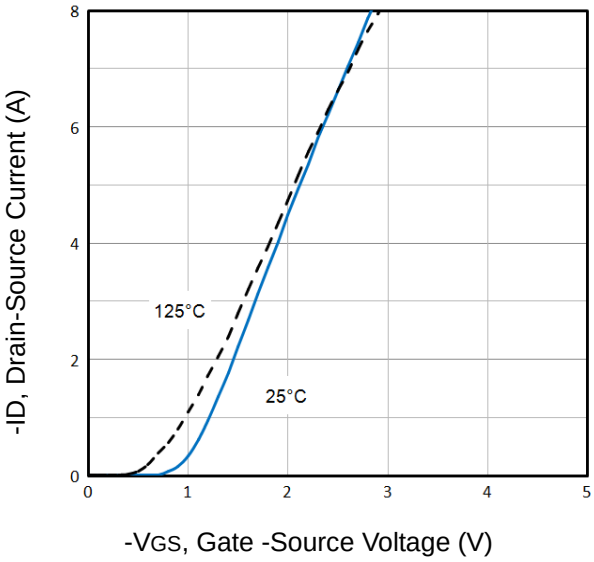


Fig3. Typical Transfer Characteristics

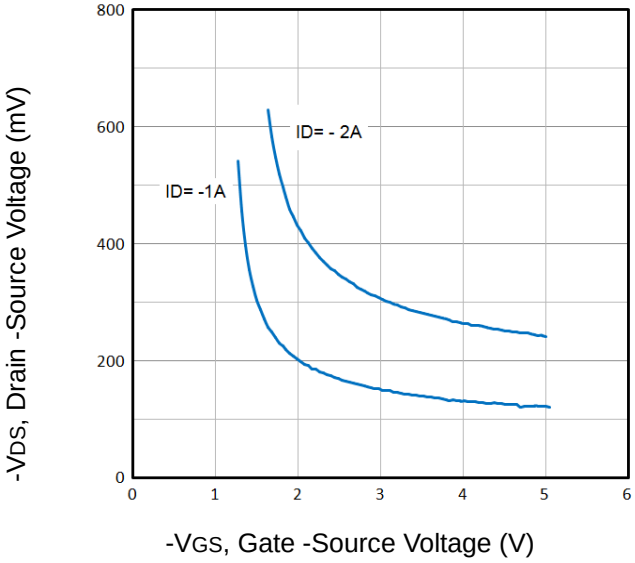


Fig4. Drain -Source Voltage vs Gate -Source Voltage

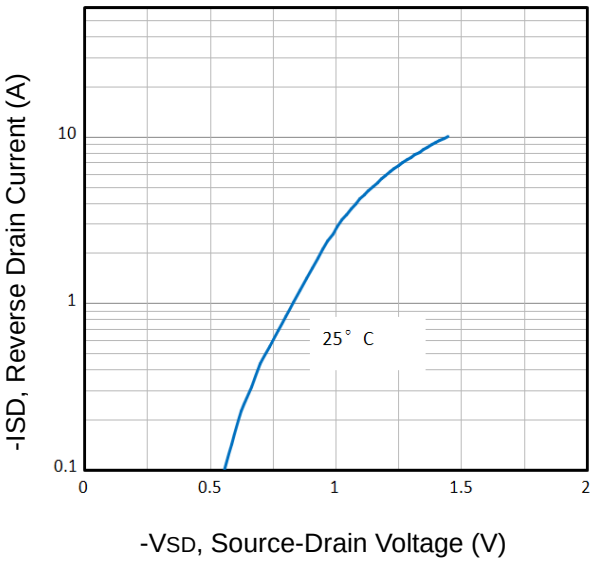


Fig5. Typical Source-Drain Diode Forward Voltage

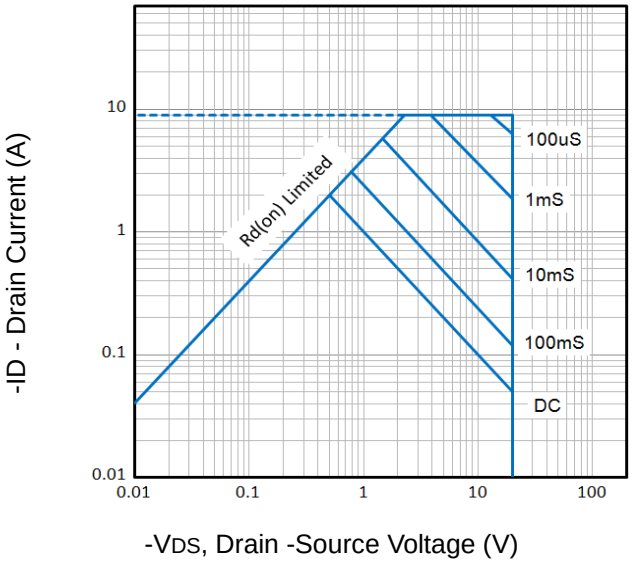


Fig6. Maximum Safe Operating Area

Typical Characteristics

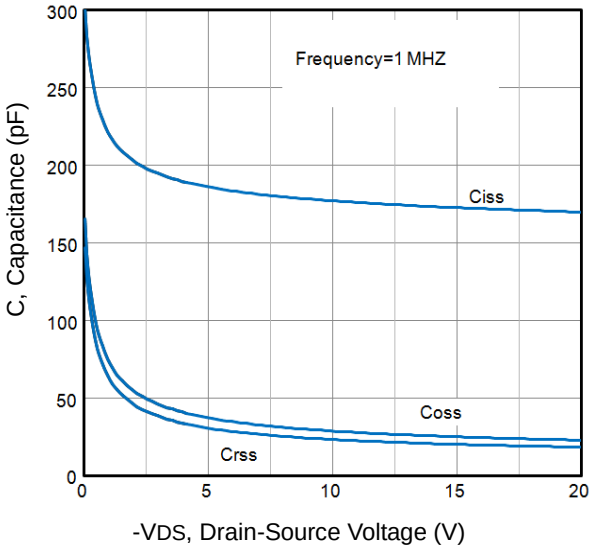


Fig7. Typical Capacitance Vs. Drain-Source Voltage

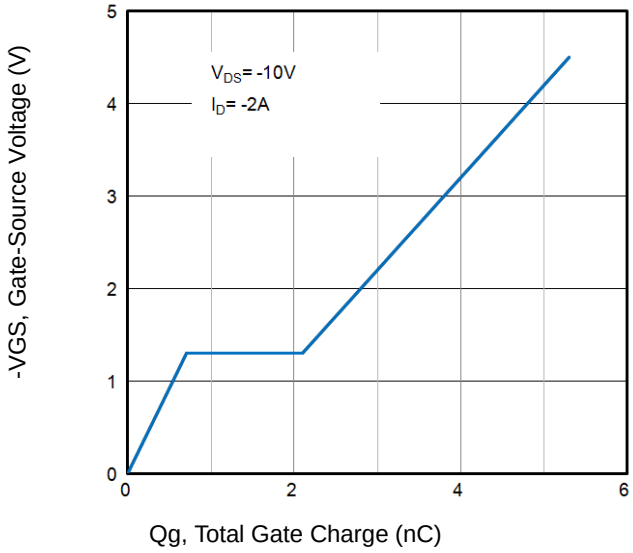


Fig8. Typical Gate Charge Vs. Gate-Source Voltage

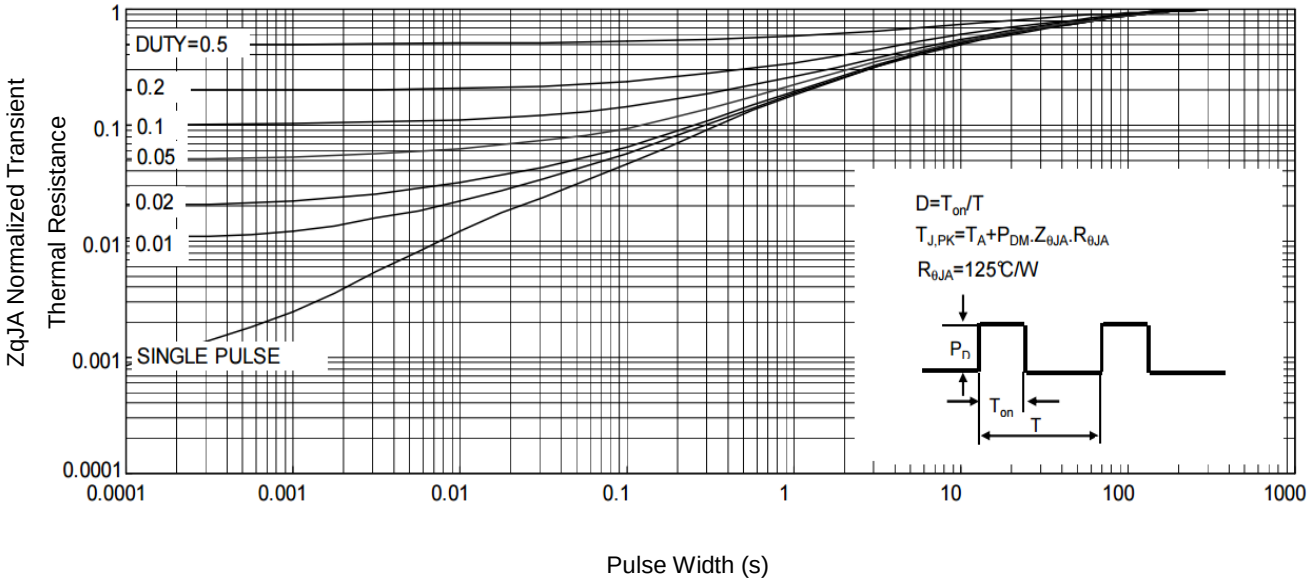


Fig9. Normalized Maximum Transient Thermal Impedance

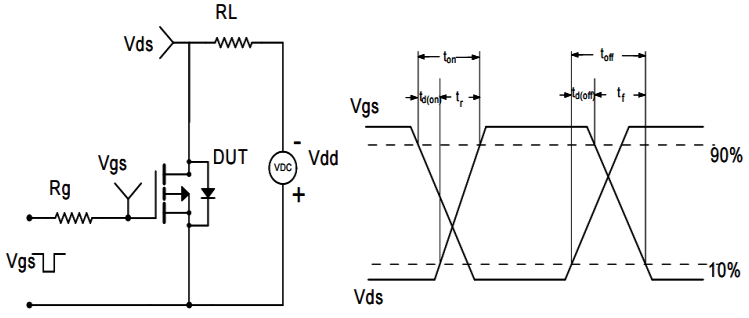
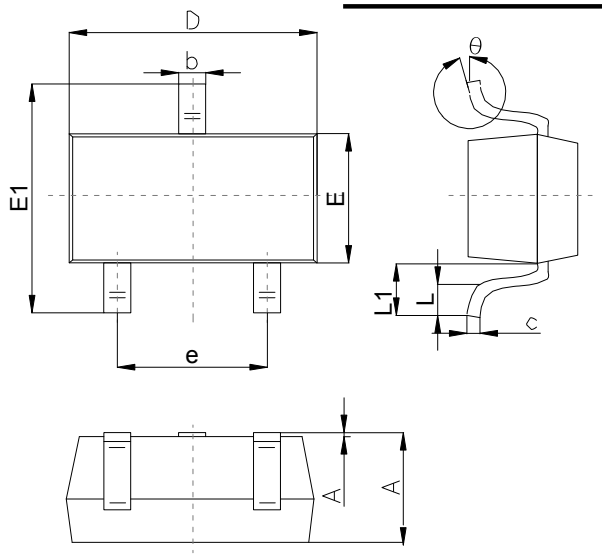


Fig10. Switching Time Test Circuit and waveforms

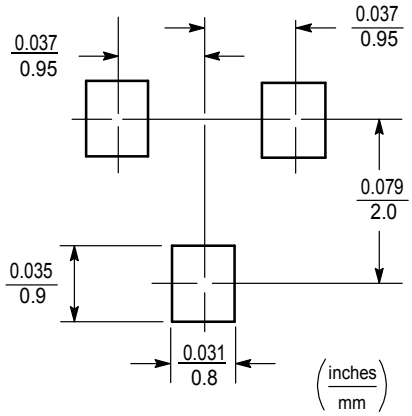
Outlitne Drawing

SOT-23 Package Outline Dimensions



Symbol	Dimensions In Millimeters		
	Min	Typ	Max
A	0.90		1.40
A1	0.00		0.10
b	0.30		0.50
c	0.08		0.20
D	2.80	2.90	3.10
E	1.20		1.60
E1	2.25		2.80
e	1.80	1.90	2.00
L	0.10		0.50
L1	0.4		0.55
θ	0°		10°

Suggested Pad Layout



Note:
1. Controlling dimension:in/millimeters. 2.General tolerance: ±0.05mm.
3.The pad layout is for reference purposes only.