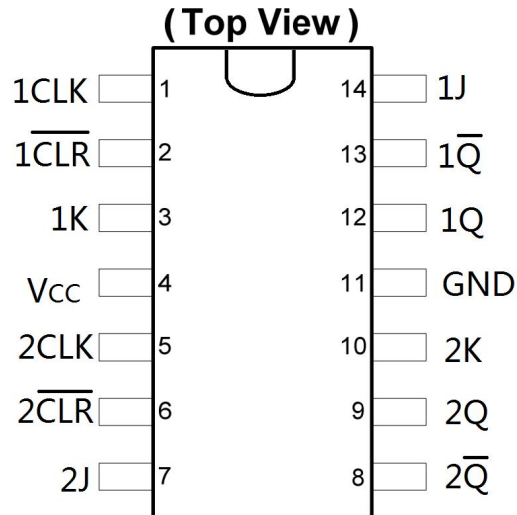


## 1. DESCRIPTION

The XD74LS73 contains two independent negative-edge-triggered flip-flops.

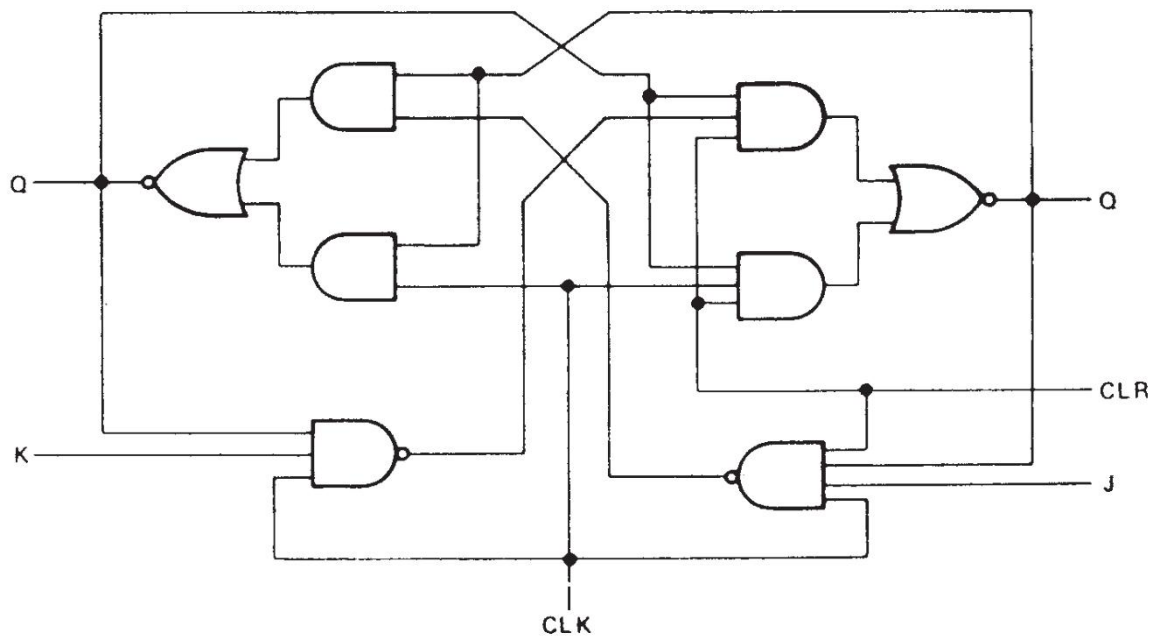
The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the Q output high.

## 2. PIN CONFIGURATIONS

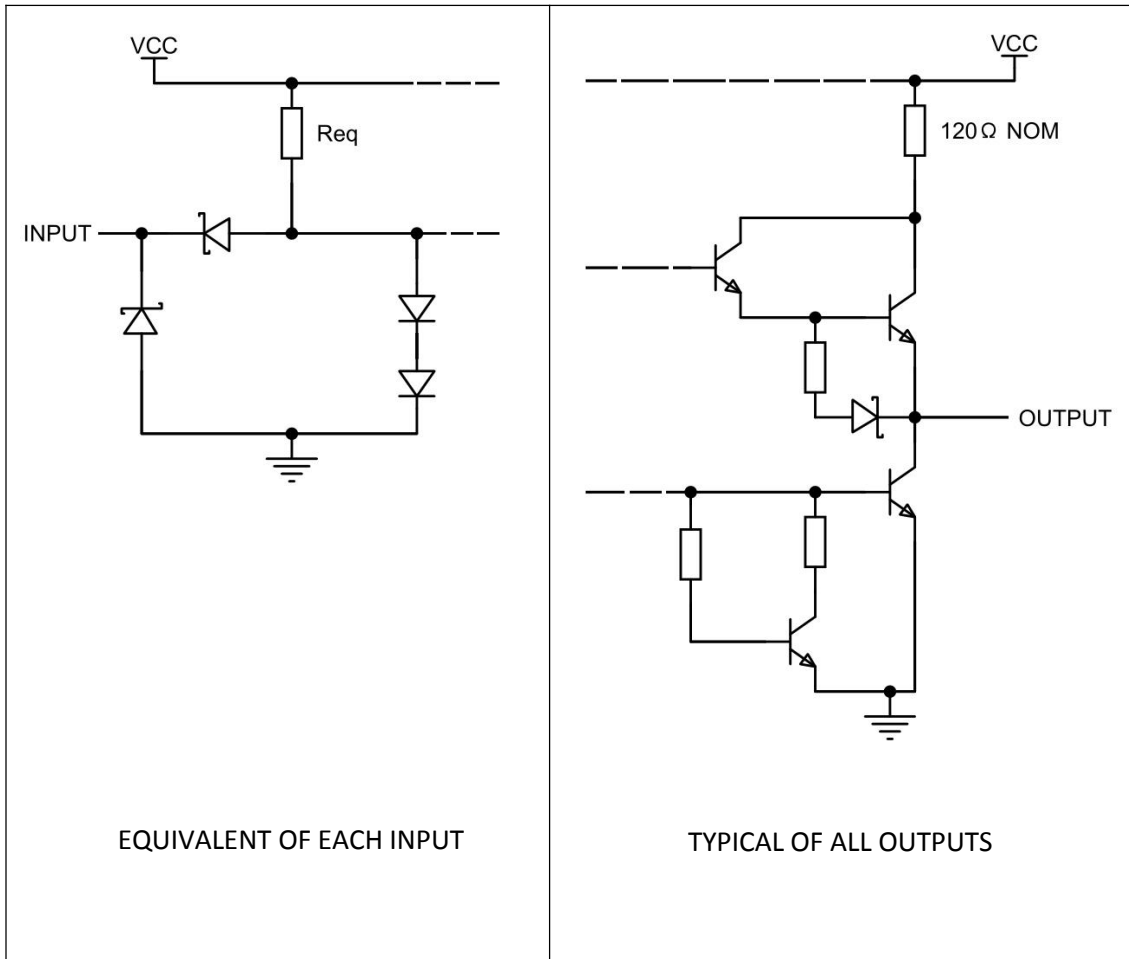


INPUTS				OUTPUTS	
$\overline{\text{CLR}}$	CLK	J	K	Q	$\overline{\text{Q}}$
L	X	X	X	L	H
H	↓	L	L	$Q_0$	$\overline{Q_0}$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	$Q_0$	$\overline{Q_0}$

### 3. LOGIC DIAGRAM



#### 4. SCHEMATICS OF INPUTS AND OUTPUTS



#### 5. ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTES)

Supply voltage, $V_{CC}$ (see Note 1).....	7V
Input voltage, $V_I$ : 74LS73.....	7V
Operating free-air temperature range: DIP package.....	0°C to 70°C
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

- NOTES: 1. Voltage values, except inter-emitter voltage, are with respect to the network ground terminal.  
2. This is the voltage between two emitters of a multiple-emitter transistor.

## 6. RECOMMENDED OPERATING CONDITIONS

		74LS73			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.75	5	5.25	V
V <sub>IH</sub>	High-level input voltage	2			V
V <sub>IL</sub>	Low-level input voltage				V
I <sub>OH</sub>	High-level output current			0.8	mA
I <sub>OL</sub>	Low-level output current			-0.4	mA
f <sub>clock</sub>	Clock frequency	0		8	MHz
t <sub>w</sub>	Pulse duration	CLK high		30	ns
		CLR low	20		
t <sub>su</sub>	Set up time-before CLK↓	Data high or low	20		ns
		CLR inactive	20		
t <sub>h</sub>	Hold time-data after CLK↓	0			ns
T <sub>A</sub>	Operating free-air temperature	0		70	°C

## 7. ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR RANGE (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS†	74LS73			UNIT
			MIN	TYP‡	MAX	
V <sub>IK</sub>		V <sub>CC</sub> = MIN, I <sub>I</sub> = -18 mA			-1.5	V
V <sub>OH</sub>		V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, I <sub>OH</sub> = 4mA	2.7	3.4		V
V <sub>OL</sub>		V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = V <sub>IL</sub> MAX I <sub>OL</sub> = 8mA	0.25	0.4		V
			0.35	0.5		
I <sub>I</sub>	J or K	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V			0.1	mA
	CLR				0.3	
	CLK				0.4	
I <sub>IH</sub>	J or K	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7 V			20	μA
	CLR				60	
	CLK				80	
I <sub>IL</sub>	J or K	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V			-0.4	mA
	CLR or CLK				-0.8	
I <sub>OS</sub> §		V <sub>CC</sub> = MAX	-20		-100	mA
I <sub>CC</sub> (Total)		V <sub>CC</sub> = MAX		4	6	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

§ Not more than one output should be shorted at a time.

## 8. SWITCHING CHARACTERISTICS, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>max</sub>			C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2kΩ, See Note 3	30	45		MHz
t <sub>PLH</sub>	CLR or CLK	Q or Q̄			15	20	ns
t <sub>PHL</sub>					15	20	ns

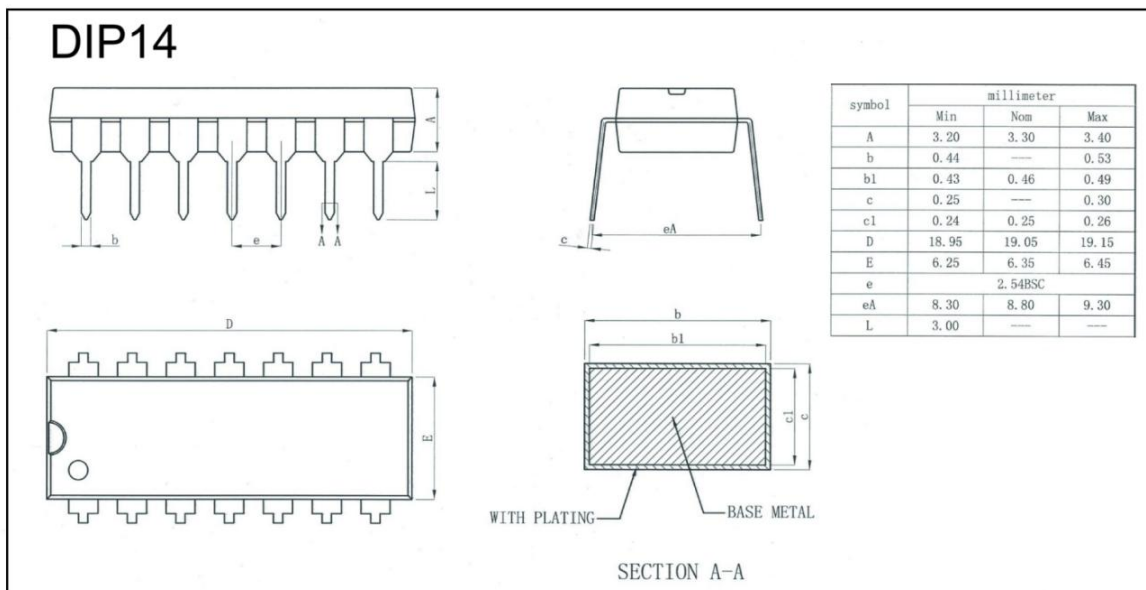
NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

## 9. ORDERING INFORMATION

### Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XD74LS73	XD74LS73	DIP14	19.05 * 6.35	-0 to 70	MSL3	Tube 25	1000

## 10. DIMENSIONAL DRAWINGS



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