CeraLink

Ceramic capacitor for fast-switching power electronic circuits

Series/Type:	**Low profile (LP)**
Ordering code:	**B58031***
Date:	2024-02-14
Version:	6.3

Known customer applications

- Power converters and inverters
- DC link / snubber / filter capacitors for power converters and inverters

Features

- High ripple current capability
- High capacitance density
- Increasing capacitance with DC bias up to operating voltage
- No limitation dV/dt
- High temperature robustness with low losses at high temperature
- Low equivalent serial inductance (ESL) and resistance (ESR)
- Ideal for high frequencies up to several MHz
- Generally low self-heating and good thermal self-regulation properties
- Qualification based on AEC-Q200 rev. D

Construction

- Multilayer technology
- RoHS-compatible PLZT ceramic (lead lanthanum zirconium titanate, see RoHS exemption 7c-II). For detailed information please refer to the *TDK Environmental protection* website.
- Copper inner electrodes
- Silver outer electrodes
- Silver coated copper-invar leadframe, recommended for reflow soldering
- Epoxy resin adhesive

General technical data

Dissipation factor	$\tan\delta$	< 0.02	
Insulation resistance	$R_{ins,\ typ}$ *)	> 1	GΩ
Operating device temperature	T_{device}	-40 … +150	°C
Weight of device		approx. 1.3	g

*) Typical insulation resistance, measured at operating voltage V_{op} and measurement time > 240 s, +25 °C

Electrical specifications and ordering codes

Lead type	$V_{pk, max}$ V	$V_{R, Tmax}$ *) V	V_{op} V	$C_{nom, typ}$ µF	$C_{eff, typ}$ µF	C_0 µF	Ordering code
L-style	650	500	400	1	0.6	0.35 ±20%	B58031I5105M062
J-style							B58031U5105M062
L-style	1000	700	600	0.5	0.25	0.14 ±20%	B58031I7504M062
J-style							B58031U7504M062
L-style	1300	900	800	0.25	0.13	0.07 ±20%	B58031I9254M062
J-style							B58031U9254M062

*) $V_{R, Tmax}$ denotes the permissible rated voltage for the maximum device temperature T_{max} = +150 °C. Operation at higher rated voltage $V_R > V_{R, Tmax}$ is possible. The permissible rated voltage V_R can be taken from the temperature derating curves on the next page.

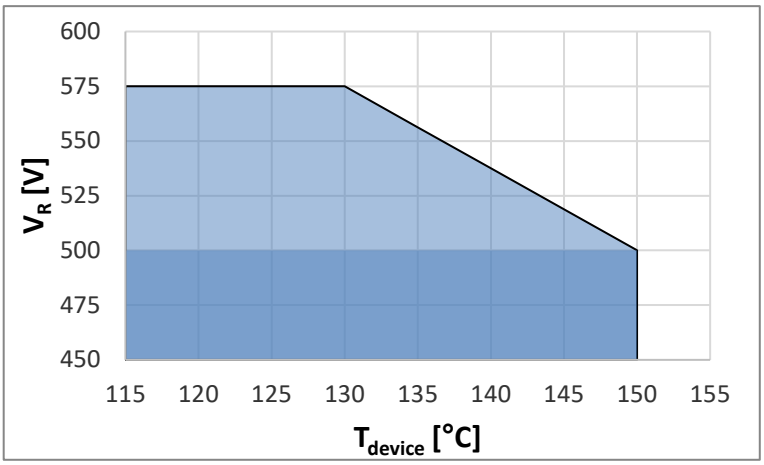
Aging

The capacitance has an aging behavior which shows a decrease of capacitance with time.
The typical aging rate is about 2.5% per logarithmic decade in hours.

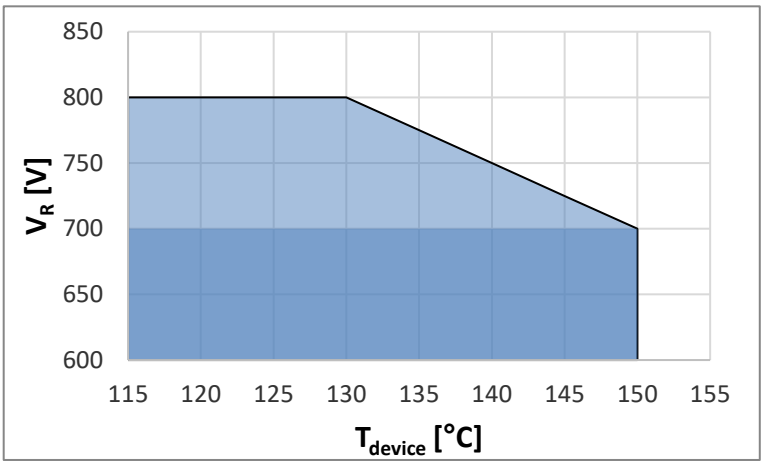
Rated voltage V_R and temperature derating

The CeraLink LP series can be operated at elevated rated voltage, i.e. $V_R \geq V_{R,\,Tmax}$. However, the device temperature of the component (measured on the ceramic surface) should be kept within the temperature-derated conditions detailed in the following figures. Higher device temperatures are permissible at reduced lifetime depending on mission profile.

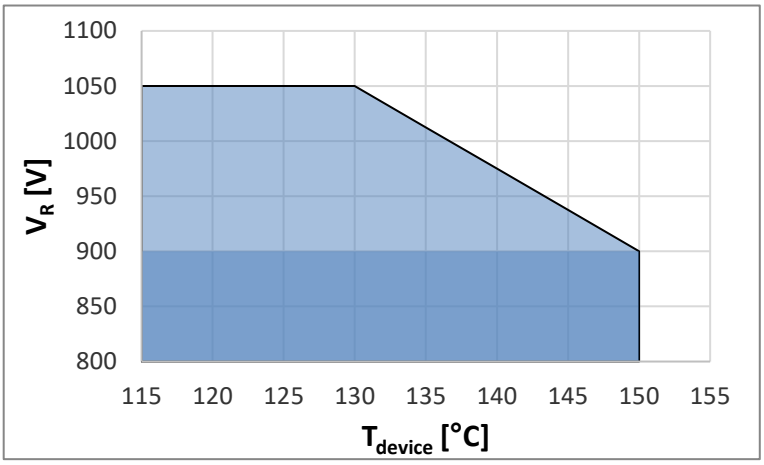
$V_{R,\,Tmax}$ = 500 V (B58031*5*)



$V_{R,\,Tmax}$ = 700 V (B58031*7*)

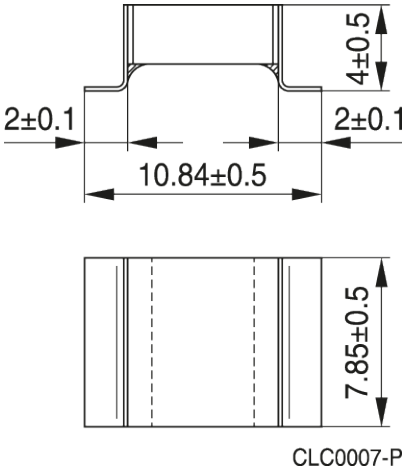


$V_{R,\,Tmax}$ = 900 V (B58031*9*)



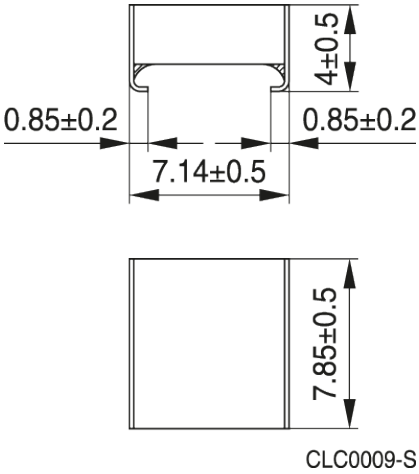
Dimensional drawings

L-style



CLC0007-P

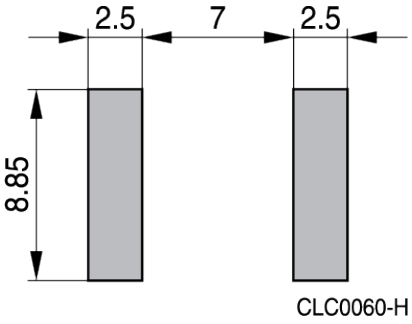
J-style



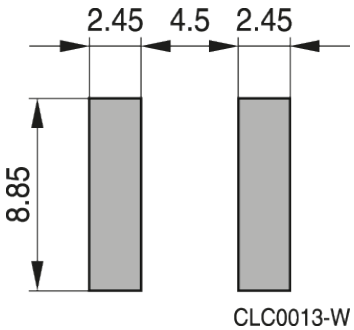
CLC0009-S

Dimensions in mm

Recommended solder pads



CLC0060-H

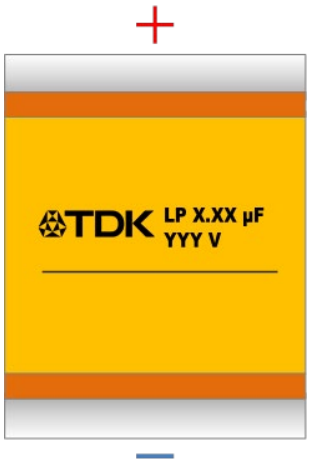


CLC0013-W

Dimensions in mm

Polarity and marking of components

L-style



J-style

Manufacturer's logo
CeraLink type
X.XX = Nominal capacitance (1, 0.5, 0.25)
YYY = Rated voltage (500, 700, 900)

Note that polarity is only for incoming inspection purposes and it does not affect operation. If put under reverse rated voltage V_R, CeraLink is repoled and works identically, see our *CeraLink Technical Guide* for further details.

Typical values as a design reference for CeraLink applications

$V_{R, Tmax}$	ESR 0 V DC, 0.5 V AC (RMS), 25 °C, 1 kHz	ESR 0 V DC, 0.5 V AC (RMS), 25 °C, 1 MHz	ESL	I_{op} *) V_{op} 100 kHz T_{amb} = 85 °C	I_{op} *) V_{op} 100 kHz T_{amb} = 105 °C
V	**Ω**	**mΩ**	**nH**	**A (RMS)**	**A (RMS)**
500	3	12	3	11	10
700	6	24	3	7	6
900	14	45	3	5	5

*) Normal operating current without forced cooling at T_{device} = +150 °C. Higher values permissible at reduced lifetime.

Application notes

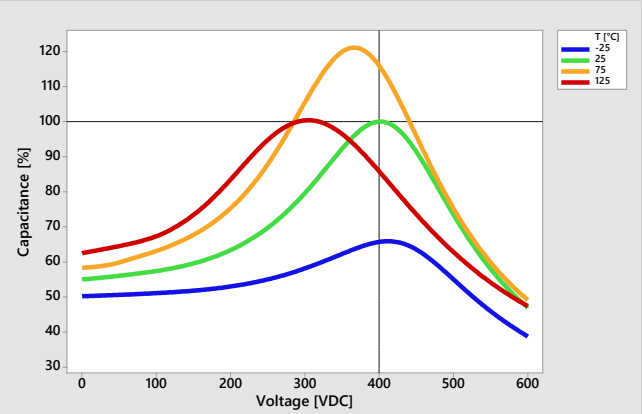
Further typical electrical characteristics as a design reference for CeraLink applications.

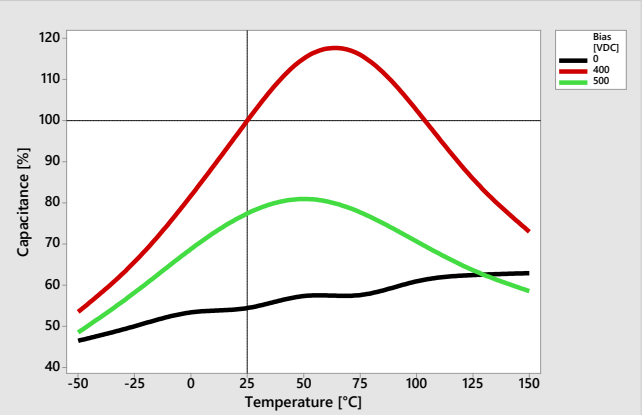
Typical characteristics as a function of temperature and voltage - $V_{R,\ Tmax}$ = 500 V

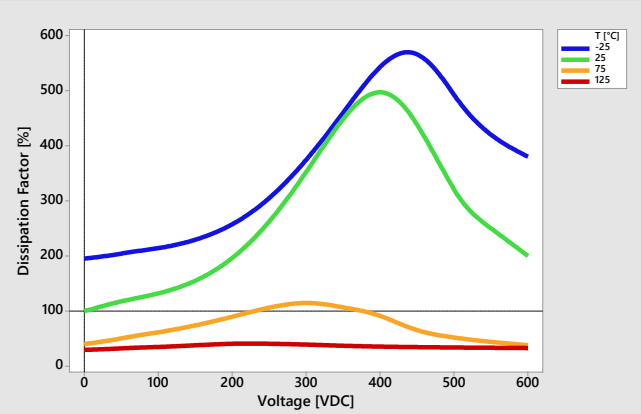
(0.5 V AC (RMS), frequency = 1 kHz)

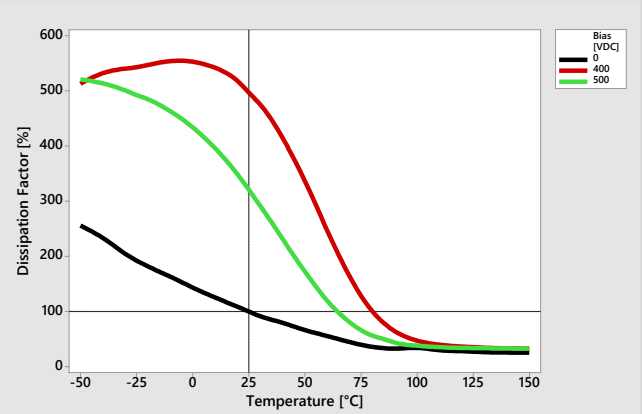
All given temperatures are device temperatures (measured on ceramic surface).

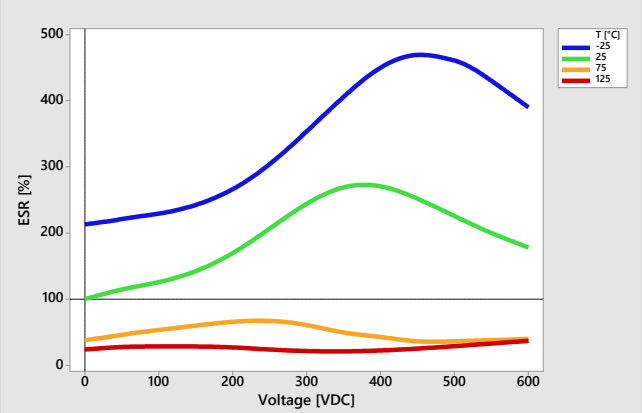
The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100% values correspond to tan δ, $C_{eff,\ typ}$ and ESR_{1kHz} which are given on page 2, 3 and 6 of this data sheet.

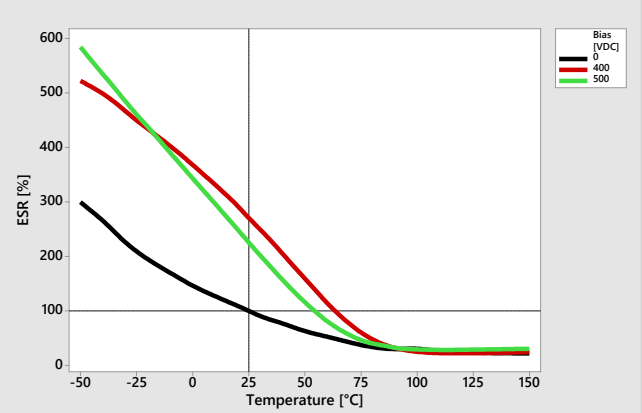




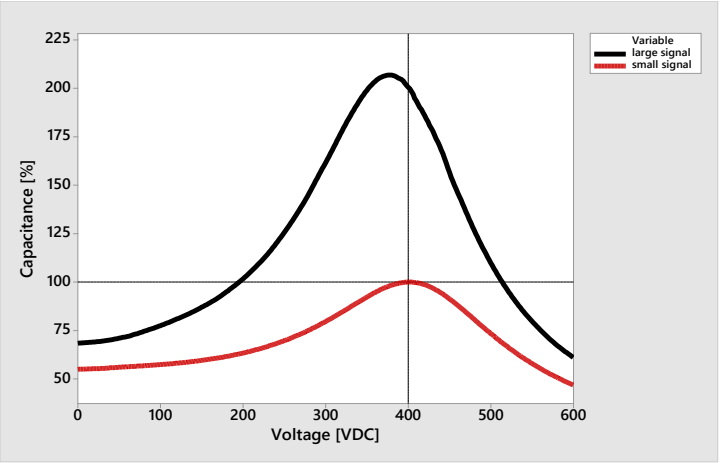








Typical capacitance values as a function of voltage - $V_{R, Tmax}$ = 500 V



Large signal capacitance:

Quasistatic (slow variation of the voltage), +25 °C.

The nominal capacitance is defined as the large signal capacitance at $V_{op.}$

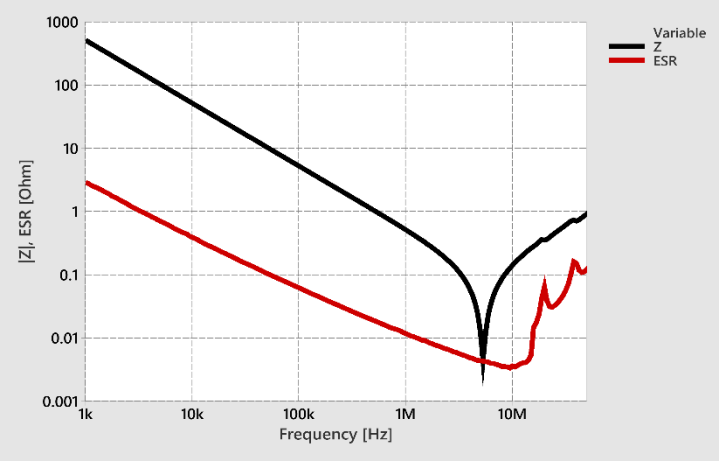
See glossary for further information.

Small signal capacitance:

0.5 V AC (RMS), 1 kHz, +25 °C

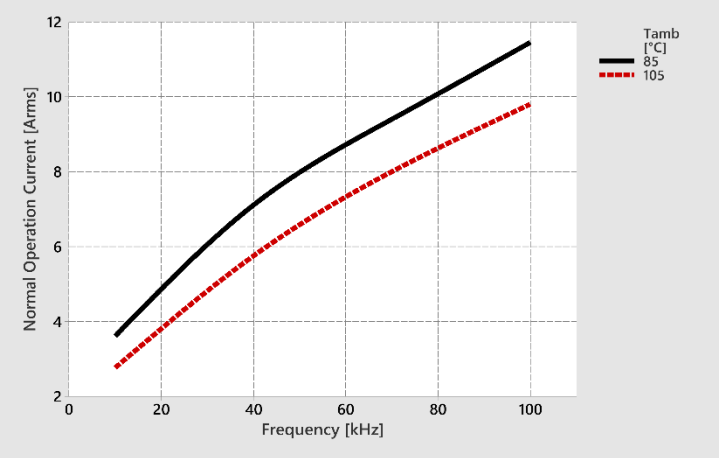
The effective capacitance is defined as the small signal capacitance at V_{op}.

Typical impedance and ESR as a function of frequency - $V_{R, Tmax}$ = 500 V



0 V DC, 0.5 V AC (RMS), T_{device} = 25 °C

Typical permissible current as a function of frequency - $V_{R, Tmax}$ = 500 V



Measurement performed at V_{op}.

The values correspond to a device temperature of +150 °C.

No forced cooling was used.

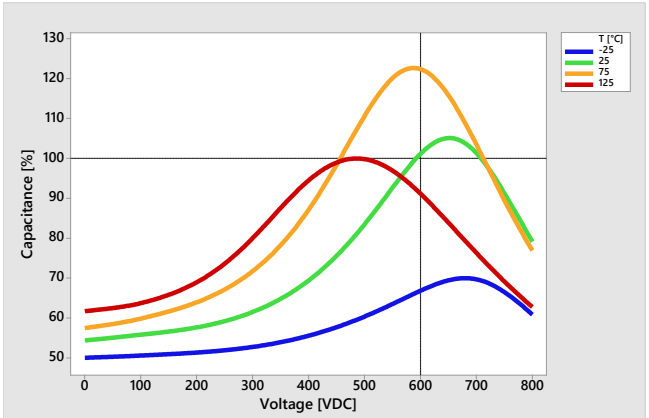
Note hat with additional cooling the typical permissible current can be significantly higher.

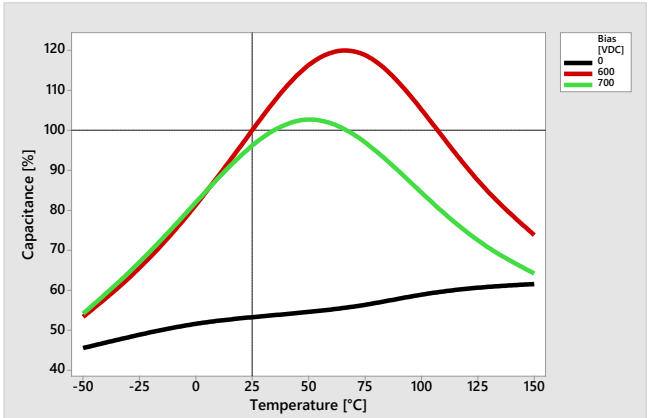
Typical characteristics as a function of temperature and voltage - $V_{R, Tmax}$ = 700 V

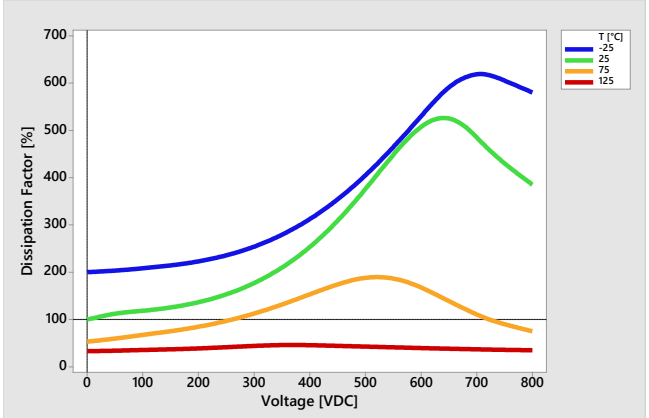
(0.5 V AC (RMS), frequency = 1 kHz)

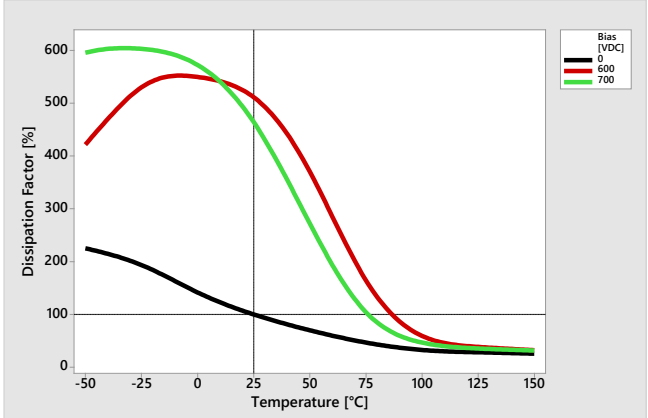
All given temperatures are device temperatures (measured on ceramic surface).

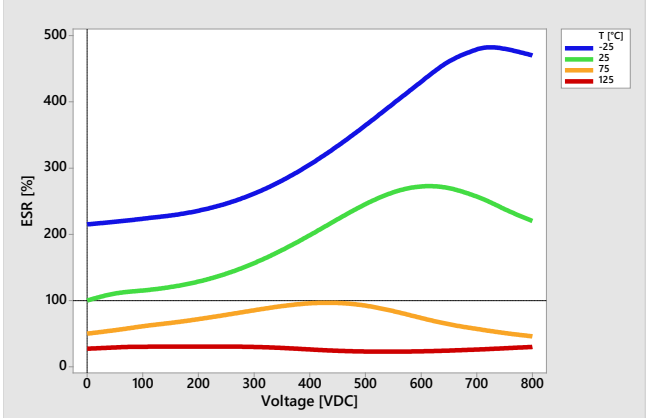
The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100% values correspond to tan δ, $C_{eff, typ}$ and ESR_{1kHz} which are given on page 2, 3 and 6 of this data sheet.

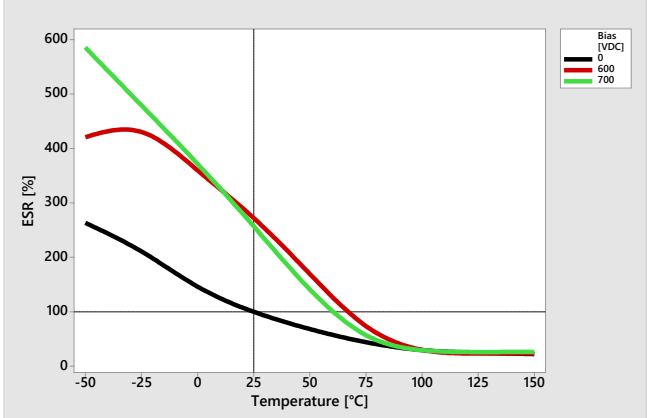




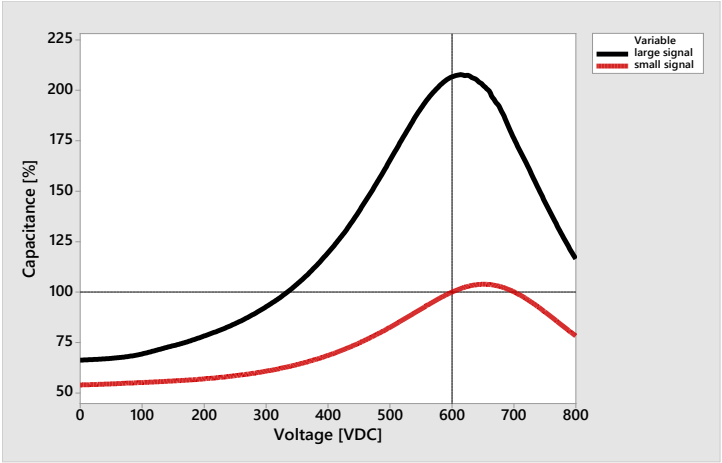








Typical capacitance values as a function of voltage - $V_{R, Tmax}$ = 700 V



Large signal capacitance:

Quasistatic (slow variation of the voltage), +25 °C.

The nominal capacitance is defined as the large signal capacitance at V_{op}.

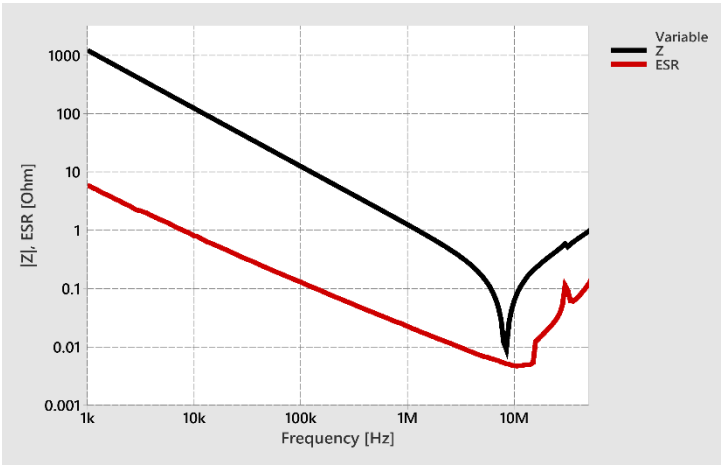
See glossary for further information.

Small signal capacitance:

0.5 V AC (RMS), 1 kHz, +25 °C

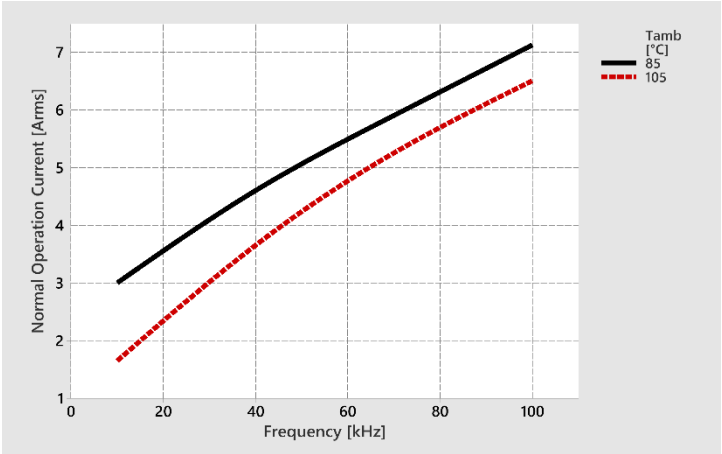
The effective capacitance is defined as the small signal capacitance at V_{op}.

Typical impedance and ESR as a function of frequency - $V_{R, Tmax}$ = 700 V



0 V DC, 0.5 V AC (RMS), T_{device} = 25 °C

Typical permissible current as a function of frequency - $V_{R, Tmax}$ = 700 V



Measurement performed at V_{op}.

The values correspond to a device temperature of 150 °C.

No forced cooling was used.

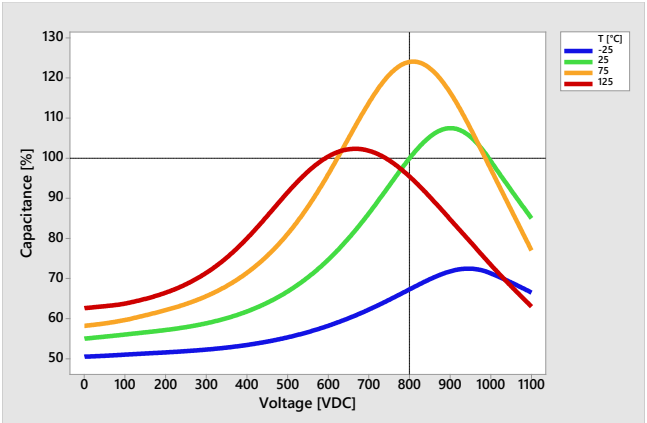
Note that with additional cooling the typical permissible current can be significantly higher.

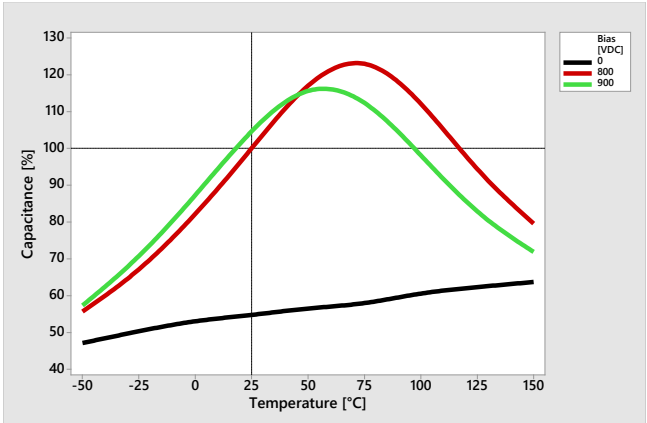
Typical characteristics as a function of temperature and voltage - $V_{R, Tmax}$ = 900 V

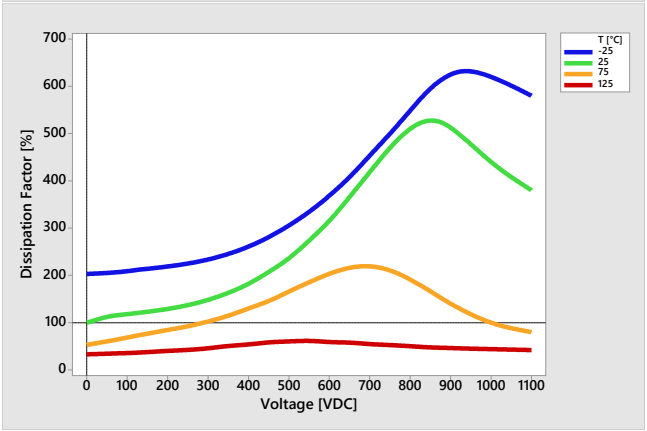
(0.5 V AC (RMS), frequency = 1 kHz)

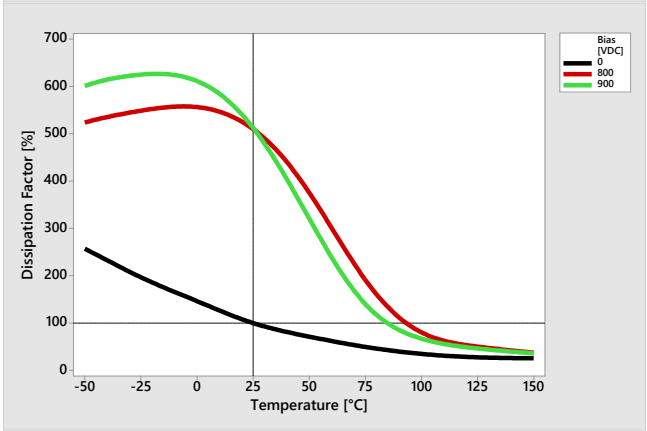
All given temperatures are device temperatures (measured on ceramic surface).

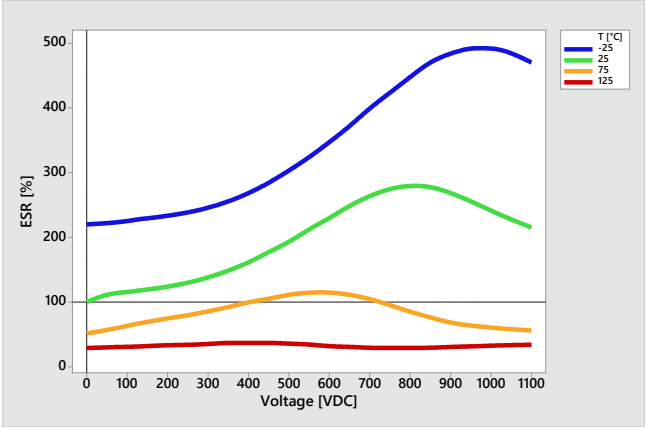
The curves show the relative changes of the capacitance, dissipation factor and ESR. The 100% values correspond to tan δ, $C_{eff, typ}$ and ESR_{1kHz} which are given on page 2, 3 and 6 of this data sheet.

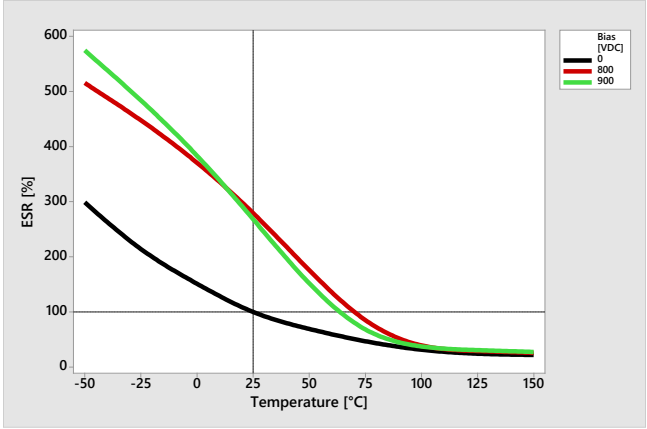




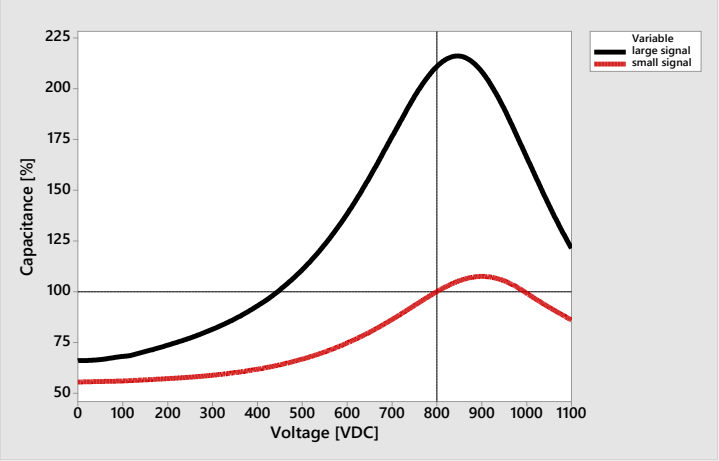








Typical capacitance values as a function of voltage - $V_{R, Tmax}$ = 900 V



Large signal capacitance:

Quasistatic (slow variation of the voltage), +25 °C.

The nominal capacitance is defined as the large signal capacitance at V_{op}.

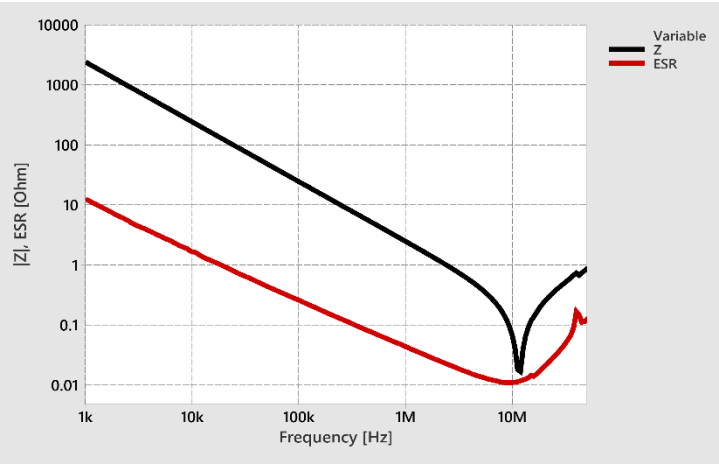
See glossary for further information.

Small signal capacitance:

0.5 V AC (RMS), 1 kHz, +25 °C

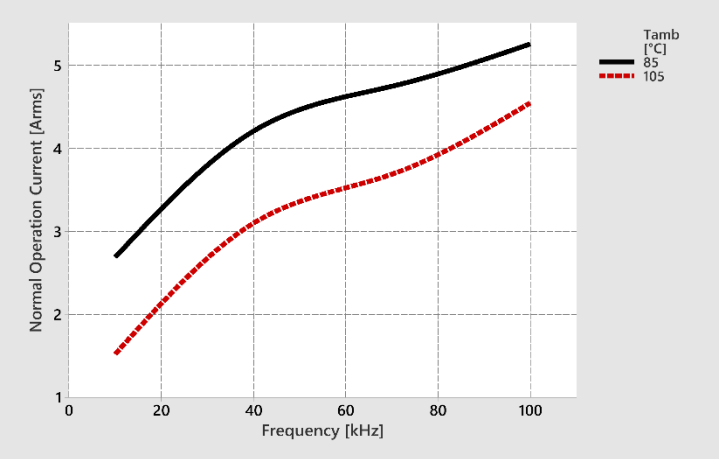
The effective capacitance is defined as the small signal capacitance at V_{op}.

Typical impedance and ESR as a function of frequency - $V_{R, Tmax}$ = 900 V



0 V DC, 0.5 V AC (RMS), T_{device} = 25 °C

Typical permissible current as a function of frequency - $V_{R, Tmax}$ = 900 V



Measurement performed at V_{op}.

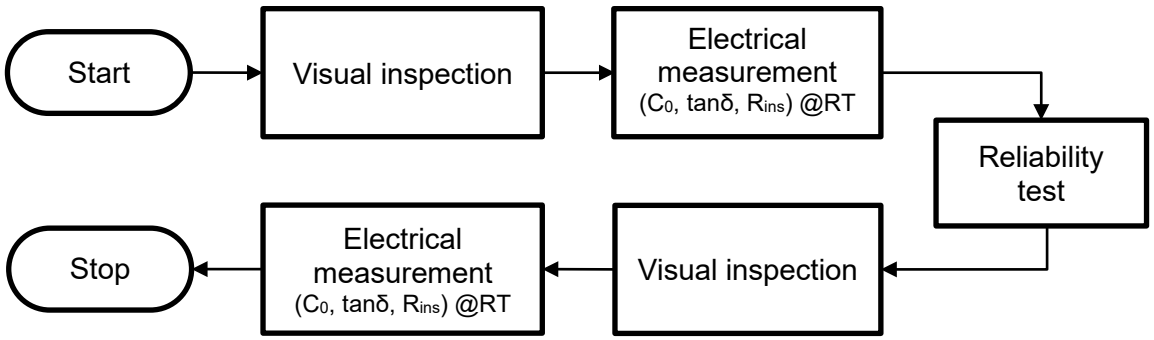
The values correspond to a device temperature of 150 °C.

No forced cooling was used.

Note that with additional cooling the typical permissible current can be significantly higher.

Reliability: test methods and conditions

General test flow



Pre- and post-measurement for AEC-Q200 tests

A. Preconditioning:

- Solder the capacitor on a PCB using the recommended soldering profile
- Check of external appearance
- Measurement of isolation resistance R_{ins} *)
  - Apply $V_{pk, max}$ for 7 seconds and measure R_{ins} at room temperature:
    Isolation resistance (@ $V_{pk, max}$, 7 s, 25 °C) **R_{ins} > 100 MΩ**
- Measurement of electrical parameters C_0 and tan δ according to specification
  - Measure C_0 and tan δ within 10 minutes to 1 hour afterwards:
    Initial capacitance (@ 0 V DC, 0.5 V AC (RMS), 1 kHz, 25 °C) **C_0 acc. spec. on page 3**
    Dissipation factor (@ 0 V DC, 0.5 V AC (RMS), 1 kHz, 25 °C) **tan δ < 0.02**

B. Performance of a specific reliability test.

C. After performing a specific test:

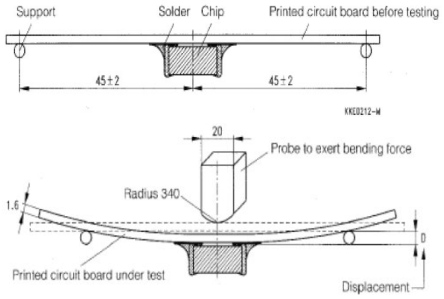
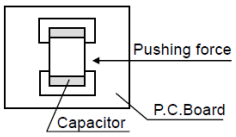
- Check the external appearance again
- Repeat the measurement of the electrical parameters
  - Apply $V_{pk, max}$ for 7 seconds and measure R_{ins} at room temperature:
    Isolation resistance (@$V_{pk, max}$, 7 s, 25 °C) **R_{ins} > 100 MΩ**
  - Measure C_0 and tan δ:
    Change of initial capacitance (@ 0 V DC, 0.5 V AC (RMS), 1 kHz, 25 °C) **$|\Delta C_0/C_0|$ < 15%**
  - Dissipation factor (@ 0 V DC, 0.5 V AC (RMS), 1 kHz, 25 °C) **tan δ < 0.05**

*) Note that the measurement of the isolation resistance R_{ins} using the described measurement conditions is for pre- and post-measurement within the scope of the AEC-Q200 reliability tests only (see next page for details).

Qualification tests based on AEC-Q200 Rev. D (Table 2)

Test	No	Standard	Test conditions	Criteria
Pre- and Post-Stress Electr. Test	1	-	As described above	Common failure criteria *).
High Temperature Exposure	3	MIL-STD-202 Method 108	+150 °C, unpowered, 1000 hours	No mechanical damage. Common failure criteria *).
Temperature Cycling	4	JESD22-A-104	-55 °C to +150 °C, ≤ 20 seconds transfer time, 15 minutes dwell time, 1000 cycles	No mechanical damage. Common failure criteria *).
Destructive Physical Analysis	5	EIA-469	-	No internal defects that might affect performance or reliability.
Biased Humidity	7	MIL-STD-202 Method 103	+85 °C, 85% rel. hum., $V_{R,\,Tmax}$, 1000 hours	No mechanical damage. Common failure criteria *).
High Temperature Operating Life (HTOL)	8	MIL-STD-202 Method 108	+150 °C, $V_{R,\,Tmax}$, 1000 hours	No mechanical damage. Common failure criteria *).
External Visual	9	MIL-STD-883 Method 2009	Visual inspection with magnifying glass	No defects that might affect performance or reliability
Physical Dimension	10	JESD22-B-100	Verify physical dimensions to the device specification using a caliper and a gauge	Within specified values in the chapter dimensional drawing
Tensile Strength (unsoldered)	11	MIL-STD-202 Method 211	Apply a force of 10 N in the shown direction. Ceramic body is clamped: 	No detaching of termination. Common failure criteria *).
Resistance to Solvent	12	MIL-STD-202 Method 215	Dipping and cleaning with isopropanol	Marking must be legible. Common failure criteria *).
Mechanical Shock	13	MIL-STD-202 Method 213	Acceleration 400 m/s² Half sine pulse duration 6 milliseconds 4000 bumps	No mechanical damage. Common failure criteria *).
Vibration	14	MIL-STD-202 Method 204	5 g / 20 min, 12 cycles, 3 axes 10 Hz to 2000 Hz	No mechanical damage. Common failure criteria *).
Resistance to Soldering Heat	15	MIL-STD-202 Method 210 Condition B	Dip test of contact areas in solder bath (+260 °C for 10 seconds)	No damage of leadframe silver coating. Common failure criteria *).
Solderability	18	See below		

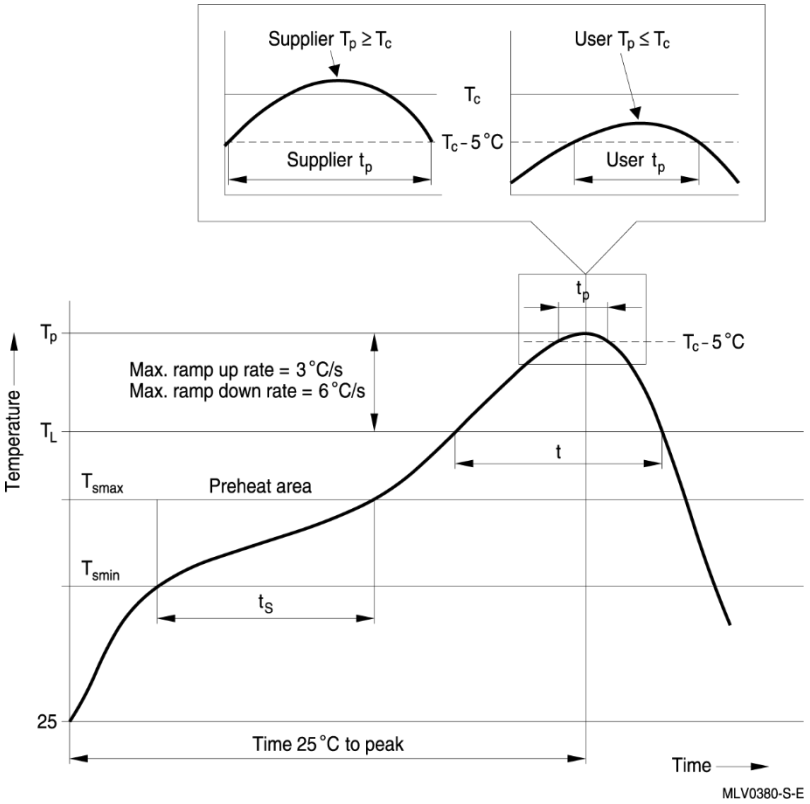
*) Common failure criteria: R_{ins}, $|\Delta C_0/C_0|$ and tanδ within defined limits (see pre- and post-measurement on prev. page).

Test	No	Standard	Test conditions	Criteria
Board Flex	21	AEC-Q200-005	Bending of 2 mm for 60 seconds  Dimensions in mm	No mechanical damage. Common failure criteria *).
Terminal Strength	22	AEC-Q200-006	Apply a force of 17.7 N for 60 seconds 	No detaching of termination. No rupture of ceramic. Common failure criteria *).

Solderability tests

Wettability (leadframe only)	J-STD-002, Method A @ 235 °C, cat. 3	Dipping of contact areas in solder bath (+235 °C for 5 seconds)	> 95% wettability of lead frame
Leaching (leadframe only)	MIL-STD-202, Method 210, cond. B	Dipping of contact areas in solder bath (+260 °C for 10 seconds)	No damage of lead frame silver coating
Reflow test	-	3 times recommended reflow soldering profile	No mechanical damage. Proper solder coating of contact areas. Common failure criteria *).

Recommended reflow soldering profile



Profile feature		SAC, Sn95.5Ag3.8Cu0.7 @ N_2 atmosphere
Preheat and soak - Temperature min - Temperature max - Time	 T_{smin} T_{smax} t_{smin} to t_{smax}	 +150 °C +200 °C 60 … 120 seconds
Average ramp-up rate	T_L to T_p	3 °C / second max.
Liquidus temperature Time at liquidus temperature	T_L t_L	+217 °C 60 … 150 seconds
Peak package body temperature	T_p[1)]	245 °C … 260 °C max.[2)]
Time (t_p)[3)] within +5 °C of specified classification temperature (T_c)		30 seconds[3)]
Average ramp-down rate	T_p to T_L	+6 °C / second max.
Time +25 °C to peak temperature		maximum 8 minutes

[1)] Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.
[2)] Depending on package thickness (cf. JEDEC J-STD-020D).
[3)] Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

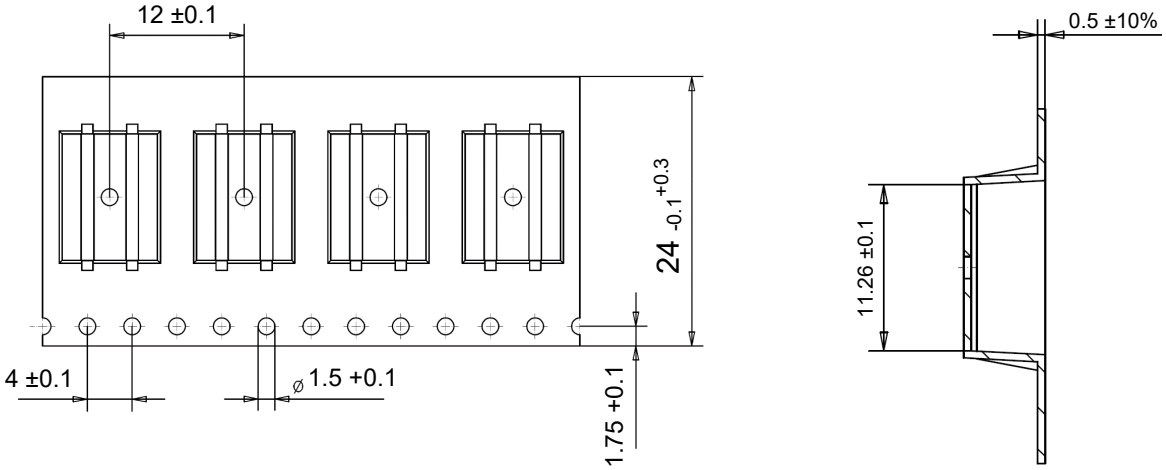
Notes:

- Note that the component is designed for reflow soldering. Consult TDK if other soldering processes are considered.
- All temperatures refer to topside of the package, measured on the package body surface.
- Max. number of reflow cycles: 3
- After the soldering process, the capacitance is lowered. Applying V_R to the device will re-establish the capacitance.
- The proposed soldering profile is based on IEC 60068-2-58 (respectively JEDEC J-STD-020D) recommendations.

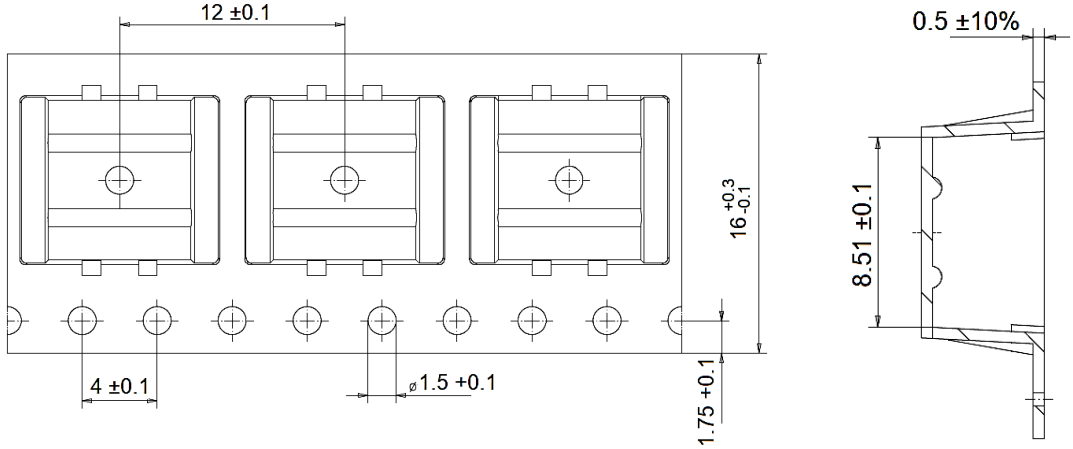
Packaging

The CeraLink LP types are delivered in a blister tape (taping to IEC 60286-3).

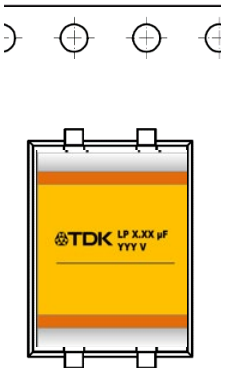
Blister tape for L-style terminal



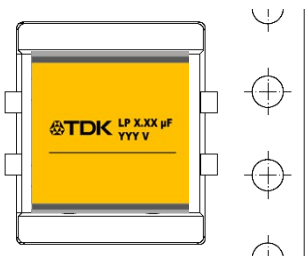
Blister tape for J-style terminal



Part orientation for L-style terminal



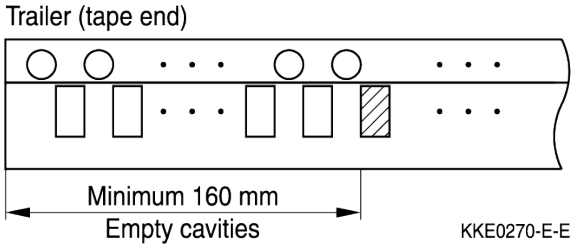
Part orientation for J-style terminal

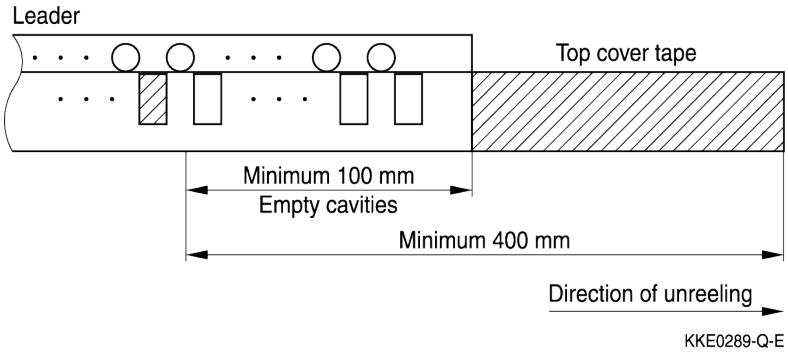


Taping information

Trailer: There is a minimum of 160 mm of carrier tape with empty compartments and sealed by the cover tape.

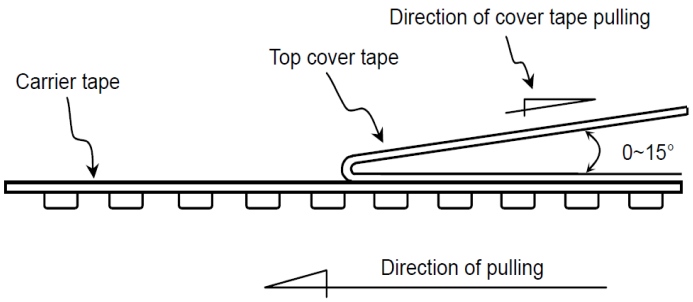
Leader: There is a minimum of 400 mm of cover tape, which includes at least 100 mm of carrier tape with empty compartments.



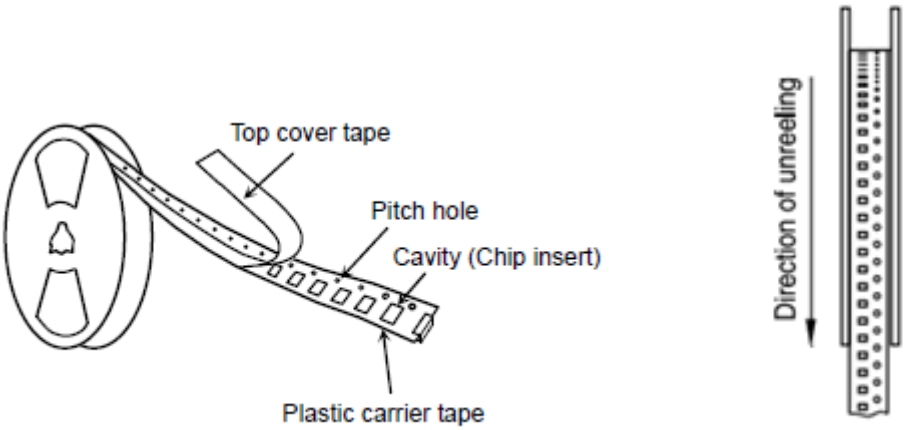


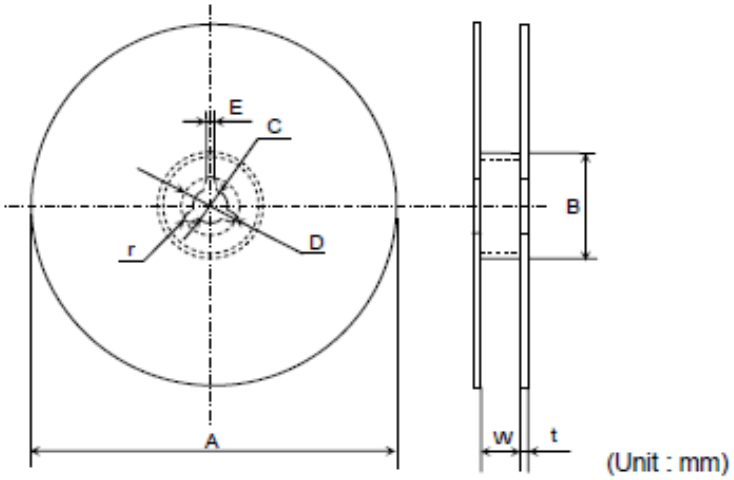
Fixing peeling strength (top tape)

The peeling strength is 0.1 to 1.3 N.



Reel packing





	L-style terminal 330-mm reel	J-style terminal 330-mm reel
A	330 ±2	330 ±2
B	100 ±1	62 ±1
C	13 +0.5/ -0.2	12.8 +0.7
D	20.2 min.	19.1 min.
E	2.2 ±0.2	1.6 ±0.5
W	24.2 +2	16.4 +2

Dimensions in mm

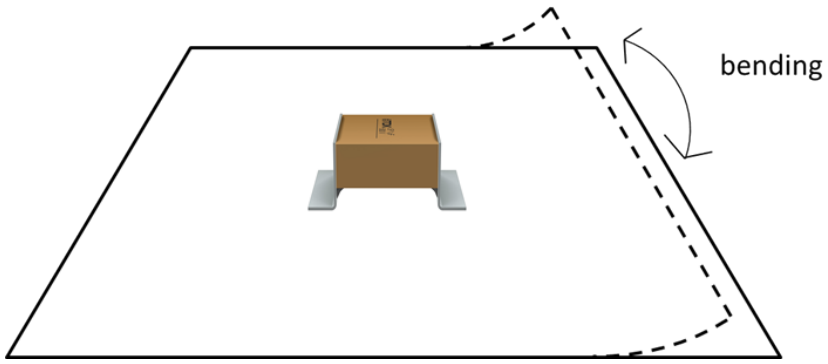
General technical information

Storage

- In order to maintain solderability, the components must be stored in a non-corrosive atmosphere. Humidity, temperature, and container materials are critical factors.
- Only store CeraLink capacitors in their original packaging. Do not open the package prior to processing. Touching the metallization of unsoldered components may change their soldering properties.
- Storage conditions in original packaging: temperature: -25 to +45 °C, relative humidity: ≤ 75% annual average, ≤ 95% on max. 30 days in a year, dew precipitation and wetness are inadmissible.
- Do not store the components where they are exposed to heat or direct sunlight. Otherwise, the packing material may be deformed, or the components may stick together, causing problems during mounting. After opening the factory seals, such as polyvinyl-sealed packages, use the components as soon as possible.
- Avoid contamination of the CeraLink surface during storage, handling, and processing.
- Avoid storing CeraLink devices in harmful environments where they are exposed to corrosive gases (e.g. SOx, Cl).
- Use CeraLink as soon as possible after opening factory seals such as polyvinyl-sealed packages.
- The product is recommended to be soldered within 12 months after shipment. Check solderability in case extended shelf life beyond the expiry date is needed.

Handling

- Do not drop CeraLink components or allow them to be chipped.
- Do not touch CeraLink with your bare hands - gloves are recommended.
- Avoid contamination of the CeraLink surface during handling.
- Do not clamp CeraLink components on the face sides (e.g. during pick-and-place). A vacuum-based pick-and-place process picking the component on the top side is recommended.
- Washing processes to remove e.g. flux are recommended but should be used with caution since they may damage the product due to the possible static or cyclic mechanical loads (e.g. ultrasonic cleaning). Mechanical loads which may cause cracks to develop on the product and its parts must be avoided, since this might lead to reduced reliability or lifetime.
- The CeraLink LP series uses copper-invar leadframes to prevent mechanical stress to the ceramic. Too much bending causes open mode. Avoid high mechanical stress like twisting after soldering on a PCB.

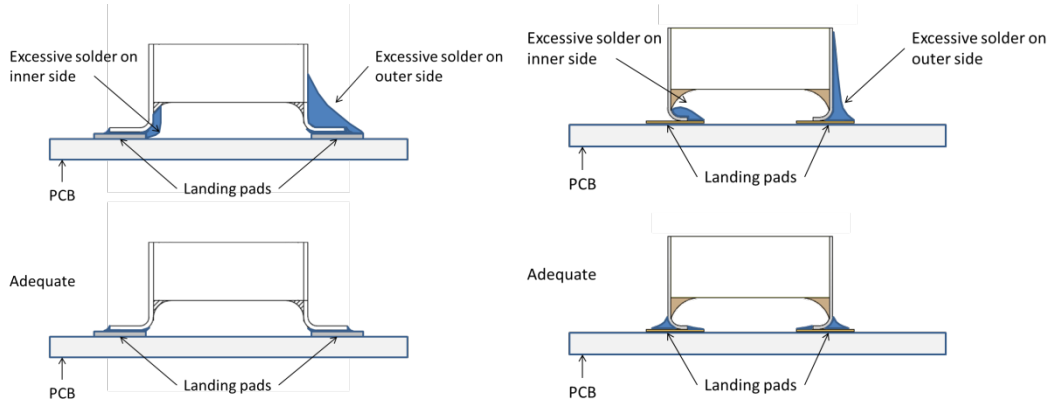


Mounting

- Do not subject CeraLink devices to mechanical stress when encapsulating them with sealing material or overmolding with plastic material. Encapsulation may also lead to worse heat dissipation. Please ask for further information
- Do not scratch the electrodes before, during, or after the mounting process.
- Avoid high mechanical stress like twisting or bending of the PCB close to the soldered CeraLink.
- Make sure contacts and housings used for assembly with CeraLink components are clean before mounting.
- The surface temperature of an operating CeraLink can be higher than the ambient temperature. Ensure that adjacent components are placed at a sufficient distance from a CeraLink to allow proper cooling.
- Avoid contamination of the CeraLink surface during processing.

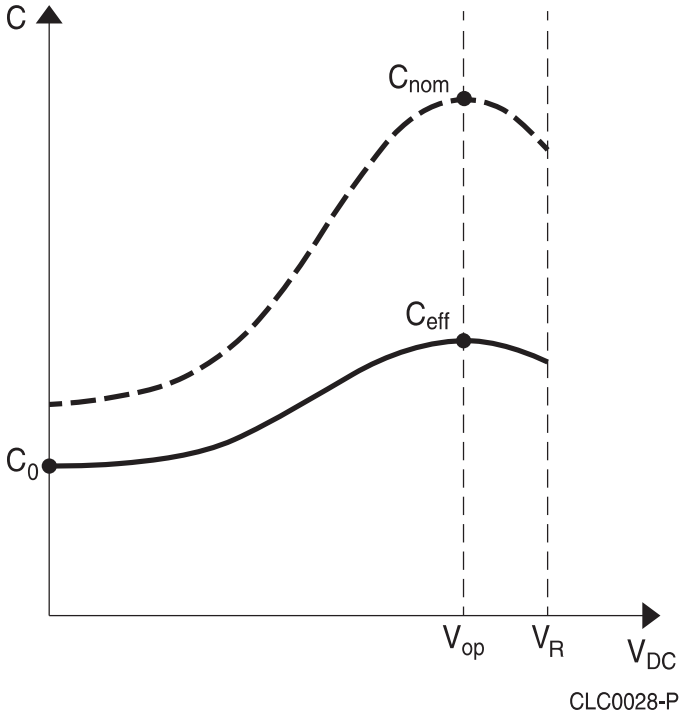
Soldering guidelines

- The use of mild, non-activated fluxes for soldering is recommended, as well as proper cleaning of the PCB (in case of doubt regarding potential chemical intolerances please contact TDK).
- Complete removal of flux is recommended to avoid surface contamination that can result in an instable and/or high leakage current.
- Use resin-type or non-activated flux.
- Bear in mind that insufficient preheating may cause ceramic cracks.
- Rapid cooling by dipping in solvent is not recommended, otherwise a component may crack.
- Excessive usage of solder paste can reduce the mechanical robustness of the device, whereas insufficient solder may cause the CeraLink to detach from the PCB. Use an adequate amount of solder paste, but on the landing pads only.



- If an unfavorable cleaning fluid is used, flux residue or foreign particles may stick to the CeraLink surface and deteriorate its insulation resistance. Insufficient or improper cleaning of the CeraLink may cause damage to the component.
- Excessive washing like ultrasonic cleaning, can affect the connection between the ceramic chip and the outer electrode. To avoid this, we give the following recommendation:
  - Power: 20 W/l max.
  - Frequency: 40 kHz max.
  - Washing time: 5 minutes max.

Glossary



Initial capacitance C_0:	Is the value at the origin of the hysteresis without any applied direct voltage.
Effective capacitance C_{eff}:	Occurs at V_{op} and is measured with an applied ripple voltage of 0.5 V AC (RMS) and 1 kHz. The CeraLink is designed to have its highest capacitance value at the operating voltage V_{op}.
Nominal capacitance C_{nom}:	Is the value derived by the tangent of the mean hysteresis (as the derivative of the mean hysteresis is C = dQ/dV).

See our *CeraLink Technical Guide* for further details.

Symbols and terms

AC	Alternating current
C_0	Initial capacitance @ 0 V DC, 0.5 V AC (RMS), 1 kHz, +25 °C
$C_{eff, typ}$	Typical effective capacitance @ V_{op}, 0.5 V AC (RMS), 1 kHz, +25 °C
$C_{nom, typ}$	Typical nominal capacitance @ V_{op}, quasistatic, +25 °C. See glossary for definition of the nominal capacitance
DC	Direct current
ESL	Equivalent serial inductance
ESR	Equivalent serial resistance
I_{op}	Operating ripple current, root mean square value of sinusoidal AC current
LP	Low profile
PCB	Printed circuit board
PLZT	Lead lanthanum zirconium titanate
R_{ins}	Insulation resistance @ $V_{pk, max}$, measurement time t = 7 s, +25 °C. For pre- and post-measurements within the scope of the AEC-Q200 reliability tests.
$R_{ins, typ}$	Insulation resistance @ V_{op}, measurement time t ≥ 240 s, +25 °C
SAC	Tin silver copper alloy; lead-free solder paste
T_{amb}	Ambient temperature
Tan δ	Dissipation factor @ 0 V DC, 0.5 V AC (RMS),1 kHz, +25°C
T_{device}	Device temperature. $T_{device} = T_{amb} + \Delta T$ (ΔT defines the self-heating of the device due to applied current).
T_{max}	Max. device temperature, T_{max} = +150°C. Reference temperature for reliability tests
V_{op}	Operating voltage at maximum attenuation capability
V_R	Rated voltage for $T_{device} \leq T_{max}$. Depends on the temperature derating defined on page 4 and can be higher than $V_{R, Tmax}$
$V_{R, Tmax}$	Rated voltage for T_{max}. Reference DC voltage for reliability tests
V AC (RMS)	Root mean square value of sinusoidal AC voltage
$V_{pk, max}$	Maximum peak operating voltage (e.g. voltage overshoots or surge pulses which occur <5% of total component lifecycle). Not for continuous operation.
ΔT	Increase of temperature during operation

Cautions and warnings

General

- Not for use in resonant circuits, where a voltage of alternating polarity occurs.
- Not for AC applications. Consult our local representative for further details.
- If used in snubber circuits, ensure that the sum of all voltages remains at the same polarity.
- Ultimately, it is always the customers' responsibility to check and decide whether this product with the properties described in this data sheet is suitable for use in a specific application in such a way that the risk of a malfunction of the products leading to personal injury or property damage to third parties is excluded.
- Depending on the individual application, CeraLink components are electrically connected to voltages and currents, which are potentially dangerous for life and health of the operator. Installation and operation of CeraLink must be done only by authorized personnel. Ensure proper and safe connections, couplers, and drivers.
- Caution: CeraLink components are highly efficient charge storing devices. Even when disconnected from a supply, the electrical energy content of a loaded component can be high and is held for a long time. Always ensure a complete discharging of the component (e.g. via a 10 kΩ resistor) before handling. Do not discharge by simple short-circuiting, because of the risk of damaging the ceramic.
- Electrical charges can be generated on disconnected components by varying load or temperature. Caution: Discharge a CeraLink before connecting it to a measuring component/electronics, when this component is not sufficiently voltage proved.

  See *Important notes* section for further details.

Design notes

- Consider derating at higher operating temperatures. As a rule, lower temperatures and voltages increase the lifetime of CeraLink devices.
- If steep surge current edges are to be expected, make sure your design is as low-inductive as possible.
- In some cases, the malfunctioning of passive electronic components or failure before the end of their service life cannot be completely ruled out in the current state of the art, even if they are operated as specified. In applications requiring a very high level of operational safety and especially when the malfunction or failure of a passive electronic component could endanger human life or health (e.g. in accident prevention, life-saving systems, or automotive battery line applications such as clamp 30), ensure by suitable design of the application or other measures (e.g. installation of protective circuitry, fuse or redundancy) that no injury or damage is sustained by third parties in the event of such a malfunction or failure.
- Specified values only apply to CeraLink components that have not been subject to prior electrical, mechanical or thermal damage. The use of CeraLink devices in line-to-ground applications is therefore not advisable, and it is only allowed together with safety countermeasures such as thermal fuses.

Operation

- Use CeraLink only within the specified operating temperature range.
- Use CeraLink only within specified voltage and current ranges.
- The CeraLink has to be operated in a dry atmosphere, which must not contain any additional chemical vapors or substances.
- Environmental conditions must not harm the CeraLink. Use the capacitors under normal atmospheric conditions only. A reduction of the oxygen partial pressure to below 1 mbar is not permissible.
- Prevent a CeraLink from contacting liquids and solvents.
- Avoid dewing and condensation.
- During operation, the CeraLink can produce audible noise due to its piezoelectric characteristic.
- CeraLink components are mainly designed for encased applications. Under all circumstances avoid exposure to:
  - direct sunlight
  - rain or condensation
  - steam, saline spray
  - corrosive gases
  - atmosphere with reduced oxygen content

This listing does not claim to be complete, but merely reflects the experience of the manufacturer.

Display of ordering codes for TDK Electronics products

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Important notes

The following applies to all products named in this publication:

1. Some parts of this publication contain **statements about the suitability of our products for certain areas of application**. These statements are based on our knowledge of typical requirements that are often placed on our products in the areas of application concerned. We nevertheless expressly point out **that such statements cannot be regarded as binding statements about the suitability of our products for a particular customer application.** As a rule we are either unfamiliar with individual customer applications or less familiar with them than the customers themselves. For these reasons, it is always ultimately incumbent on the customer to check and decide whether a product with the properties described in the product specification is suitable for use in a particular customer application.
2. We also point out that **in individual cases, a malfunction of electronic components or failure before the end of their usual service life cannot be completely ruled out in the current state of the art, even if they are operated as specified.** In customer applications requiring a very high level of operational safety and especially in customer applications in which the malfunction or failure of an electronic component could endanger human life or health (e.g. in accident prevention or life-saving systems), it must therefore be ensured by means of suitable design of the customer application or other action taken by the customer (e.g. installation of protective circuitry or redundancy) that no injury or damage is sustained by third parties in the event of malfunction or failure of an electronic component.
3. **The warnings, cautions and product-specific notes must be observed.**
4. In order to satisfy certain technical requirements, **some of the products described in this publication may contain substances subject to restrictions in certain jurisdictions (e.g. because they are classed as hazardous)**. Useful information on this will be found in our Material Data Sheets on the Internet (www.tdk-electronics.tdk.com/material). Should you have any more detailed questions, please contact our sales offices.
5. We constantly strive to improve our products. Consequently, **the products described in this publication may change from time to time**. The same is true of the corresponding product specifications. Please check therefore to what extent product descriptions and specifications contained in this publication are still applicable before or when you place an order.

   We also **reserve the right to discontinue production and delivery of products**. Consequently, we cannot guarantee that all products named in this publication will always be available. The aforementioned does not apply in the case of individual agreements deviating from the foregoing for customer-specific products.
6. Unless otherwise agreed in individual contracts, **all orders are subject to our General Terms and Conditions of Supply.**
7. **Our manufacturing sites serving the automotive business apply the IATF 16949 standard.** The IATF certifications confirm our compliance with requirements regarding the quality management system in the automotive industry. Referring to customer requirements and customer specific requirements (“CSR”) TDK always has and will continue to have the policy of respecting individual agreements. Even if IATF 16949 may appear to support the acceptance of unilateral requirements, we hereby like to emphasize that **only requirements mutually agreed upon can and will be implemented in our Quality Management System.** For clarification purposes we like to point out that obligations from IATF 16949 shall only become legally binding if individually agreed upon.

Important notes

8. The trade names EPCOS, CarXield, CeraCharge, CeraDiode, CeraLink, CeraPad, CeraPlas, CSMP, CTVS, DeltaCap, DigiSiMic, FilterCap, FormFit, InsuGate, LeaXield, MediPlas, MiniBlue, MiniCell, MKD, MKK, ModCap, MotorCap, PCC, PhaseCap, PhaseCube, PhaseMod, PhiCap, PiezoBrush, PlasmaBrush, PowerHap, PQSine, PQvar, SIFERRIT, SIFI, SIKOREL, SilverCap, SIMDAD, SiMic, SIMID, SineFormer, SIOV, SurfIND, ThermoFuse, WindCap, XieldCap are **trademarks registered or pending** in Europe and in other countries. Further information will be found on the Internet at www.tdk-electronics.tdk.com/trademarks.

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