MCF8329A Sensorless Field Oriented Control (FOC) Three-phase BLDC Gate Driver

1 Features

- Three-phase BLDC gate driver with integrated sensorless motor control algorithm
  - Code-free single shunt Field Oriented Control
  - Supports up to 1.8 kHz (electrical frequency)
  - Support flux weakening control
  - Forward and reverse windmilling support
  - Analog, PWM, freq., or I^2C based control input
  - Configurable motor startup and stop options
  - Optional closed-loop speed or power or current control or modulation index control
  - 5-point configurable reference profile support
  - Anti-voltage surge prevents overvoltage
  - Improved acoustic performance with automatic dead time compensation
  - Support maximum torque per ampere (MTPA)
  - Offline motor back EMF measurement
  - Variable monitoring through DACOUT
- 65-V Three-phase gate driver
  - Drives 3 high-side and 3 low-side N-Channel MOSFETs, 4.5 to 60-V operating voltage
  - Supports 100% PWM duty cycle
  - Bootstrap-based gate driver architecture
  - 1-A/2-A Maximum peak source/sink current
- Integrated current sense amplifier
  - Adjustable gain (5, 10, 20, 40 V/V)
- Low-power sleep mode
  - 5-µA (maximum) at V_{PVDD} = 24-V, T_A = 25°C
- Speed loop accuracy: < 3% with internal clock
- Configurable non-volatile memory (EEPROM) to store device configuration
- Supports up to 75-kHz PWM frequency for low inductance motor support
- Accurate LDO (AVDD) 3.3-V ±3%, 50-mA support with AVDD connected to VREG
- Independent driver shutdown path (DRVOFF)
- Spread spectrum for EMI mitigation
- A suite of integrated protection features
  - Supply under-voltage lockout (UVLO)
  - Motor lock detection (3 different types)
  - Over-current protection (OCP)
  - Thermal shutdown (TSD)
  - Fault condition indication pin (nFAULT)
  - Optional fault diagnostics over I^2C interface

2 Applications

- Brushless-DC (BLDC) Motor Modules
- Cordless Vacuum Cleaners
- Washer and Dishwashers Pumps
- Appliance Fans and Pumps
- Cordless Garden and Power Tools, Lawnmowers

3 Description

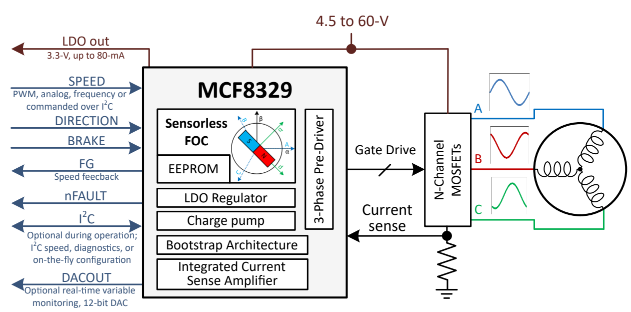
The MCF8329A provides a single-chip, code-free sensorless FOC solution for applications driving brushless-DC motors (BLDC) or Permanent Magnet Synchronous motor (PMSM). The MCF8329A provides three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. The device generates the correct gate drive voltages using an internal charge pump and enhances the high-side MOSFETs using a bootstrap circuit. A trickle charge pump is included to support a 100% duty cycle. The MCF8329A can operate from a single power supply and supports a wide input supply range of 4.5 to 60 V.

The algorithm configuration can be stored in non-volatile EEPROM, which allows the device to operate stand-alone once it has been configured. Motor current is sensed using an integrated current-sensing amplifier supporting a single external shunt resistor. MCF8329A integrates a large number of protection features, intended to protect the device, motor, and system against fault events.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
MCF8329A1IREER	VQFN (36)	5.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2023	*	Initial Release

5 Pin Configuration and Functions

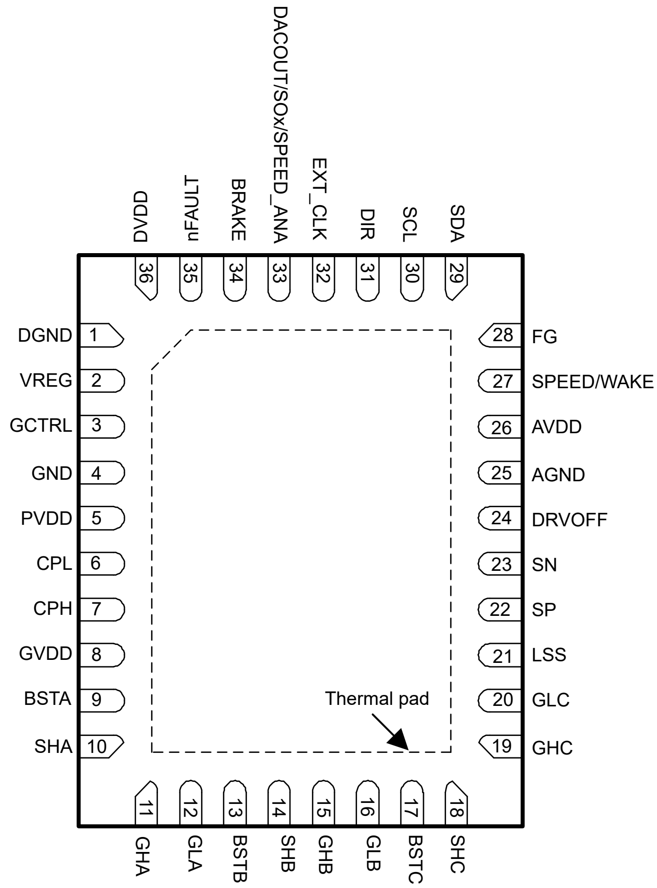

Figure 5-1. MCF8329A 36-Pin VQFN With Exposed Thermal Pad Top View

Table 5-1. Pin Functions

PIN	36-pin Package	TYPE[(1)]	DESCRIPTION
NAME	MCF8329A1I		
AGND	25	GND	Device analog ground
AVDD	26	PWR	3.3-V regulator output. Connect a X5R or X7R, 1-µF, 6.3-V ceramic capacitor between the AVDD and AGND pins. This regulator can source up to 50 mA external (if AVDD shorted to VREG) . TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin.
BRAKE	34	I	High → brake the motor Low → normal operation Connect to GND via 10-kΩ resistor, if not used
BSTA	9	O	Bootstrap output pin. Connect a X5R or X7R, 1-µF, 25-V ceramic capacitor between BSTA and SHA.
BSTB	13	O	Bootstrap output pin. Connect a X5R or X7R, 1-µF, 25-V ceramic capacitor between BSTB and SHB.
BSTC	17	O	Bootstrap output pin. Connect a X5R or X7R, 1-µF, 25-V ceramic capacitor between BSTC and SHC.
CPH	7	PWR	Charge pump switching node. Connect a X5R or X7R, PVDD-rated ceramic capacitor between the CPH and CPL pins. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin.
CPL	6	PWR	

Table 5-1. Pin Functions (continued)

PIN	36-pin Package	TYPE[(1)]	DESCRIPTION
NAME	MCF8329A1I		
DACOUT/SOx/SPEED_ANA	33	I/O	Multipurpose pin. Configurable as DAC output, current sense amplifier output or analog reference input.
DGND	1	GND	Device digital ground
DIR	31	I	Direction of motor spinning; When low, phase driving sequence is OUT A → OUT C → OUT B When high, phase driving sequence is OUT A → OUT B → OUT C Connect to GND via 10-kΩ resistor, if not used
DRVOFF	24	I	Independent driver shutdown path. Pulling DRVOFF high turns off all external MOSFETs by putting the gate drivers into the pull-down state. This signal bypasses and overrides the digital and control core.
DVDD	36	PWR	1.5-V internal regulator output. Connect a X5R or X7R, 1-µF, 6.3-V ceramic capacitor between the DVDD and DGND pins.
EXT_CLK	32	I	External clock reference input in external clock reference mode.
FG	28	O	Motor speed indicator output. Open-drain output requires an external pull-up resistor to 1.8 to 5-V. External pull up resistor needs to be connected even if the pin functionality is not used.
GCTRL	3	O	Gate control for external MOSFET used as regulator to supply current to digital subsystem through VREG pin. This functionality helps to reduce power dissipation inside the device.
GHA	11	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET
GHB	15	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET
GHC	19	O	High-side gate driver output. Connect to the gate of the high-side power MOSFET
GLA	12	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET
GLB	16	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET
GLC	20	O	Low-side gate driver output. Connect to the gate of the low-side power MOSFET
GND	4	GND	Device power ground
GVDD	8	PWR	Gate driver power supply output. Connect a X5R or X7R, 30-V rated ceramic ≥ 10-uF local capacitance between the GVDD and GND pins. TI recommends a capacitor value of >10x C_{BSTx} and voltage rating at least twice the normal operating voltage of the pin.
LSS	21	PWR	Low side source pin, connect all sources of the external low-side MOSFETs here. This pin is the sink path for the low-side gate driver, and serves as an input to monitor the low-side MOSFET VDS voltage and VSEN_OCP voltage.
nFAULT	35	O	Fault indicator. This pin is pulled logic-low with fault condition. Open-drain output requires an external pull-up resistor to 1.8V to 5 V. External pull up resistor needs to be connected even if the pin functionality is not used.
PVDD	5	PWR	Gate driver power supply input. Connect to the bridge power supply. Connect a X5R or X7R, 0.1- µF, >2x PVDD-rated ceramic and >10-uF local capacitance between the PVDD and GND pins. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the pin.
SCL	30	I	I^2C clock input
SDA	29	I/O	I^2C data line
SHA	10	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SHB	14	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SHC	18	I/O	High-side source pin. Connect to the high-side power MOSFET source. This pin is an input for the VDS monitor and the output for the high-side gate driver sink.
SN	23	I	Current sense amplifier input. Connect to the low-side of the current shunt resistor.

Table 5-1. Pin Functions (continued)

PIN	36-pin Package	TYPE[1]	DESCRIPTION
NAME	MCF8329A1I		
SP	22	I	Low-side current shunt amplifier input. Connect to the low-side power MOSFET source and high-side of the current shunt resistor.
SPEED/ WAKE	27	I	Multifunction input. Device sleep/wake input. Device control input; supports analog, PWM or frequency based reference (speed or power or current or modulation index) input.
VREG	2	PWR	Voltage regulator input supply for internal DVDD LDO. Connect to AVDD or external 3-5.5 V. Connect a X5R or X7R, 1-µF, 6.3-V ceramic capacitor between the VREG and DGND pins.
Thermal pad	-	PWR	Must be connected to ground

(1) I = input, O = output, GND = ground pin, PWR = power, NC = no connect

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply pin voltage	PVDD	-0.3	65	V
Bootstrap pin voltage	BSTx	-0.3	80	V
Bootstrap pin voltage	BSTx with respect to SHx	-0.3	20	V
Bootstrap pin voltage	BSTx with respect to GHx	-0.3	20	V
Charge pump pin voltage	CPL, CPH	-0.3	V_{GVDD}	V
Voltage difference between ground pins	GND, DGND, AGND	-0.3	0.3	V
Voltage regulator pin voltage (VREG)	VREG	-0.3	6	V
Gate control pin voltage (GCTRL)	GCTRL	-0.3	7	V
Gate driver regulator pin voltage	GVDD	-0.3	20	V
Digital regulator pin voltage	DVDD	-0.3	1.7	V
Analog regulator pin voltage	AVDD	-0.3	4	V
Logic pin voltage	BRAKE, DRVOFF, DIR, EXT_CLK, SCL, SDA, SPEED/WAKE, DACOUT/SOx/SPEED_ANA	-0.3	6	V
Open drain pin output voltage	nFAULT, FG	-0.3	6	V
High-side gate drive pin voltage	GHx	-8	80	V
Transient 500-ns high-side gate drive pin voltage	GHx	-10	80	V
High-side gate drive pin voltage	GHx with respect to SHx	-0.3	20	V
High-side source pin voltage	SHx	-8	70	V
Transient 500-ns high-side source pin voltage	SHx	-10	72	V
Low-side gate drive pin voltage	GLx with respect to LSS	-0.3	20	V
Transient 500-ns low-side gate drive pin voltage(2)	GLx with respect to LSS	-1	20	V
Low-side gate drive pin voltage	GLx with respect to GVDD		0.3	V
Transient 500-ns low-side gate drive pin voltage	GLx with respect to GVDD		1	V
Low-side source sense pin voltage	LSS	-1	1	V
Transient 500-ns low-side source sense pin voltage	LSS	-10	8	V
Gate drive current	GHx, GLx	Internally Limited	Internally Limited	A
Shunt amplifier input pin voltage	SN, SP	-1	1	V
Transient 500-ns shunt amplifier input pin voltage	SN, SP	-10	8	V
Ambient temperature, T_A		–40	125	°C
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
(2) Supports upto 5A for 500 nS when GLx-LSS is negative

6.2 ESD Ratings Comm

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{PVDD}	Power supply voltage	PVDD	4.5		60	V
V_{PVDD_RAMP}	Power supply voltage ramp rate at power up	PVDD			30	V/us
V_{BST}	Bootstrap pin voltage with respect to SHx	SPEED/WAKE = High, Outputs are switching	4		20	V
I_{AVDD} (1)	Regulator external load current (AVDD connected to VREG)	AVDD			50	mA
$I_{TRICKLE}$	Trickle charge pump external load current	BSTx			2	µA
V_{VREG}	VREG pin voltage	VREG	2.2		5.5	V
V_{IN}	Logic input voltage	BRAKE, DRVOFF, DIR, EXT_CLK, SPEED/WAKE, SDA, SCL	0		5.5	V
f_{PWM}	PWM frequency		0		75	kHz
V_{OD}	Open drain pullup voltage	FG, nFAULT			5.5	V
I_{OD}	Open drain output current	nFAULT			-10	mA
I_{GS} (1)	Total average gate-drive current (Low Side and High Side Combined)	I_{GHx}, I_{GLx}			30	mA
V_{SHSL}	Slew Rate on SHx pins				4	V/ns
C_{BOOT}	Capacitor between BSTx and SHx				4.7(2)	µF
C_{GVDD}	Capacitor between GVDD and GND				130	µF
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed
(2) Current flowing through boot diode (DBOOT) needs to be limited for C_{BSTx} > 4.7µF.

6.4 Thermal Information 1pkg

THERMAL METRIC(1)		MCF8329A	UNIT
		REE (VQFN)	
		36	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (PVDD, GVDD, AVDD, DVDD, VREG, GCTRL)						
I_{PVDDQ}	PVDD sleep mode current	V_{PVDD} = 24V, $V_{SPEED/WAKE}$ = 0, T_A = 25 °C, AVDD connected to VREG		3	5	µA
		$V_{SPEED/WAKE}$ = 0, T_A = 125 °C, AVDD connected to VREG		3.5	6	µA
I_{PVDDS}	PVDD standby mode current	V_{PVDD} = 24 V, $V_{SPEED/WAKE}$ < V_{EN_SB}, DRVOFF = LOW, T_A = 25 °C, AVDD connected to VREG		25	28	mA
		$V_{SPEED/WAKE}$ < V_{EN_SB} , DRVOFF = LOW, AVDD connected to VREG		25	28	mA
I_{PVDD}	PVDD active mode current	V_{PVDD} = 24 V, $V_{SPEED/WAKE}$ > V_{EX_SL}, PWM_FREQ_OUT = 0011b (25 kHz), T_J = 25 °C, No FETs and motor connected, AVDD connected to VREG		28	30	mA
		V_{PVDD} = 24 V, $V_{SPEED/WAKE}$ > V_{EX_SL}, PWM_FREQ_OUT = 0011b (25 kHz), No FETs and motor connected, AVDD connected to VREG		28	30	mA
		V_{PVDD} = 8 V, $V_{SPEED/WAKE}$ > V_{EX_SL}, PWM_FREQ_OUT = 0011b (25 kHz), T_J = 25 °C, No FETs and motor connected, AVDD not connected to VREG, VREG = 3.3V external		8.5	14.1	mA
		V_{PVDD} = 24 V, $V_{SPEED/WAKE}$ > V_{EX_SL}, PWM_FREQ_OUT = 0011b (25 kHz), No FETs and motor connected, AVDD not connected to VREG, VREG = 3.3V external		8.5	11.1	mA
I_{VREG}	VREG pin active mode current	$V_{SPEED/WAKE}$ > V_{EX_SL}, PWM_FREQ_OUT = 0011b (25 kHz), VREG connected to AVDD			25	mA
IL_{BSx}	Bootstrap pin leakage current	V_{BSTx} = V_{SHx} = 60V, V_{GVDD} = 0V, $V_{SPEED/WAKE}$ = LOW	5	10	16	µA
IL_{BS_TRAN}	Bootstrap pin active mode transient leakage current	GLx = GHx = Switching at 20kHz, No FETs connected	60	115	300	µA
V_{GVDD_RT}	GVDD Gate driver regulator voltage (Room Temperature)	V_{PVDD} ≥ 40 V, I_{GS} = 10 mA, T_J= 25°C	11.8	13	15	V
		22 V ≤V_{PVDD} ≤ 40 V, I_{GS} = 30 mA, T_J= 25°C	11.8	13	15	V
		8 V ≤V_{PVDD} ≤ 22 V, I_{GS} = 30 mA, T_J= 25°C	11.8	13	15	V
		6.75 V ≤V_{PVDD} ≤ 8 V, I_{GS} = 10 mA, T_J= 25°C	11.8	13	14.5	V
		4.5 V ≤V_{PVDD} ≤ 6.75 V, I_{GS} = 10 mA, T_J= 25°C	2*V_{PVDD} - 1		13.5	V
V_{GVDD}	GVDD Gate driver regulator voltage	V_{PVDD} ≥ 40 V, I_{GS} = 10 mA	11.5		15.5	V
		22 V ≤V_{PVDD} ≤ 40 V, I_{GS} = 30 mA	11.5		15.5	V
		8 V ≤V_{PVDD} ≤ 22 V; I_{GS} = 30 mA	11.5		15.5	V
		6.75 V ≤V_{PVDD} ≤ 8 V, I_{GS} = 10 mA	11.5		14.5	V
		4.5 V ≤V_{PVDD} ≤ 6.75 V, I_{GS} = 10 mA	2*V_{PVDD} - 1.4		13.5	V

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{AVDD_RT}	AVDD Analog regulator voltage (Room Temperature)	V_{PVDD} ≥ 6 V, 0 mA ≤ I_{AVDD} ≤ 30 mA, T_J= 25°C	3.26	3.3	3.33	V
		V_{PVDD} ≥ 6 V, 30 mA ≤ I_{AVDD} ≤ 80 mA, T_J= 25°C	3.2	3.3	3.4	V
		V_{PVDD} ≤ 6 V, 0 mA ≤ I_{AVDD} ≤ 50 mA, T_J= 25°C	3.13	3.3	3.46	V
V_{DVDD}	Digital regulator voltage	VREG = 3.3V	1.4	1.55	1.65	V
V_{AVDD}	AVDD Analog regulator voltage	V_{PVDD} ≥ 6 V, 0 mA ≤ I_{AVDD} ≤ 80 mA	3.2	3.3	3.4	V
		V_{PVDD} ≤ 6 V, 0 mA ≤ I_{AVDD} ≤ 50 mA	3.125	3.3	3.5	V
V_{GCTRL}	Gate control volatge	V_{PVDD} > 4.5 V	4.9	5.7	6.5	V
GATE DRIVERS (GHx, GLx, SHx, SLx)						
V_{GSHx_LO}	High-side gate drive low level voltage	I_{GHx} = -100 mA; V_{GVDD} = 12V; No FETs connected	0.05	0.11	0.24	V
V_{GSHx_HI}	High-side gate drive high level voltage (V_{BSTx} - V_{GHx})	I_{GHx} = 100 mA; V_{GVDD} = 12V; No FETs connected	0.28	0.44	0.82	V
V_{GSLx_LO}	Low-side gate drive low level voltage	I_{GLx} = -100 mA; V_{GVDD} = 12V; No FETs connected	0.05	0.11	0.27	V
V_{GSLx_HI}	Low-side gate drive high level voltage (V_{GVDD} - V_{GLx})	I_{GLx} = 100 mA; V_{GVDD} = 12V; No FETs connected	0.28	0.44	0.82	V
$R_{DS(ON)\_PU\_HS}$	High-side pullup switch resistance	I_{GHx} = 100 mA; V_{GVDD}= 12V	2.7	4.5	8.4	Ω
$R_{DS(ON)\_PD\_HS}$	High-side pulldown switch resistance	I_{GHx} = 100 mA; V_{GVDD} = 12V	0.5	1.1	2.4	Ω
$R_{DS(ON)\_PU\_LS}$	Low-side pullup switch resistance	I_{GLx} = 100 mA; V_{GVDD} = 12V	2.7	4.5	8.3	Ω
$R_{DS(ON)\_PD\_LS}$	Low-side pulldown switch resistance	I_{GLx} = 100 mA; V_{GVDD} = 12V	0.5	1.1	2.8	Ω
I_{DRIVEP_HS}	High-side peak source gate current	V_{GSHx} = 12V	550	1000	1575	mA
I_{DRIVEN_HS}	High-side peak sink gate current	V_{GSHx} = 0V	1150	2000	2675	mA
I_{DRIVEP_LS}	Low-side peak source gate current	V_{GSLx} = 12V	550	1000	1575	mA
I_{DRIVEN_LS}	Low-side peak sink gate current	V_{GSLx} = 0V	1150	2000	2675	mA
R_{PD_LS}	Low-side passive pull down	GLx to LSS	80	100	120	kΩ
R_{PDSA_HS}	High-side semiactive pull down	GHx to SHx, V_{GSHx} = 2V	8	10	12.5	kΩ
BOOTSTRAP DIODES						
V_{BOOTD}	Bootstrap diode forward voltage	I_{BOOT} = 100 µA			0.8	V
		I_{BOOT} = 100 mA			1.6	V
R_{BOOTD}	Bootstrap dynamic resistance ($\Delta V_{BOOTD}/\Delta I_{BOOT}$)	I_{BOOT} = 100 mA and 50 mA	4.5	5.5	9	Ω
LOGIC-LEVEL INPUTS (BRAKE, DIR, EXT_CLK, SCL, SDA, SPEED/WAKE)						
V_{IL}	Input logic low voltage	AVDD = 3 to 3.6 V			0.25*AVDD	V
V_{IH}	Input logic high voltage	AVDD = 3 to 3.6 V	0.65*AVDD			V
V_{HYS}	Input hysteresis		50	500	800	mV
I_{IL}	Input logic low current	AVDD = 3 to 3.6 V	-0.15		0.15	µA
I_{IH}	Input logic high current	AVDD = 3 to 3.6 V	-0.3		0.1	µA
R_{PD_SPEED}	Input pulldown resistance	SPEED/WAKE pin To GND	0.6	1	1.4	MΩ
LOGIC-LEVEL INPUTS (DRVOFF)						
V_{IL}	Input logic low voltage				0.8	V
V_{IH}	Input logic high voltage		2.2			V

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{HYS}	Input hysteresis		200	400	650	mV
I_{IL}	Input logic low current	Pin Voltage = 0 V;	-1	0	1	µA
I_{IH}	Input logic high current	Pin Voltage = 5 V;	7	20	35	µA
R_{PD_DRVOFF}	Input pulldown resistance	DRVOFF To GND	100	200	300	kΩ
OPEN-DRAIN OUTPUTS (nFAULT, FG)						
V_{OL}	Output logic low voltage	I_{OD} =-5 mA			0.4	V
I_{OZ}	Output logic high current	V_{OD} = 3.3 V	0		0.5	µA
SPEED INPUT - ANALOG MODE						
V_{ANA_FS}	Analog full-speed voltage		2.95	3	3.05	V
V_{ANA_RES}	Analog voltage resolution			732		µV
SPEED INPUT - PWM MODE						
f_{PWM}	PWM input frequency		0.01		95	kHz
Res_{PWM}	PWM input resolution	f_{PWM} = 0.01 to 0.35 kHz	11	12	13	bits
		f_{PWM} = 0.35 to 2 kHz	12	13	14	bits
		f_{PWM} = 2 to 3.5 kHz	11	11.5	12	bits
		f_{PWM} = 3.5 to 7 kHz	13	13.5	14	bits
		f_{PWM} = 7 to 14 kHz	12	12.5	13	bits
		f_{PWM} = 14 to 29.2 kHz	11	11.5	12	bits
		f_{PWM} = 29.3 to 60 kHz	10	10.5	11	bits
		f_{PWM} = 60 to 95 kHz	8	9	10	bits
SPEED INPUT - FREQUENCY MODE						
f_{PWM_FREQ}	PWM input frequency range	Duty cycle = 50%	3		32767	Hz
SLEEP MODE						
V_{EN_SL}	Analog voltage to enter sleep mode	SPEED_MODE = 00b (analog mode)			40	mV
V_{EX_SL}	Analog voltage to exit sleep mode		2.6			V
t_{DET_ANA}	Time needed to detect wake up signal on SPEED/WAKE pin	SPEED_MODE = 00b (analog mode), $V_{SPEED/WAKE}$ > V_{EX_SL}	0.5	1	1.5	µs
t_{WAKE}	Wakeup time from sleep mode	$V_{SPEED/WAKE}$ > V_{EX_SL} to DVDD voltage available, SPEED_MODE = 00b (analog mode)		3	5	ms
$t_{EX\_SL\_DR\_ANA}$	Time taken to drive motor after exiting from sleep mode	SPEED_MODE = 00b (analog mode) $V_{SPEED/WAKE}$ > V_{EX_SL}, ISD detection disabled			30	ms
t_{DET_PWM}	Time needed to detect wake up signal on SPEED pin	SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), $V_{SPEED/WAKE}$ > V_{IH}	0.5	1	1.5	µs
t_{WAKE_PWM}	Wakeup time from sleep mode	$V_{SPEED/WAKE}$ > V_{IH} to DVDD voltage available and release nFault, SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode)		3	5	ms
$t_{EX\_SL\_DR\_PWM}$	Time taken to drive motor after wakeup from sleep state	SPEED_MODE = 01b (PWM mode) $V_{SPEED/WAKE}$ > V_{IH}, ISD detection disabled			30	ms
$t_{DET\_SL\_ANA}$	Time needed to detect sleep command	SPEED_MODE = 00b (analog mode) $V_{SPEED/WAKE}$ < V_{EN_SL}, SLEEP_ENTRY_TIME = 00b or 01b	0.5	1	2	ms

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DET\_SL\_PWM}$	Time needed to detect sleep command	SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), $V_{SPEED/WAKE}$ < V_{IL}(PWM mode and Frequency mode), SLEEP_ENTRY_TIME = 00b	0.035	0.05	0.065	ms
		SPEED_MODE = 01b (PWM mode), or 11b (Frequency mode), $V_{SPEED/WAKE}$ < V_{IL}(PWM mode and Frequency mode), SLEEP_ENTRY_TIME = 01b	0.14	0.2	0.26	ms
		SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode) or 00b (analog mode), $V_{SPEED/WAKE}$ < V_{IL}(PWM mode and Frequency mode), $V_{SPEED/WAKE}$ < V_{EN_SL} (analog mode), SLEEP_ENTRY_TIME = 10b	14	20	26	ms
		SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode) or 00b (analog mode), $V_{SPEED/WAKE}$ < V_{IL}(PWM mode and Frequency mode), $V_{SPEED/WAKE}$ < V_{EN_SL} (analog mode), SLEEP_ENTRY_TIME = 11b	140	200	260	ms
t_{EN_SL}	Time needed to stop driving motor after detecting sleep command	$V_{SPEED/WAKE}$ < V_{EN_SL} (analog mode) or $V_{SPEED/WAKE}$ < V_{IL} (PWM and frequency mode)		1	2	ms
STANDBY MODE						
$t_{EX\_SB\_DR\_ANA}$	Time taken to drive motor after exiting standby mode	SPEED_MODE = 00b (analog mode) V_{SPEED} > V_{EN_SB}, ISD detection disabled			6	ms
$t_{EX\_SB\_DR\_PWM}$	Time taken to drive motor after exiting standby mode	SPEED_MODE = 01b (PWM mode) V_{SPEED} > V_{IH}, ISD detection disabled			6	ms
$t_{DET\_SB\_ANA}$	Time needed to detect standby mode	SPEED_MODE = 00b (analog mode) V_{SPEED} < V_{EN_SB}	0.5	1	2	ms
$t_{EN\_SB\_PWM}$	Time needed to detect standby command	SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), V_{SPEED} < V_{IL}, SLEEP_ENTRY_TIME = 00b	0.035	0.05	0.065	ms
		SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), V_{SPEED} < V_{IL}, SLEEP_ENTRY_TIME = 01b	0.14	0.2	0.26	ms
		SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), V_{SPEED} < V_{IL}, SLEEP_ENTRY_TIME = 10b	14	20	26	ms
		SPEED_MODE = 01b (PWM mode) or 11b (Frequency mode), V_{SPEED} < V_{IL}, SLEEP_ENTRY_TIME = 11b	140	200	260	ms
$t_{EN\_SB\_DIG}$	Time needed to detect standby mode	SPEED_MODE = 10b (I2C mode), SPEED_CMD = 0		1	2	ms
t_{EN_SB}	Time needed to stop driving motor after detecting standby command	V_{SPEED} < V_{EN_SL} (analog mode) or V_{SPEED} < V_{IL} (PWM mode) or SPEED command = 0 (I2C mode)		1	2	ms
OSCILLATOR						

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{OSCREF}	External clock reference	EXT_CLK_CONFIG = 000b		8		kHz
		EXT_CLK_CONFIG = 001b		16		kHz
		EXT_CLK_CONFIG = 010b		32		kHz
		EXT_CLK_CONFIG = 011b		64		kHz
		EXT_CLK_CONFIG = 100b		128		kHz
		EXT_CLK_CONFIG = 101b		256		kHz
		EXT_CLK_CONFIG = 110b		512		kHz
		EXT_CLK_CONFIG = 111b		1024		kHz
PROTECTION CIRCUITS						
V_{VREG_UVLO}	Regulator input undervoltage lockout (VREG-UVLO)	Supply rising	1.8	1.9	2	V
		Supply falling	1.7	1.8	1.9	V
$V_{VREG\_UVLO\_HYS}$	Regulator UVLO hysteresis	Rising to falling threshold	30	100	160	mV
$t_{VREG\_UVLO\_DEG}$	Regulator UVLO deglitch time			5		µs
V_{DVDD_UVLO}	Digital regulator undervoltage lockout (DVDD-UVLO)	Supply rising	1.2	1.25	1.32	V
V_{DVDD_UVLO}	Digital regulator undervoltage lockout (DVDD-UVLO)	Supply falling	1.25	1.35	1.45	V
V_{PVDD_UV}	PVDD undervoltage lockout threshold	V_{PVDD} rising	4.3	4.4	4.5	V
		V_{PVDD} falling	4	4.1	4.25	
$V_{PVDD\_UV\_HYS}$	PVDD undervoltagelockout hysteresis	Rising to falling threshold	225	265	325	mV
$t_{PVDD\_UV\_DG}$	PVDD undervoltage deglitch time		10	20	30	µs
V_{AVDD_POR}	AVDD supply POR threshold	AVDD rising	2.7	2.85	3.0	V
		AVDD falling	2.5	2.65	2.8	
$V_{AVDD\_POR\_HYS}$	AVDD POR hysteresis	Rising to falling threshold	170	200	250	mV
$t_{AVDD\_POR\_DG}$	AVDD POR deglitch time		7	12	22	µs
V_{GVDD_UV}	GVDD undervoltage threshold	V_{GVDD} rising	7.3	7.5	7.8	V
		V_{GVDD} falling	6.4	6.7	6.9	V
$V_{GVDD\_UV\_HYS}$	GVDD undervoltage hysteresis	Rising to falling threshold	800	900	1000	mV
$t_{GVDD\_UV\_DG}$	GVDD undervoltage deglitch time		5	10	15	µs
V_{BST_UV}	Bootstrap undervoltage threshold	V_{BSTx}- V_{SHx}; V_{BSTx} rising	3.9	4.45	5	V
		V_{BSTx}- V_{SHx}; V_{BSTx} falling	3.7	4.2	4.8	V
$V_{BST\_UV\_HYS}$	Bootstrap undervoltage hysteresis	Rising to falling threshold	150	220	285	mV
$t_{BST\_UV\_DG}$	Bootstrap undervoltage deglitch time		2	4	6	µs

4.5 V ≤ V_{PVDD} ≤ 60 V, –40°C ≤ T_J ≤ 150°C (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{PVDD} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DS_LVL}	V_{DS} overcurrent protection threshold Reference	SEL_VDS_LVL = 0000	0.04	0.06	0.08	V
		SEL_VDS_LVL = 0001	0.09	0.12	0.15	V
		SEL_VDS_LVL = 0010	0.14	0.18	0.23	V
		SEL_VDS_LVL = 0011	0.19	0.24	0.29	V
		SEL_VDS_LVL = 0100	0.23	0.3	0.37	V
		SEL_VDS_LVL = 0101	0.3	0.36	0.43	V
		SEL_VDS_LVL = 0110	0.35	0.42	0.5	V
		SEL_VDS_LVL = 0111	0.4	0.48	0.56	V
		SEL_VDS_LVL = 1000	0.5	0.6	0.7	V
		SEL_VDS_LVL = 1001	0.65	0.8	0.9	V
		SEL_VDS_LVL = 1010	0.85	1	1.15	V
		SEL_VDS_LVL = 1011	1	1.2	1.34	V
		SEL_VDS_LVL = 1100	1.2	1.4	1.58	V
		SEL_VDS_LVL = 1101	1.4	1.6	1.78	V
		SEL_VDS_LVL = 1110	1.6	1.8	2	V
		SEL_VDS_LVL = 1111	1.7	2	2.2	V
V_{SENSE_LVL}	V_{SENSE} overcurrent protection threshold	LSS to GND pin = 0.5V	0.48	0.5	0.52	V
t_{DS_BLK}	V_{DS} overcurrent protection blanking time		0.5	1	2.7	µs
t_{DS_DG}	V_{DS} and V_{SENSE} overcurrent protection deglitch time		1.5	3	5	µs
$t_{SD\_SINK\_DIG}$	DRVOFF peak sink current duration		3	5	7	µs
t_{SD_DIG}	DRVOFF digital shutdown delay		0.5	1.5	2.2	µs
t_{SD}	DRVOFF analog shutdown delay		7	14	21	µs
T_{OTSD}	Thermal shutdown temperature	T_J rising;	160	170	187	°C
T_{HYS}	Thermal shutdown hysteresis		16	20	23	°C
I^2C Serial Interface						
V_{I2C_L}	LOW-level input voltage		-0.5		0.3*AVDD	V
V_{I2C_H}	HIGH-level input voltage		0.7*AVDD		5.5	V
V_{I2C_HYS}	Hysterisis		0.05*AVDD			V
V_{I2C_OL}	LOW-level output voltage	open-drain at 2mA sink current	0		0.4	V
I_{I2C_OL}	LOW-level output current	V_{I2C_OL} = 0.6V			6	mA
I_{I2C_IL}	Input current on SDA and SCL		-10[1]		10[1]	µA
C_i	Capacitance for SDA and SCL				10	pF
t_{of}	Output fall time from V_{I2C_H}(min) to V_{I2C_L}(max)	Standard Mode			250[2]	ns
		Fast Mode			250[2]	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	Fast Mode	0		50[3]	ns
EEPROM						
EE_{Prog}	Programing voltage		1.35	1.5	1.65	V
EE_{RET}	Retention	T_A = 25 ℃		100		Years
		T_J = -40 to 150 ℃	10			Years
EE_{END}	Endurance	T_J = -40 to 150 ℃	1000			Cycles
		T_J = -40 to 85 ℃	20000			Cycles

(1) If AVDD is switched off, I/O pins must not obstruct the SDA and SCL lines.

(2) The maximum tf for the SDA and SCL bus lines (300 ns) is longer than the specified maximum tof for the output stages (250 ns). This allows series protection resistors (Rs) to be connected between the SDA/SCL pins and the SDA/SCL bus lines without exceeding the maximum specified tf.
(3) Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns

6.6 Characteristics of the SDA and SCL bus for Standard and Fast mode

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
Standard-mode						
f_{SCL}	SCL clock frequency		0		100	kHz
t_{HD_STA}	Hold time (repeated) START condition	After this period, the first clock pulse is generated	4			µs
t_{LOW}	LOW period of the SCL clock		4.7			µs
t_{HIGH}	HIGH period of the SCL clock		4			µs
t_{SU_STA}	Set-up time for a repeated START condition		4.7			µs
t_{HD_DAT}	Data hold time (1)	I2C bus devices	0 (2)		(3)	µs
t_{SU_DAT}	Data set-up time		250			ns
t_r	Rise time for both SDA and SCL signals				1000	ns
t_f	Fall time of both SDA and SCL signals (2) (5) (6) (7)				300	ns
t_{SU_STO}	Set-up time for STOP condition		4			µs
t_{BUF}	Bus free time between STOP and START condition		4.7			µs
C_b	Capacitive load for each bus line (8)				400	pF
t_{VD_DAT}	Data valid time (9)				3.45 (3)	µs
t_{VD_ACK}	Data valid acknowledge time (10)				3.45 (3)	µs
V_{nL}	Noise margin at the LOW level	For each connected device (including hysteresis)	0.1*AVDD			V
V_{nh}	Noise margin at the HIGHlevel	For each connected device (including hysteresis)	0.2*AVDD			V
Fast-mode						
f_{SCL}	SCL clock frequency		0		400	KHz
t_{HD_STA}	Hold time (repeated) START condition	After this period, the first clock pulse is generated	0.6			µs
t_{LOW}	LOW period of the SCL clock		1.3			µs
t_{HIGH}	HIGH period of the SCL clock		0.6			µs
t_{SU_STA}	Set-up time for a repeated START condition		0.6			µs
t_{HD_DAT}	Data hold time (1)		0 (2)		(3)	µs
t_{SU_DAT}	Data set-up time		100 (4)			ns
t_r	Rise time for both SDA and SCL signals		20		300	ns
t_f	Fall time of both SDA and SCL signals (2) (5) (6) (7)		20 x (AVDD/ 5.5V)		300	ns
t_{SU_STO}	Set-up time for STOP condition		0.6			µs
t_{BUF}	Bus free time between STOP and START condition		1.3			µs
C_b	Capacitive load for each bus line (8)				400	pF
t_{VD_DAT}	Data valid time (9)				0.9 (3)	µs
t_{VD_ACK}	Data valid acknowledge time (10)				0.9 (3)	µs

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{nL}	Noise margin at the LOW level	For each connected device (including hysteresis)	0.1*AVDD			V
V_{nh}	Noise margin at the HIGHlevel	For each connected device (including hysteresis)	0.2*AVDD			V

(1) t_{HD_DAT} is the data hold time that is measured from the falling edge of SCL, applies to data in transmission and the acknowledge.
(2) A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
(3) The maximum t_{HD_DAT} could be 3.45 μs and .9 μs for Standard-mode and Fast-mode, but must be less than the maximum of t_{VD_DAT} or t_{VD_ACK} by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretched the SCL, the data must be valid by the set-up time before it releases the clock.
(4) A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement t_{SU_DAT} 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)}$ + t_{SU_DAT} = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.
(5) If mixed with HS-mode devices, faster fall times according to Table 10 are allowed.
(6) The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
(7) In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
(8) The maximum bus capacitance allowable may vary from the value depending on the actual operating voltage and frequency of the application.
(9) t_{VD_DAT} = time for data signal from SCL LOW to SDA output (HIGH or LOW, depending on which one is worse).
(10) t_{VD_ACK} = time for Acknowledgement signal from SCL LOW to SDA output (HIGH or LOW, dependging on which one is worse).

6.7 Typical Characteristics

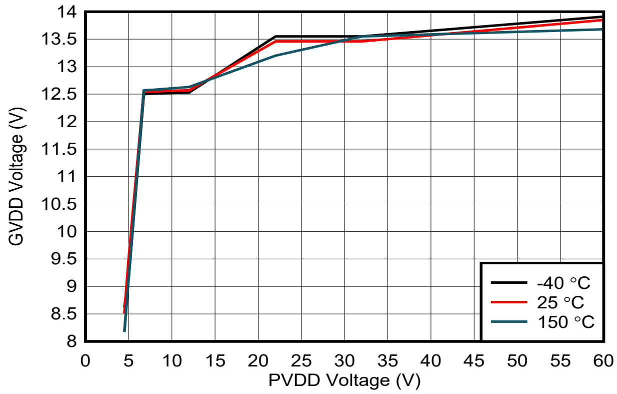

Figure 6-1. GVDD Voltage over PVDD Voltage

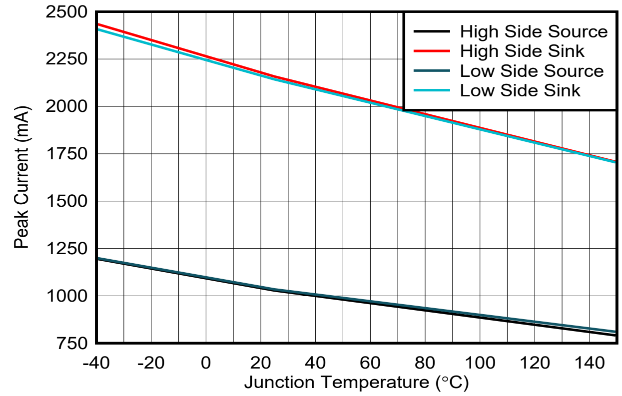

Figure 6-2. Driver Peak Current over Junction Temperature

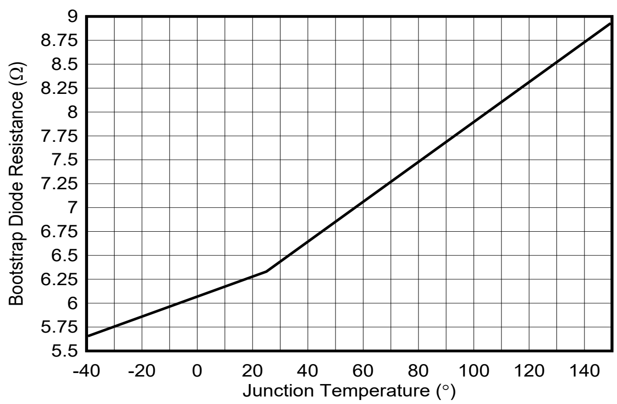

Figure 6-3. Bootstrap Diode Resistance over Junction Temperature

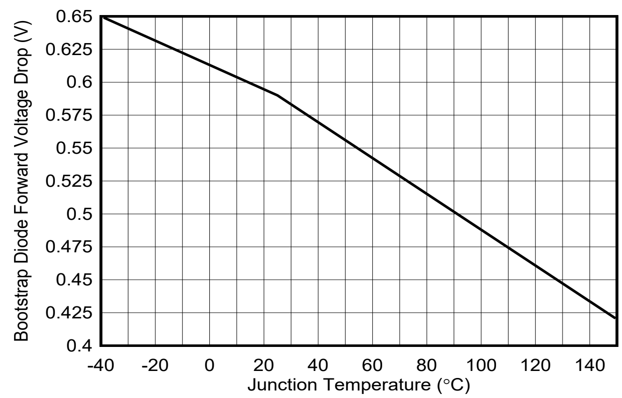

Figure 6-4. Bootstrap Diode Forward Voltage Drop over Junction Temperature

7 Detailed Description

7.1 Overview

The MCF8329A provides a code-free sensorless FOC solution with an integrated three-phase gate driver for driving high-speed brushless-DC motors. Motor current is sensed using an integrated current sensing amplifier with the need for external sense resistors in a single shunt configuration. The device can operate from a single power supply and integrates an LDO that generates the necessary voltage rails for the device and can be used to power external circuits.

MCF8329A implements Sensorless FOC, and so an external microcontroller is not required to spin the brushless DC motor. The algorithm is implemented in a fixed-function state machine, so no coding is needed. The algorithm is highly configurable through register settings ranging from motor start-up behavior to closed-loop operation. Register settings can be stored in non-volatile EEPROM, which allows the device to operate stand-alone once it has been configured. The device allows for high-level monitoring; any variable in the algorithm can be displayed and observed as an analog output via a 12-bit DAC. This feature provides an effective method to tune speed or power loops as well as motor acceleration. The device receives a reference command through a PWM input, analog voltage, frequency input, or I^2C command. The device can be configured to control motor speed (speed control) DC input power (power control) or the quadrature (q-) axis current (current control) or directly the voltage applied (vq and vd) to the motor (modulation index control or open loop voltage control).

In-built protection features include power-supply undervoltage lockout (PVDD_UVLO), regulator undervoltage lockout (GVDD_UV), bootstrap undervoltage lockout (BST_UV), VDS overcurrent protection (OCP), sense resistor overcurrent protection (SEN_OCP), motor lock detection and overtemperature shutdown (OTSD). Fault events are indicated by the nFAULT pin with detailed fault information available in the status registers.

A standard I^2C provides a simple method for configuring the various device settings and reading fault diagnostic information through an external controller.

The MCF8329A device is available in a 0.4-mm pin pitch, VQFN surface-mount package. The VQFN package size is 5 mm × 4 mm.

7.2 Functional Block Diagram

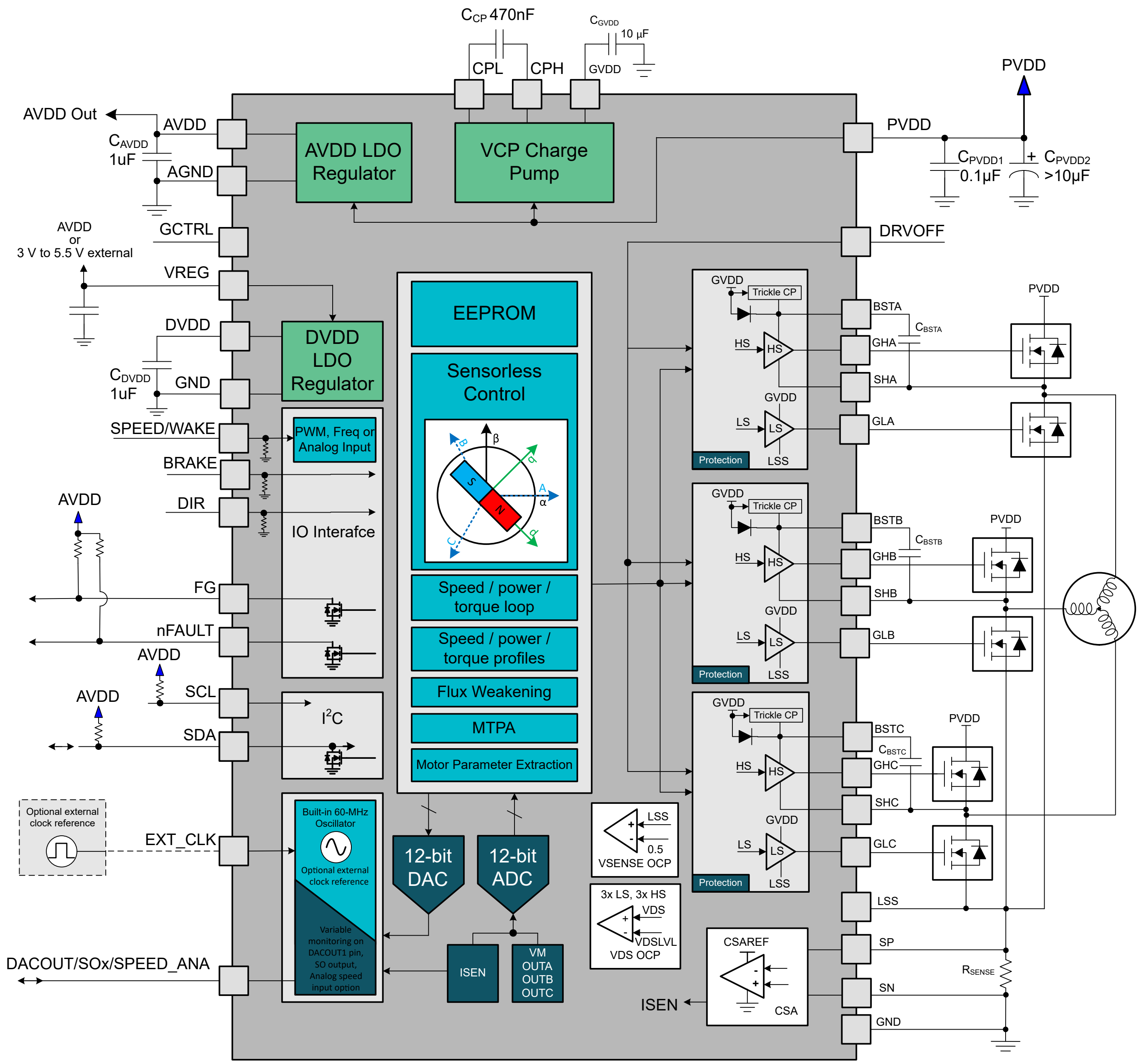

Figure 7-1. MCF8329A Functional Block Diagram

7.3 Feature Description

Table 7-1 lists the recommended values of the external components for the driver.

Table 7-1. MCF8329A External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{PVDD1}	PVDD	PGND	X5R or X7R, 0.1-µF, >2x PVDD-rated capacitor
C_{PVDD2}	PVDD	PGND	≥ 10 µF, >2x PVDD-rated bulk capacitor
C_{CP}	CPH	CPL	X5R or X7R, 470-nF, PVDD-rated capacitor
C_{AVDD}	AVDD	AGND	X5R or X7R, ≥1-µF, 6.3-V capacitor
C_{GVDD}	GVDD	GND	X5R or X7R, ≥10-uF, 30-V-rated capacitor
C_{DVDD}	DVDD	GND	X5R or X7R, 1-µF, ≥ 4-V. In order for DVDD to accurately regulate output voltage, capacitor should have effective capacitance between 0.6-µF to 1.3-µF at 1.5-V across operating temperature.
C_{VREG}	VREG	GND	X5R or X7R, ≥1-µF, 10-V capacitor
C_{BSTx}	BSTx	SHx	X5R or X7R, 1-µF (typical), 25-V-rated capacitor
R_{nFAULT}	1.8 to 5 V Supply	nFAULT	5.1-kΩ, Pullup resistor
R_{FG}	1.8 to 5 V Supply	FG	5.1-kΩ, Pullup resistor
R_{SDA}	1.8 to 5 V Supply	SDA	5.1-kΩ, Pullup resistor
R_{SCL}	1.8 to 5 V Supply	SCL	5.1-kΩ, Pullup resistor
R_{BRAKE}	BRAKE	GND	Optional <10-kΩ resistor for better noise immunity, if BRAKE pin is used
R_{DIR}	DIR	GND	Optional <10-kΩ resistor for better noise immunity, if DIR pin is used

Note

1. The internal pull-up resistor (to AVDD) for both FG and nFAULT pins can be enabled by configuring PULLUP_ENABLE to 1b. Any change to this bit needs to be written to EEPROM followed by a power recycle to take effect. When PULLUP_ENABLE is set to 1b, no external pull-up resistor should be provided.
2. The FG and nFAULT pins needs to be pulled high prior to the device entering active state if the external supply is used with external pull up and with internal pull up disabled.
3. DIR and BRAKE pins each have an internal pull-down resistor of 100-kΩ. When these pins are used, an additional pull-down resistor of 10-kΩ may be added externally for additional noise immunity.
4. SPEED/WAKE pin has an internal pull-down resistor of 1-MΩ. In analog speed input mode, a suitable R-C filter can be added externally to reduce noise. In PWM speed input mode, SPEED_PIN_GLITCH_FILTER can be appropriately configured for glitch rejection.

7.3.1 Three Phase BLDC Gate Drivers

The MCF8329A device integrates three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. A charge pump is used to generate the GVDD to supply the correct gate bias voltage across a wide operating voltage range. The low side gate outputs are driven directly from GVDD, while the high side gate outputs are driven using a bootstrap circuit with an integrated diode, and an internal trickle charge pump provides support for 100% duty cycle operation.

7.3.2 Gate Drive Architecture

The gate driver device uses a complimentary, push-pull topology for both the high-side and low-side drivers. This topology allows for both a strong pullup and pulldown of the external MOSFET gates. The low side gate drivers are supplied directly from the GVDD regulator supply. For the high-side gate drivers, a bootstrap diode and capacitor are used to generate the floating high-side gate voltage supply. The bootstrap diode is integrated and an external bootstrap capacitor is used on the BSTx pin. To support 100% duty cycle control, a trickle charge pump is integrated into the device. The trickle charge pump is connected to the BSTx node to prevent voltage drop due to the leakage currents of the driver and external MOSFET.

The high-side gate driver has a semi-active pull down and low side gate has a passive pull-down to help prevent the external MOSFET from turning ON during sleep state or when the power supply is disconnected.

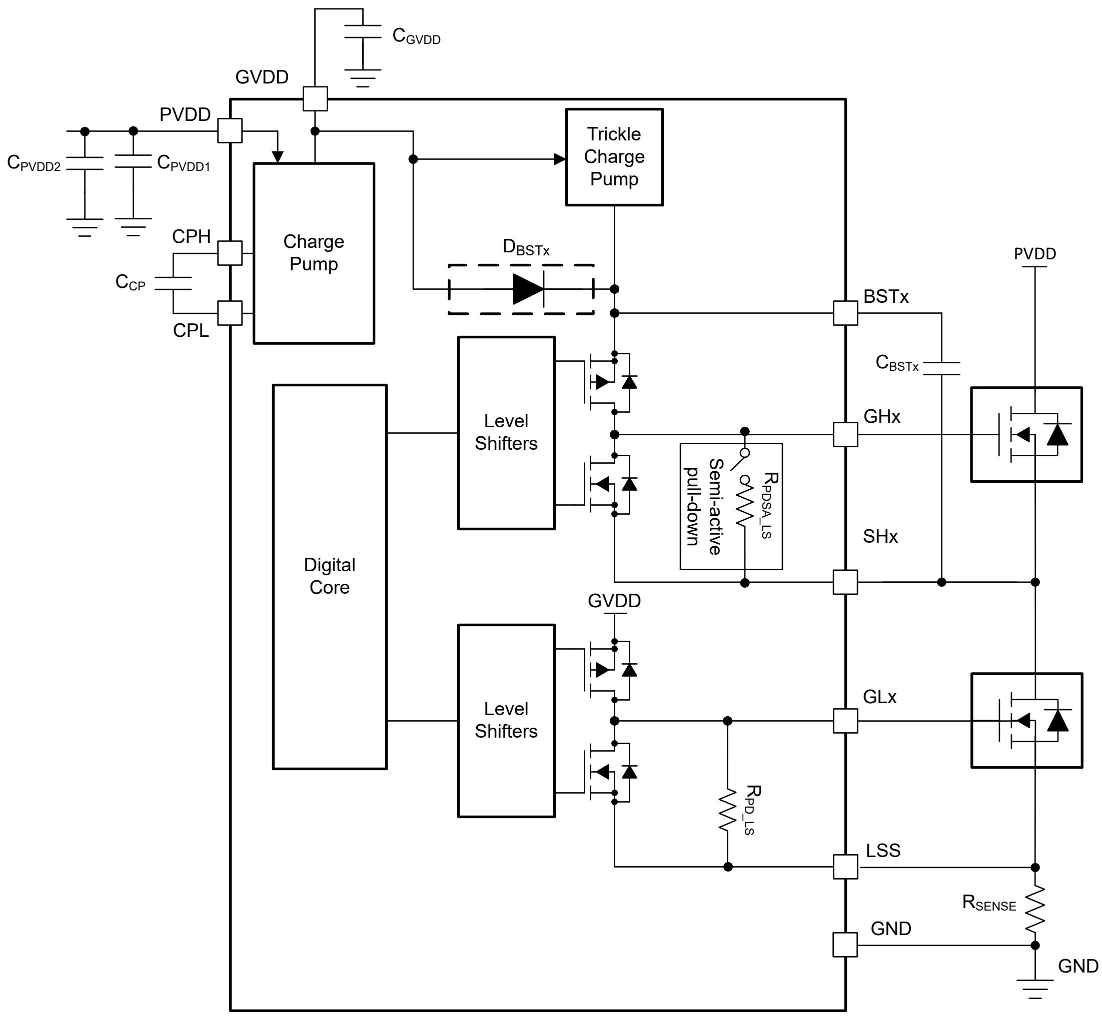

Figure 7-2. Gate Driver Block Diagram

7.3.2.1 Dead time and Cross Conduction Prevention

The MCF8329A provides digital dead time insertion between the high side and low side PWM signals, to prevent both external MOSFETs of each half-bridge from switching on at the same time. Digital dead time can be adjusted between 50 ns and 1000 ns by configuring the EEPROM register DIG_DEAD_TIME.

7.3.3 AVDD Linear Voltage Regulator

A 3.3-V, 80-mA linear regulator is integrated into the MCF8329A and is available for use by external circuitry. If VREG is connected to AVDD, then only 50 mA is available for use by external circuitry. The output of the LDO is fixed to 3.3-V. This regulator can provide the supply voltage for a low-power MCU or other circuitry with low supply current needs. The output of the AVDD regulator should be bypassed near the AVDD pin with an X5R or X7R, 1-µF, 6.3-V ceramic capacitor routed back to the AGND pin.

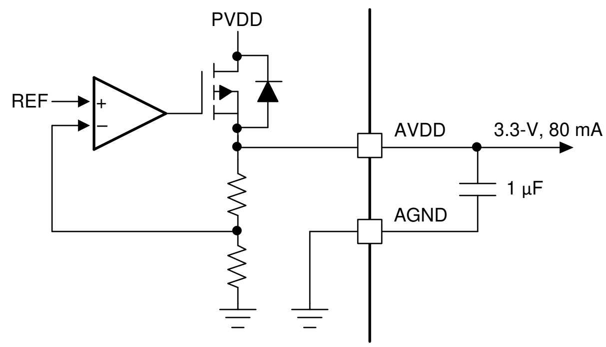

Figure 7-3. AVDD Linear Regulator Block Diagram

The power dissipated in the device by the AVDD linear regulator can be calculated as Equation 1:

$$P = (V_{PVDD} - V_{AVDD}) \times I_{AVDD} \quad (1)$$

For example, at a V_{PVDD} of 24-V, drawing 20-mA out of AVDD results in power dissipation as shown in Equation 2.

$$P = (24\ V - 3.3\ V) \times 20\ mA = 414\ mW \quad (2)$$

7.3.4 DVDD Voltage Regulator

VREG pin is used as the supply input for the integrated DVDD voltage regulator. There are several options available for providing a supply voltage to the VREG pin, either an external 3 V to 5.5 V supply (30 mA source) can be used or AVDD can be connected to VREG or an external MOSFET controlled by GCTRL pin can be used.

7.3.4.1 AVDD Powered VREG

When neither the external MOSFET regulator nor external supply is used, connect AVDD to the VREG pin (see Figure 7-4). In this mode, digital circuitry which are connected to DVDD will be powered using AVDD. In this mode capability of AVDD supporting external load will be reduced to 50 mA.

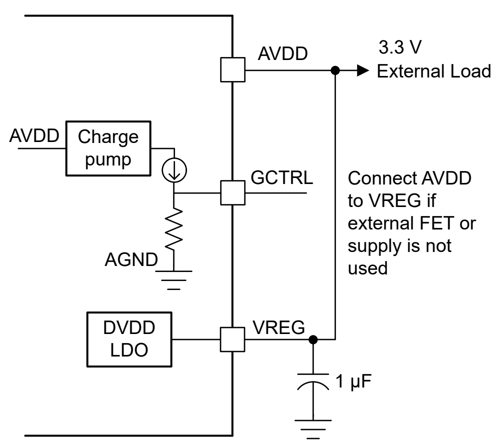

Figure 7-4. AVDD Powering VREG

7.3.4.2 External Supply for VREG

MCF8329A provides provision to connect the external supply voltage to the VREG pin (see Figure 7-5). In this mode, the GCTRL pin should be left floating and the external regulator should be connected to the VREG pin. When external MOSFET or external supply is used to power DVDD then the maximum external load supported by AVDD is 80 mA

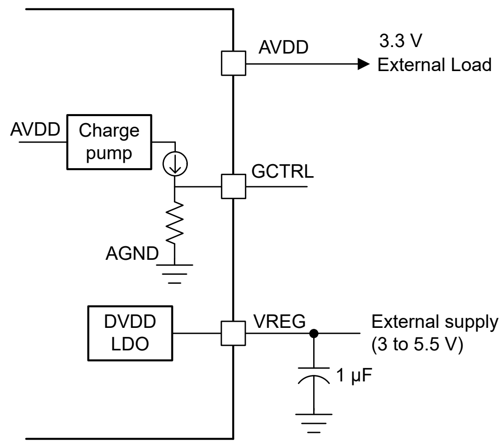

Figure 7-5. External Supply for VREG

7.3.4.3 External MOSFET for VREG Supply

MCF8329A provides option to drive external MOSFET which can act as regulator and can be used to power internal digital circuitry through VREG pin (see Section 7.3.4.3). In this case VREG must not be connected to AVDD or external 3.3 V / 5 V power supply. This option of connecting external MOSFET can be used to reduce power dissipation in MCF8329A and transfer the power loss to the external MOSFET, for use cases that have thermal challenges.

The $V_{GS(th)}$ of external MOSFET has to be selected to ensure that the VREG voltage is between 2.2 V to 5.5 V across operating conditions. Refer toSection 8.2.1for application example design calculations. The input capacitance of external MOSFET need to be less than 2 nF to meet startup time $_{EX\_SL\_DR\_ANA}$(Analog input) or $t_{EX\_SL\_DR\_PWM}$ (PWM input).

Note

The GCTRL pin is a high impedance node (> 1 MΩ) and this pin should not be loaded externally other than the external MOSFET gate and C_{GCTRL}. External loading on GCTRL pin (to GND) reduces the voltage at GCTRL pin and VREG pin.

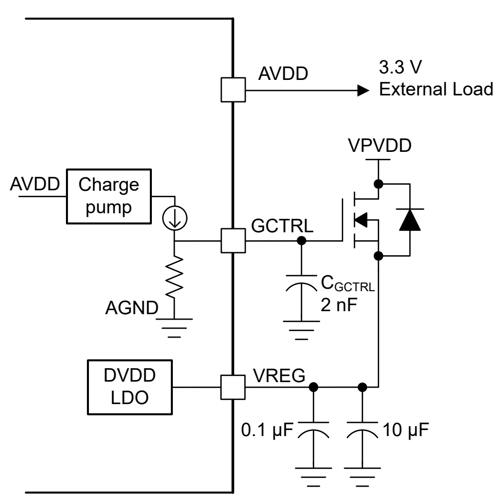

Figure 7-6. External MOSFET Voltage Regulator for VREG

7.3.5 Low-Side Current Sense Amplifier

MCF8329A integrates a high-performance low-side current sense amplifier for current measurements using a low-side shunt resistor. Low-side current measurements are used for multiple control features and protections in

MCF8329A. The current sense amplifiers feature configurable gain (5 V/V, 10 V/V, 20 V/V, and 40 V/V) through EEPROM setting. The current sense amplifier can support sensing bidirectional current through the low-side shunt resistor.

MCF8329A internally generates common mode voltage of $V_{REF}/2$ to obtain maximum resolution for current measurement for both the direction of current. V_{REF} is an internally generated reference voltage having a typical value of 3 V.

Use Equation 3 to design the value of the shunt resistor (R_{SENSE}) connected between SP and SN, for the range of current (I) through the low side single shunt and the selected current sense amplifier gain configured by EEPROM bits CSA_GAIN.

$$R_{SENSE} = \frac{V_{SO} - \frac{V_{REF}}{2}}{CSA\_GAIN \times I} \quad (3)$$

Note

TI recommends designing the shunt resistor R_{SENSE}value to limit the current sense amplifier output voltage (V_{SO}) between 0.25 V and 3 V across the operating range of low-side single shunt resistor current (I) at the selected gain of CSA_GAIN. Appropriately size the shunt resistor power rating based on the I^2R_{SENSE} losses with sufficient margin.

7.3.6 Device Interface Modes

MCF8329A supports the I2C interface to provide end application design suited for either flexibility or simplicity. Along with the I2C interface, the device supports I/O pins like FG, nFAULT, DIR, BRAKE, SPEED/WAKE, DACOUT/SOx/SPEED_ANA, EXT_CLK, DRVOFF. The pinout and interface options are compatible with MCT8329A and let application designers evaluate with one interface version and potentially switch to another control method with minimal modifications to their design.

7.3.6.1 Interface - Control and Monitoring

- **BRAKE**: When BRAKE pin is driven 'High', MCF8329A enters brake state. Brake state is low side braking (see Low-Side Braking). MCF8329A decreases output speed to a value defined by BRAKE_SPEED_THRESHOLD before entering brake state. As long as BRAKE is driven 'High', MCF8329A stays in brake state. Brake pin input can be overwritten by configuring BRAKE_INPUT over the I^2C interface.
- **DIR**: The DIR pin decides the direction of motor spin; when driven 'High', the sequence is OUTA → OUTB → OUTC, and when driven 'Low' the sequence is OUTA → OUTC → OUTB. DIR pin input can be overwritten by configuring DIR_INPUT over the I^2C interface.
- **DRVOFF**: When DRVOFF pin is driven 'High', MCF8329A turns off all external MOSFETs by putting the gate drivers into the pull-down state. When DRVOFF is driven 'Low', MCF8329A returns to normal state of operation, as if restarting the motor. DRVOFF does not cause the device to go to sleep or standby mode; the digital core is still active.
- **SPEED/WAKE**: The SPEED/WAKE pin is used to control motor speed (or power or current or modulation index) and wake up MCF8329A from sleep mode. SPEED/WAKE pin can be configured to accept PWM, frequency or analog control input signals. The pin is used to enter and exit from sleep and standby mode.
- **DACOUT/SOx/SPEED_ANA**: The DACOUT/SOx/SPEED_ANA pin provides a multiplexed functionality and the pin can be configured as a DACOUT output pin or current sense amplifier output pin or as speed (or power or current or open loop voltage) control analog input pin. With the pin DACOUT/SOx/SPEED_ANA configured as DACOUT, the device allows monitoring of algorithm variables, speed etc (see Section 7.5.2) . With the pin DACOUT/SOx/SPEED_ANA configured as SOx, the device allows monitoring of integrated current sense amplifier output (V_{SOx}). With the pin DACOUT/SOx/SPEED_ANA configured as SPEED_ANA enable the user to give analog control input for speed or power or voltage through the DACOUT/SOx/SPEED_ANA pin and in that case the SPEED/WAKE pin can be used as an independent speed or standby control input pin. The pin functionality can be configured through EEPROM register bit DAC_SOX_ANA_CONFIG.

- **EXT_CLK**: The EXT_CLK pin can be used to provide an external clock reference and in that case the internal clock gets calibrated using the external clock.
- **FG**: The FG pin provides pulses which are proportional to motor speed (see Section 7.3.22).
- **nFAULT**: The nFAULT pin provides fault status in device or motor operation.

7.3.6.2 I^2C Interface

The MCF8329A supports an I^2C serial communication interface that allows an external controller to send and receive data. This I^2C interface lets the external controller configure the EEPROM and read detailed fault and motor state information. The I^2C bus is a two-wire interface using the SCL and SDA pins which are described as follows:

- The SCL pin is the clock signal input.
- The SDA pin is the data input and output.

7.3.7 Motor Control Input Options

The MCF8329A offers four ways of controlling the motor:

1. SPEED Control: In speed control mode, the speed of the motor is controlled using a closed loop PI control according to the input reference.
2. POWER Control: In power control mode, the DC input power of the inverter power stage is controlled using a closed loop PI control according to the input reference.
3. CURRENT Control: In current control mode, the torque controlling current (iq) is controlled using a closed loop PI control according to the input reference. In this mode the speed/power control loop is disabled.
4. MODULATION INDEX Control (VOLTAGE Control): In voltage control mode, the voltage applied to the motor is controlled according to the input reference.

The device can accept four types of input reference signal as configured by SPEED_MODE.

- PWM input on SPEED/WAKE pin by varying duty cycle of input signal
- Frequency input on SPEED/WAKE pin by varying frequency of input signal
- Analog input on SPEED/WAKE pin or DACOUT/SOx/SPEED_ANA pin by varying amplitude of input signal
- Over I^2C by configuring DIGITAL_SPEED_CTRL

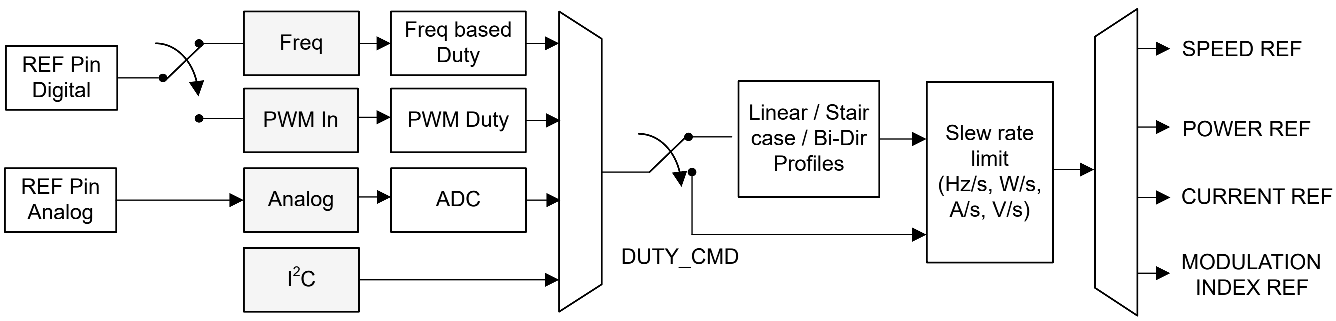

Figure 7-7. Multiplexing the Reference Input Command

The signal path from REF (SPEED/WAKE or DACOUT/SOx/SPEED_ANA) pin input (or I^2C based speed input) to output reference (SPEED REF or POWER REF or CURRENT REF or MODULATION INDEX REF) shown in Figure 7-7.

7.3.7.1 Analog-Mode Motor Control

Analog input based motor control can be configured by setting SPEED_MODE to 00b. In this mode, the duty command (DUTY_CMD) varies with the analog voltage input ($V_{SPEED/WAKE}$) on the SPEED/WAKE pin or DACOUT/SOx/SPEED_ANA pin (configurable via DAC_SOX_ANA_CONFIG). When $0 < V_{SPEED/WAKE} < V_{EN\_SB}$, DUTY_CMD is set to zero. When $V_{EN\_SB} < V_{SPEED/WAKE} < V_{ANA\_FS}$, DUTY_CMD varies linearly with $V_{SPEED/WAKE}$ as shown in Figure 7-8 . When $V_{SPEED/WAKE} > V_{ANA\_FS}$, DUTY_CMD is clamped to 100%.

With DACOUT/SOx/SPEED_ANA pin used as the analog control input, the SLEEP/WAKE pin can be independently used to control the sleep or standby entry and exit as described in Table 7-6.

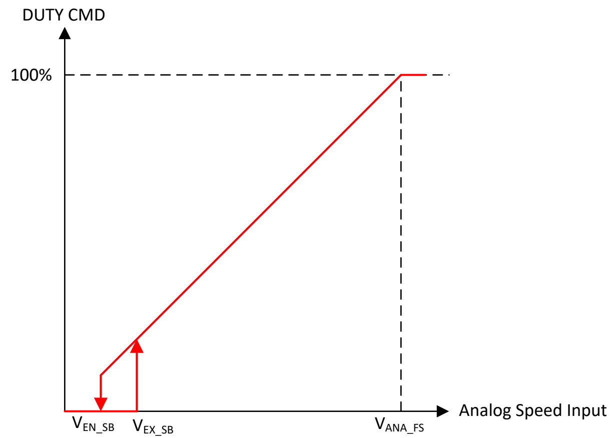

Figure 7-8. Analog-Mode Speed Control

7.3.7.2 PWM-Mode Motor Control

PWM-based motor control can be configured by setting SPEED_MODE to 01b. In this mode, the PWM duty cycle applied to the SPEED/WAKE pin can be varied from 0 to 100%, and duty command (DUTY_CMD) varies linearly with the applied PWM duty cycle. When 0 ≤ $Duty_{SPEED}$ ≤ $Duty_{EN\_SB}$, DUTY_CMD is set to zero. When $Duty_{EX\_SB}$ ≤ $Duty_{SPEED}$ ≤ 100%, DUTY_CMD varies linearly with $Duty_{SPEED}$ as shown in Figure 7-9. $Duty_{EX\_SB}$ and $Duty_{EN\_SB}$ are the standby entry and exit thresholds - refer Section 7.4.1.2 for more information on $Duty_{EX\_SB}$ and $Duty_{EN\_SB}$. The frequency of the PWM input signal applied to the SPEED/WAKE pin is defined as f_{PWM} and the range for this frequency can be configured through SPD_RANGE_SEL.

Note

1. f_{PWM} is the frequency of the PWM signal the device can accept at the SPEED/WAKE pin to control motor speed. It does not correspond to the PWM output frequency that is applied to the motor phases. The PWM output frequency can be configured through PWM_FREQ_OUT (see Section 7.3.17).
2. SLEEP_ENTRY_TIME should be set longer than the off time in the PWM signal ($V_{SPEED/WAKE}$ < V_{IL}) at the lowest duty input. For example, if f_{PWM} is 10 kHz and the lowest duty input is 2%, SLEEP_ENTRY_TIME should be more than 98 μs to ensure there is no unintended sleep/standby entry.

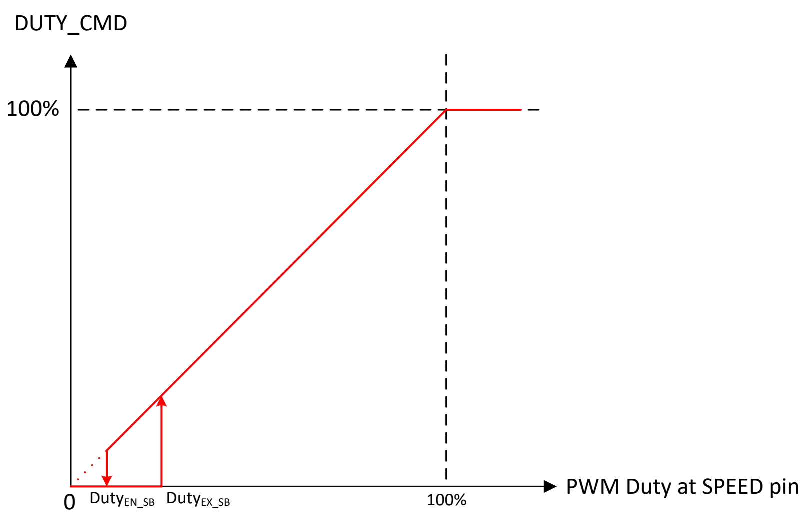

Figure 7-9. PWM-Mode Motor Control

7.3.7.3 Frequency-Mode Motor Control

Frequency-based motor control is configured by setting SPEED_MODE to 11b. In this mode, duty command varies linearly as a function of the frequency of the square wave input at the SPEED (SPEED/WAKE) pin. When $0 \le Freq_{SPEED} \le Freq_{EN\_SB}$, DUTY_CMD is set to zero. When $Freq_{EX\_SB} \le Freq_{SPEED} \le$ INPUT_MAXIMUM_FREQ, DUTY_CMD varies linearly with $Freq_{SPEED}$ as shown in Figure 7-10. $Freq_{EX\_SB}$ and $Freq_{EN\_SB}$ are the standby entry and exit thresholds - refer Section 7.4.1.2 for more information on $Freq_{EX\_SB}$ and $Freq_{EN\_SB}$. Input frequency greater than INPUT_MAXIMUM_FREQ clamps the DUTY_CMD to 100%.

Note

TI recommends a logic low signal on the SPEED/WAKE pin to provide a zero reference in frequency mode control.

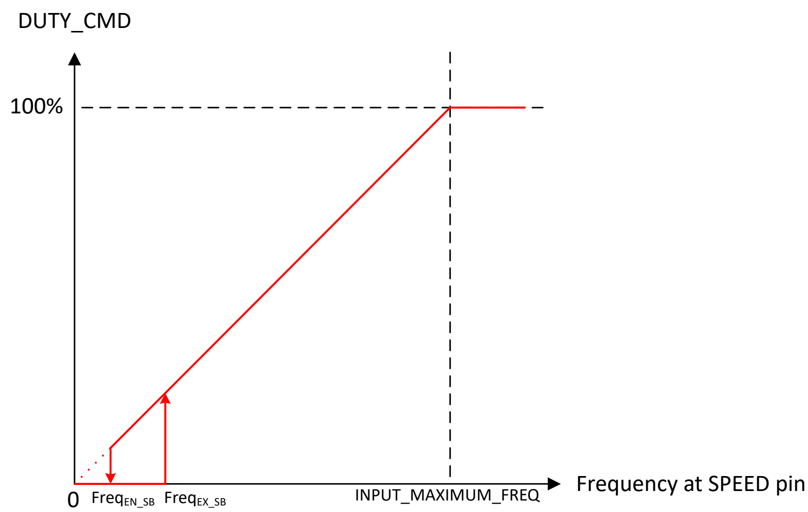

Figure 7-10. Frequency-Mode Motor Control

7.3.7.4 I²C based Motor Control

I²C based serial interface can be used for motor control by setting SPEED_MODE to 10b. In this mode, the duty command can be written directly into DIGITAL_SPEED_CTRL register. The sleep entry and exit are controlled through SLEEP/WAKE as described in Table 7-6.

7.3.7.5 Input Control Reference Profiles

MCF8329A supports three different kinds of profiles (linear, step, forward-reverse) to convert the DUTY_CMD to the reference control signal. The input control reference signal can be motor speed, DC input power, motor current (i_q), or motor voltage (modulation index control) as configured by CTRL_MODE. The different profiles can be configured through REF_PROFILE_CONFIG. When REF_PROFILE_CONFIG is set to 00b, the profiler is not applied and the input reference is the same as the duty command (DUTY_CMD) as explained in Section 7.3.7.6.

In speed control mode, the profiler output REF_X corresponds to the percentage of Maximum Speed (configured by MAX_SPEED) as shown in Equation 4. In power control mode, the profiler output REF_X corresponds to the percentage of Maximum Power (configured by MAX_POWER) as shown in Unable to auto-generate link text. In the current control mode (i_q control) the profiler output REF_X corresponds to the percentage of ILIMIT as shown in Equation 6. In voltage control mode (Modulation index control mode) REF_X corresponds to the percentage of V_d and V_q modulation index applied voltage to the motor.

$$SPEED\ REF(Hz) = \frac{REF\_X}{255} \times Maximum\ Speed\ (Hz) \tag{4}$$

$$POWER\ REF(W) = \frac{REF\_X}{255} \times Maximum\ Power\ (W) \tag{5}$$

$$CURRENT\ (i_q)\ REF(W) = \frac{REF\_X}{255} \times ILIMIT\ (A) \quad (6)$$

$$MODULATION\ INDEX\ REF(V_s) = \frac{REF\_X}{255} \times 100\% \quad (7)$$

When REF_PROFILE_CONFIG is set to 00b, any change in DUTY_CMD by a value less than DUTY_HYS does not produce any change in SPEED REF or POWER REF or CURRENT REF or MODULATION INDEX REF; DUTY_HYS provides a hysteresis window around DUTY_CMD for noise immunity.

7.3.7.5.1 Linear Control Profiles

Note

For all three profiles (linear, step, forward/reverse),

- When MCF8329A is configured as a sleep device, a zero input reference (0-V in analog mode, 0% duty in PWM mode, DIGITAL_SPEED_CTRL = 0b in I2C mode or 0-Hz in frequency mode) will stop the motor.
- When MCF8329A is configured as a standby device, a zero input command will result in motor operating at reference level (speed, power, current or voltage) set by REF_OFF1.

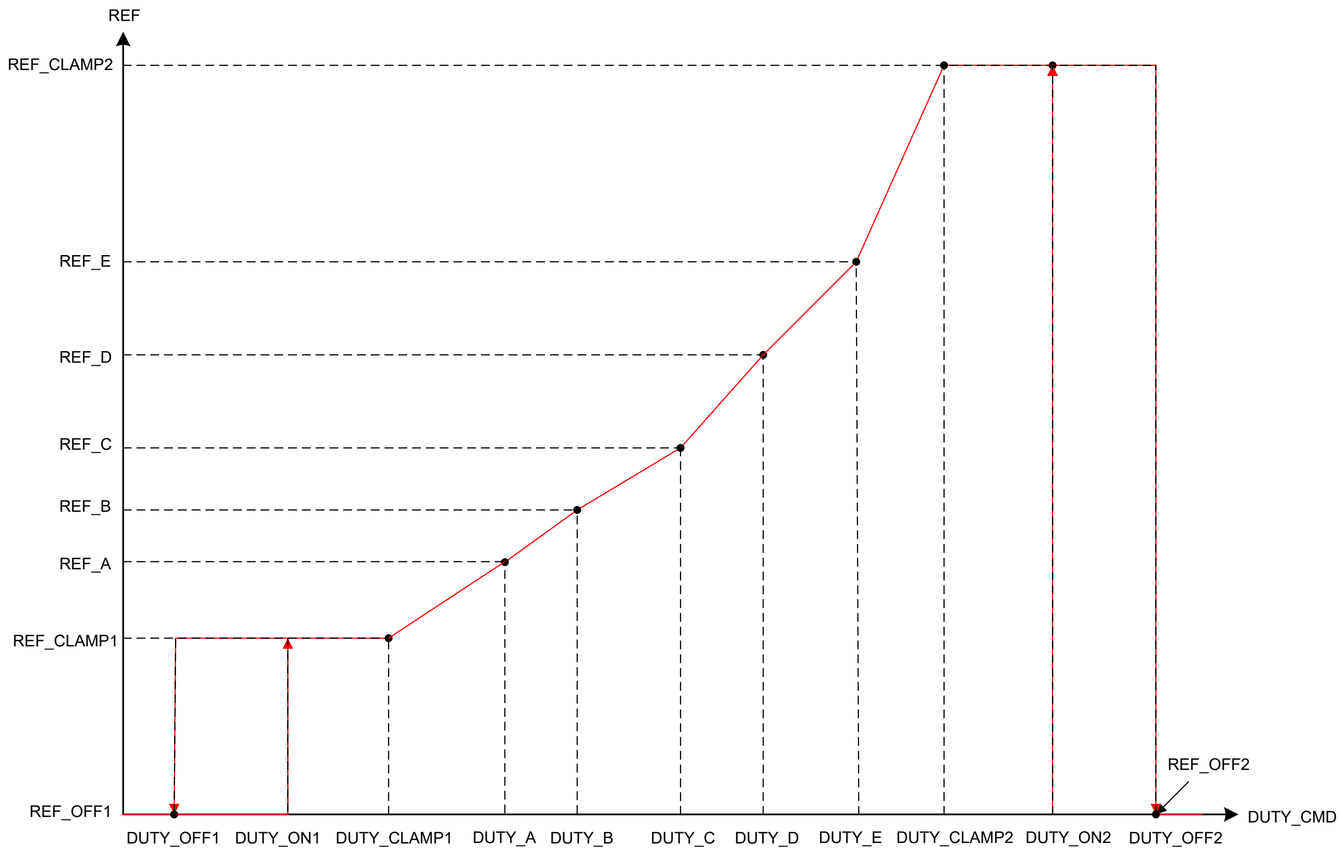

Figure 7-11. Linear Control Profiles

Linear control profiles can be configured by setting REF_PROFILE_CONFIG to 01b. Linear profiles feature input control references which change linearly between REF_CLAMP1 and REF_CLAMP2 with different slopes which can be set by configuring DUTY_x and REF_x combination.

- DUTY_OFF1 configures the duty command below which the reference will be REF_OFF1.

- DUTY_OFF1 and DUTY_ON1configures a hysteresis around reference control input REF_CLAMP1 and REF_OFF1 as shown in Figure 7-11.
- DUTY_CLAMP1 configures the duty command till which reference will be constant with a value REF_CLAMP1. DUTY_CLAMP1 can be placed anywhere between DUTY_OFF1 and DUTY_A.
- DUTY_A configures the duty command for reference REF_A. The reference changes from REF_CLAMP1 to REF_A linearly between DUTY_CLAMP1 and DUTY_A. DUTY_A to DUTY_E has to be in the same order as shown in Figure 7-11.
- DUTY_B configures the duty command for reference REF_B. The reference changes linearly between DUTY_A and DUTY_B.
- DUTY_C configures the duty command for reference REF_C. The reference changes linearly between DUTY_B and DUTY_C.
- DUTY_D configures the duty command for reference REF_D. The reference changes linearly between DUTY_C and DUTY_D.
- DUTY_E configures the duty command for reference REF_E. The reference changes linearly between DUTY_D and DUTY_E.
- DUTY_CLAMP2 configures the duty command above which the reference will be constant at REF_CLAMP2. REF_CLAMP2 configures this constant reference between DUTY_CLAMP2 and DUTY_OFF2 . The reference changes linearly between DUTY_E and DUTY_CLAMP2. DUTY_CLAMP2 can be placed anywhere between DUTY_E and DUTY_OFF2.
- DUTY_OFF2 and DUTY_ON2 configures a hysteresis around reference control input REF_CLAMP2 and REF_OFF2 as shown in Figure 7-11.
- DUTY_OFF2 configures the duty command above which the reference will change from REF_CLAMP2 to REF_OFF2.

7.3.7.5.2 Staircase Control Profiles

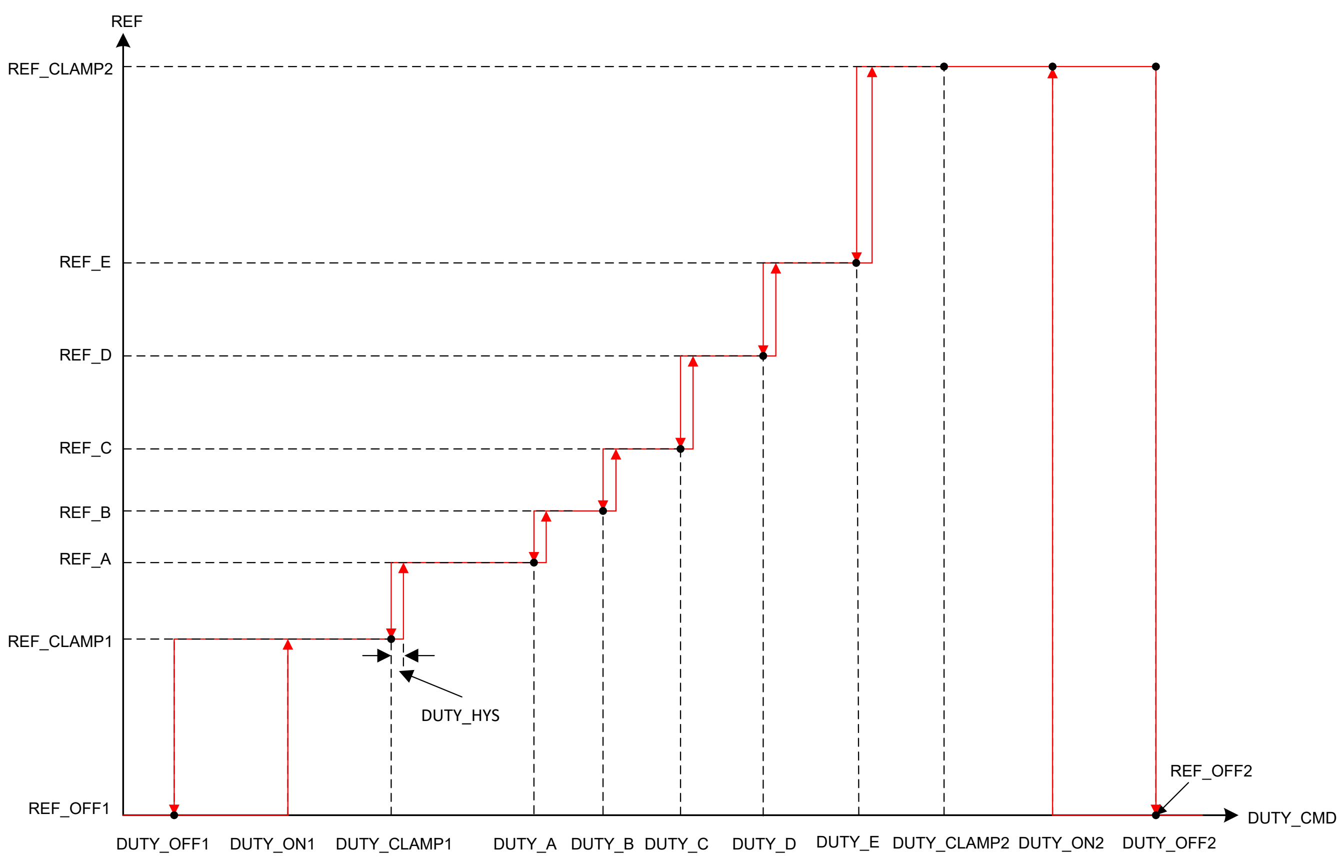

Figure 7-12. Staircase Control Profiles

Staircase control profiles can be configured by setting REF_PROFILE_CONFIG to 10b. Staircase profiles feature input control reference changes in steps between REF_CLAMP1 and REF_CLAMP2, by configuring DUTY_x and REF_x.

- DUTY_OFF1 configures the duty command below which the reference will be REF_OFF1.
- DUTY_OFF1 and DUTY_ON1configures a hysteresis around reference control input REF_CLAMP1 and REF_OFF1 as shown in Figure 7-12.
- DUTY_CLAMP1 configures the duty command till which reference will be constant. REF_CLAMP1 configures this constant reference between DUTY_OFF1 and DUTY_CLAMP1. DUTY_CLAMP1 can be placed anywhere between DUTY_OFF1 and DUTY_A.
- DUTY_A configures the duty command for reference REF_A. There is a step change in reference from REF_CLAMP1 to REF_A at DUTY_CLAMP1. DUTY_A to DUTY_E has to be in the same order as shown in Figure 7-12.
- DUTY_B configures the duty command for reference REF_B. There is a step change in reference from REF_A to REF_B at DUTY_A.
- DUTY_C configures the duty command for reference REF_C. There is a step change in reference from REF_B to REF_C at DUTY_B.
- DUTY_D configures the duty command for reference REF_D. There is a step change in reference from REF_C to REF_D at DUTY_C.
- DUTY_E configures the duty command for reference REF_E. There is a step change in reference from REF_D to REF_E at DUTY_D.
- DUTY_CLAMP2 configures the duty command above which the reference will be constant at REF_CLAMP2. REF_CLAMP2 configures this constant reference between DUTY_CLAMP2 and DUTY_OFF2. There is a step change in reference from REF_E to REF_CLAMP2 at DUTY_E. DUTY_CLAMP2 can be placed anywhere between DUTY_E and DUTY_OFF2.
- DUTY_OFF2 and DUTY_ON2 configures a hysteresis around reference control input REF_CLAMP2 and REF_OFF2 as shown in Figure 7-12.
- DUTY_OFF2 configures the duty command above which the reference will change from REF_CLAMP2 to REF_OFF2.
- DUTY_HYS configures the hysteresis during every step change at DUTY_CLAMP1, DUTY_A to DUTY_E.

7.3.7.5.3 Forward-Reverse Profiles

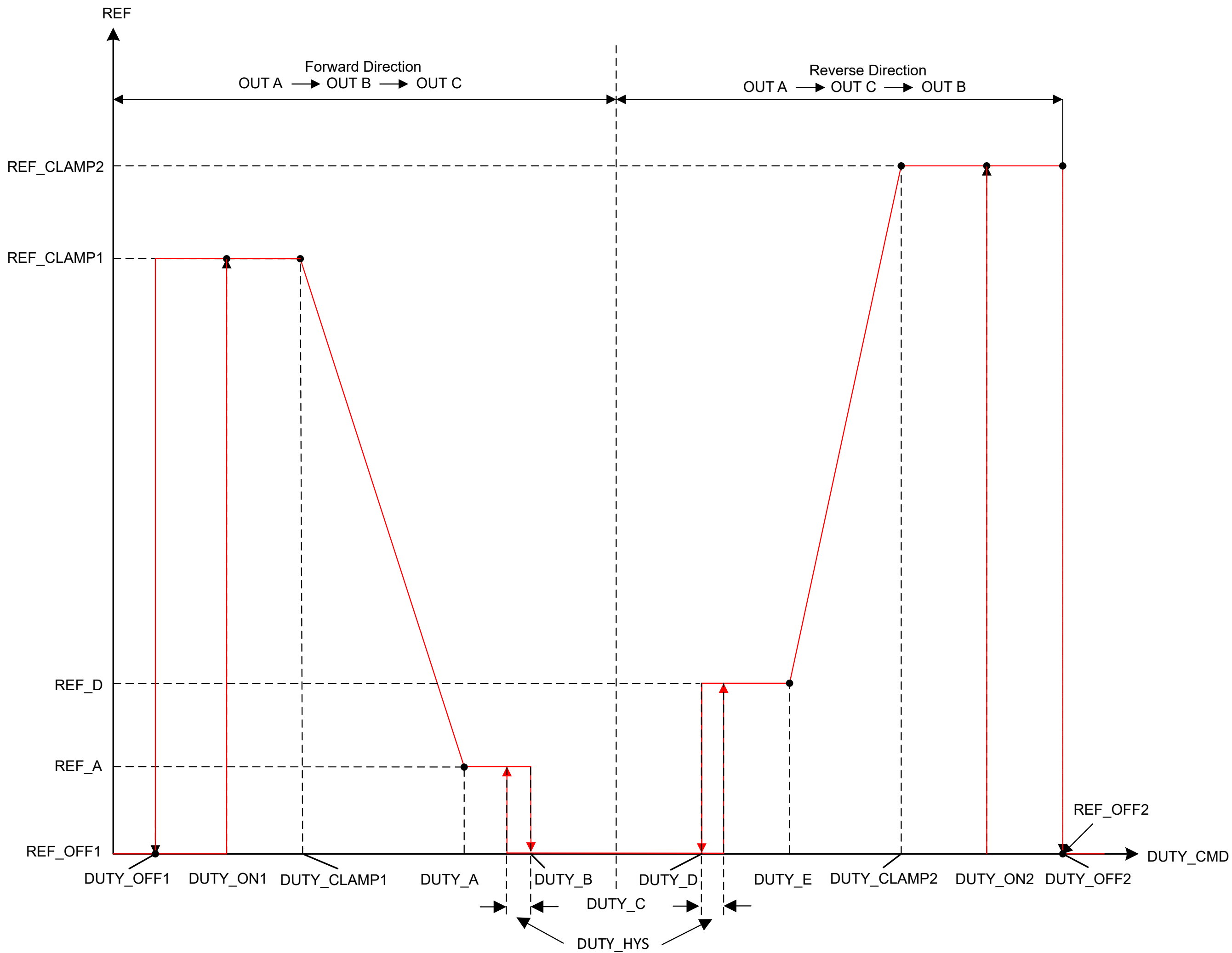

Figure 7-13. Forward Reverse Control Profiles

Forward-Reverse control profiles can be configured by setting REF_PROFILE_CONFIG to 11b. Forward-Reverse profiles feature direction change through adjusting the duty command. DUTY_C configures duty command at which the direction will be changed. The Forward-Reverse speed profile can be used to eliminate the separate signal used to control the motor direction.

Note

The direction change functionality through DIR pin and DIR_INPUT bits are disabled in forward reverse profile mode.

- DUTY_OFF1 configures the duty command below which the reference will be REF_OFF1.
- DUTY_OFF1 and DUTY_ON1configures a hysteresis around reference control input REF_CLAMP1 and REF_OFF1 as shown in Figure 7-13.
- DUTY_CLAMP1 configures the duty command till which reference will be constant. REF_CLAMP1 configures this constant reference between DUTY_OFF1 and DUTY_CLAMP1. DUTY_CLAMP1 can be placed anywhere between DUTY_OFF1 and DUTY_A.
- DUTY_A configures the duty command for reference REF_A. The reference changes linearly between DUTY_CLAMP1 and DUTY_A. DUTY_A to DUTY_E has to be in the same order as shown in Figure 7-13.

- DUTY_B configures the duty command above which MCF8329A will be in off state. The reference remains constant at REF_A between DUTY_A and DUTY_B.
- DUTY_C configures the duty command at which the direction is changed
- DUTY_D configures the duty command above which the MCF8329A will be in running state in the reverse direction. REF_D configures constant reference between DUTY_D and DUTY_E.
- DUTY_E configures the duty command above which reference changes linearly between DUTY_E and DUTY_CLAMP2.
- DUTY_CLAMP2 configures the duty command above which the reference will be constant at REF_CLAMP2. REF_CLAMP2 configures this constant reference between DUTY_CLAMP2 and DUTY_OFF2. DUTY_CLAMP2 can be placed anywhere between DUTY_E and DUTY_OFF2.
- DUTY_OFF2 and DUTY_ON2 configures a hysteresis around reference control input REF_CLAMP2 and REF_OFF2 as shown in Figure 7-13.
- DUTY_OFF2 configures the duty command above which the reference changes in the reverse direction from REF_CLAMP2 to REF_OFF2.
- DUTY_HYS configures the hysteresis during step change at DUTY_B and DUTY_D.

7.3.7.6 Control Input Transfer Function without Profiler

The input control signal can be motor speed, DC input power, motor current (i_q), or motor voltage (modulation index) as configured by CTRL_MODE.

Speed Input Transfer Function

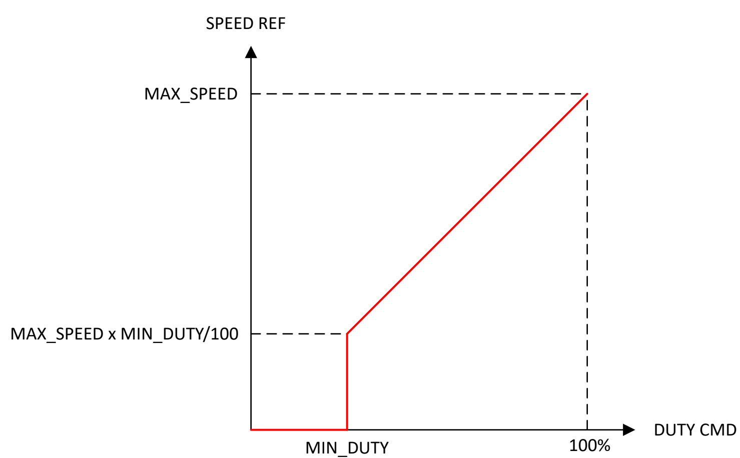

Figure 7-14. Speed Input Transfer Function

Figure 7-14 shows the relationship between DUTY CMD and SPEED REF. When the speed loop is enabled, DUTY CMD sets the SPEED REF in Hz. MAX_SPEED sets the SPEED REF at DUTY CMD of 100%. MIN_DUTY sets the minimum SPEED REF (MIN_DUTY x MAX_SPEED). If MAX_SPEED is set to 0, SPEED REF is clamped to zero (irrespective of DUTY CMD) and the motor is in a stopped state.

Power Input Transfer Function

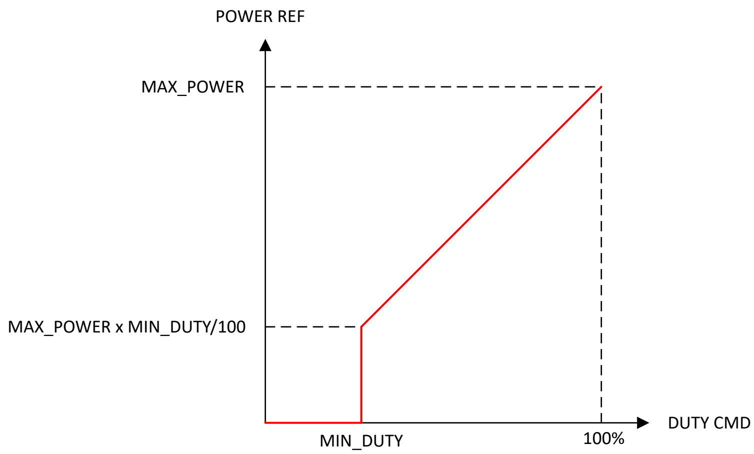

Figure 7-15. Power Input Transfer Function

Figure 7-15 shows the relationship between DUTY CMD and POWER REF. When the power loop is enabled, DUTY CMD sets the POWER REF in Watt. MAX_POWER sets the POWER REF at DUTY CMD of 100%. MIN_DUTY sets the minimum POWER REF (MIN_DUTY x MAX_POWER). If MAX_POWER is set to 0, POWER REF is clamped to zero (irrespective of DUTY CMD) and the motor is in a stopped state.

Current Input Transfer Function

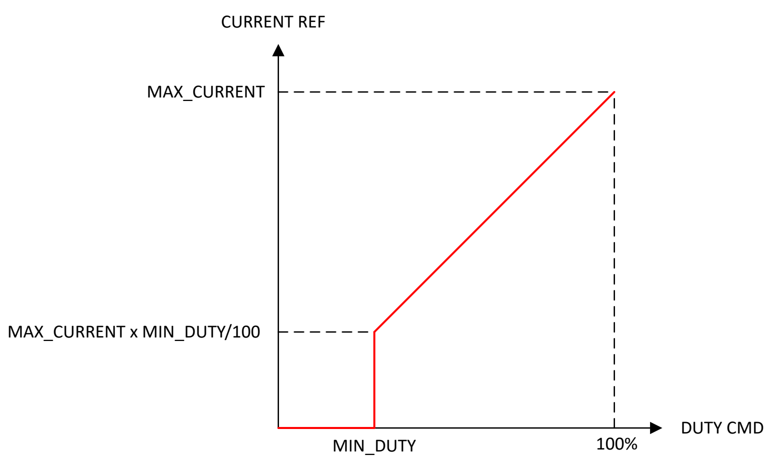

Figure 7-16. Current Input Transfer Function

Figure 7-16 shows the relationship between DUTY_CMD and CURRENT_REF. When the current loop is enabled, DUTY_CMD sets the q-axis CURRENT_REF (i_{q_ref})in Ampere. MAX_CURRENT is the same as ILIMIT and sets the CURRENT_REF at DUTY CMD of 100%. MIN_DUTY sets the minimum CURRENT_REF (MIN_DUTY x MAX_CURRENT).

Note

1. In MCF8329A, MIN_DUTY is set as 1%. Any duty command (DUTY_CMD) or reference (REF_X from input profiles) value set to < 1% will result in target reference (SPEED REF or POWER REF or CURRENT REF or MODULATION INDEX REF) being clamped to zero and motor to be in stopped state.

Modulation Index Input Transfer Function

In modulation index control mode, the voltage applied to the motor (direct axis component of modulation index V_d and quadrature axis component of modulation index V_q) is proportional to the DUTY_CMD (from MIN_DUTY to 100% PWM duty applied to motor). For DUTY CMD less than MIN_DUTY, the applied voltage to the motor is clamped to zero by making the duty cycle to zero.

7.3.8 Bootstrap Capacitor Initial Charging

MCF8329A provides a way to precharge the bootstrap capacitor during start-up. The algorithm uses a sequence to charge each phase bootstrap capacitor by turning on the external low-side MOSFETs using PWM turn-on pulses on GLx pins as shown in Figure 7-17. In the charging sequence, the low side MOSFET is switched at a frequency set by PWM_FREQ_OUT with an on time of $t_{LS\_ON\_BC}$ (5% on time duty cycle). Each phase is charged for a period equal to one third of BST_CHRG_TIME.

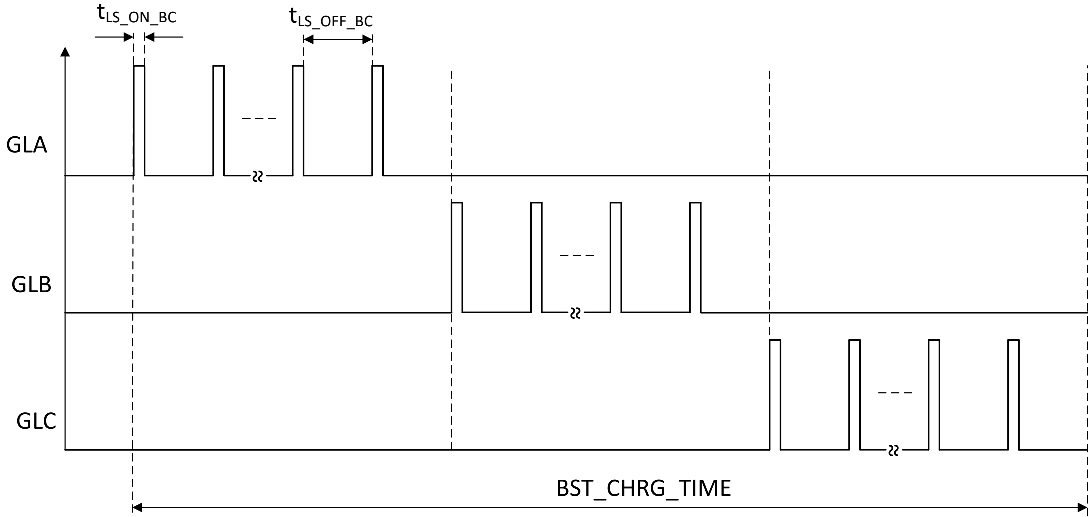

Figure 7-17. Bootstrap Capacitor Precharging at Start up

7.3.9 Starting the Motor Under Different Initial Conditions

The motor can be in one of three states when MCF8329A begins the start-up process. The motor may be stationary, spinning in the forward direction, or spinning in the reverse direction. The MCF8329A includes a number of features to allow for reliable motor start-up under all of these conditions. Figure 7-18 shows the motor start-up flow for each of the three initial motor states.

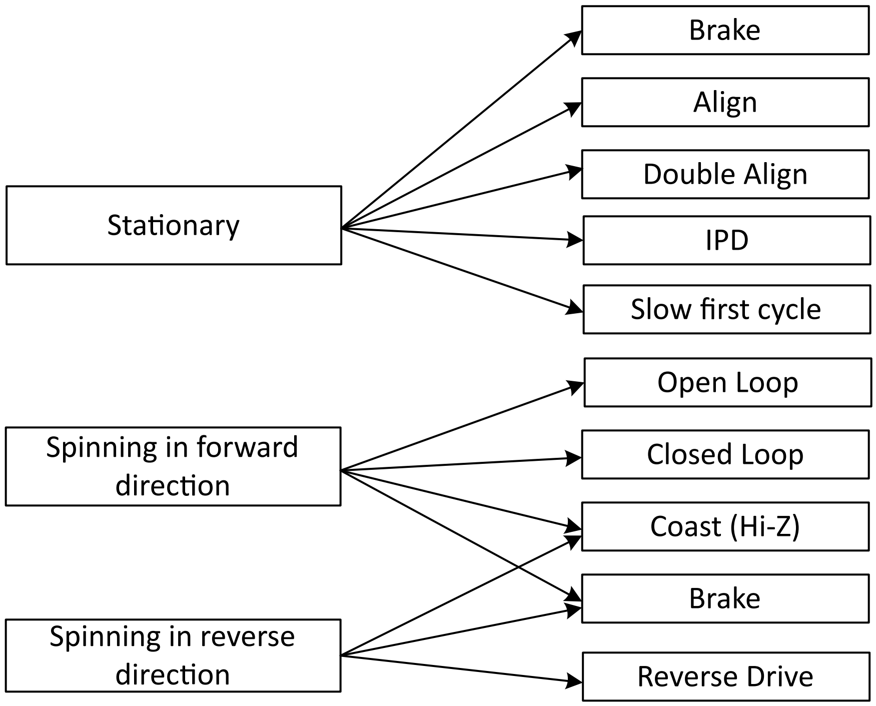

Figure 7-18. Starting the motor under different initial conditions

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Note

"Forward" means "spinning in the same direction as the commanded direction", and "Reverse" means "spinning in the opposite direction as the commanded direction".

7.3.9.1 Case 1 – Motor is Stationary

If the motor is stationary, the commutation must be initialized to be in phase with the position of the motor. The MCF8329A provides various options to initialize the commutation logic to the motor position and reliably start the motor.

- The align and double align techniques force the motor into alignment by applying a voltage across a particular motor phase to force the motor to rotate in alignment with this phase.
- Initial position detect (IPD) determines the position of the motor based on the deterministic inductance variation, which is often present in BLDC motors.
- The slow first cycle method starts the motor by applying a low frequency cycle to align the rotor position to the applied commutation by the end of one electrical rotation.

MCF8329A also provides a configurable brake option to ensure the motor is stationary before initiating one of the above start-up methods. Device enters open loop acceleration after going through the configured start-up method.

7.3.9.2 Case 2 – Motor is Spinning in the Forward Direction

If the motor is spinning forward (same direction as the commanded direction) with sufficient speed (BEMF), the MCF8329A resynchronizes with the spinning motor and continues commutation by going directly to closed loop operation. If the motor speed is too low for closed loop operation, MCF8329A enters open loop operation to accelerate the motor till it reaches sufficient speed to enter closed loop operation. By resynchronizing to the spinning motor, the user achieves the fastest possible start-up time for this initial condition. This resynchronization feature can be enabled or disabled through RESYNC_EN. If resynchronization is disabled, the MCF8329A can be configured to wait for the motor to coast to a stop and/or apply a brake. After the motor has stopped spinning, the motor start-up sequence proceeds as in Case 1, considering the motor is stationary.

7.3.9.3 Case 3 – Motor is Spinning in the Reverse Direction

If the motor is spinning in the reverse direction (the opposite direction as the commanded direction), the MCF8329A provides several methods to change the direction and drive the motor to the target speed reference in the commanded direction.

The reverse drive method allows the motor to be driven so that it decelerates through zero speed. The motor achieves the shortest possible spin-up time when spinning in the reverse direction.

If reverse drive is not enabled, then the MCF8329A can be configured to wait for the motor to coast to a stop and/or apply a brake. After the motor has stopped spinning, the motor start-up sequence proceeds as in Case 1, considering the motor is stationary.

Note

Take care when using the reverse drive or brake feature to ensure that the current is limited to an acceptable level and that the supply voltage does not surge as a result of energy being returned to the power supply.

7.3.10 Motor Start Sequence (MSS)

Figure 7-19 shows the motor-start sequence implemented in the MCF8329A device.

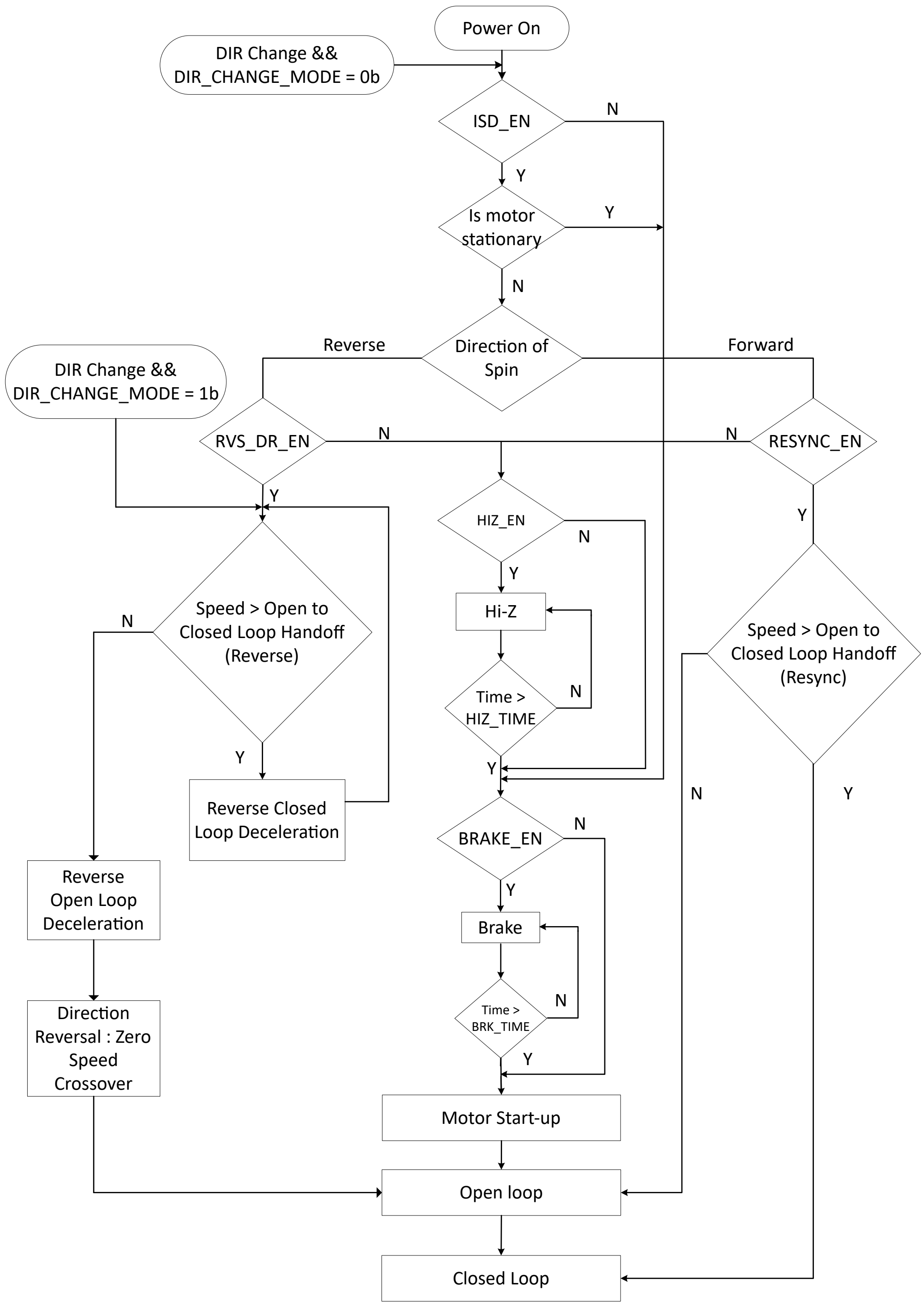

Figure 7-19. Motor Starting-up Flow

Power-On State	This is the initial state of the Motor Start Sequence (MSS). The MSS starts in this state on initial power-up or whenever the MCF8329A device comes out of standby or sleep mode.
DIR Change && DIR_CHANGE_MODE = 0b Judgement	In MCF8329A, if direction change command is detected and DIR_CHANGE_MODE is set to 0b during any state (including closed loop), the device re-starts the MSS.
ISD_EN Judgement	After power-on, the MCF8329A MSS enters the ISD_EN judgement where it checks to see if the initial speed detect (ISD) function is enabled (ISD_EN = 1b). If ISD is disabled, the MSS proceeds directly to the BRAKE_EN judgement. If ISD is enabled, MSS advances to the ISD (Is Motor Stationary) state.
ISD State	The MSS determines the initial condition (speed, direction of spin) of the motor (see Initial Speed Detect (ISD)). If motor is deemed to be stationary (motor BEMF < STAT_DETECT_THR), the MSS proceeds to BRAKE_EN judgement. If the motor is not stationary, MSS proceeds to verify the direction of spin.
Direction of Spin Judgement	The MSS determines whether the motor is spinning in the forward or the reverse direction. If the motor is spinning in the forward direction, the MCF8329A proceeds to the RESYNC_EN judgement. If the motor is spinning in the reverse direction, the MSS proceeds to the RVS_DR_EN judgement.
RESYNC_EN Judgement	If RESYNC_EN is set to 1b, MCF8329A proceeds to Speed > Open to Closed Loop Handoff (Re-sync) judgement. If RESYNC_EN is set to 0b, MSS proceeds to HIZ_EN judgement.
Speed > Open to Closed Loop Handoff (Re-sync) Judgement	If motor speed > FW_DRV_RESYN_THR, MCF8329A uses the speed and position information from the ISD state to transition to the closed loop state (see Motor Resynchronization) directly. If motor speed < FW_DRV_RESYN_THR, MCF8329A transitions to open loop state.
RVS_DR_EN Judgement	The MSS checks to see if the reverse drive function is enabled (RVS_DR_EN = 1). If it is enabled, the MSS transitions to check speed of the motor in reverse direction. If the reverse drive function is not enabled, the MSS advances to the HIZ_EN judgement.
Speed > Open to Closed Loop Handoff (Reverse) Judgement	The MSS checks to see if the reverse speed is high enough for MCF8329A to decelerate in closed loop. Till the speed (in reverse direction) is high enough, MSS stays in reverse closed loop deceleration. If speed is too low, then the MSS transitions to reverse open loop deceleration.
Reverse Closed Loop, Open Loop Deceleration and Zero Speed Crossover	The MCF8329A resynchronizes in the reverse direction, decelerates the motor in closed loop till motor speed falls below the handoff threshold. (see *Reverse Drive*). When motor speed in reverse direction is too low, the MCF8329A switches to open-loop, decelerates the motor in open-loop, crosses zero speed, and accelerates in the forward direction in open-loop before entering closed loop operation after motor speed is sufficiently high.
HIZ_EN Judgement	The MSS checks to determine whether the coast (Hi-Z) function is enabled (HIZ_EN =1). If the coast function is enabled, the MSS advances to the coast routine. If the coast function is disabled, the MSS advances to the BRAKE_EN judgement.
Coast (Hi-Z) Routine	The device coasts the motor by turning OFF all six MOSFETs for a certain time configured by HIZ_TIME.
BRAKE_EN Judgement	The MSS checks to determine whether the brake function is enabled (BRAKE_EN =1). If the brake function is enabled, the MSS advances to the brake routine. If the brake function is disabled, the MSS advances to the motor start-up state (see Section 7.3.10.4).

Brake Routine MCF8329A implements a brake by turning on all three low-side MOSFETS for BRK_TIME.

Closed Loop State In this state, the MCF8329A drives the motor with FOC.

Note

User should ensure adequate start up time to fully charge the bootstrap capacitors. One way to charge the boot capacitor is by providing enough time with low side brake at start up. Other ways is to use the bootstrap precharging routine. With ISD operation, the device will initiate ISD only after bootstrap voltage crosses the UVLO threshold.

7.3.10.1 Initial Speed Detect (ISD)

The ISD function is used to identify the initial condition of the motor and is enabled by setting ISD_EN to 1b. The initial speed, position and direction is determined by sampling the phase voltage through the internal ADC. ISD can be disabled by setting ISD_EN to 0b. If the function is disabled (ISD_EN set to 0b), the MCF8329A does not perform the initial speed detect function and proceeds to check if the brake routine (BRAKE_EN) is enabled.

7.3.10.2 Motor Resynchronization

The motor resynchronization function works when the ISD and resynchronization functions are both enabled and the device determines that the initial state of the motor is spinning in the forward direction (same direction as the commanded direction). The speed and position information measured during ISD are used to initialize the drive state of the MCF8329A, which can transition directly into closed loop (or open loop if motor speed is not sufficient for closed loop operation) state without needing to stop the motor. In the MCF8329A, motor resynchronization can be enabled/disabled through RESYNC_EN bit. If motor resynchronization is disabled, the device proceeds to check if the motor coast (Hi-Z) routine is enabled.

7.3.10.3 Reverse Drive

The MCF8329A uses the reverse drive function to change the direction of the motor rotation when ISD_EN and RVS_DR_EN are both set to 1b and the ISD determines the motor spin direction to be opposite to that of the commanded direction. Reverse drive includes synchronizing with the motor speed in the reverse direction, reverse decelerating the motor through zero speed, changing direction, and accelerating in open loop in forward (or commanded) direction until the device transitions into closed loop in forward direction (see Figure 7-20). . MCF8329A provides the option of using the forward direction parameters or a separate set of reverse drive parameters by configuring REV_DRV_CONFIG.

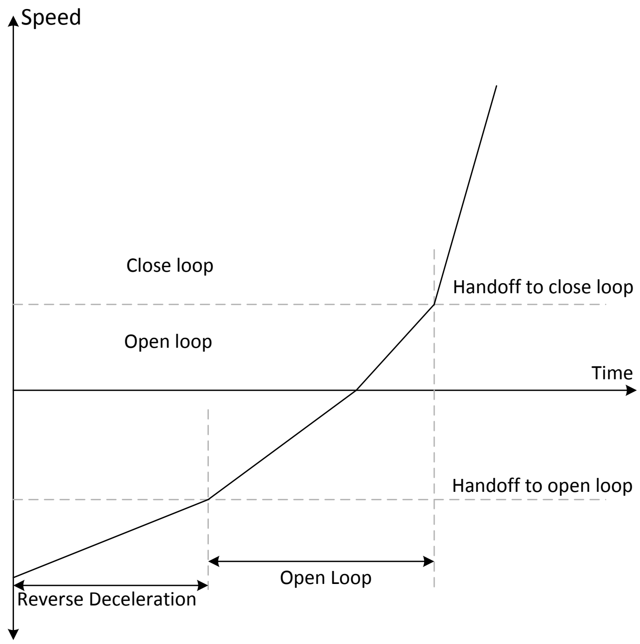

Figure 7-20. Reverse Drive Function

7.3.10.3.1 Reverse Drive Tuning

MCF8329A provides the option of tuning the open to closed loop handoff threshold, open loop acceleration (and deceleration) rates and open loop current limit in reverse drive to values different to those used in forward drive operation; the reverse drive specific parameters can be used by setting REV_DRV_CONFIG to 1b. If REV_DRV_CONFIG is set to 0b, MCF8329A uses the equivalent parameters configured for forward drive operation during the reverse drive operation too.

The speed at which motor enters the open loop in reverse direction can be configured using REV_DRV_HANDOFF_THR. For a smooth transition without jerks or loss of synchronization, user can configure an appropriate current limit when the motor is spinning in open loop during speed reversal using REV_DRV_OPEN_LOOP_CURRENT. The open loop acceleration rates for the forward direction during speed reversal are defined using REV_DRV_OPEN_LOOP_ACCEL_A1 and REV_DRV_OPEN_LOOP_ACCEL_A2. The reverse drive open loop deceleration rate, when the motor is decelerating in the opposite direction to zero speed, can be configured as a percentage of reverse drive open loop acceleration using REV_DRV_OPEN_LOOP_DEC.

7.3.10.4 Motor Start-up

There are different options available for motor start-up from a stationary position and these options can be configured by MTR_STARTUP. In align and double align mode, the motor is aligned to a known position by injecting a DC current. In IPD mode, the rotor position is estimated by applying 6 different high-frequency pulses. In slow first cycle mode, the motor is started by applying a low frequency cycle.

7.3.10.4.1 Align

Align is enabled by configuring MTR_STARTUP to 00b. The MCF8329A aligns the motor by injecting a DC current through a particular phase pattern for a certain time configured by ALIGN_TIME. The phase pattern during align is generated based on ALIGN_ANGLE. In the MCF8329A, the current limit during align is configured through ALIGN_OR_SLOW_CURRENT LIMIT.

A fast change in the phase current may result in a sudden change in the driving torque and this could result in acoustic noise. To avoid this, the MCF8329 ramps up the current from 0 to the current limit at a configurable ramp rate set by ALIGN_SLOW_RAMP_RATE. At the end of align routine the motor, will be aligned at the known position.

7.3.10.4.2 Double Align

Double align is enabled by configuring MTR_STARTUP to 01b. Single align is not reliable when the initial position of the rotor is 180º out of phase with the applied phase pattern. In this case, it is possible to have start-up failures using single align. In order to improve the reliability of align based start-up, the MCF8329A provides the option of double align start-up. In double align start-up, MCF8329A uses a phase pattern for the second align that is 90º ahead of the first align phase pattern. In double align, relevant parameters like align time, current limit, ramp rate are the same as in the case of single align - two different phase patterns are applied in succession with the same parameters to ensure that the motor will be aligned to a known position irrespective of initial rotor position.

7.3.10.4.3 Initial Position Detection (IPD)

Initial Position Detection (IPD) can be enabled by configuring MTR_STARTUP to 10b. In IPD, inductive sense method is used to determine the initial position of the motor using the spatial variation in the motor inductance.

Align or double align may result in the motor spinning in the reverse direction before starting open loop acceleration. IPD can be used in such applications where reverse rotation of the motor is unacceptable. IPD does not wait for the motor to align with the commutation and therefore can allow for a faster motor start-up sequence. IPD works well when the inductance of the motor varies as a function of position. IPD works by pulsing current in to the motor and hence can generate acoustics which must be taken into account when determining the best start-up method for a particular application.

7.3.10.4.3.1 IPD Operation

IPD operates by sequentially applying six different phase patterns according to the following sequence: BC-> CB-> AB-> BA-> CA-> AC (see Figure 7-21). When the current reaches the threshold configured by IPD_CURR_THR, the MCF8329A stops driving the particular phase pattern and measures the time taken to reach the current threshold from when the particular phase pattern was applied. Thus, the time taken to reach IPD_CURR_THR is measured for all six phase patterns - this time varies as a function of the inductance in the motor windings. The state with the shortest time represents the state with the minimum inductance. The minimum inductance is because of the alignment of the north pole of the motor with this particular driving state.

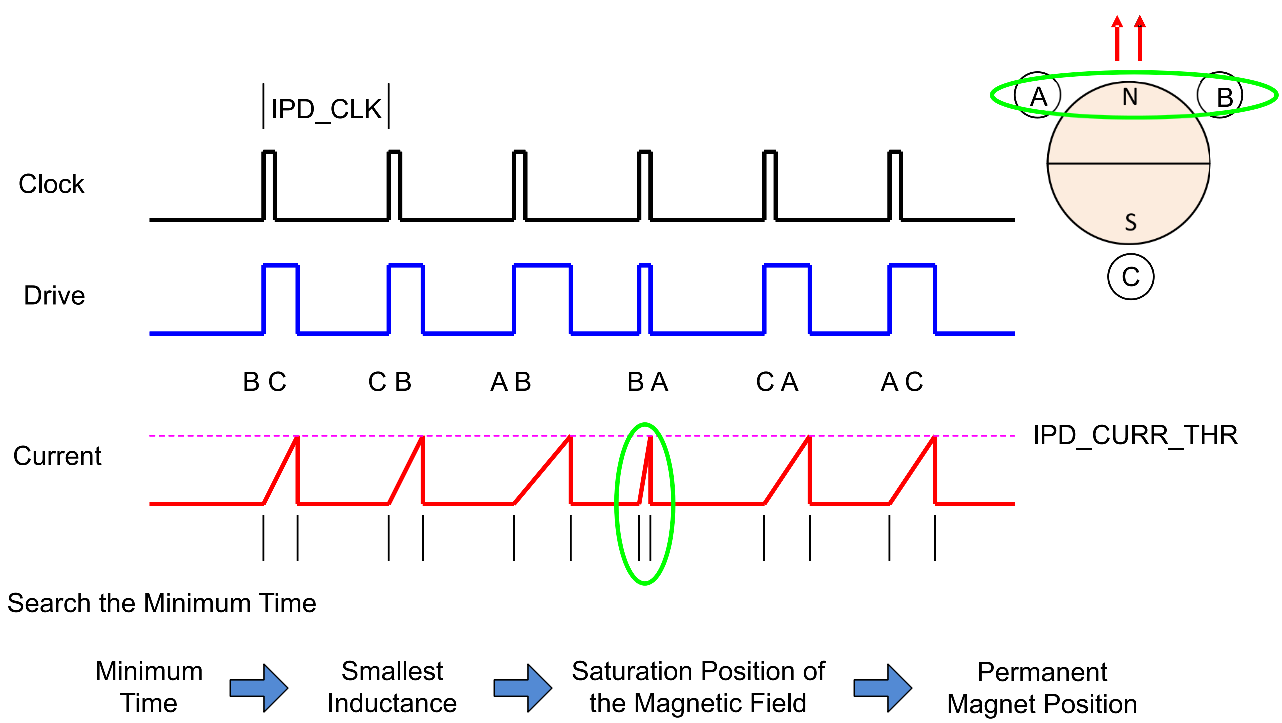

Figure 7-21. IPD Function

Note

The minimum configurable IPD_CURR_THR depends on CSA_GAIN setting.

- For CSA_GAIN = 40 V/V : Minimum configurable IPD_CURR_THR is 20 %
- For CSA_GAIN = 20 V/V : Minimum configurable IPD_CURR_THR is 10 %
- For CSA_GAIN = 10 V/V : Minimum configurable IPD_CURR_THR is 5 %
- For CSA_GAIN = 5 V/V : Minimum configurable IPD_CURR_THR is 2.5 %

7.3.10.4.3.2 IPD Release

IPD release uses Hi-Z mode, both the high-side (HSA) and low-side (LSC) MOSFETs are turned OFF and the current recirculates through the body diodes back to the power supply (see Figure 7-22).

The Hi-Z mode during IPD release can result in a voltage increase on motor DC supply voltage VM (V_{PVDD}). The user must manage this with an appropriate selection of either a clamp circuit or by providing sufficient capacitance between V_{PVDD} and GND to absorb the energy.

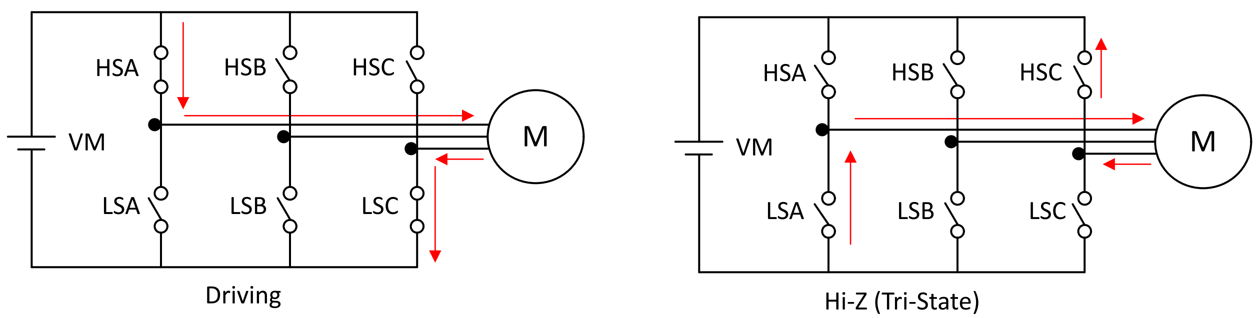

Figure 7-22. IPD Release Hi-Z mode

7.3.10.4.3.3 IPD Advance Angle

After the initial position is detected, the MCF8329A begins driving the motor in open loop at an angle specified by IPD_ADV_ANGLE.

Advancing the drive angle anywhere from 0° to 180° results in positive torque. Advancing the drive angle by 90° results in maximum initial torque. Applying maximum initial torque could result in uneven acceleration to the rotor. Select the IPD_ADV_ANGLE to allow for smooth acceleration in the application (see Figure 7-23).

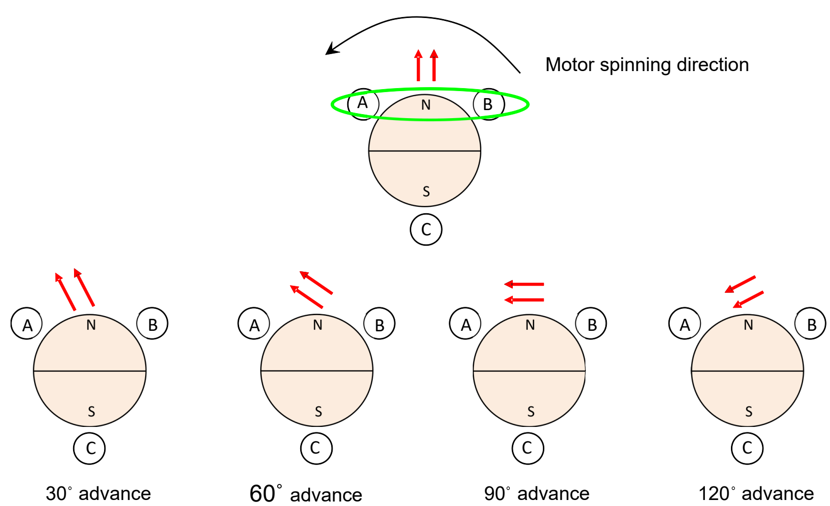

Figure 7-23. IPD Advance Angle

7.3.10.4.4 Slow First Cycle Startup

Slow First Cycle start-up is enabled by configuring MTR_STARTUP to 11b. In slow first cycle start-up, the MCF8329A starts motor commutation at a frequency defined by SLOW_FIRST_CYC_FREQ. The frequency configured is used only for first cycle, and then the motor commutation follows acceleration profile configured by open loop acceleration coefficients A1 and A2. The slow first cycle frequency has to be configured to be slow enough to allow motor to synchronize with the commutation sequence. This mode is useful when fast startup is desired as it significantly reduces the align time.

7.3.10.4.5 Open loop

Upon completing the motor position initialization with either align, double align, IPD or slow first cycle, the MCF8329A begins to accelerate the motor in open loop. During open loop, the speed is increased with a fixed current limit. In open loop, the control PI loops for I_q and I_d actively control the currents. The angle during open loop is provided from the ramp generator as shown in Figure 7-24

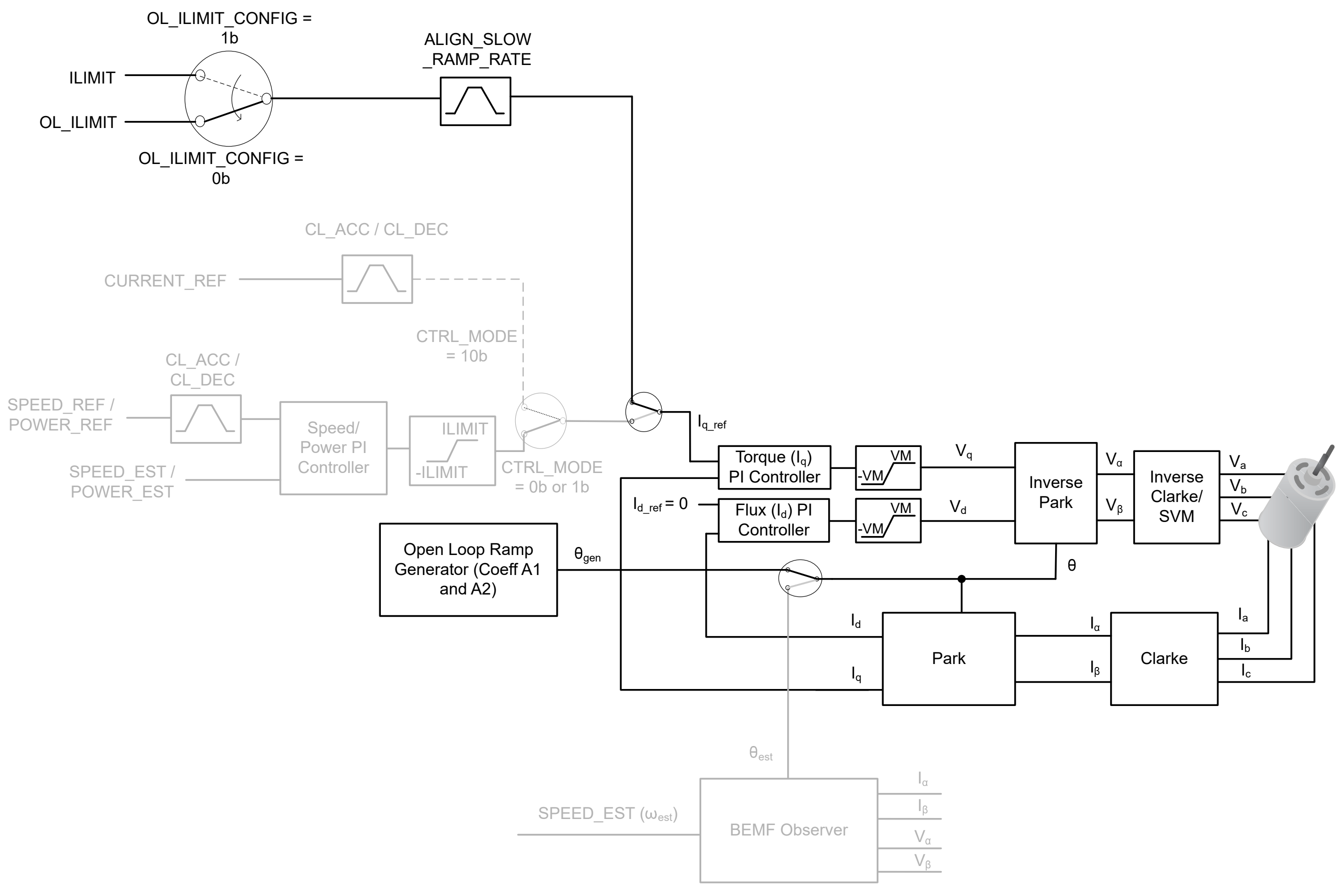

Figure 7-24. Open Loop

In MCF8329A, the current limit threshold is configured through OL_ILIMIT_CONFIG and is set by ILIMIT or OL_ILIMIT based on configuration of OL_ILIMIT_CONFIG. The function of the open-loop operation is to drive the motor to a speed at which the motor generates sufficient BEMF to allow the back-EMF observer to accurately detect the position of the rotor. The motor is accelerated in open loop and speed at any given time is determined by Equation 8. In MCF8329A, open loop acceleration coefficients, A1 and A2 are configured through OL_ACC_A1 and OL_ACC_A2 respectively.

$$\text{Speed}(t) = A1 * t + 0.5 * A2 * t^2 \quad (8)$$

7.3.10.4.6 Transition from Open to Closed Loop

Once the motor has reached a sufficient speed for the back-EMF observer to estimate the angle and speed of the motor, the MCF8329A transitions into closed loop state. This handoff speed is automatically determined based on the measured back-EMF and motor speed. Users also have an option to manually set the handoff speed by configuring OPN_CL_HANDOFF_THR and setting AUTO_HANDOFF_EN to 0b. In order to have smooth transition and avoid speed transients, the theta_error (Θ_{gen} - Θ_{est}) is decreased linearly after transition. The ramp rate of theta_error reduction can be configured using THETA_ERROR_RAMP_RATE. If the current limit set during the open loop is high and if it is not reduced before transition to closed loop, the motor speed may momentarily rise to higher values than SPEED_REF after transition into closed loop. In order to avoid such speed variations, configure the IQ_RAMP_EN to 1b, so that i_{q_ref} decreases prior to transition into closed loop. However if the final speed reference (SPEED_REF) is more than two times the open loop to closed loop hand off speed (OPN_CL_HANDOFF_THR), then i_{q_ref} is not decreased independent of the IQ_RAMP_EN setting, to enable faster motor acceleration.

After hand off to closed loop at a sufficient speed, there could be still some theta error, as the estimators may not be fully aligned. A slow acceleration can be used after the open loop to closed loop transition, ensuring that the theta error reduces to zero. The slow acceleration can be configured using CL_SLOW_ACC.

Figure 7-25 shows the control sequence in open to closed loop transition. The current i_{q_ref} reduces to a lower value in current decay region, if IQ_RAMP_EN is set to 1b. If IQ_RAMP_EN is set to 0b, then the current decay region will not be present in the transition sequence.

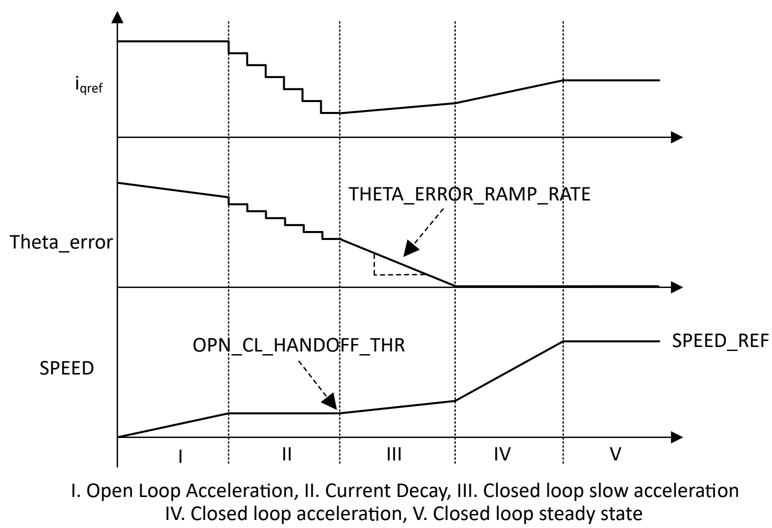

Figure 7-25. Control Sequence in Open to Closed Loop Transition

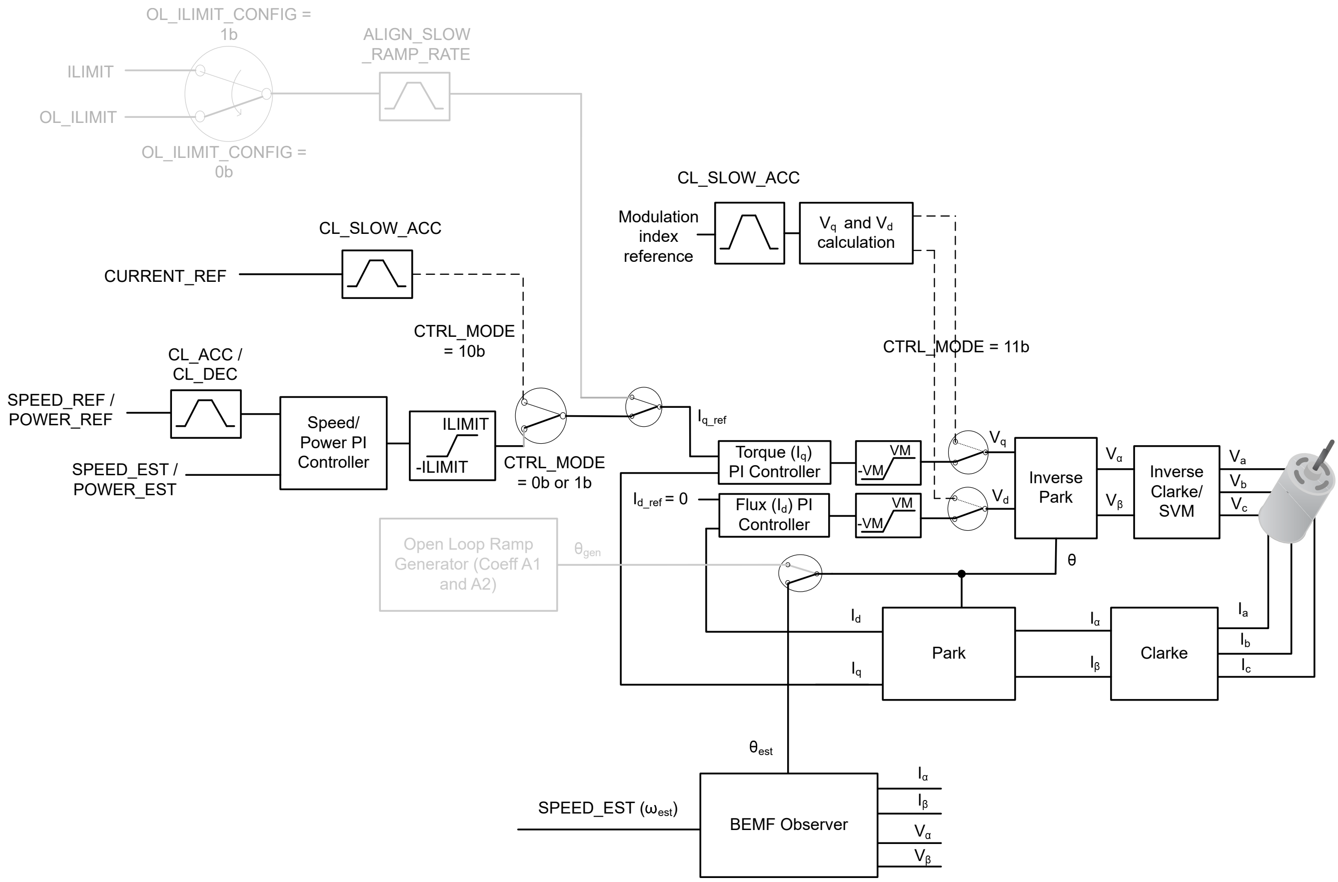

Figure 7-26. Open to Closed Loop Transition Control Block Diagram

7.3.11 Closed Loop Operation

The MCF8329A drives the motor using Field Oriented Control (FOC) as shown in Figure 7-27. In closed loop operation, the motor angle (Θ_{est}) and speed (Speed_est) are estimated using the back-EMF observer. The speed and current regulation are achieved using PI control loop. In order to achieve maximum efficiency, the direct axis current is set to zero ($I_{d\_ref} = 0$), which will ensure that stator and rotor field are orthogonal (90° out of phase) to each other. If flux weakening or MTPA is enabled I_{d_ref} can be zero or a negative value during closed loop operation.

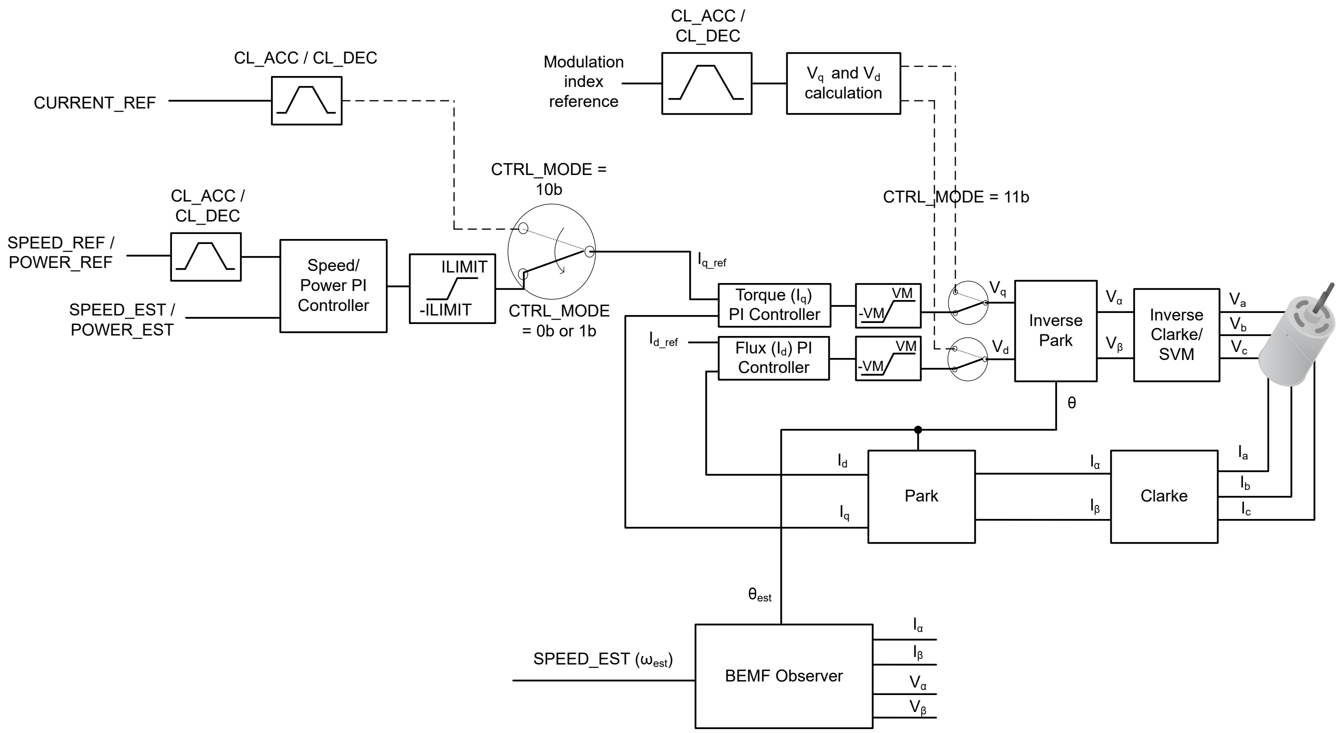

Figure 7-27. Closed Loop FOC Control

7.3.11.1 Closed loop accelerate

During closed loop acceleration/deceleration, MCF8329A provides the option of configuring the slew rate of the reference input. This allows for a linear change in reference input (speed or power or current or modulation index) even when there is a step change in reference input (from Analog, PWM, Frequency or I^2C) as seen in Figure 7-28. This slew rate can be configured so as to prevent sudden changes in the torque applied to the motor which could result in acoustic noise. The closed loop acceleration/deceleration slew rate parameter, CL_ACC/CL_DEC, sets the slew rate of the reference during acceleration and deceleration (when AVS is not active) respectively.

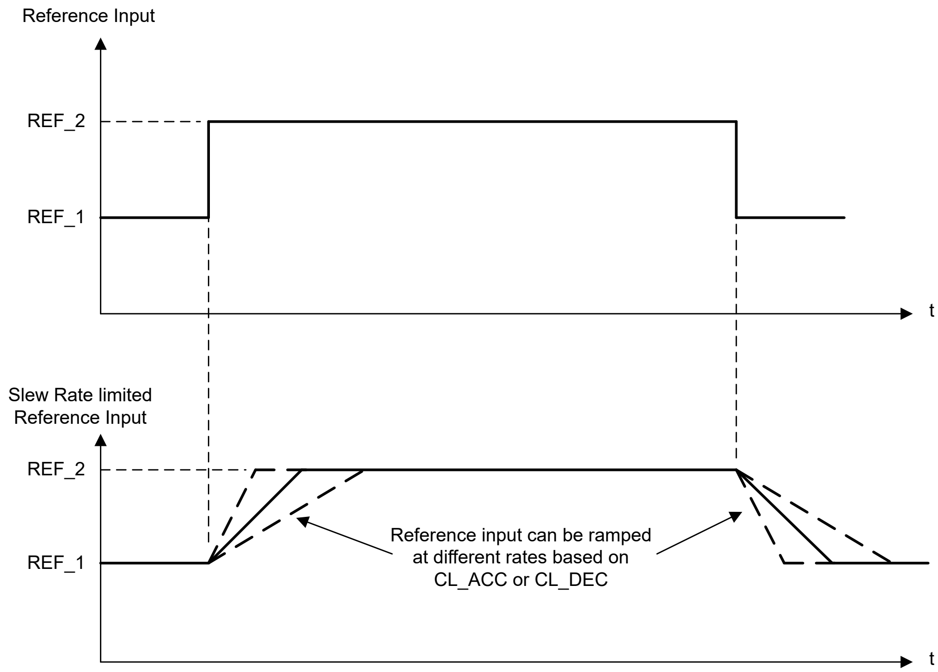

Figure 7-28. Closed Loop Acceleration/Deceleration Slew Rate

7.3.11.2 Speed PI Control

The integrated speed control loop helps maintain a constant speed over varying operating conditions. The K_p and K_i coefficients are configured through SPD_LOOP_KP and SPD_LOOP_KI. The output of the speed loop is used to generate the current reference for torque control (I_{q_ref}). The output of the speed loop is limited to implement a current limit. The current limit is set by configuring ILIMIT. When output of the speed loop saturates, the integrator is disabled to prevent integral wind-up.

SPEED_REF is derived from the duty command input and speed profiles configured by the user and SPEED_MEAS is the estimated speed from the back-EMF observer.

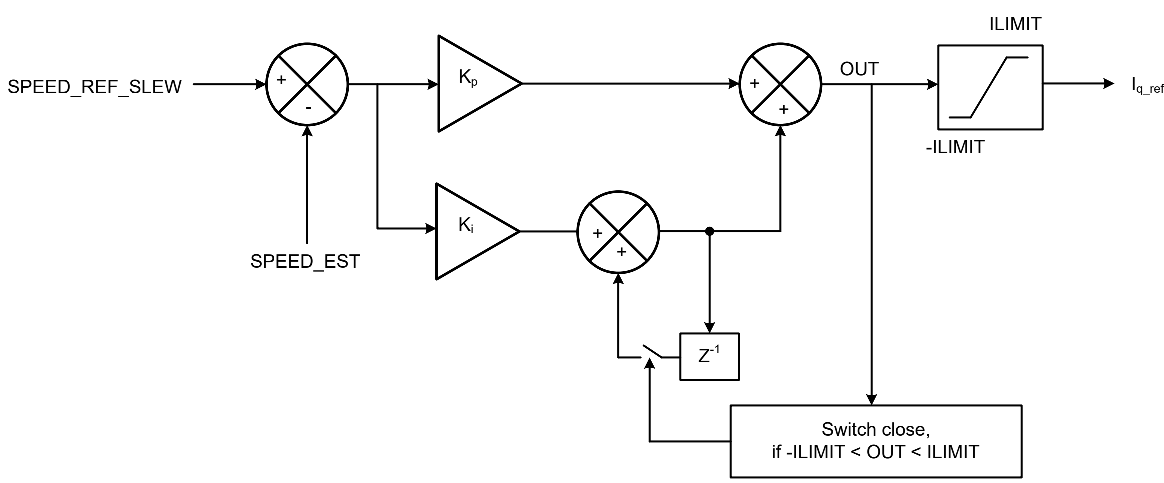

Figure 7-29. Speed PI Control

7.3.11.3 Current PI Control

The MCF8329A has two PI controllers, one each for I_d and I_q to control flux and torque separately. K_p and K_i coefficients are the same for both PI controllers and are configured through CURR_LOOP_KP and CURR_LOOP_KI. The outputs of the current control loops are used to generate voltage signals V_d and V_q to be applied to the motor. The outputs of the current loops are clamped to supply voltage V_M. I_d current PI loop is executed first and output of I_d current PI loop V_d is checked for saturation. When the output of the current loop saturates, the integration is disabled to prevent integral wind-up.

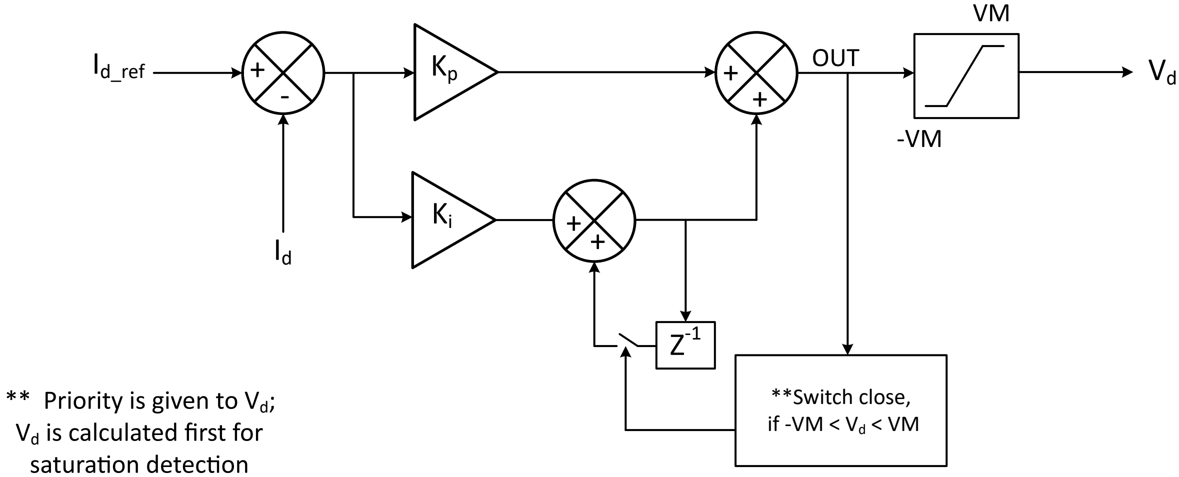

Figure 7-30. I_d Current PI Control

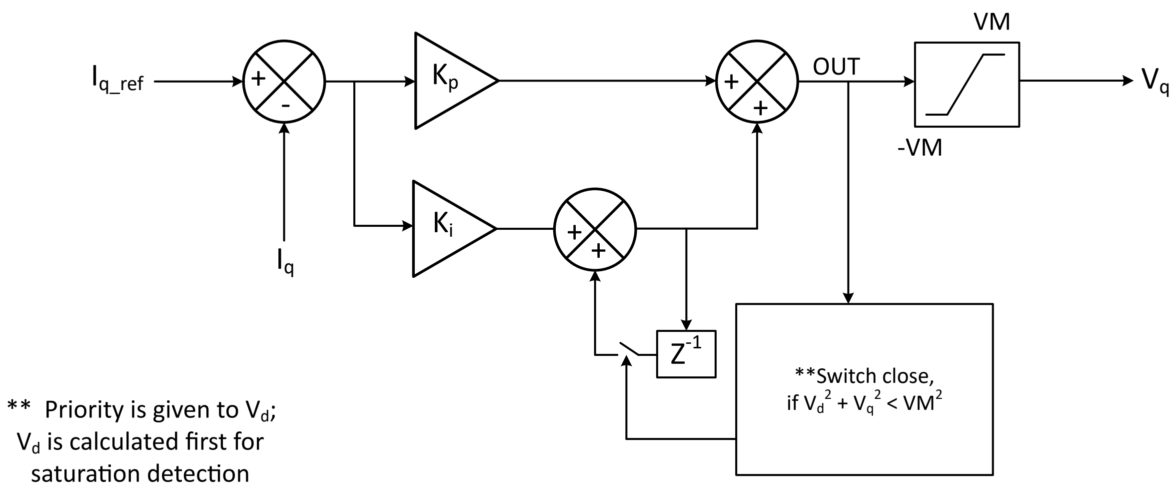

Figure 7-31. I_q Current PI Control

7.3.11.4 Power Loop

MCF8329A provides an option of regulating the (input DC) power instead of motor speed for a closed loop power control. Input power regulation (instead of motor speed) mode is selected by setting CTRL_MODE to 01b. The maximum power that MCF8329A can draw from the DC input supply is set by MAX_POWER. The K_p and K_i coefficients for power loop are configured through SPD_LOOP_KP and SPD_LOOP_KI.

$$POWER\ REF(W) = DUTY\ CMD \times Maximum\ Power\ (W) \quad (9)$$

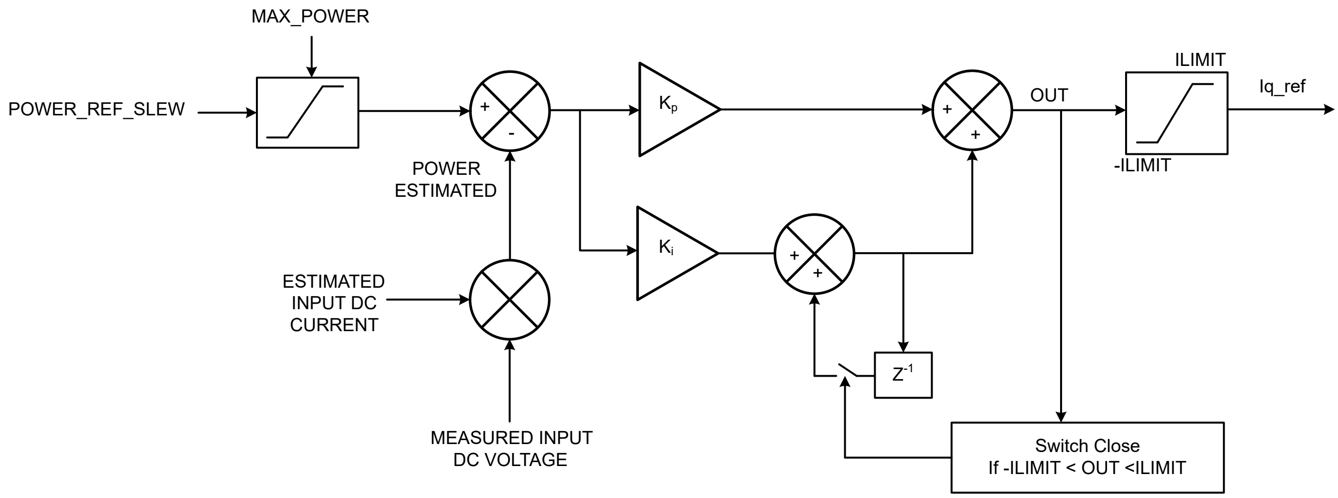

Figure 7-32. Closed Loop Power Control

7.3.11.5 Modulation Index Control

MCF8329A provides voltage control mode, selected by setting CTRL_MODE to 11b. The closed loop speed control, power control and current control (i_q and i_d) are disabled in this mode. The applied V_q and V_d are controlled directly using the user defined modulation index reference voltage (VOLTAGE REF) and the lead angle setting. The VOLTAGE REF varies from MIN_DUTY to 100%.

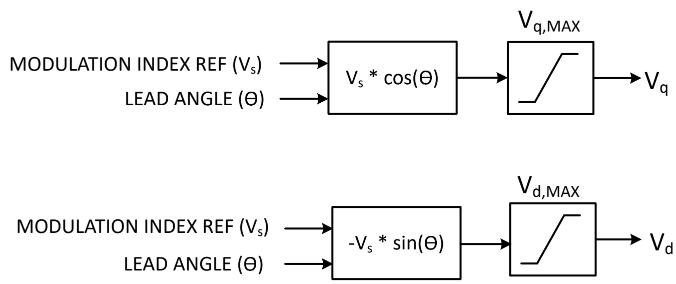

Figure 7-33. Open Loop Voltage Control

Note

1. The maximum modulation index (Vs) supported in modulation control mode depends on DIG_DEAD_TIME, SINGLE_SHUNT_BLANKING_TIMES, and PWM_FREQ_OUT settings.
2. MCF8329A is not designed to support recirculation stop mode during modulation index control mode.

7.3.12 Maximum Torque Per Ampere (MTPA) Control

PMSM or BLDC motors with magnetic saliency produces a reluctance torque from the difference between the direct-d axis inductance and the quadrature q-axis inductance. The maximum efficiency of the IPM motors can be achieved by proper selection of the current vector ratio between magnetic torque current and reluctance torque current in the total current. MCF8329A provides the maximum torque per ampere control and in that, for a given bus current, it is possible to obtain the best torque performance by setting the d axis current reference as a function of the q axis current reference as per the equation below.

$$i_d = \frac{\psi_m}{2\left(L_q - L_d\right)}\left(1 - \sqrt{1 + \frac{4\left(L_q - L_d\right)^2 i_q^2}{\psi_m^2}}\right) \tag{10}$$

Lq and Ld are inductance of the d and q axis. iq is the Q-axis current and ψm is the BEMF constant. In case of motors without saliency in the rotor, the inductance of d and q axis are the same and hence the point of maximum torque is always the one where d-axis current reference is 0. For motors with saliency, the d-axis reference can be set as a function of the q-axis reference as derived in the equation above so as to generate the maximum torque for any current drawn from the DC bus.

7.3.13 Flux Weakening Control

PMSM motors can be operated not only in the constant torque region below the base speed (normally rated speed) but also in the constant power region above the base speed, but the base speed can be varied according to current and voltage limitation. MCF8329A provides a flux weakening control, to increase the speed beyond the motor rated speed. The flux weakening can be enabled by setting 1b to FLUX_WEAKENING_EN. The flux weakening control uses a PI control loop as shown in Figure 7-34, to create the I_{dref}. Kp and Ki coefficients for flux weakening loop are configured through FLUX_WEAKENING_KP and FLUX_WEAKENING_KI.

The absolute maximum value of flux weakening current reference (I_{d_FW}) can be limited as a percentage of ILIMIT by configuring FLUX_WEAKENING_CURRENT_RATIO. If FLUX_WEAKENING_CURRENT_RATIO = 0b, then only circular limit is in place, in that case $i_q{}^2 + i_d{}^2$ is limited to ILIMIT. If I_{d_FW} absolute value increases then i_q is reduced to meet circular limit.

User can configure the modulation index reference, V_{s_ref} (shown in Equation 11) below that the flux weakening is not active and I_{d_FW} is made to zero. The configuration is available in the bits FLUX_WEAKENING_REF ERENCE.

$$V_{s\_ref} = \sqrt{V_{q\_ref}^2 + V_{d\_ref}^2} \tag{11}$$

The I_{dref} can be zero or minimum of i_d reference from flux weakening or MTPA. The variable FLUX_MODE_REFERENCE is available in the volatile memory (RAM) and a non-zero value can overwrite I_{d_FW} and I_{d_MTPA}.

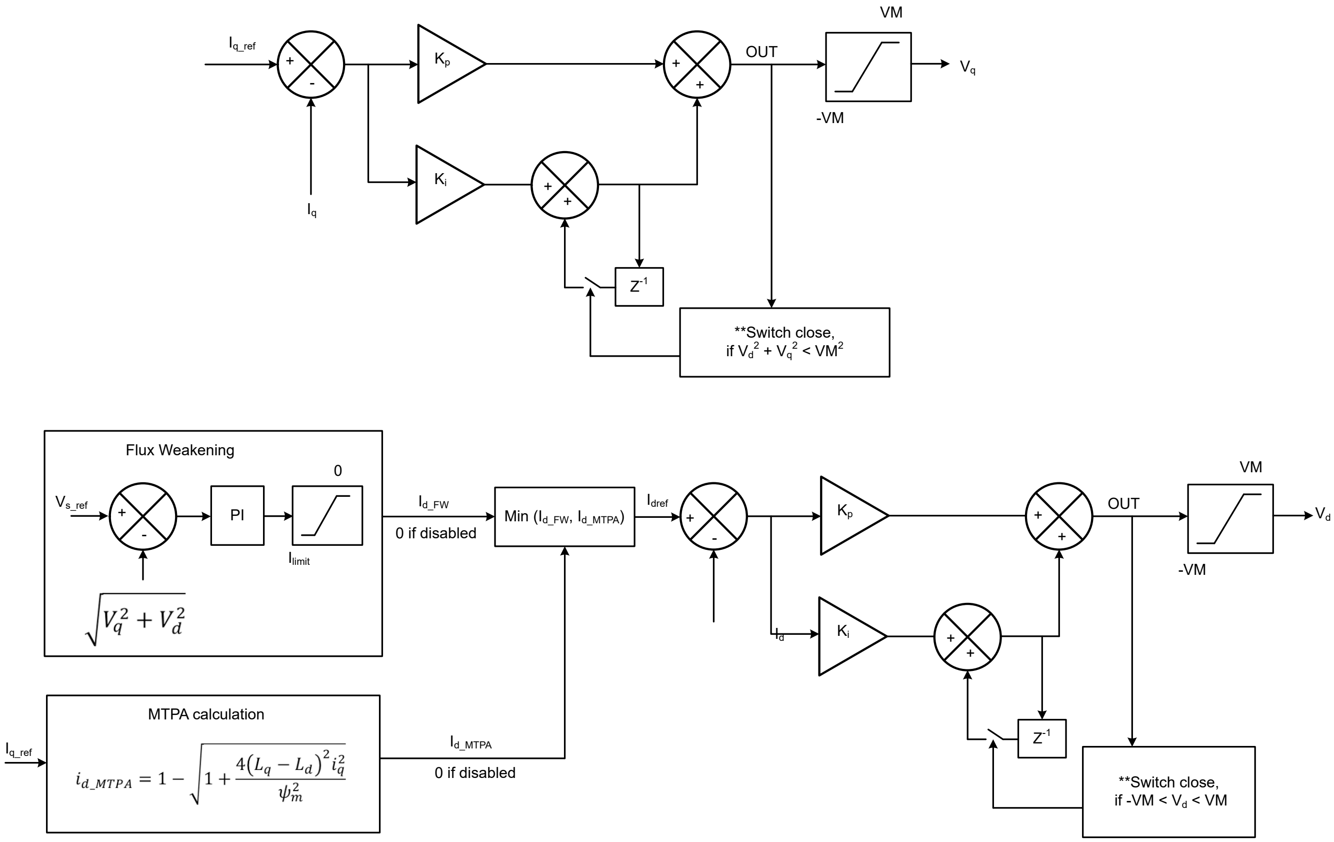

Figure 7-34. Flux Weakening Control

7.3.14 Motor Parameters

The MCF8329A uses the motor resistance, motor inductance and motor back-EMF constant to estimate motor position when operating in closed loop. The MCF8329A has the capability of measuring motor back-EMF constant in the offline state (see Motor Parameter Extraction Tool (MPET)). Offline measurement of motor back-EMF constant, when enabled, takes place before normal motor operation. The user can also disable the offline measurement and configure motor parameters through EEPROM. This feature of offline motor parameter measurement is useful to account for motor to motor variation during manufacturing.

7.3.14.1 Motor Resistance

For a wye-connected motor, the motor phase resistance refers to the resistance from the phase output to the center tap, R_{PH} (denoted as R_{PH} in Figure 7-35). For a delta-connected motor, the motor phase resistance refers to the equivalent phase to center tap in the wye configuration in Figure 7-35.

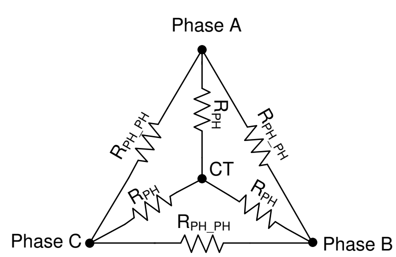

Figure 7-35. Motor Resistance

For both the delta-connected and the wye-connected motor, the easy way to get the equivalent R_{PH} is to measure the resistance between two phase terminals (R_{PH_PH}), and then divide this value by two, R_{PH} = ½

R_{PH_PH}. In wye-connected motor, if user has access to center tap (CT), R_{PH} can also be measured between center tap (CT) and phase terminal.

Configure the motor resistance (R_{PH}) to a nearest value from Table 7-2.

Table 7-2. Motor Resistance Look-Up Table

MOTOR_RES (HEX)	R_{PH} (Ω)	MOTOR_RES (HEX)	R_{PH} (Ω)	MOTOR_RES (HEX)	R_{PH} (Ω)	MOTOR_RES (HEX)	R_{PH} (Ω)
0x00	Not Valid	0x40	0.145	0x80	0.465	0xC0	2.1
0x01	0.006	0x41	0.150	0x81	0.470	0xC1	2.2
0x02	0.007	0x42	0.155	0x82	0.475	0xC2	2.3
0x03	0.008	0x43	0.160	0x83	0.480	0xC3	2.4
0x04	0.009	0x44	0.165	0x84	0.485	0xC4	2.5
0x05	0.010	0x45	0.170	0x85	0.490	0xC5	2.6
0x06	0.011	0x46	0.175	0x86	0.495	0xC6	2.7
0x07	0.012	0x47	0.180	0x87	0.50	0xC7	2.8
0x08	0.013	0x48	0.185	0x88	0.51	0xC8	2.9
0x09	0.014	0x49	0.190	0x89	0.52	0xC9	3.0
0x0A	0.015	0x4A	0.195	0x8A	0.53	0xCA	3.2
0x0B	0.016	0x4B	0.200	0x8B	0.54	0xCB	3.4
0x0C	0.017	0x4C	0.205	0x8C	0.55	0xCC	3.6
0x0D	0.018	0x4D	0.210	0x8D	0.56	0xCD	3.8
0x0E	0.019	0x4E	0.215	0x8E	0.57	0xCE	4.0
0x0F	0.020	0x4F	0.220	0x8F	0.58	0xCF	4.2
0x10	0.022	0x50	0.225	0x90	0.59	0xD0	4.4
0x11	0.024	0x51	0.230	0x91	0.60	0xD1	4.6
0x12	0.026	0x52	0.235	0x92	0.61	0xD2	4.8
0x13	0.028	0x53	0.240	0x93	0.62	0xD3	5.0
0x14	0.030	0x54	0.245	0x94	0.63	0xD4	5.2
0x15	0.032	0x55	0.250	0x95	0.64	0xD5	5.4
0x16	0.034	0x56	0.255	0x96	0.65	0xD6	5.6
0x17	0.036	0x57	0.260	0x97	0.66	0xD7	5.8
0x18	0.038	0x58	0.265	0x98	0.67	0xD8	6.0
0x19	0.040	0x59	0.270	0x99	0.68	0xD9	6.2
0x1A	0.042	0x5A	0.275	0x9A	0.69	0xDA	6.4
0x1B	0.044	0x5B	0.280	0x9B	0.70	0xDB	6.6
0x1C	0.046	0x5C	0.285	0x9C	0.72	0xDC	6.8
0x1D	0.048	0x5D	0.290	0x9D	0.74	0xDD	7.0
0x1E	0.050	0x5E	0.295	0x9E	0.76	0xDE	7.2
0x1F	0.052	0x5F	0.300	0x9F	0.78	0xDF	7.4
0x20	0.054	0x60	0.305	0xA0	0.80	0xE0	7.6
0x21	0.056	0x61	0.310	0xA1	0.82	0xE1	7.8
0x22	0.058	0x62	0.315	0xA2	0.84	0xE2	8.0
0x23	0.060	0x63	0.320	0xA3	0.86	0xE3	8.2
0x24	0.062	0x64	0.325	0xA4	0.88	0xE4	8.4
0x25	0.064	0x65	0.330	0xA5	0.90	0xE5	8.6
0x26	0.066	0x66	0.335	0xA6	0.92	0xE6	8.8
0x27	0.068	0x67	0.340	0xA7	0.94	0xE7	9
0x28	0.070	0x68	0.345	0xA8	0.96	0xE8	9.2

Table 7-2. Motor Resistance Look-Up Table (continued)

MOTOR_RES (HEX)	R_{PH} (Ω)	MOTOR_RES (HEX)	R_{PH} (Ω)	MOTOR_RES (HEX)	R_{PH} (Ω)	MOTOR_RES (HEX)	R_{PH} (Ω)
0x29	0.072	0x69	0.350	0xA9	0.98	0xE9	9.4
0x2A	0.074	0x6A	0.355	0xAA	1.00	0xEA	9.6
0x2B	0.076	0x6B	0.360	0xAB	1.05	0xEB	9.8
0x2C	0.078	0x6C	0.365	0xAC	1.10	0xEC	10.0
0x2D	0.080	0x6D	0.370	0xAD	1.15	0xED	10.5
0x2E	0.082	0x6E	0.375	0xAE	1.20	0xEE	11.0
0x2F	0.084	0x6F	0.380	0xAF	1.25	0xEF	11.5
0x30	0.086	0x70	0.385	0xB0	1.30	0xF0	12.0
0x31	0.088	0x71	0.390	0xB1	1.35	0xF1	12.5
0x32	0.090	0x72	0.395	0xB2	1.40	0xF2	13.0
0x33	0.092	0x73	0.400	0xB3	1.45	0xF3	13.5
0x34	0.094	0x74	0.405	0xB4	1.50	0xF4	14.0
0x35	0.096	0x75	0.410	0xB5	1.55	0xF5	14.5
0x36	0.098	0x76	0.415	0xB6	1.60	0xF6	15.0
0x37	0.100	0x77	0.420	0xB7	1.65	0xF7	15.5
0x38	0.105	0x78	0.425	0xB8	1.70	0xF8	16.0
0x39	0.110	0x79	0.430	0xB9	1.75	0xF9	16.5
0x3A	0.115	0x7A	0.435	0xBA	1.80	0xFA	17.0
0x3B	0.120	0x7B	0.440	0xBB	1.85	0xFB	17.5
0x3C	0.125	0x7C	0.445	0xBC	1.90	0xFC	18.0
0x3D	0.130	0x7D	0.450	0xBD	1.95	0xFD	18.5
0x3E	0.135	0x7E	0.455	0xBE	2.00	0xFE	19.0
0x3F	0.140	0x7F	0.460	0xBF	2.05	0xFF	20.0

7.3.14.2 Motor Inductance

For a wye-connected motor, the motor phase inductance refers to the inductance from the phase output to the center tap, L_{PH} (denoted as L_{PH} in Figure 7-36). For a delta-connected motor, the motor phase inductance refers to the equivalent phase to center tap in the wye configuration in Figure 7-36.

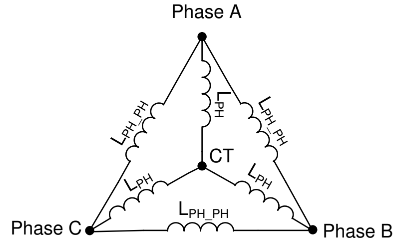

Figure 7-36. Motor Inductance

For both the delta-connected motor and the wye-connected motor, the easy way to get the equivalent L_{PH} is to measure the inductance between two phase terminals (L_{PH_PH}), and then divide this value by two, L_{PH} = ½ L_{PH_PH}. In wye-connected motor, if user has access to center tap (CT), L_{PH} can also be measured between center tap (CT) and phase terminal.

Configure the motor inductance (L_{PH}) to a nearest value from Table 7-3.

Table 7-3. Motor Inductance Look-Up Table

MOTOR_IND (HEX)	L_{PH} (mH)	MOTOR_IND (HEX)	L_{PH} (mH)	MOTOR_IND (HEX)	L_{PH} (mH)	MOTOR_IND (HEX)	L_{PH} (mH)
0x00	Not Valid	0x40	0.145	0x80	0.465	0xC0	2.1
0x01	0.006	0x41	0.150	0x81	0.470	0xC1	2.2
0x02	0.007	0x42	0.155	0x82	0.475	0xC2	2.3
0x03	0.008	0x43	0.160	0x83	0.480	0xC3	2.4
0x04	0.009	0x44	0.165	0x84	0.485	0xC4	2.5
0x05	0.010	0x45	0.170	0x85	0.490	0xC5	2.6
0x06	0.011	0x46	0.175	0x86	0.495	0xC6	2.7
0x07	0.012	0x47	0.180	0x87	0.50	0xC7	2.8
0x08	0.013	0x48	0.185	0x88	0.51	0xC8	2.9
0x09	0.014	0x49	0.190	0x89	0.52	0xC9	3.0
0x0A	0.015	0x4A	0.195	0x8A	0.53	0xCA	3.2
0x0B	0.016	0x4B	0.200	0x8B	0.54	0xCB	3.4
0x0C	0.017	0x4C	0.205	0x8C	0.55	0xCC	3.6
0x0D	0.018	0x4D	0.210	0x8D	0.56	0xCD	3.8
0x0E	0.019	0x4E	0.215	0x8E	0.57	0xCE	4.0
0x0F	0.020	0x4F	0.220	0x8F	0.58	0xCF	4.2
0x10	0.022	0x50	0.225	0x90	0.59	0xD0	4.4
0x11	0.024	0x51	0.230	0x91	0.60	0xD1	4.6
0x12	0.026	0x52	0.235	0x92	0.61	0xD2	4.8
0x13	0.028	0x53	0.240	0x93	0.62	0xD3	5.0
0x14	0.030	0x54	0.245	0x94	0.63	0xD4	5.2
0x15	0.032	0x55	0.250	0x95	0.64	0xD5	5.4
0x16	0.034	0x56	0.255	0x96	0.65	0xD6	5.6
0x17	0.036	0x57	0.260	0x97	0.66	0xD7	5.8
0x18	0.038	0x58	0.265	0x98	0.67	0xD8	6.0
0x19	0.040	0x59	0.270	0x99	0.68	0xD9	6.2
0x1A	0.042	0x5A	0.275	0x9A	0.69	0xDA	6.4
0x1B	0.044	0x5B	0.280	0x9B	0.70	0xDB	6.6
0x1C	0.046	0x5C	0.285	0x9C	0.72	0xDC	6.8
0x1D	0.048	0x5D	0.290	0x9D	0.74	0xDD	7.0
0x1E	0.050	0x5E	0.295	0x9E	0.76	0xDE	7.2
0x1F	0.052	0x5F	0.300	0x9F	0.78	0xDF	7.4
0x20	0.054	0x60	0.305	0xA0	0.80	0xE0	7.6
0x21	0.056	0x61	0.310	0xA1	0.82	0xE1	7.8
0x22	0.058	0x62	0.315	0xA2	0.84	0xE2	8.0
0x23	0.060	0x63	0.320	0xA3	0.86	0xE3	8.2
0x24	0.062	0x64	0.325	0xA4	0.88	0xE4	8.4
0x25	0.064	0x65	0.330	0xA5	0.90	0xE5	8.6
0x26	0.066	0x66	0.335	0xA6	0.92	0xE6	8.8
0x27	0.068	0x67	0.340	0xA7	0.94	0xE7	9
0x28	0.070	0x68	0.345	0xA8	0.96	0xE8	9.2
0x29	0.072	0x69	0.350	0xA9	0.98	0xE9	9.4
0x2A	0.074	0x6A	0.355	0xAA	1.00	0xEA	9.6
0x2B	0.076	0x6B	0.360	0xAB	1.05	0xEB	9.8

Table 7-3. Motor Inductance Look-Up Table (continued)

MOTOR_IND (HEX)	L_{PH} (mH)	MOTOR_IND (HEX)	L_{PH} (mH)	MOTOR_IND (HEX)	L_{PH} (mH)	MOTOR_IND (HEX)	L_{PH} (mH)
0x2C	0.078	0x6C	0.365	0xAC	1.10	0xEC	10.0
0x2D	0.080	0x6D	0.370	0xAD	1.15	0xED	10.5
0x2E	0.082	0x6E	0.375	0xAE	1.20	0xEE	11.0
0x2F	0.084	0x6F	0.380	0xAF	1.25	0xEF	11.5
0x30	0.086	0x70	0.385	0xB0	1.30	0xF0	12.0
0x31	0.088	0x71	0.390	0xB1	1.35	0xF1	12.5
0x32	0.090	0x72	0.395	0xB2	1.40	0xF2	13.0
0x33	0.092	0x73	0.400	0xB3	1.45	0xF3	13.5
0x34	0.094	0x74	0.405	0xB4	1.50	0xF4	14.0
0x35	0.096	0x75	0.410	0xB5	1.55	0xF5	14.5
0x36	0.098	0x76	0.415	0xB6	1.60	0xF6	15.0
0x37	0.100	0x77	0.420	0xB7	1.65	0xF7	15.5
0x38	0.105	0x78	0.425	0xB8	1.70	0xF8	16.0
0x39	0.110	0x79	0.430	0xB9	1.75	0xF9	16.5
0x3A	0.115	0x7A	0.435	0xBA	1.80	0xFA	17.0
0x3B	0.120	0x7B	0.440	0xBB	1.85	0xFB	17.5
0x3C	0.125	0x7C	0.445	0xBC	1.90	0xFC	18.0
0x3D	0.130	0x7D	0.450	0xBD	1.95	0xFD	18.5
0x3E	0.135	0x7E	0.455	0xBE	2.00	0xFE	19.0
0x3F	0.140	0x7F	0.460	0xBF	2.05	0xFF	20.0

7.3.14.3 Motor Back-EMF constant

The back-EMF constant describes the motor phase-to-neutral back-EMF voltage as a function of the motor speed. For a wye-connected motor, the motor BEMF constant refers to the BEMF as a function of time from the phase output to the center tap, Kt_{PH_N} (denoted as Kt_{PH_N} in Figure 7-37). For a delta-connected motor, the motor BEMF constant refers to the equivalent phase to center tap in the wye configuration in Figure 7-37.

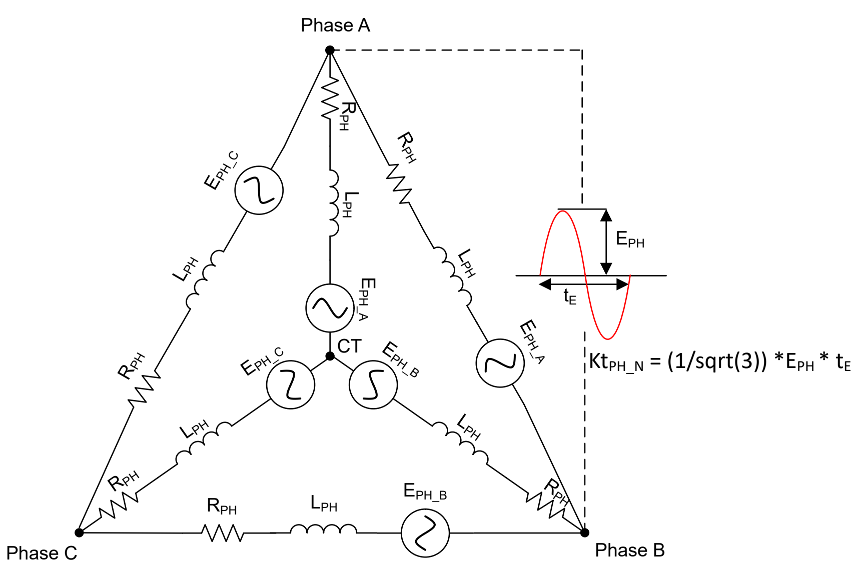

Figure 7-37. Motor back-EMF constant

For both the delta-connected motor and the wye-connected motor, the easy way to get the equivalent Kt_{PH_N} is to measure the peak value of BEMF on scope for one electrical cycle between two phase terminals (E_{PH}), and then multiply by time duration of one electrical cycle and in order to convert from phase-to-phase to phase-to-neutral divide by sqrt(3) as shown in Equation 12 .

$$Kt_{PH\_N} = {}^{1}\!/_{\sqrt{3}} \times E_{PH} \times t_E \quad (12)$$

Configure the motor BEMF constant (Kt_{PH_N}) to a nearest value from Table 7-4.

Table 7-4. Motor BEMF constant Look-Up Table

MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)
0x00	Self Measurement (see Motor Parameter Extraction Tool (MPET))	0x40	14.5	0x80	46.5	0xC0	210
0x01	0.6	0x41	15.0	0x81	47.0	0xC1	220
0x02	0.7	0x42	15.5	0x82	47.5	0xC2	230
0x03	0.8	0x43	16.0	0x83	48.0	0xC3	240
0x04	0.9	0x44	16.5	0x84	48.5	0xC4	250
0x05	1.0	0x45	17.0	0x85	49.0	0xC5	260
0x06	1.1	0x46	17.5	0x86	49.5	0xC6	270
0x07	1.2	0x47	18.0	0x87	50.0	0xC7	280
0x08	1.3	0x48	18.5	0x88	51	0xC8	290
0x09	1.4	0x49	19.0	0x89	52	0xC9	300
0x0A	1.5	0x4A	19.5	0x8A	53	0xCA	320
0x0B	1.6	0x4B	20.0	0x8B	54	0xCB	340
0x0C	1.7	0x4C	20.5	0x8C	55	0xCC	360
0x0D	1.8	0x4D	21.0	0x8D	56	0xCD	380
0x0E	1.9	0x4E	21.5	0x8E	57	0xCE	400
0x0F	2.0	0x4F	22.0	0x8F	58	0xCF	420
0x10	2.2	0x50	22.5	0x90	59	0xD0	440
0x11	2.4	0x51	23.0	0x91	60	0xD1	460
0x12	2.6	0x52	23.5	0x92	61	0xD2	480
0x13	2.8	0x53	24.0	0x93	62	0xD3	500
0x14	3.0	0x54	24.5	0x94	63	0xD4	520
0x15	3.2	0x55	25.0	0x95	64	0xD5	540
0x16	3.4	0x56	25.5	0x96	65	0xD6	560
0x17	3.6	0x57	26.0	0x97	66	0xD7	580
0x18	3.8	0x58	26.5	0x98	67	0xD8	600
0x19	4.0	0x59	27.0	0x99	68	0xD9	620
0x1A	4.2	0x5A	27.5	0x9A	69	0xDA	640
0x1B	4.4	0x5B	28.0	0x9B	70	0xDB	660
0x1C	4.6	0x5C	28.5	0x9C	72	0xDC	680
0x1D	4.8	0x5D	29.0	0x9D	74	0xDD	700
0x1E	5.0	0x5E	29.5	0x9E	76	0xDE	720
0x1F	5.2	0x5F	30.0	0x9F	78	0xDF	740
0x20	5.4	0x60	30.5	0xA0	80	0xE0	760

Table 7-4. Motor BEMF constant Look-Up Table (continued)

MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)	MOTOR_BEMF_CONST (HEX)	Kt_{PH_N} (mV/Hz)
0x21	5.6	0x61	31.0	0xA1	82	0xE1	780
0x22	5.8	0x62	31.5	0xA2	84	0xE2	800
0x23	6.0	0x63	32.0	0xA3	86	0xE3	820
0x24	6.2	0x64	32.5	0xA4	88	0xE4	840
0x25	6.4	0x65	33.0	0xA5	90	0xE5	860
0x26	6.6	0x66	33.5	0xA6	92	0xE6	880
0x27	6.8	0x67	34.0	0xA7	94	0xE7	900
0x28	7.0	0x68	34.5	0xA8	96	0xE8	920
0x29	7.2	0x69	35.0	0xA9	98	0xE9	940
0x2A	7.4	0x6A	35.5	0xAA	100	0xEA	960
0x2B	7.6	0x6B	36.0	0xAB	105	0xEB	980
0x2C	7.8	0x6C	36.5	0xAC	110	0xEC	1000
0x2D	8.0	0x6D	37.0	0xAD	115	0xED	1050
0x2E	8.2	0x6E	37.5	0xAE	120	0xEE	1100
0x2F	8.4	0x6F	38.0	0xAF	125	0xEF	1150
0x30	8.6	0x70	38.5	0xB0	130	0xF0	1200
0x31	8.8	0x71	39.0	0xB1	135	0xF1	1250
0x32	9.0	0x72	39.5	0xB2	140	0xF2	1300
0x33	9.2	0x73	40.0	0xB3	145	0xF3	1350
0x34	9.4	0x74	40.5	0xB4	150	0xF4	1400
0x35	9.6	0x75	41.0	0xB5	155	0xF5	1450
0x36	9.8	0x76	41.5	0xB6	160	0xF6	1500
0x37	10.0	0x77	42.0	0xB7	165	0xF7	1550
0x38	10.5	0x78	42.5	0xB8	170	0xF8	1600
0x39	11.0	0x79	43.0	0xB9	175	0xF9	1650
0x3A	11.5	0x7A	43.5	0xBA	180	0xFA	1700
0x3B	12.0	0x7B	44.0	0xBB	185	0xFB	1750
0x3C	12.5	0x7C	44.5	0xBC	190	0xFC	1800
0x3D	13.0	0x7D	45.0	0xBD	195	0xFD	1850
0x3E	13.5	0x7E	45.5	0xBE	200	0xFE	1900
0x3F	14.0	0x7F	46.0	0xBF	205	0xFF	2000

7.3.15 Motor Parameter Extraction Tool (MPET)

The MCF8329A uses motor winding resistance, motor winding inductance and Back-EMF constant to estimate motor position in closed loop operation. The MPET routine measures motor back EMF constant and mechanical load inertia and frictional coefficients. Offline measurement of parameters takes place before normal motor operation. TI recommends to estimate the motor parameters before motor start-up to minimize the impact caused due to possible parameter variations.

Figure 7-38 shows the sequence of operation in the MPET routine. The MPET routine is entered when either the MPET_CMD bit is set to 1b or a non-zero target speed is set. The MPET routine consists of four steps namely, IPD, Open Loop Acceleration, Current Ramp Down and Coasting. Each one of these steps are executed if the condition shown in Figure 7-38 evaluates to TRUE; if the condition evaluates to FALSE, the algorithm bypasses that particular step and moves on to the next step in the sequence. Once all the steps are completed (or bypassed), the algorithm exits the MPET routine. If target speed is set to a non-zero value, the algorithm begins the start-up and acceleration sequence (to target speed reference) once MPET routine is exited.

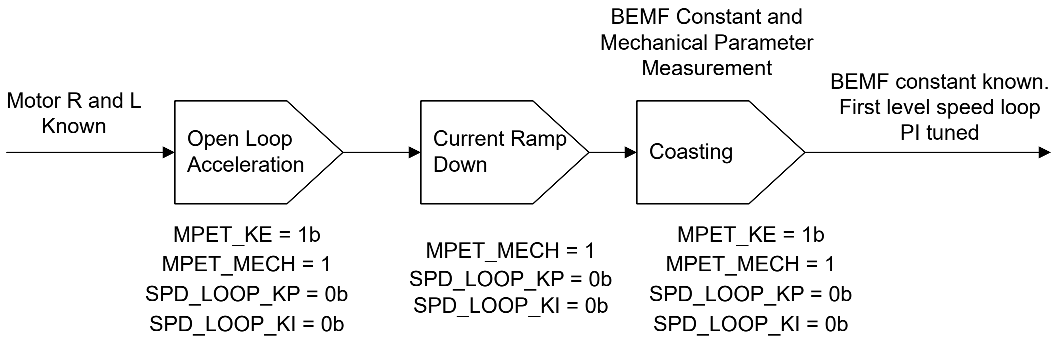

Figure 7-38. MPET Sequence

TI proprietary MPET routine includes following sequence of operation.

- **Open loop Acceleration**: The MPET routine run align and then open loop acceleration if the back-EMF constant or mechanical parameter measurement are enabled by setting MPET_KE = 1b and MPET_MECH = 1b. The MPET routine incorporates the sequences for mechanical parameter measurement, if the speed loop PI constants are defined as zero, even if MPET_MECH = 0b. User can configure MPET specific open loop configuration parameters or use normal motor operation open loop configuration parameters. The open loop configuration selection is done using MPET_KE_MEAS_PARAMETER_SELECT. With MPET_KE_MEAS_PARAMETER_SELECT = 1b, the speed slew rate is defined using MPET_OPEN_LOOP_SLEW_RATE, the open loop current reference is defined using MPET_OPEN_LOOP_CURR_REF and the open loop speed reference is defined using MPET_OPEN_LOOP_SPEED_REF. With MPET_KE_MEAS_PARAMETER_SELECT = 0b, the speed slew rate is defined using OL_ACC_A1 and OL_ACC_A2, the current reference is OL_ILIMIT, and speed ref is OPN_CL_HANDOFF_THR speed.
- **Current Ramp Down**: After open loop acceleration, if the mechanical parameter measurement is enabled, then the MPET routine optimizes the motor current to lower value sufficient to support the load. If mechanical parameter measurement is disabled (MPET_MECH = 0b, or non-zero speed loop PI parameters) then the MPET will not have the current ramp down sequence.
- **Coasting**: MPET routine completes the sequence by allowing the motor to coast by enabling Hi-Z. The motor back EMF and indicative values of mechanical parameters are measured during the motor coasting period. If the motor back EMF is lower than the threshold defined in STAT_DETECT_THR, the MPET_BEMF_FAULT is generated.

Selecting the parameters from EEPROM or MPET

The MPET estimated values are available in the MTR_PARAMS Register. Setting the MPET_WRITE_SHADOW bit to 1, writes the MPET estimated values to the shadow registers and the user-configured (from EEPROM) values in MOTOR_BEMF_CONST, SPD_LOOP_KP and SPD_LOOP_KI shadow registers will be overwritten by the estimated values from MPET. If any of the shadow registers are initialized to zero (from EEPROM registers), the MPET estimated values are used for those registers independent of the MPET_WRITE_SHADOW setting. The MPET calculates the current loop KP and KI by using the user entered resistance and inductance. The MPET does an estimation of the mechanical parameters including the inertia and frictional coefficient at the shaft (includes both motor and shaft coupled load). These values are used to set an initial values speed loop KP and KI. The estimated speed loop KP and KI setting can be used as an initial setting only and TI recommends to tune these parameters on application by the user based on the performance requirement.

Note

1. TI recommends to set the bit VdcFilterDisable to 1b during MPET measurement.
2. FG signal is not accurate during MPET.
3. If CURRENT_LOOP_KP and CURRENT_LOOP_KI are set to zero, then MCF8329A automatically calculate these coefficients using motor resistance and inductance values.

7.3.16 Anti-Voltage Surge (AVS)

When a motor is driven, energy is transferred from the power supply into the motor. Some of this energy is stored in the form of inductive and mechanical energy. If the speed command suddenly drops such that the BEMF voltage generated by the motor is greater than the voltage that is applied to the motor, then the mechanical energy of the motor is returned to the power supply and the V_{PVDD} voltage surges. The AVS feature works to prevent this voltage surge on V_{PVDD} and can be enabled by setting AVS_EN to 1b. AVS can be disabled by setting AVS_EN to 0b. When AVS is disabled, the deceleration rate is configured through CL_DEC_CONFIG.

7.3.17 Output PWM Switching Frequency

The MCF8329A provides the option to configure the output PWM switching frequency of the MOSFETs through PWM_FREQ_OUT. PWM_FREQ_OUT has range of 10-75 kHz. In order to select optimal output PWM switching frequency, user has to make tradeoff between the current ripple and the switching losses. Generally, motors having lower L/R ratio require higher PWM switching frequency to reduce current ripple.

Note

PWM frequency in multiples of 15 kHz enables high current loop bandwidth and gives best performance at high speed motor operation.

7.3.18 Active Braking

Decelerating the motor quickly requires the motor mechanical energy to be extracted from the rotor in a fast and controlled manner. However, the DC supply voltage increases if the motor mechanical energy is returned to the power supply during the deceleration process. MCF8329A is capable of decelerating the motor quickly without pumping energy back into the supply voltage by using a novel technique called active braking. ACTIVE_BRAKE_EN should be set to 1b to enable active braking and prevent DC bus voltage spike during fast motor deceleration. Active braking can also be used during reverse drive (see Reverse Drive) or motor stop (see Active Spin-Down) to reduce the motor speed quickly without DC voltage spike.

The maximum limit on the current sourced from the DC bus (i_{dc_ref}) during active braking can be configured using ACTIVE_BRAKE_CURRENT_LIMIT. The power flow control during active braking is achieved by using both Q-axis (i_q) and D-axis (i_d) components of current. The D-axis current reference (i_{d_ref}) is generated from the error between DC bus current limit (i_{dc_ref}) and the estimated DC bus current (i_{dc}) using a PI controller. The i_{dc} value is estimated from the measured phase currents, phase voltage and DC bus voltage, using power balance equation (equating the instantaneous DC bus power to sum of all three instantaneous phase power assuming 100% efficiency). During active braking, the DC bus current limit (i_{dc_ref}) starts from zero and linearly increases to ACTIVE_BRAKE_CURRENT_LIMIT with current slew rate as defined by ACTIVE_BRAKE_BUS_CURRENT_SLEW_RATE. The gain constants of PI controller can be configured using ACTIVE_BRAKE_KP and ACTIVE_BRAKE_KI. Figure 7-39 shows the active braking id current control loop.

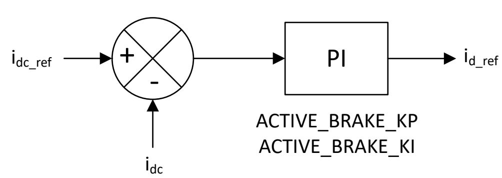

Figure 7-39. Active Braking Current Control Loop for i_{d_ref}

ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY sets the minimum difference between the initial and target speed above which active braking will be entered. For example, consider ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY is set to 10%; if the initial speed is 100% and target speed is set to 95%, MCF8329A uses AVS instead of active braking to reach 95% speed since the difference in commanded speed change (5%) is less than ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY (10%).

ACTIVE_BRAKE_SPEED_DELTA_LIMIT_EXIT sets the difference between the current and target speed below which active braking will be exited. For example, consider ACTIVE_BRAKE_SPEED_DELTA_LIMIT_EXIT is set to 5%; if the initial motor speed is 100% and target speed is set to 10%, MCF8329A uses active braking to reduce the motor speed to 15%; upon reaching 15% speed, MCF8329A exits active braking and uses AVS to decelerate the motor speed to 10%.

ACTIVE_BRAKE_MOD_INDEX_LIMIT sets the modulation index below which active braking will be used. For example, consider ACTIVE_BRAKE_MOD_INDEX_LIMIT is set to 50%, ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY is set to 5%, ACTIVE_BRAKE_SPEED_DELTA_LIMIT_EXIT is set to 2.5%. If the initial motor speed is at 70% (corresponding modulation index is 90%) and target speed is 40% (corresponding modulation index is 60%), MCF8329A uses AVS to decelerate the motor till target speed of 40% since the modulation index (60%) corresponding to final speed is higher than ACTIVE_BRAKE_MOD_INDEX_LIMIT of 50%. In the same case, if final speed command is 10% (corresponding modulation index is 30%), MCF8329A uses AVS till 30% speed (corresponding modulation index is 50%), switches to active braking from 30% to 15% speed (final speed of 10% + ACTIVE_BRAKE_SPEED_DELTA_LIMIT_EXIT of 5%) and uses AVS again from 15% to 10% speed to complete the active braking. TI recommends starting active braking tuning with ACTIVE_BRAKE_MOD_INDEX_LIMIT set to 100%; if there is a DC bus voltage spike observed during active braking, reduce ACTIVE_BRAKE_MOD_INDEX_LIMIT in steps so as to eliminate this voltage spike. If ACTIVE_BRAKE_MOD_INDEX_LIMIT is set to 0%, MCF8329A decelerates in AVS (even when ACTIVE_BRAKE_EN is set to 1b) in the forward direction; in reverse direction (during direction change), ACTIVE_BRAKE_MOD_INDEX_LIMIT is not applicable and therefore MCF8329A decelerates in active braking.

Note

1. ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY, ACTIVE_BRAKE_SPEED_DELTA_LIMIT_EXIT and ACTIVE_BRAKE_MOD_INDEX_LIMIT are applicable only during deceleration in forward direction and not used during direction change.
2. ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY should be set higher than ACTIVE_BRAKE_SPEED_DELTA_LIMIT_EXIT for active braking operation.
3. During active (or closed loop) braking, I_{q_ref} is clamped to -ILIMIT. This (I_{q_ref} being clamped to -ILIMIT) may result in the speed PI loop getting saturated and SPEED_LOOP_SATURATION bit getting set to 1b during deceleration. This bit is automatically set to 0b once the deceleration is completed and the speed PI loop is out of saturation. Hence, speed loop saturation fault should be ignored during deceleration.
4. Active braking is only available in speed control mode.

7.3.19 Dead Time Compensation

Dead time is inserted between the switching instants of high-side and low-side MOSFET in a half bridge leg to avoid shoot-through condition. Due to dead time insertion, the expected voltage and applied voltage at the phase node differ based on the phase current direction. The phase node voltage distortion introduces undesired distortion in the phase current causing audible noise. The distortion in current waveform due to dead time appear as sixth harmonic of fundamental frequency in the dq reference frame. The MCF8329A integrates a proprietary dead time compensation, so that the current distortion due to dead time is alleviated. The dead time compensation can be enabled or disabled by configuring DEADTIME_COMP_EN. Even when DEADTIME_COMP_EN is set to 1b (compensation enabled), dead time compensation is disabled when motor electrical frequency exceeds 108-Hz.

7.3.20 Voltage Sense Scaling

The MCF8329A integrates dynamic voltage scaling to improve the resolution of phase voltage and DC bus voltage sensing. The DC bus voltage is sensed at the PVDD pin. The motor phase voltage and DC bus voltage is sensed using an integrated voltage divider with voltage scaling of 5 V/V or 10 V/V or 20 V/V, to limit the sense voltage to less than 3-V across operating voltage. Setting the bit DYN_VOLT_SCALING_EN = 0b disables dynamic voltage scaling and MCF8329A uses 20 V/V gain. Setting the bit DYN_VOLT_SCALING_EN = 1b enables dynamic voltage scaling and MCF8329A sense the DC bus voltage during motor start up and select the appropriate voltage scaling of 5 V/V or 10 V/V or 20 V/V.

Note

TI recommends to disable dynamic voltage scaling in case of DC bus voltage more than 15 V is expected.

7.3.21 Motor Stop Options

The MCF8329A provides different options for stopping the motor which can be configured by MTR_STOP.

7.3.21.1 Coast (Hi-Z) Mode

Coast (Hi-Z) mode is configured by setting MTR_STOP to 000b. When motor stop command is received, the MCF8329A turns off all the external MOSFETs creating Hi-Z state at the phase motor terminals. When the MCF8329A transitions from driving the motor into a Hi-Z state, the inductive current in the motor windings continues to flow and the energy returns to the power supply through the body diodes in the MOSFET output stage (see example Figure 7-40).

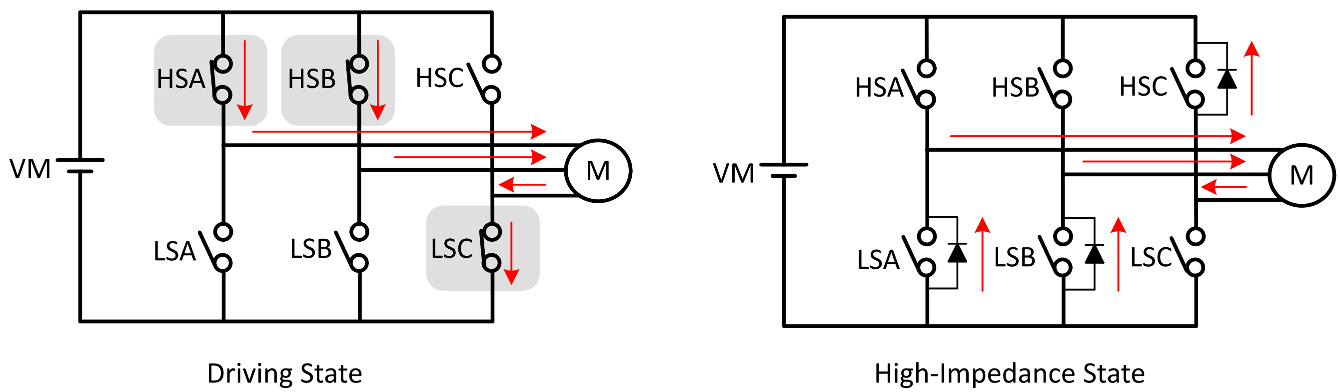

Figure 7-40. Coast (Hi-Z) Mode

In this example, current is applied to the motor through the high-side phase-A MOSFET (HSA), high-side phase-B MOSFET(HSB) and returned through the low-side phase-C MOSFET (LSC). When motor stop command is received all 6 MOSFETs transition to Hi-Z state and the inductive energy returns to supply through body diodes of MOSFETs LSA, LSB and HSC.

7.3.21.2 Recirculation Mode

Recirculation mode is configured by setting MTR_STOP to 001b. In order to prevent the inductive energy from returning to DC input supply during motor stop, the MCF8329A allows current to circulate within the external MOSFETs by selectively turning OFF some of the active (ON) MOSFETs for a certain time (auto calculated recirculation time to allow the inductive current to decay to zero) before transitioning into Hi-Z by turning OFF the remaining MOSFETs.

Depending on the phase voltage pattern at the time of receiving the stop command, either low-side (see Figure 7-41) or high-side recirculation (see Figure 7-42) will be used to stop the motor without sending the inductive energy back to the DC input supply.

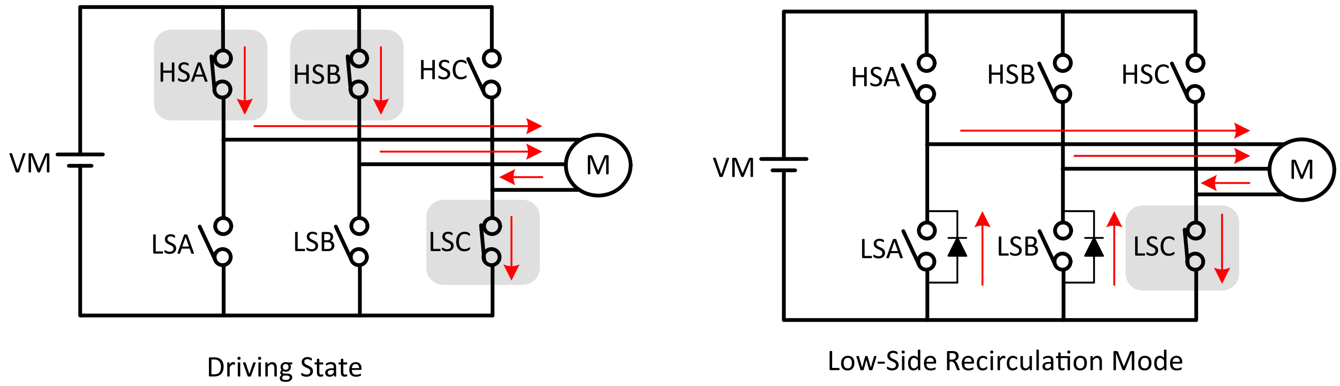

Figure 7-41. Low-Side Recirculation

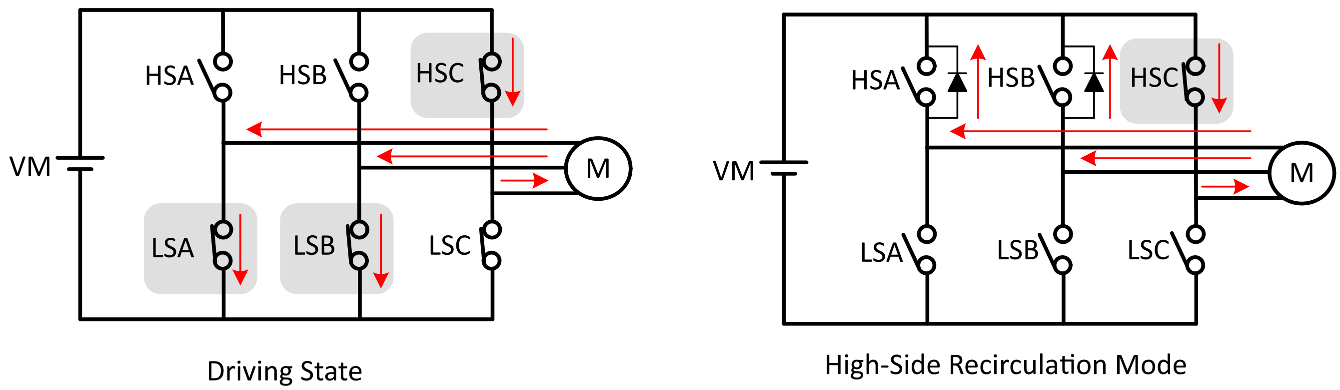

Figure 7-42. High-Side Recirculation

Note

1. Recirculation stop is not supported when the motor is in flux weakening zone or MTPA or in active brake mode, and when motor is in any of these states then recirculation stop mode is over written with Hi-Z.
2. Recirculation mode is not supported in modulation index control mode and TI recommends to use other stop modes if modulation index control mode is used.

7.3.21.3 Low-Side Braking

Low-side braking mode is configured by setting MTR_STOP to 010b or 011b. When a motor stop command is received, the output speed is reduced to a value defined by BRAKE_SPEED_THRESHOLD prior to turning all low-side MOSFETs ON (see example Figure 7-43) for a time configured by MTR_STOP_BRK_TIME. If the motor speed is below BRAKE_SPEED_THRESHOLD prior to receiving stop command, then the MCF8329A transitions directly into the brake state. After applying the brake for MTR_STOP_BRK_TIME, the MCF8329A transitions into the Hi-Z state by turning OFF all MOSFETs.

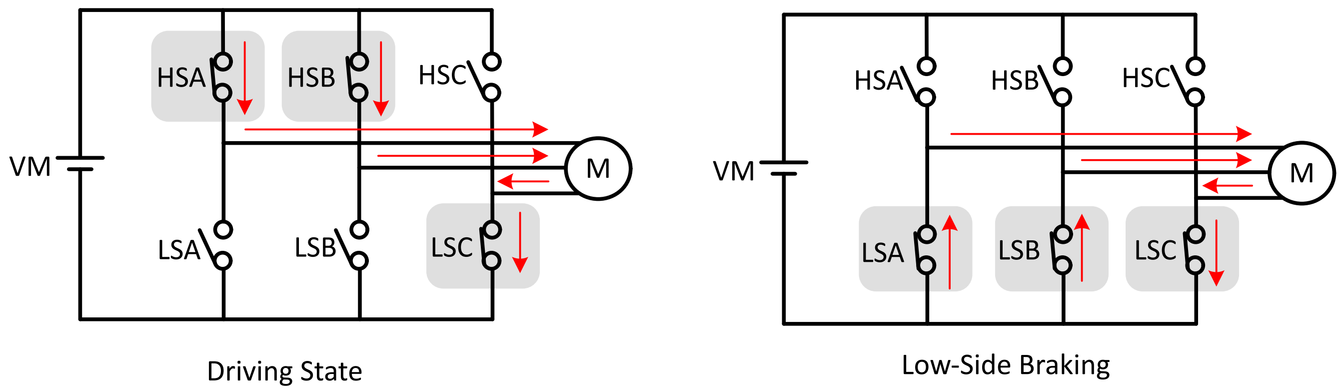

Figure 7-43. Low-Side Braking

The MCF8329A can also enter low-side braking through BRAKE pin input. When BRAKE pin is pulled to HIGH state, the output speed is reduced to a value defined by BRAKE_SPEED_THRESHOLD prior to turning all low-side MOSFETs ON. In this case, MCF8329A stays in low-side brake state till BRAKE pin changes to LOW state.

7.3.21.4 Active Spin-Down

Active spin down mode is configured by setting MTR_STOP to 100b. When a motor stop command is received, the MCF8329A reduces SPEED_REF to ACT_SPIN_THR and then transitions to Hi-Z state by turning all MOSFETs OFF. The advantage of this mode is that by reducing SPEED_REF, the motor is decelerated to lower speed thereby reducing the phase currents before entering Hi-Z. Now, when the motor transitions into Hi-Z state, the energy transfer to the power supply is reduced. The threshold ACT_SPIN_THR needs to configured high enough for MCF8329A to not lose synchronization with the motor.

7.3.22 FG Configuration

The MCF8329A provides information about the motor speed through the Frequency Generate (FG) pin. In MCF8329A, the FG pin output is configured through FG_CONFIG. When FG_CONFIG is configured to 0b, the FG output is active as long as the MCF8329A is driving the motor. When FG_CONFIG is configured to 1b, the MCF8329A provides an FG output as long as the MCF8329A is driving the motor and also during coasting until the motor back-EMF falls below the threshold configured by FG_BEMF_THR.

7.3.22.1 FG Output Frequency

The FG output frequency can be configured by FG_DIV. Many applications require the FG output to provide a pulse for every mechanical rotation of the motor Different FG_DIV configurations can accomplish this for 2-pole up to 30-pole motors.

Figure 7-44 shows the FG output when MCF8329A has been configured to provide FG pulses once every electrical cycle (2 poles), once every two electrical cycle (4 poles), once every three electrical cycles (6 poles), once every four electrical cycles (8 poles), and so on.

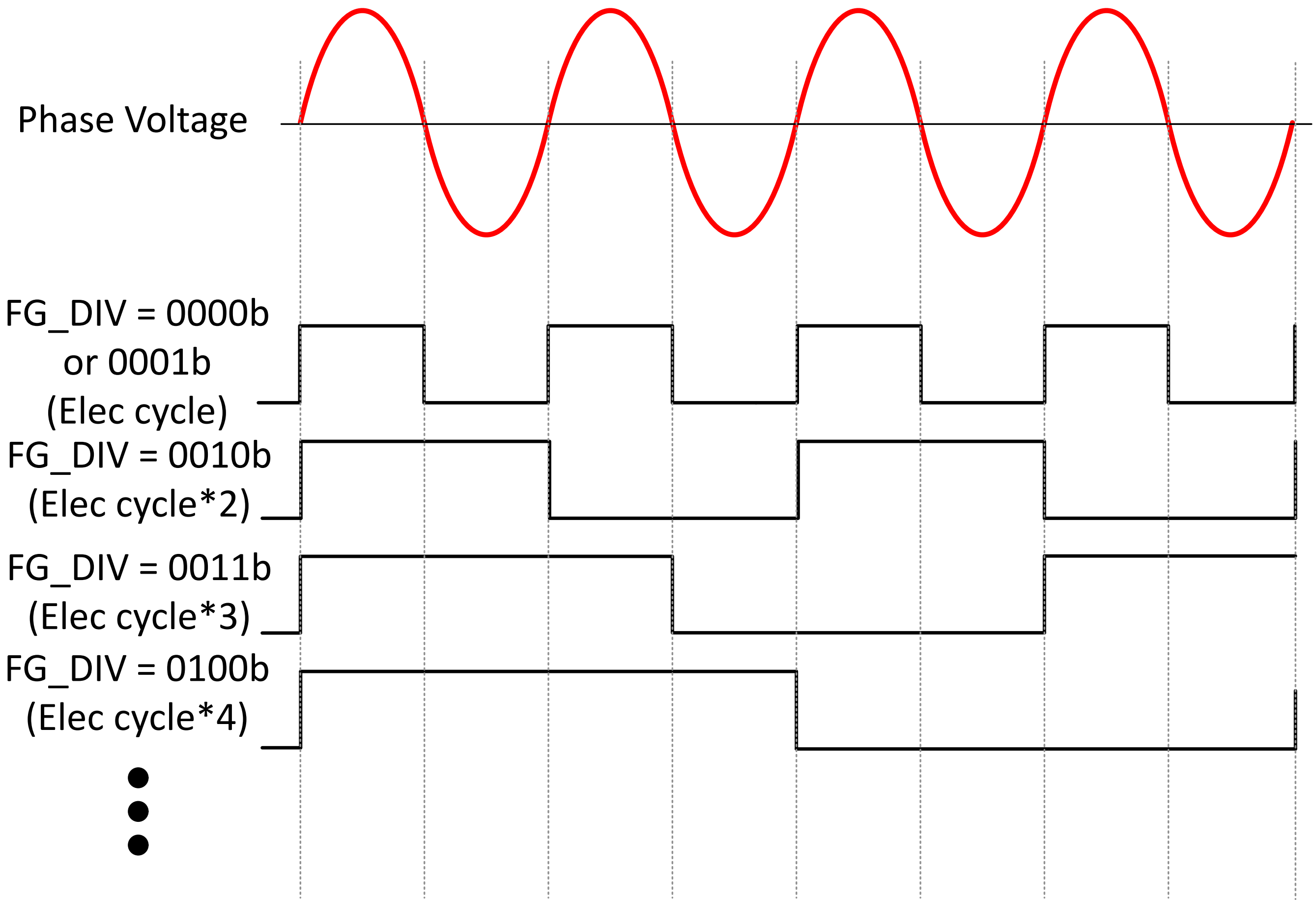

Figure 7-44. FG Frequency Divider

7.3.22.2 FG in Open-Loop

During closed loop (commutation) operation, the driving speed (FG output frequency) and the actual motor speed are synchronized. During open-loop operation, however, FG may not reflect the actual motor speed. The open loop and closed loop here refers to the motor commutation method and not referred to closed loop speed or power control.

The MCF8329A provides three options for controlling the FG output during open loop, as shown in Figure 7-45. The selection of these options is configured through FG_SEL.

If FG_SEL is set to,

- 00b : Output FG in ISD, open loop and closed loop.
- 01b : Output FG in only closed loop. FG pin will be Hi-Z (high with external pull up) during open loop.
- 10b: The FG output will reflect the driving frequency during open loop operation in the first motor start-up cycle after power-on, sleep/standby; FG will be Hi-Z (high with external pull up) during open loop operation in subsequent start-up cycles.

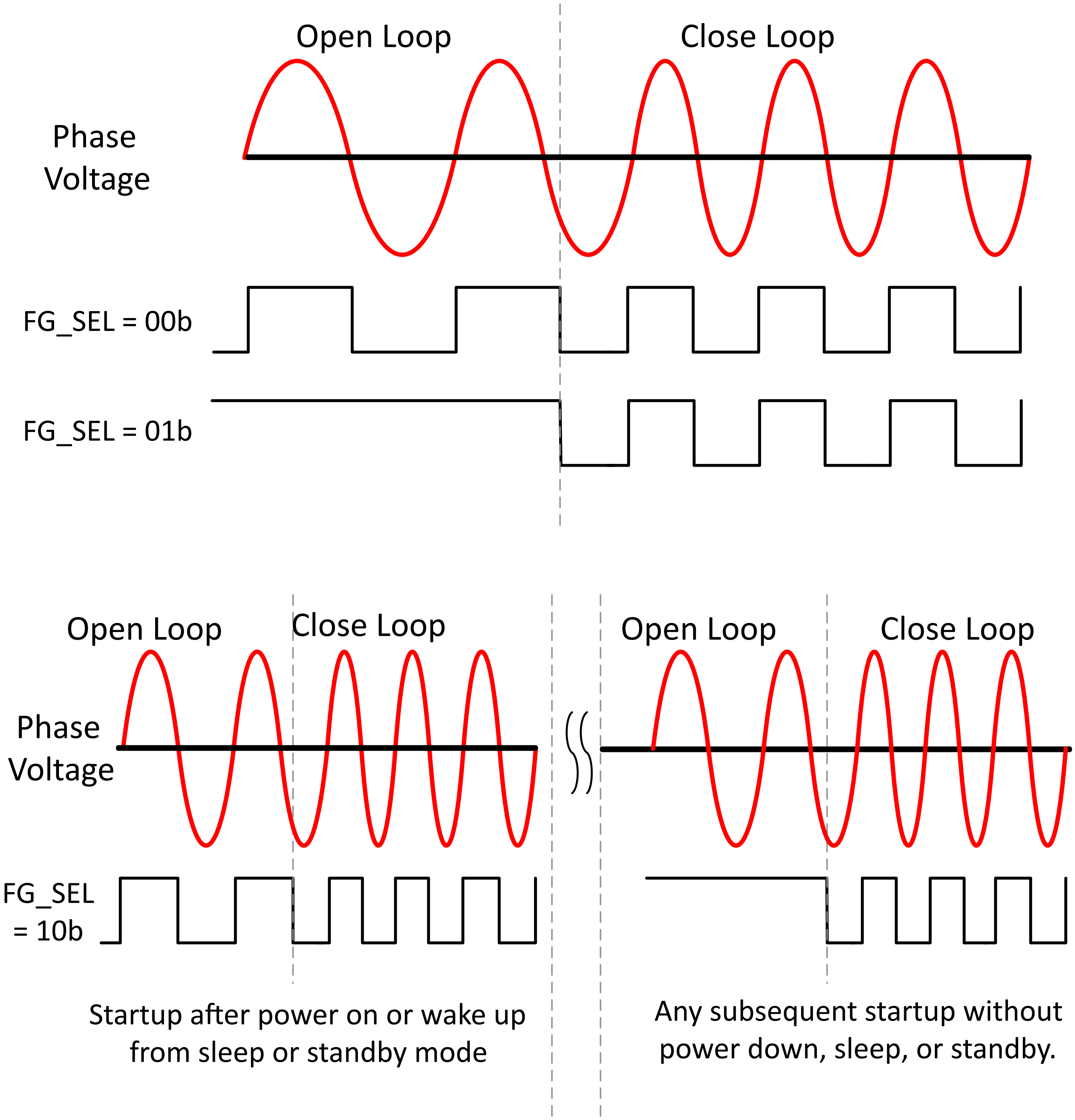

Figure 7-45. FG Behavior During Open Loop

7.3.22.3 FG During Motor Stop

The FG pin state when the motor stops rotating can be defined using FG_IDLE_CONFIG. The motor stop is decided by FG_BEMF_THR.

7.3.22.4 FG Behaviour During Fault

The FG behaviour during faults (those reported on nFAULT pin) can be configured using FG_FAULT_CONFIG.

7.3.23 DC Bus Current Limit

The DC bus current limit feature can be used in applications to limit the current supplied by source without entering the constant current mode. The DC bus current limit feature can be enabled by setting BUS_CURRENT_LIMIT_ENABLE to 1b. The DC bus current limit threshold can be configured using BUS_CURRENT_LIMIT. The DC bus current limit limits the speed reference and a functional diagram is shown in Figure 7-46, Figure 7-47 and Figure 7-48. Enabling this feature may restrict the speed of the motor so that current drawn from source is limited. The algorithm estimates the bus current using the measured phase currents, phase voltage and DC bus voltage. The current limit status is reported on BUS_CURRENT_LIMIT_STATUS.

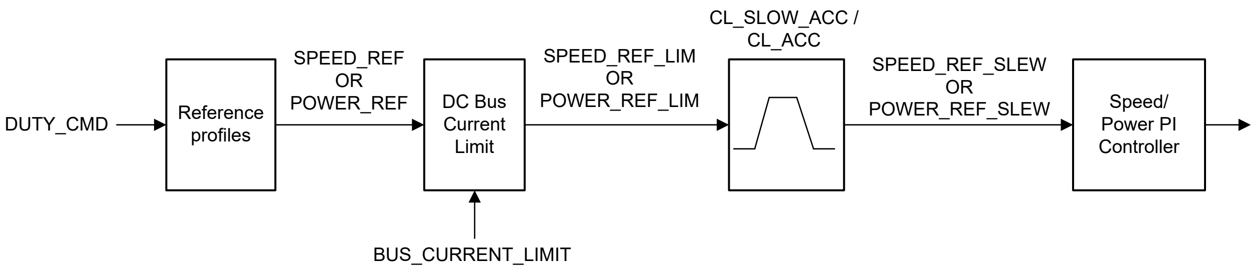

Figure 7-46. DC Bus Current Limit Functional Block Diagram in Speed or Power Control Mode

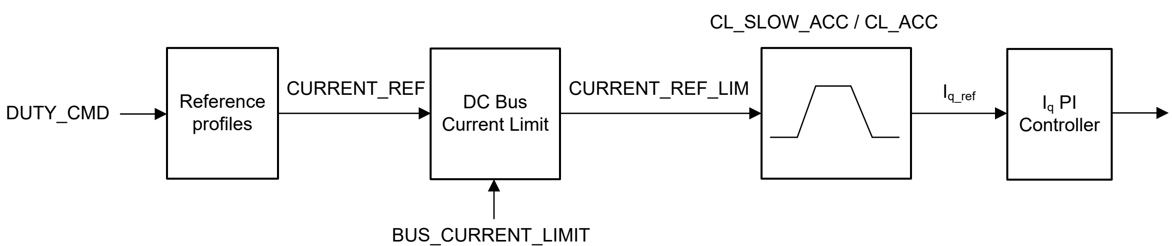

Figure 7-47. DC Bus Current Limit Functional Block Diagram in Current Control Mode

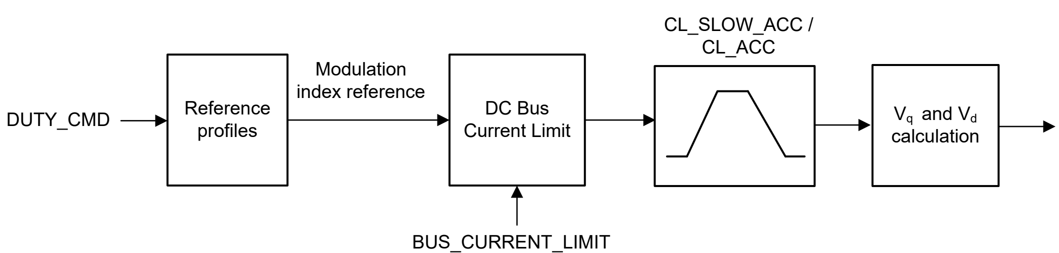

Figure 7-48. DC Bus Current Limit Functional Block Diagram in Modulation Index Control Mode

Note

1. DC bus current limit feature is not available when active braking is enabled.
2. MCF8329A implements a 5% hysteresis around BUS_CURRENT_LIMIT to avoid chattering around this set-point.

7.3.24 Protections

The MCF8329A is protected from a host of fault events including motor lock, PVDD under-voltage, AVDD under-voltage, GVDD under-voltage, bootstrap under-voltage, over temperature and overcurrent events. Table 7-5 summarizes the response, recovery modes, gate driver status, reporting mechanism for different faults.

Note

1. Actionable and report only faults (latched or retry) are always reported on nFAULT pin (as logic low).
2. Priority order for multi-fault scenarios is latched > slower retry time fault > faster retry time fault > report only fault. For example, if a latched and retry fault happen simultaneously, the device stays latched in fault mode until user issues clear fault command by writing 1b to CLR_FLT or through a power recycle. If two retry faults with different retry times happen simultaneously, the device retries only after the longer (slower) retry time lapses.
3. Recovery refers only to state of gate driver after the fault condition is removed. Automatic indicates that the device automatically recovers (and gate driver outputs and hence external FETs are active) when retry time lapses after the fault condition is removed. Latched indicates that the device waits for clearing of fault condition (by writing 1b to CLR_FLT bit) or through a power recycle.
4. The GVDD under-voltage, BST under voltage, VDS OCP, SENSE OCP faults can take up to 200-ms after fault response (gate driver outputs pulled low to put the external FETs in Hi-Z) to be reported on nFAULT pin (as logic low).
5. Latched faults can take up to 200-ms after CLR_FLT command is issued (over I2C) to be cleared.
6. CLR_FLT command (over I2C) can clean all the faults including latched, retry and auto recovery faults.

Table 7-5. Fault Action and Response

FAULT	CONDITION	CONFIGURATION	REPORT	GATE DRIVER	LOGIC	RECOVERY
PVDD under-voltage (PVDD_UV)	$V_{PVDD} < V_{PVDD\_UV}$	—	nFAULT	Disabled	Disabled	Automatic: $V_{PVDD} > V_{PVDD\_UV}$
AVDD POR (AVDD_POR)	$V_{AVDD} < V_{AVDD\_POR}$	—	nFAULT	Disabled	Disabled	Automatic: $V_{AVDD} > V_{AVDD\_POR}$
GVDD under-voltage (GVDD_UV)	$V_{GVDD} < V_{GVDD\_UV}$	GVDD_UV_MODE = 0b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low [2]	Active	Latched: CLR_FLT
		GVDD_UV_MODE = 1b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low [2]	Active	Retry: t_{LCK_RETRY}
BSTx under-voltage (BST_UV)	$V_{BSTx} - V_{SHx} < V_{BST\_UV}$	DIS_BST_FLT = 0b BST_UV_MODE = 0b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low [2]	Active	Latched: CLR_FLT
		DIS_BST_FLT = 0b BST_UV_MODE = 1b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low [2]	Active	Retry: t_{LCK_RETRY}
V_{DS} overcurrent (VDS_OCP)	$V_{DS} > V_{SEL\_VDS\_LVL}$	DIS_VDS_FLT = 0b VDS_FLT_MODE = 0b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low [2]	Active	Latched: CLR_FLT
		DIS_VDS_FLT = 0b VDS_FLT_MODE = 1b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low [2]	Active	Retry: t_{LCK_RETRY}
V_{SENSE} overcurrent (SEN_OCP)V_{SENSE} overcurrent (SEN_OCP)	$V_{SP} > V_{SENSE\_LVL}$	DIS_SNS_FLT = 0b SNS_FLT_MODE = 0b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low [2]	Active	Latched: CLR_FLT
		DIS_SNS_FLT = 0b SNS_FLT_MODE = 1b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low [2]	Active	Retry: t_{LCK_RETRY}

Table 7-5. Fault Action and Response (continued)

FAULT	CONDITION	CONFIGURATION	REPORT	GATE DRIVER	LOGIC	RECOVERY
3 Motor Lock (MTR_LCK)	Motor lock: Abnormal Speed; No Motor Lock; Abnormal BEMF	MTR_LCK_MODE = 0000b or 0001b	nFAULT and CONTROLLER_FAULT _STATUS register	Pulled Low [2](MOSFETs in Hi-Z)	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 0010b or 0011b	nFAULT and CONTROLLER_FAULT _STATUS register	Low side brake logic	Active	Latched: CLR_FLT
		MTR_LCK_MODE = 0100b or 0101b	nFAULT and CONTROLLER_FAULT _STATUS register	Pulled Low [2](MOSFETs in Hi-Z)	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 0110b or 0111b	nFAULT and CONTROLLER_FAULT _STATUS register	Low side brake logic	Active	Retry: t_{LCK_RETRY}
		MTR_LCK_MODE = 1000b	nFAULT and CONTROLLER_FAULT _STATUS register	Active	Active	No action
		MTR_LCK_MODE = 1001b to 1111b	None	Active	Active	No action
Hardware Lock-Detection Current Limit (HW_LOCK_ILIMIT)	Phase Current > HW_LOCK_ILIMIT	HW_LOCK_ILIMIT_MODE = 0000b or 0001b	nFAULT and CONTROLLER_FAULT _STATUS register	Pulled Low [2](MOSFETs in Hi-Z)	Active	Latched: CLR_FLT
		HW_LOCK_ILIMIT_MODE =0010b or 0011b	nFAULT and CONTROLLER_FAULT _STATUS register	Low-side brake logic	Active	Latched: CLR_FLT
		HW_LOCK_ILIMIT_MODE = 0100b or 0101b	nFAULT and CONTROLLER_FAULT _STATUS register	Pulled Low [2](MOSFETs in Hi-Z)	Active	Retry: t_{LCK_RETRY}
		HW_LOCK_ILIMIT_MODE = 0110b or 0111b	nFAULT and CONTROLLER_FAULT _STATUS register	Low-side brake logic	Active	Retry: t_{LCK_RETRY}
		HW_LOCK_ILIMIT_MODE= 1000b	nFAULT and CONTROLLER_FAULT _STATUS register	Active	Active	No action
		HW_LOCK_ILIMIT_MODE = 1001b to 1111b	None	Active	Active	No action

Table 7-5. Fault Action and Response (continued)

FAULT	CONDITION	CONFIGURATION	REPORT	GATE DRIVER	LOGIC	RECOVERY
ADC based Lock-Detection Current Limit (LOCK_ILIMIT)	Phase Current > LOCK_ILIMIT	LOCK_ILIMIT_MODE = 0000b or 0001b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low [2](MOSFETs in Hi-Z)	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 0010b or 0011b	nFAULT and CONTROLLER_FAULT_STATUS register	Low-side brake logic	Active	Latched: CLR_FLT
		LOCK_ILIMIT_MODE = 0100b or 0101b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low [2](MOSFETs in Hi-Z)	Active	Retry: t_{LCK_RETRY}
		LOCK_ILIMIT_MODE = 0110b or 0111b	nFAULT and CONTROLLER_FAULT_STATUS register	Low-side brake logic	Active	Retry: t_{LCK_RETRY}
		LOCK_ILIMIT_MODE = 1000b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
		LOCK_ILIMIT_MODE = 1001b to 1111b	None	Active	Active	No action
IPD Timeout Fault (IPD_T1_FAULT)	IPD TIME > 500ms (approx), during IPD current ramp up or ramp down	IPD_TIMEOUT_FAULT_EN = 0b	-	Active	Active	No action
		IPD_TIMEOUT_FAULT_EN = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low [2](MOSFETs in Hi-Z)	Active	Retry: t_{LCK_RETRY}
IPD Frequency Fault (IPD_FREQ_FAULT)	IPD pulse before the current decay in previous IPD	IPD_FREQ_FAULT_EN = 0b	-	Active	Active	No action
		IPD_FREQ_FAULT_EN = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low [2](MOSFETs in Hi-Z)	Active	Retry: t_{LCK_RETRY}
MPET Back-EMF Fault (MPET_BEMF_FAULT)	Motor Back EMF < STAT_DETECT_THR	MPET_CMD = 1 or MPET_KE = 1	nFAULT and CONTROLLER_FAULT_STATUS register	Hi-Z	Active	Latched: CLR_FLT
Maximum V_{PVDD} (over-voltage) fault	V_{PVDD} > MAX_VM_MOTOR, if MAX_VM_MOTOR ≠ 000b	MAX_VM_MODE = 0b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low [2](MOSFETs in Hi-Z)	Active	Latched: CLR_FLT
		MAX_VM_MODE = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low [2](MOSFETs in Hi-Z)	Active	Automatic: (V_{VM} < MAX_VM_MOTOR - VM_UV_OV_HYS) V
Minimum V_{PVDD} (under-voltage) fault	V_{PVDD} < MIN_VM_MOTOR, if MIN_VM_MOTOR ≠ 000b	MIN_VM_MODE = 0b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low [2](MOSFETs in Hi-Z)	Active	Latched: CLR_FLT
		MIN_VM_MODE = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low [2](MOSFETs in Hi-Z)	Active	Automatic: (V_{VM} > MIN_VM_MOTOR + VM_UV_OV_HYS) V

Table 7-5. Fault Action and Response (continued)

FAULT	CONDITION	CONFIGURATION	REPORT	GATE DRIVER	LOGIC	RECOVERY
Bus Current Limit	I_{VM} > BUS_CURRENT_LIMIT	BUS_CURRENT_LIMIT_ENABLE = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Active; motor speed/ power/ current will be restricted to limit DC bus current	Active	Automatic: Restriction is removed when I_{VM} < BUS_CURRENT_LIMIT
Current Loop Saturation	Indication of current loop saturation due to lower V_{VM}	SATURATION_FLAGS_EN = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Active; motor speed/ power/ current may not reach reference	Active	Automatic: motor will reach reference operating point upon exiting saturation
Speed/power Loop Saturation	Indication of speed/power loop saturation due to lower V_{VM}, lower ILIMIT setting etc.,	SATURATION_FLAGS_EN = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Active; motor speed/ power may not reach reference	Active	Automatic: motor will reach reference operating point upon exiting saturation
External Watchdog Fault	Time between watchdog tickles > EXT_WD_CONFIG	EXT_WD_EN = 1b EXT_WD_FAULT = 0b	nFAULT and CONTROLLER_FAULT_STATUS register	Active	Active	No action
		EXT_WD_EN = 1b EXT_WD_FAULT = 1b	nFAULT and CONTROLLER_FAULT_STATUS register	Pulled Low [2]	Active	Latched: CLR_FLT
Thermal shutdown (TSD)	$T_J > T_{TSD}$	OTS_AUTO_RECOVERY = 0b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low [2]	Active	Latched: CLR_FLT
		OTS_AUTO_RECOVERY = 1b	nFAULT and GATE_DRIVER_FAULT_STATUS Register	Pulled Low [2]	Active	Automatic: $T_J < T_{OTSD} - T_{HYS}$

1. Disabled: Passive pull down for GLx and semi-active pull down for GHx
2. Pulled Low: GHx and GLx are actively pulled low by the gate driver

Note

Any fault reporting on nFAULT pin or CONTROLLER_FAULT_STATUS register or GATE_DRIVER_FAULT_STATUS register can have a latency up to 200 ms.

7.3.24.1 PVDD Supply Undervoltage Lockout (PVDD_UV)

If at any time the power supply voltage on the PVDD pin falls below the V_{PVDD_UV} threshold for longer than the $t_{PVDD\_UV\_DG}$ time, the device detects a PVDD undervoltage event. After detecting the undervoltage condition, the gate driver is disabled, the charge pump is disabled, the internal digital logic is disabled, and the nFAULT pin is driven low. Normal operation starts again (the gate driver becomes operable and the nFAULT pin is released) when the PVDD pin rises above V_{PVDD_UV}.

7.3.24.2 AVDD Power on Reset (AVDD_POR)

If at any time the supply voltage on the AVDD pin falls below the V_{AVDD_POR} threshold for longer than the $t_{AVDD\_POR\_DG}$ time, the device enters an inactive state, disabling the gate driver, the charge pump, and the internal digital logic, and nFAULT is driven low. Normal operation (digital logic operational) requires AVDD to exceed V_{AVDD_POR} level.

7.3.24.3 GVDD Undervoltage Lockout (GVDD_UV)

If at any time the voltage on the GVDD pin falls lower than the V_{GVDD_UV} threshold voltage for longer than the $t_{GVDD\_UV\_DG}$ time, the device detects a GVDD undervoltage event. After detecting the GVDD_UV undervoltage event, all of the gate driver outputs are driven low to disable the external MOSFETs, the charge pump is still running and nFAULT pin is driven low.

The device can be configured in a latched fault state or retry mode upon a GVDD_UV condition using the GVDD_UV_MODE bit. With GVDD_UV_MODE = 0b, normal operation resumes after the GVDD_UV condition is cleared and a clear fault command is issued through the CLR_FLT bit. With GVDD_UV_MODE = 1b, normal operation resumes after the GVDD_UV condition is cleared and a time period of t_{LCK_RETRY} is elapsed.

7.3.24.4 BST Undervoltage Lockout (BST_UV)

If at any time the voltage across BSTx and SHx pins falls lower than the V_{BST_UV} threshold voltage for longer than the $t_{BST\_UV\_DG}$ time, the device detects a BST undervoltage event. After detecting the BST_UV event, all of the gate driver outputs are driven low to disable the external MOSFETs, and nFAULT pin is driven low. BST_UV can be disabled by configuring DIS_BST_FLT to 1b.

The device can be configured in a latched fault state or retry mode upon a BST_UV condition using the BST_UV_MODE bit. With BST_UV_MODE = 0b, normal operation resumes after the BST_UV condition is cleared and a clear fault command is issued through the CLR_FLT bit. With BST_UV_MODE = 1b, normal operation resumes after the BST_UV condition is cleared and a time period of t_{LCK_RETRY} is elapsed.

7.3.24.5 MOSFET VDS Overcurrent Protection (VDS_OCP)

The device has adjustable VDS voltage monitors to detect overcurrent or short-circuit conditions on the external power MOSFETs. A MOSFET overcurrent event is sensed by monitoring the VDS voltage drop across the external MOSFET $R_{DS(on)}$. The high-side VDS monitors measure between the PVDD and SHx pins and the low-side VDS monitors measure between the SHx and LSS pins. If the voltage across external MOSFET exceeds the threshold set by SEL_VDS_LVL for longer than the t_{DS_DG} deglitch time, a V_{DS_OCP} event is recognized. After detecting the VDS overcurrent event, all of the gate driver outputs are driven low to disable the external MOSFETs and nFAULT pin is driven low. V_{DS_OCP} can be disabled by configuring DIS_VDS_FLT to 1b.

The device can be configured in a latched fault state or retry mode upon a V_{DS_OCP} event using the VDS_FLT_MODE bit. With VDS_FLT_MODE = 0b, normal operation resumes after the V_{DS_OCP} condition is cleared and a clear fault command is issued through the CLR_FLT bit. With VDS_FLT_MODE = 1b, normal operation resumes after the V_{DS_OCP} condition is cleared and a time period of t_{LCK_RETRY} is elapsed.

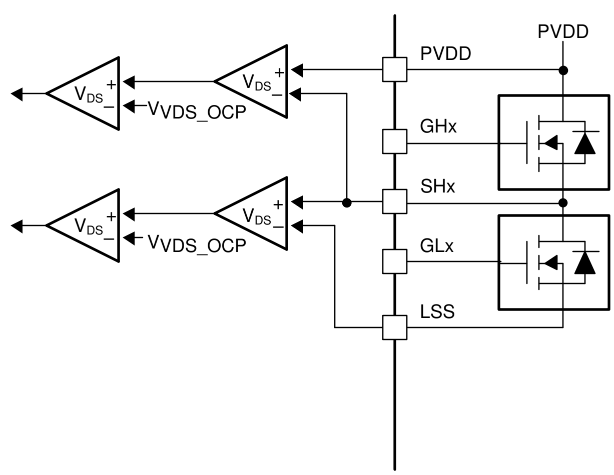

Figure 7-49. MCF8329A VDS Monitors

7.3.24.6 VSENSE Overcurrent Protection (SEN_OCP)

Overcurrent is also monitored by sensing the voltage drop across the external current sense resistor between LSS and GND pin. If at any time the voltage on the LSS input exceeds the VSEN_OCP threshold for longer than the t_{DS_DG} deglitch time, a SEN_OCP event is recognized. After detecting the SEN_OCP overcurrent event, all of the gate driver outputs are driven low to disable the external MOSFETs and nFAULT pin is driven low. The V_{SENSE} threshold is fixed at 0.5 V. V_{SEN_OCP} can be disabled by configuring DIS_SNS_FLT to 1b.

The device can be configured in a latched fault state or retry mode upon a V_{DS_OCP} event using the SNS_FLT_MODE bit. With SNS_FLT_MODE = 0b, normal operation resumes after the V_{SEN_OCP} condition is cleared and a clear fault command is issued through the CLR_FLT bit. With SNS_FLT_MODE = 1b, normal operation resumes after the V_{SEN_OCP} condition is cleared and a time period of t_{LCK_RETRY} is elapsed.

7.3.24.7 Thermal Shutdown (OTSD)

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{OTSD}), an OTSD event is recognized. After detecting the OTSD overtemperature event, all of the gate driver outputs are driven low to disable the external MOSFETs, and nFAULT pin is driven low. The over temperature protection can be configured for a latched mode or automatic recovery mode by configuring OTS_AUTO_RECOVERY. In latched mode, normal operation resumes after the T_{OTSD} condition is cleared and a clear fault command is issued through the CLR_FLT bit. In automatic recovery mode, normal operation resumes after the T_{OTSD} condition is cleared.

7.3.24.8 Hardware Lock Detection Current Limit (HW_LOCK_ILIMIT)

The hardware lock detection current limit function provides a configurable threshold for limiting the current to prevent damage to the system. The output of current sense amplifier is connected to hardware comparator. If at any time, the voltage on the output of CSA exceeds HW_LOCK_ILIMIT threshold for a time longer than $t_{HW\_LOCK\_ILIMIT}$, a HW_LOCK_ILIMIT event is recognized and action is taken according to the HW_LOCK_ILIMIT_MODE. The threshold is set through HW_LOCK_ILIMIT, the $t_{HW\_LCK\_ILIMIT}$ is set through the HW_LOCK_ILIMIT_DEG. HW_LOCK_ILIMIT_MODE bit can operate in four different modes: HW_LOCK_ILIMIT latched shutdown, HW_LOCK_ILIMIT automatic retry, HW_LOCK_ILIMIT report only, and HW_LOCK_ILIMIT disabled.

7.3.24.8.1 HW_LOCK_ILIMIT Latched Shutdown (HW_LOCK_ILIMIT_MODE = 00xxb)

When a HW_LOCK_ILIMIT event happens in this mode, the status of MOSFET will be configured by HW_LOCK_ILIMIT_MODE and nFAULT is driven low. Status of MOSFETs during HW_LOCK_ILIMIT:

- HW_ LOCK_ILIMIT_MODE = 0000b or 0001b: All MOSFETs are turned OFF.
- HW_LOCK_ILIMIT_MODE = 0010b or 0011b: All-low side MOSFETs are turned ON.

The CONTROLLER_FAULT and HW_LOCK_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the HW_LOCK_ILIMIT condition clears and a clear fault command is issued through the CLR_FLT bit.

7.3.24.8.2 HW_LOCK_ILIMIT Automatic recovery (HW_LOCK_ILIMIT_MODE = 01xxb)

When a HW_LOCK_ILIMIT event happens in this mode, the status of MOSFET will be configured by HW_LOCK_ILIMIT_MODE and nFAULT is driven low. Status of MOSFET during HW_LOCK_ILIMIT:

- HW_LOCK_ILIMIT_MODE = 0100b or 0101b: All MOSFETs are turned OFF.
- HW_LOCK_ILIMIT_MODE = 0110b or 0111b: All low-side MOSFETs are turned ON

The CONTROLLER_FAULT and HW_LOCK_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the t_{LCK_RETRY} (configured by LCK_RETRY) time lapses. The CONTROLLER_FAULT and HW_LOCK_ILIMIT bits are reset to 0b after the t_{LCK_RETRY} period expires.

7.3.24.8.3 HW_LOCK_ILIMIT Report Only (HW_LOCK_ILIMIT_MODE = 1000b)

No protective action is taken when a HW_ LOCK_ILIMIT event happens in this mode. The hardware lock detection current limit event is reported by setting the CONTROLLER_FAULT and HW_LOCK_ILIMIT bits to 1b in the fault status registers and nFAULT is pulled low. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the HW_LOCK_ILIMIT condition clears and a clear fault command is issued through the CLR_FLT bit.

7.3.24.8.4 HW_LOCK_ILIMIT Disabled (HW_LOCK_ILIMIT_MODE= 1001b to 1111b)

No action is taken when a HW_LOCK_ILIMIT event happens in this mode.

7.3.24.9 Lock Detection Current Limit (LOCK_ILIMIT)

The lock detection current limit function provides a configurable threshold for limiting the current to prevent damage to the system. The MCF8329A continuously monitors the output of the current sense amplifier (CSA) through the ADC. If at any time, any phase current exceeds LOCK_ILIMIT for a time longer than t_{LCK_ILIMIT}, a LOCK_ILIMIT event is recognized and action is taken according to LOCK_ILIMIT_MODE. The threshold is set through LOCK_ILIMIT and the t_{LCK_ILIMIT} is set through LOCK_ILIMIT_DEG. LOCK_ILIMIT_MODE can be set to four different modes: LOCK_ILIMIT latched shutdown, LOCK_ILIMIT automatic retry, LOCK_ILIMIT report only and LOCK_ILIMIT disabled.

7.3.24.9.1 LOCK_ILIMIT Latched Shutdown (LOCK_ILIMIT_MODE = 00xxb)

When a LOCK_ILIMIT event happens in this mode, the status of external MOSFETs will be configured by LOCK_ILIMIT_MODE and nFAULT is driven low. Status of external MOSFETs driven from MCF8329A during LOCK_ILIMIT:

- LOCK_ILIMIT_MODE = 0000b or 0001b: All MOSFETs are turned OFF, the gate driver outputs pulled low.
- LOCK_ILIMIT_MODE = 0010b or 0011b: All low-side MOSFETs (gate driver outputs) are turned ON.

The CONTROLLER_FAULT and LOCK_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the LOCK_ILIMIT condition clears and a clear fault command is issued through the CLR_FLT bit.

7.3.24.9.2 LOCK_ILIMIT Automatic Recovery (LOCK_ILIMIT_MODE = 01xxb)

When a LOCK_ILIMIT event happens in this mode, the status of external MOSFETs will be configured by LOCK_ILIMIT_MODE and nFAULT is driven low. Status of external MOSFETs driven from MCF8329A during LOCK_ILIMIT:

- LOCK_ILIMIT_MODE = 0100b or 0101b: All MOSFETs are turned OFF, the gate driver outputs pulled low.
- LOCK_ILIMIT_MODE = 0110b or 0111b: All low-side MOSFETs (gate driver outputs) are turned ON

The CONTROLLER_FAULT and LOCK_ILIMIT bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the t_{LCK_RETRY} (configured by LCK_RETRY) time lapses. The CONTROLLER_FAULT and LOCK_ILIMIT bits are reset to 0b after the t_{LCK_RETRY} period expires.

7.3.24.9.3 LOCK_ILIMIT Report Only (LOCK_ILIMIT_MODE = 1000b)

No protective action is taken when a LOCK_ILIMIT event happens in this mode. The lock detection current limit event is reported by setting the CONTROLLER_FAULT and LOCK_ILIMIT bits to 1b in the fault status registers and nFAULT is pulled low. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the LOCK_ILIMIT condition clears and a clear fault command is issued through the CLR_FLT bit.

7.3.24.9.4 LOCK_ILIMIT Disabled (LOCK_ILIMIT_MODE = 1xx1b)

No action is taken when a LOCK_ILIMIT event happens in this mode.

7.3.24.10 Motor Lock (MTR_LCK)

The MCF8329A continuously checks for different motor lock conditions (see Motor Lock Detection) during motor operation. When one of the enabled lock condition happens, a MTR_LCK event is recognized and action is taken according to the MTR_LCK_MODE.

All locks can be enabled or disabled individually and retry times can be configured through LCK_RETRY. MTR_LCK_MODE bit can operate in four different modes: MTR_LCK latched shutdown, MTR_LCK automatic retry, MTR_LCK report only and MTR_LCK disabled.

7.3.24.10.1 MTR_LCK Latched Shutdown (MTR_LCK_MODE = 00xxb)

When a MTR_LCK event happens in this mode, the status of external MOSFETs will be configured by MTR_LCK_MODE and nFAULT is driven low. Status of external MOSFETs during MTR_LCK:

- MTR_LCK_MODE = 0000b or 0001b: All external MOSFETs are turned OFF, the gate driver outputs pulled low.
- MTR_LCK_MODE = 0010b or 0011b: All low-side MOSFETs (gate driver outputs) are turned ON.

The CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits are set to 1b in the fault status registers. Normal operation resumes (gate driver operation and the nFAULT pin is released) when the MTR_LCK condition clears and a clear fault command is issued through the CLR_FLT bit.

7.3.24.10.2 MTR_LCK Automatic Recovery (MTR_LCK_MODE= 01xxb)

When a MTR_LCK event happens in this mode, the status of MOSFETs will be configured by MTR_LCK_MODE and nFAULT is driven low. Status of MOSFETs during MTR_LCK:

- MTR_LCK_MODE = 0100b or 0101b: All external MOSFETs are turned OFF, the gate driver outputs pulled low.
- MTR_LCK_MODE = 0110b or 0111b: All low-side MOSFETs (gate driver outputs) are turned ON.

The CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits are set to 1b in the fault status registers. Normal operation resumes automatically (gate driver operation and the nFAULT pin is released) after the t_{LCK_RETRY} (configured by LCK_RETRY) time lapses. The CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits are reset to 0b after the t_{LCK_RETRY} period expires.

7.3.24.10.3 MTR_LCK Report Only (MTR_LCK_MODE = 1000b)

No protective action is taken when a MTR_LCK event happens in this mode. The motor lock event is reported by setting the CONTROLLER_FAULT, MTR_LCK and respective motor lock condition bits to 1b in the fault status registers and nFAULT pin is pulled low. The gate drivers continue to operate. The external controller manages this condition by acting appropriately. The reporting clears when the MTR_LCK condition clears and a clear fault command is issued through the CLR_FLT bit.

7.3.24.10.4 MTR_LCK Disabled (MTR_LCK_MODE = 1xx1b)

No action is taken when a MTR_LCK event happens in this mode.

7.3.24.11 Motor Lock Detection

The MCF8329A provides different lock detect mechanisms to determine if the motor is in a locked state. Multiple detection mechanisms work together to ensure the lock condition is detected quickly and reliably. In addition to detecting if there is a locked motor condition, the MCF8329A can also identify and take action if there is no motor connected to the system. Each of the lock detect mechanisms and the no-motor detection can be disabled by their respective register bits.

7.3.24.11.1 Lock 1: Abnormal Speed (ABN_SPEED)

MCF8329A monitors the speed continuously and at any time the speed exceeds LOCK_ABN_SPEED, an ABN_SPEED lock event is recognized and action is taken according to the MTR_LCK_MODE.

The threshold is set through the LOCK_ABN_SPEED register. ABN_SPEED lock can be enabled/disabled by LOCK1_EN.

7.3.24.11.2 Lock 2: Abnormal BEMF (ABN_BEMF)

MCF8329 estimates back-EMF in order to run motor optimally in closed loop. This estimated back-EMF is compared against the expected back-EMF calculated using the estimated speed and the BEMF constant. Whenever motor is stalled the estimated back-EMF is inaccurate due to lower back-EMF at low speed. When the difference between estimated and expected back-EMF exceeds ABNORMAL_BEMF_THR, an abnormal BEMF fault is triggered and action is taken according to the MTR_LCK_MODE.

ABN_BEMF lock can be enabled/disabled by LOCK2_EN.

7.3.24.11.3 Lock3: No-Motor Fault (NO_MTR)

The MCF8329A continuously monitors phase currents on all three phases; if any phase current stays below NO_MTR_THR for 500ms during open loop, a NO_MTR event is recognized. The response to the NO_MTR event is configured through MTR_LCK_MODE. NO_MTR lock can be enabled/disabled by LOCK3_EN.

Note

For a reliable detection of no-motor fault, ensure that the open loop time is sufficiently higher than 500 ms.

7.3.24.12 MPET Faults

An error during BEMF constant measurement is reported using MPET_BEMF_FAULT. This fault gets triggered when the measured back EMF is less than the threshold set in STAT_DETECT_THR. One example of such fault scenario can be the motor stall while running in open loop due to incorrect open loop configuration used.

7.3.24.13 IPD Faults

The MCF8329A uses 12-bit timers to estimate the time during the current ramp up in IPD, when the motor start-up is configured as IPD (MTR_STARTUP is set to 10b). During IPD, the algorithm checks for a successful current ramp-up to IPD_CURR_THR, starting with an IPD clock of 10MHz; if unsuccessful (timer overflow before current reaches IPD_CURR_THR), IPD is repeated with lower frequency clocks of 1MHz, 100kHz, and 10kHz sequentially. If the IPD timer overflows (current does not reach IPD_CURR_THR) with all the four clock frequencies, then the IPD_T1_FAULT gets triggered. The user can enable IPD timeout (IPD timer overflow) by setting IPD_TIMEOUT_FAULT_EN to 1b.

IPD gives incorrect results if the next IPD pulse is commanded before the complete decay of current due to present IPD pulse. The MCF8329A can generate a fault called IPD_FREQ_FAULT during such a scenario by setting IPD_FREQ_FAULT_EN to 1b. The IPD_FREQ_FAULT maybe triggered if the IPD frequency is too high for the IPD current limit or if the motor inductance is too high for the IPD frequency and IPD current limit.

7.4 Device Functional Modes

7.4.1 Functional Modes

7.4.1.1 Sleep Mode

In sleep mode all gate drivers are disabled, the GVDD regulator is disabled ,the AVDD regulator is disabled, the sense amplifier, and the I^2C bus are disabled. The device can be configured to enter sleep (instead of standby) mode by configuring DEV_MODE to 1b. The entry and exit from sleep state as described in Table 7-6.

Table 7-6. Conditions to Enter or Exit Sleep Modes

INPUT REFERENCE COMMAND MODE	ENTER SLEEP, DEV_MODE = 1b	EXIT FROM SLEEP	ENTER STANDBY, DEV_MODE = 0b	EXIT FROM STANDBY
Analog input at SPEED/ WAKE pin	$V_{SPEED/WAKE} < V_{EN\_SL}$ for $t_{DET\_SL\_ANA}$ if SLEEP_ENTRY_TIME = 00b or 01b; for $t_{DET\_SL\_PWM}$ if SLEEP_ENTRY_TIME = 10b or 11b	$V_{SPEED/WAKE} > V_{EX\_SL}$	$V_{SPEED/WAKE} < V_{EN\_SB}$	$V_{SPEED/WAKE} > V_{EX\_SB}$
Analog input at DACOUT/SOx/SPEED_ANA pin	$V_{SPEED/WAKE} < V_{IL}$	$V_{SPEED/WAKE} > V_{IH}$	$V_{SPEED/WAKE} < V_{IL}$ or $V_{DACOUT/SOx/SPEED\_ANA} < V_{EN\_SB}$	$V_{SPEED/WAKE} > V_{IH}$ and $V_{DACOUT/SOx/SPEED\_ANA} > V_{EX\_SB}$
PWM	$V_{SPEED/WAKE} < V_{IL}$ for $t_{DET\_SL\_PWM}$	$V_{SPEED/WAKE} > V_{IH}$ for t_{DET_PWM}	$Duty_{SPEED/WAKE} < Duty_{EN\_SB}$ for $t_{DET\_SL\_PWM}$	$Duty_{SPEED/WAKE} > Duty_{EX\_SB}$ for t_{DET_PWM}
Frequency	$V_{SPEED/WAKE} < V_{IL}$ for $t_{DET\_SL\_PWM}$	$V_{SPEED/WAKE} > V_{IH}$ for t_{DET_PWM}	$Freq_{SPEED/WAKE} < Freq_{EN\_SB}$ for $t_{DET\_SL\_PWM}$	$Freq_{SPEED/WAKE} > Freq_{EX\_SB}$ for t_{DET_PWM}
I^2C	$V_{SPEED/WAKE} < V_{IL}$	$V_{SPEED/WAKE} > V_{IH}$	$V_{SPEED/WAKE} < V_{IL}$ or DIGITAL_SPEED_CTRL < $DIGITAL\_SPEED\_CTRL_{EN\_SB}$	$V_{SPEED/WAKE} > V_{IH}$ and DIGITAL_SPEED_CTRL > $DIGITAL\_SPEED\_CTRL_{EX\_SB}$

Note

During power-up and power-down of the device, the nFAULT pin is held low as the internal regulators are disabled. After the regulators have been enabled, the nFAULT pin is automatically released.

7.4.1.2 Standby Mode

In standby mode the gate driver, AVDD LDO and I^2C bus are active. The device can be configured to enter standby mode by configuring DEV_MODE to 0b. The device enters standby mode when the reference command after the profiler is zero.

The thresholds for entering and exiting standby mode in different input modes are as follows,

Table 7-7. Standby Mode Entry/Exit Thresholds

Control Input Source	Standby entry/exit thresholds	REF_PROFILE_CONFIG = 00b	REF_PROFILE_CONFIG ≠ 00b
Analog	V_{EN_SB} or V_{EX_SB}	Maximum of (1%, DUTY_HYS) x V_{ANA_FS}	REF_X = 1% of MAX_SPEED or MAX_POWER or ILIMIT or MODULATION INDEX
PWM	$Duty_{EN\_SB}$ or $Duty_{EX\_SB}$	Maximum of (1%, DUTY_HYS)	REF_X = 1% of MAX_SPEED or MAX_POWER or ILIMIT or MODULATION INDEX
I^2C	$DIGITAL\_SPEED\_CTRL_{EN\_SB}$ or $DIGITAL\_SPEED\_CTRL_{EX\_SB}$	Maximum of (1%, DUTY_HYS) x 32767	REF_X = 1% of MAX_SPEED or MAX_POWER or ILIMIT or MODULATION INDEX

Table 7-7. Standby Mode Entry/Exit Thresholds (continued)

Control Input Source	Standby entry/exit thresholds	REF_PROFILE_CONFIG = 00b	REF_PROFILE_CONFIG ≠ 00b
Frequency	$Freq_{EN\_SB}$ or $Freq_{EX\_SB}$	Maximum of (1%, DUTY_HYS) x INPUT_MAXIMUM_FREQ (subject to minimum of 3Hz)	REF_X = 1% of MAX_SPEED or MAX_POWER or ILIMIT or MODULATION INDEX

Note

If the control source is analog input through the pin DACOUT/SOx/SPEED_ANA, or if the control input source is DIGITAL_SPEED_CTRL in I^2C mode then a logic low on SPEED/WAKE pin put the device in to standby mode.

7.4.1.3 Fault Reset (CLR_FLT)

In the case of latched faults, the device goes into a partial shutdown state to help protect the power MOSFETs and system. When the fault condition clears, the device can go to the operating state again by setting the CLR_FLT to 1b.

7.5 External Interface

7.5.1 DRVOFF - Gate Driver Shutdown Functionality

When DRVOFF is driven high, the gate driver goes into shutdown. DRVOFF bypasses the digital control logic inside the device, and is connected directly to the gate driver output (see Figure 7-50). This pin provides a mechanism for externally monitored faults to disable gate driver by directly bypassing the internal control logic. When MCF8329A detect logic high on the DRVOFF pin, the device disables the gate driver and puts it into pull down mode (see Figure 7-51). The gate driver shutdown sequence proceeds as shown in Figure 7-51. When the gate driver initiates the shutdown sequence, the active driver pull down is applied at I_{SINK} current for the $t_{SD\_SINK\_DIG}$ time, after which the gate driver moves to passive pull down mode.

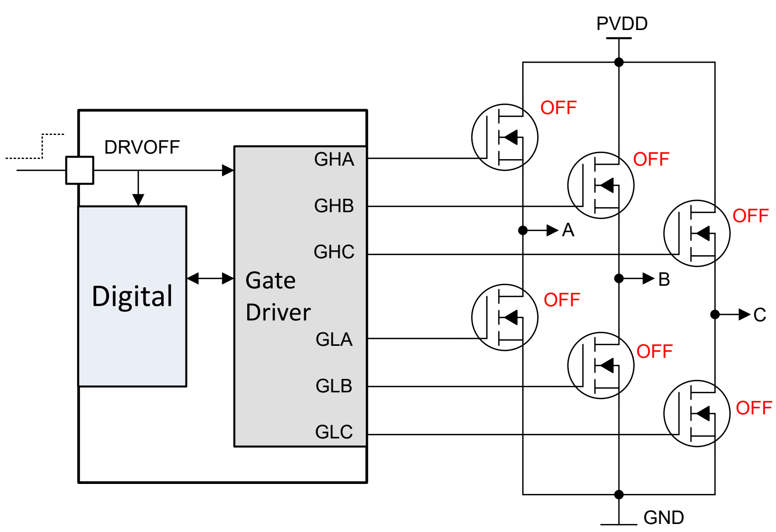

Figure 7-50. DRVOFF Gate Driver Output State

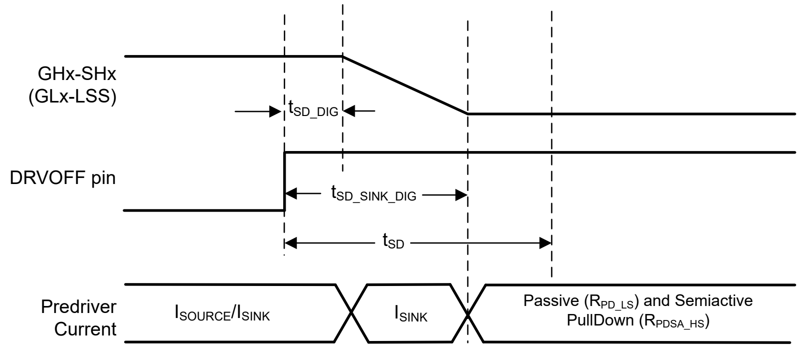

Figure 7-51. Gate Driver Shutdown Sequence

Note

Pulling the DRVOFF pin high does not cause the device to enter sleep or standby mode and the digital core is still active. The DRVOFF status is reported on DRV_OFF bit and has a latency of up to 200 ms between the pin status change to DRV_OFF bit status update. The DRVOFF is not reported on nFAULT pin, however nFAULT pin can go low if a motor fault happens when DRVOFF goes to logic high during motor operation. When DRVOFF is pulled from high to low, MCF8329A execute motor start sequence (with a latency up to 200 ms after pulling DRVOFF pin low) as described in Section 7.3.10.

7.5.2 DAC outputs

MCF8329A has a 12-bit DAC which output analog voltage equivalent of digital variables on DACOUT pin with resolution of 12 bits and maximum voltage is 3-V. Signals available on DACOUT pin is useful in tracking algorithm variables in real-time and can be used for tuning speed controller or motor acceleration time. The address for variables for DACOUT is configured using DACOUT1_VAR_ADDR.

Note

The DACOUT value for a selected variable may not be accurate during fault, brake, or HiZ states.

7.5.3 Current Sense Amplifier Output

MCF8329A can provide the built-in current sense amplifier's output on the DACOUT/SOx/SPEED_ANA pin by configuring DACOUT/SOx/SPEED_ANA.

7.5.4 Oscillator Source

MCF8329A has a built-in oscillator that is used as the clock source for all digital peripherals and timing measurements. Default configuration for MCF8329A is to use the internal oscillator and it is sufficient to drive the motor without need for any external crystal or clock sources.

In case MCF8329A does not meet accuracy requirements of timing measurement or speed loop, then MCF8329A has an option to support an external clock reference.

In order to improve EMI performance, MCF8329A provides the option of modulating the clock frequency by enabling Spread Spectrum Modulation (SSM) through SPREAD_SPECTRUM_MODULATION_DIS.

7.5.4.1 External Clock Source

Speed loop accuracy of MCF8329A over wide operating temperature range can be improved by providing more accurate optional clock reference on EXT_CLK pin as shown in Figure 7-52. EXT_CLK will be used to calibrate internal clock oscillator and match the accuracy of the external clock. External clock source can be selected by configuring CLK_SEL to 11b and setting EXT_CLK_EN to 1b. The external clock source frequency can be configured through EXT_CLK_CONFIG.

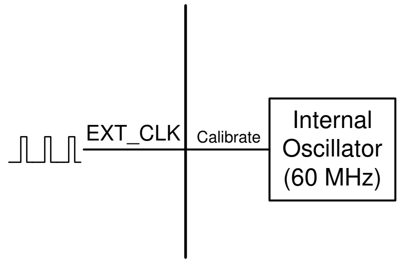

Figure 7-52. External Clock Reference

Note

External clock is optional and can be used when higher clock accuracy is needed. MCF8329A will always power up using the internal oscillator in all modes.

7.6 EEPROM access and I²C interface

7.6.1 EEPROM Access

MCF8329A has 1024 bits (16 rows of 64 bits each) of EEPROM, which are used to store the motor configuration parameters. Erase operations are row-wise (all 64 bits are erased in a single erase operation), but 32-bit write and read operations are supported. EEPROM can be written and read using the I²C serial interface but erase cannot be performed using I²C serial interface. The shadow registers corresponding to the EEPROM are located at addresses 0x000080-0x0000AE.

Note

MCF8329A allows EEPROM write and read operations only when the motor is not spinning.

7.6.1.1 EEPROM Write

In MCF8329A, EEPROM write procedure is as follows,

1. Write register 0x000080 (ISD_CONFIG) with ISD and reverse drive configuration like resync enable, reverse drive enable, stationary detect threshold, reverse drive handoff threshold etc.
2. Write register 0x000082 (REV_DRIVE_CONFIG) with reverse drive and active brake configuration like reverse drive open loop acceleration, active brake current limit, Kp, Ki values etc.
3. Write register 0x000084 (MOTOR_STARTUP1) with motor start-up configuration like start-up method, IPD parameters, align parameters etc.
4. Write register 0x000086 (MOTOR_STARTUP2) with motor start-up configuration like open loop acceleration, open loop current limit, first cycle frequency etc.
5. Write register 0x000088 (CLOSED_LOOP1) with motor control configuration like closed loop acceleration, PWM frequency, FG signal parameters etc.
6. Write register 0x00008A (CLOSED_LOOP2) with motor control configuration like motor winding resistance and inductance, motor stop options, brake speed threshold etc.
7. Write register 0x00008C (CLOSED_LOOP3) with motor control configuration like motor BEMF constant, current loop Kp, Ki etc.
8. Write register 0x00008E (CLOSED_LOOP4) with motor control configuration like speed loop Kp, Ki and maximum speed.
9. Write register 0x000090 (FAULT_CONFIG1) with fault control configuration like multiple current limits, lock current limit and actions, retry times etc.
10. Write register 0x000092 (FAULT_CONFIG2) with fault control configuration like hardware current limit actions, OV, UV limits and actions, abnormal speed level, no motor threshold etc.
11. Write registers 0x000094 – 0x00009E (SPEED_PROFILES1-6) with speed profile configuration like profile type, duty cycle, speed clamp level, duty cycle clamp level etc.
12. Write register 0x0000A0 (INT_ALGO_1) with miscellaneous configuration like ISD run time and timeout, MPET parameters etc.
13. Write register 0x0000A2 (INT_ALGO_2) with miscellaneous configuration like additional MPET parameters, IPD high resolution enable, active brake current slew rate, flux weakening etc.
14. Write registers 0x0000A4 (PIN_CONFIG1) with pin configuration for speed input mode (analog or PWM), BRAKE pin mode etc.
15. Write registers 0x0000A6 and 0x0000A8 (DEVICE_CONFIG1 and DEVICE_CONFIG2) with device configuration like pins clock source select, pin 33 configuration, watch dog configuration etc.
16. Write register 0x0000AA (PERI_CONFIG1) with peripheral configuration like dead time, bus current limit, DIR input, SSM enable etc.
17. Write registers 0x0000AC and 0x0000AE (GD_CONFIG1 and GD_CONFIG2) with gate driver configuration like slew rate, CSA gain, OCP level, mode, OVP enable, level, buck voltage level, buck current limit etc.
18. Write 0x8A500000 into register 0x0000EA to write the shadow register(0x000080-0x0000AE) values into the EEPROM.
19. Wait for 300ms for the EEPROM write operation to complete.

Steps 1-17 can be selectively executed based on registers/parameters that need to be modified. After all shadow registers have been updated with the required values, step 18 should be executed to copy the contents of the shadow registers into the EEPROM.

Note

EEPROM reserved bit field defaults settings must not be changed. To avoid changing the content of reserved bits, TI recommends using “read-modify-write” sequence to perform EEPROM write operation.

7.6.1.2 EEPROM Read

In MCF8329A, EEPROM read procedure is as follows,

1. Write 0x40000000 into register 0x0000EA to read the EEPROM data into the shadow registers (0x000080-0x0000AE).
2. Wait for 100ms for the EEPROM read operation to complete.
3. Read the shadow register values,1 or 2 registers at a time, using the I^2C read command as explained in Section 7.6.2. Shadow register addresses are in the range of 0x000080-0x0000AE. Register address increases in steps of 2 for 32-bit read operation (since each address is a 16-bit location).

7.6.2 I^2C Serial Interface

MCF8329A interfaces with an external MCU over an I^2C serial interface. MCF8329A is an I^2C target to be interfaced with a controller. External MCU can use this interface to read/write from/to any non-reserved register in MCF8329A

Note

For reliable communication, a 100-µs delay should be used between every byte transferred over the I^2C bus.

7.6.2.1 I^2C Data Word

The I^2C data word format is shown in Table 7-8.

Table 7-8. I^2C Data Word Format

TARGET_ID	R/W	CONTROL WORD	DATA	CRC-8
A6 - A0	W0	CW23 - CW0	D15 / D31/ D63 - D0	C7 - C0

Target ID and R/W Bit: The first byte includes the 7-bit I^2C target ID (0x01), followed by the read/write command bit. Every packet in MCF8329A the communication protocol starts with writing a 24-bit control word and hence the R/W bit is always 0.

24-bit Control Word: The Target Address is followed by a 24-bit control bit. The control word format is shown in Table 7-9.

Table 7-9. 24-bit Control Word Format

OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR
CW23	CW22	CW21- CW20	CW19 - CW16	CW15 - CW12	CW11 - CW0

Each field in the control word is explained in detail below.

OP_R/W – Read/Write: R/W bit gives information on whether this is a read operation or write operation. Bit value 0 indicates it is a write operation. Bit value 1 indicates it is a read operation. For write operation, MCF8329A will expect data bytes to be sent after the 24-bit control word. For read operation, MCF8329A will expect an I^2C read request with repeated start or normal start after the 24-bit control word.

CRC_EN – Cyclic Redundancy Check(CRC) Enable: MCF8329A supports CRC to verify the data integrity. This bit controls whether the CRC feature is enabled or not.

DLEN – Data Length: DLEN field determines the length of the data that will be sent by external MCU to MCF8329A. MCF8329A protocol supports three data lengths: 16-bit, 32-bit and 64-bit.

Table 7-10. Data Length Configuration

DLEN Value	Data Length
00b	16-bit
01b	32-bit
10b	64-bit
11b	Reserved

MEM_SEC – Memory Section: Each memory location in MCF8329A is addressed using three separate entities in the control word – Memory Section, Memory Page, Memory Address. Memory Section is a 4-bit field which denotes the memory section to which the memory location belongs like RAM, ROM etc.

MEM_PAGE – Memory Page: Memory page is a 4-bit field which denotes the memory page to which the memory location belongs.

MEM_ADDR – Memory Address: Memory address is the last 12-bits of the address. The complete 22-bit address is constructed internally by MCF8329A using all three fields – Memory Section, Memory Page, Memory Address. For memory locations 0x000000-0x000800, memory section is 0x0, memory page is 0x0 and memory address is the lowest 12 bits(0x000 for 0x000000, 0x080 for 0x000080 and 0x800 for 0x000800)

Data Bytes: For a write operation to MCF8329A, the 24-bit control word is followed by data bytes. The DLEN field in the control word should correspond with the number of bytes sent in this section.

CRC Byte: If the CRC feature is enabled in the control word, CRC byte has to be sent at the end of a write transaction. Procedure to calculate CRC is explained in CRC Byte Calculation below.

7.6.2.2 I²C Write Operation

MCF8329A write transaction over I²C involves the following sequence (see Figure 7-53).

1. I²C start condition.
2. Start is followed by the I²C target ID byte, made up of 7-bit target ID along with the R/W bit set to 0b. ACK in yellow box indicates that MCF8329A has processed the received target ID which has matched with it's I²C target ID and therefore will proceed with this transaction. If target ID received does not match with the I²C ID of MCF8329A, then the transaction is ignored. and no ACK is sent by MCF8329A.
3. The target ID byte is followed by the 24-bit control word sent one byte at a time. Bit 23 in the control word is 0b as it is a write transaction. ACK in blue boxes correspond to acknowledgements sent by MCF8329A to the controller that the previous byte (of control word) has been received and next byte can be sent.
4. The 24-bit control word is then followed by the data bytes. The number of data bytes sent by the controller depends on the DLEN field in the control word.
   a. While sending data bytes, the LSB byte is sent first. Refer to Section 7.6.2.4 for more details.
   b. 16-bit/32-bit write – The data sent is written to the address mentioned in control word.
   c. 64-bit Write – 64-bit is treated as two successive 32-bit writes. The address mentioned in control word is taken as Addr_1. Addr_2 is internally calculated by MCF8329A by incrementing Addr_1 by 0x2. A total of 8 data bytes are sent. The first 4 bytes (sent in LSB first) are written to Addr_1 and the next 4 bytes are written to Addr_2.
   d. ACK in blue boxes (after every data byte) correspond to the acknowledgement sent by MCF8329A to the controller that the previous data byte has been received and next data byte can be sent.
5. If CRC is enabled, the packet ends with a CRC byte. CRC is calculated for the entire packet (Target ID + W bit, Control Word, Data Bytes). MCF8329A will send an ACK on receiving the CRC byte.
6. I²C Stop condition from the controller to terminate the transaction.

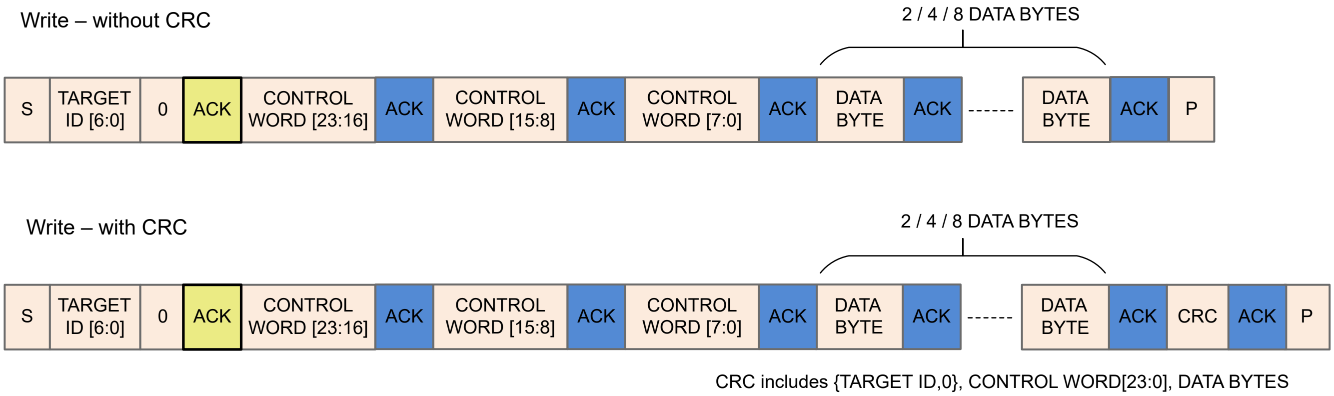

Figure 7-53. I²C Write Transaction Sequence

7.6.2.3 I²C Read Operation

MCF8329A read transaction over I²C involves the following sequence (see Figure 7-54).

1. I²C Start condition from the controller to initiate the transaction.
2. Start is followed by the I²C target ID byte, made up of 7-bit target ID along with the R/W bit set to 0b. ACK (in yellow box) indicates that MCF8329A has processed the received target ID which has matched with it's I²C target ID and therefore will proceed with this transaction. If target ID received does not match with the I²C ID of MCF8329A, then the transaction is ignored and no ACK is sent by MCF8329A.
3. The target ID byte is followed by the 24-bit control word sent one byte at a time. Bit 23 in the control word is set to 1b as it is a read transaction. ACK (in blue boxes) correspond to acknowledgements sent by MCF8329A to the controller that the previous byte (of control word) has been received and next byte can be sent.
4. The control word is followed by a Repeated Start (RS, start without a preceding stop) or normal Start (P followed by S) to initiate the data (to be read back) transfer from MCF8329A to I²C controller. RS or S is followed by the 7-bit target ID along with R/W bit set to 1b to initiate the read transaction. MCF8329A sends an ACK (in grey box after RS) to the controller to acknowledge the receipt of read transaction request.
5. Post acknowledgement of read transaction request, MCF8329A sends the data bytes on SDA one byte at a time. The number of data bytes sent by MCF8329A depends on the DLEN field in the control word.
   a. While sending data bytes, the LSB byte is sent first. Refer the examples in Section 7.6.2.4 for more details.
   b. 16-bit/32-bit Read – The data from the address mentioned in control word is sent back to the controller.
   c. 64-bit Read – 64-bit is treated as two successive 32-bit reads. The address mentioned in control word is taken as Addr_1. Addr_2 is internally calculated by MCF8329A by incrementing Addr_1 by 0x2. A total of 8 data bytes are sent by MCF8329A. The first 4 bytes (sent in LSB first) are read from Addr_1 and the next 4 bytes are read from Addr_2.
   d. ACK in orange boxes correspond to acknowledgements sent by the controller to MCF8329A that the previous byte has been received and next byte can be sent.
6. If CRC is enabled in the control word, then MCF8329A sends an additional CRC byte at the end. Controller has to read the CRC byte and then send the last ACK (in orange). CRC is calculated for the entire packet (Target ID + W bit, Control Word, Target ID + R bit, Data Bytes).
7. I²C Stop condition from the controller to terminate the transaction.

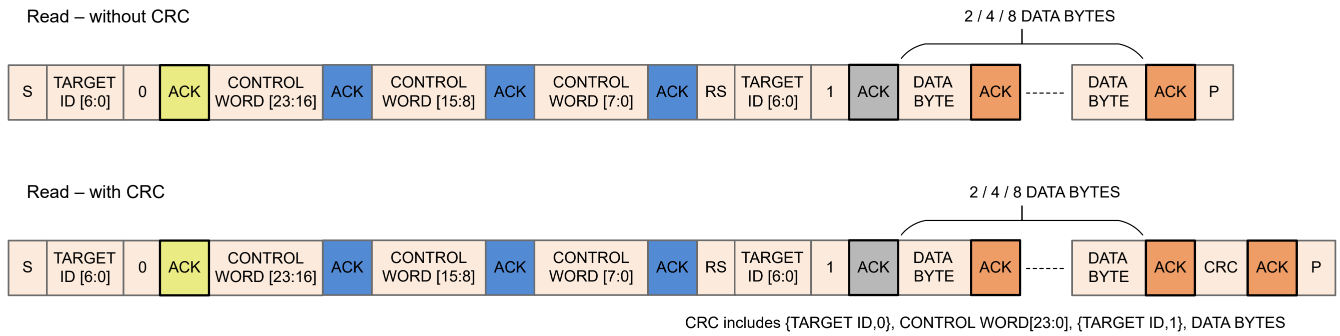

Figure 7-54. I^{2}C Read Transaction Sequence

7.6.2.4 Examples of I^{2}C Communication Protocol Packets

All values used in this example section are in hex format. I^{2}C target ID used in the examples is 0x60.

Example for 32-bit Write Operation: Address – 0x00000080, Data – 0x1234ABCD, CRC Byte – 0x45 (Sample value; does not match with the actual CRC calculation)

Table 7-11. Example for 32-bit Write Operation Packet

Start Byte		Control Word 0				Control Word 1		Control Word 2	Data Bytes				CRC
Target ID	I^{2}C Write	OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	DB0	DB1	DB2	DB3	CRC Byte
A6-A0	W0	CW23	CW22	CW21-CW20	CW19-CW16	CW15-CW12	CW11-CW8	CW7-CW0	D7-D0	D7-D0	D7-D0	D7-D0	C7-C0
0x60	0x0	0x0	0x1	0x1	0x0	0x0	0x0	0x80	0xCD	0xAB	0x34	0x12	0x45
0xC0		0x50				0x00		0x80	0xCD	0xAB	0x34	0x12	0x45

Example for 64-bit Write Operation: Address - 0x00000080, Data Address 0x00000080 - Data 0x01234567, Data Address 0x00000082 – Data 0x89ABCDEF, CRC Byte – 0x45 (Sample value; does not match with the actual CRC calculation)

Table 7-12. Example for 64-bit Write Operation Packet

Start Byte		Control Word 0				Control Word 1		Control Word 2	Data Bytes	CRC
Target ID	I^{2}C Write	OP_R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	DB0 - DB7	CRC Byte
A6-A0	W0	CW23	CW22	CW21-CW20	CW19-CW16	CW15-CW12	CW11-CW8	CW7-CW0	[D7-D0] x 8	C7-C0
0x60	0x0	0x0	0x1	0x2	0x0	0x0	0x0	0x80	0x67452301EFCDAB89	0x45
0xC0		0x60				0x00		0x80	0x67452301EFCDAB89	0x45

Example for 32-bit Read Operation: Address – 0x00000080, Data – 0x1234ABCD, CRC Byte – 0x56 (Sample value; does not match with the actual CRC calculation)

Table 7-13. Example for 32-bit Read Operation Packet

Start Byte		Control Word 0				Control Word 1		Control Word 2	Start Byte		Byte 0	Byte 1	Byte 2	Byte 3	Byte 4
Target ID	I^{2}C Write	R/W	CRC_EN	DLEN	MEM_SEC	MEM_PAGE	MEM_ADDR	MEM_ADDR	Target ID	I^{2}C Read	DB0	DB1	DB2	DB3	CRC Byte
A6-A0	W0	CW23	CW22	CW21-CW20	CW19-CW16	CW15-CW12	CW11-CW8	CW7-CW0	A6-A0	W0	D7-D0	D7-D0	D7-D0	D7-D0	C7-C0
0x60	0x0	0x1	0x1	0x1	0x0	0x0	0x0	0x80	0x60	0x1	0xCD	0xAB	0x34	0x12	0x56
0xC0		0xD0				0x00		0x80	0xC1		0xCD	0xAB	0x34	0x12	0x56

7.6.2.5 Internal Buffers

MCF8329A uses buffers internally to store the data received on I^2C. Highest priority is given to collecting data on the I^2C Bus. There are 2 buffers (ping-pong) for I^2C Rx Data and 2 buffers (ping-pong) for I^2C Tx Data.

A write request from external MCU is stored in Rx Buffer 1 and then the parsing block is triggered to work on this data in Rx Buffer 1. While MCF8329A is processing a write packet from Rx Buffer 1, if there is another new read/write request, the entire data from the I^2C bus is stored in Rx Buffer 2 and it will be processed after the current request.

MCF8329A can accommodate a maximum of two consecutive read/write requests. If MCF8329A is busy due to high priority interrupts, the data sent will be stored in internal buffers (Rx Buffer 1 and Rx Buffer 2). At this point, if there is a third read/write request, the Target ID will be NACK'd as the buffers are already full.

During read operations, the read request is processed and the read data from the register is stored in the Tx Buffer along with the CRC byte, if enabled. Now if the external MCU initiates an I^2C Read (Target ID + R bit), the data from this Tx Buffer is sent over I^2C. Since there are two Tx Buffers, register data from 2 MCF8329A reads can be buffered. Given this scenario, if there is a third read request, the control word will be stored in the Rx Buffer 1, but it will not be processed by MCF8329A as the Tx Buffers are full.

Once a data is read from Tx Buffer, the data is no longer stored in the Tx buffer. The buffer is cleared and it becomes available for the next data to be stored. If the read transaction was interrupted in between and if the MCU had not read all the bytes, external MCU can initiate another I^2C read (only I^2C read, without any control word information) to read all the data bytes from first.

7.6.2.6 CRC Byte Calculation

An 8-bit CCIT polynomial ($x^8 + x^2 + x + 1$) and CRC initial value 0xFF is used for CRC computation.

CRC Calculation in Write Operation: When the external MCU writes to MCF8329A, if the CRC is enabled, the external MCU has to compute an 8-bit CRC byte and add the CRC byte at the end of the data. MCF8329A will compute CRC using the same polynomial internally and if there is a mismatch, the write request is discarded. Input data for CRC calculation by external MCU for write operation are listed below:

1. Target ID + write bit.
2. Control word – 3 bytes
3. Data bytes – 2/4/8 bytes

CRC Calculation in Read Operation: When the external MCU reads from MCF8329A, if the CRC is enabled, MCF8329A sends the CRC byte at the end of the data. The CRC computation in read operation involves the start byte, control words sent by external MCU along with data bytes sent by MCF8329A. Input data for CRC calculation by external MCU to verify the data sent by MCF8329A are listed below :

1. Target ID + write bit
2. Control word – 3 bytes
3. Target ID + read bit
4. Data bytes – 2/4/8 bytes

7.7 EEPROM (Non-Volatile) Register Map

7.7.1 Algorithm_Configuration Registers

Table 7-14 lists the memory-mapped registers for the Algorithm_Configuration registers. All register offset addresses not listed in Table 7-14 should be considered as reserved locations and the register contents should not be modified.

Table 7-14. ALGORITHM_CONFIGURATION Registers

Offset	Acronym	Register Name	Section
80h	ISD_CONFIG	ISD Configuration	Section 7.7.1.1
82h	REV_DRIVE_CONFIG	Reverse Drive Configuration	Section 7.7.1.2
84h	MOTOR_STARTUP1	Motor Startup Configuration1	Section 7.7.1.3
86h	MOTOR_STARTUP2	Motor Startup Configuration2	Section 7.7.1.4
88h	CLOSED_LOOP1	Close Loop Configuration1	Section 7.7.1.5
8Ah	CLOSED_LOOP2	Close Loop Configuration2	Section 7.7.1.6
8Ch	CLOSED_LOOP3	Close Loop Configuration3	Section 7.7.1.7
8Eh	CLOSED_LOOP4	Close Loop Configuration4	Section 7.7.1.8
94h	REF_PROFILES1	Reference Profile Configuration1	Section 7.7.1.9
96h	REF_PROFILES2	Reference Profile Configuration2	Section 7.7.1.10
98h	REF_PROFILES3	Reference Profile Configuration3	Section 7.7.1.11
9Ah	REF_PROFILES4	Reference Profile Configuration4	Section 7.7.1.12
9Ch	REF_PROFILES5	Reference Profile Configuration5	Section 7.7.1.13
9Eh	REF_PROFILES6	Reference Profile Configuration6	Section 7.7.1.14

Complex bit access types are encoded to fit into small table cells. Table 7-15 shows the codes that are used for access types in this section.

Table 7-15. Algorithm_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.7.1.1 ISD_CONFIG Register (Offset = 80h) [Reset = 00000000h]

ISD_CONFIG is shown in Table 7-16.

Return to the Summary Table.

Register to configure initial speed detect settings

Table 7-16. ISD_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	ISD_EN	R/W	0h	ISD Enable 0h = Disable 1h = Enable
29	BRAKE_EN	R/W	0h	Brake enable during MSS 0h = Disable 1h = Enable
28	HIZ_EN	R/W	0h	Hi-Z enable during MSS 0h = Disable 1h = Enable
27	RVS_DR_EN	R/W	0h	Reverse Drive Enable 0h = Disable 1h = Enable
26	RESYNC_EN	R/W	0h	Resynchronization Enable 0h = Disable 1h = Enable
25-22	FW_DRV_RESYN_THR	R/W	0h	Minimum Speed threshold to resynchronize to close loop (% of MAX_SPEED) 0h = 5% 1h = 10% 2h = 15% 3h = 20% 4h = 25% 5h = 30% 6h = 35% 7h = 40% 8h = 45% 9h = 50% Ah = 55% Bh = 60% Ch = 70% Dh = 80% Eh = 90% Fh = 100%
21	RESERVED	R/W	0h	Reserved
20-17	SINGLE_SHUNT_BLANKING_TIME	R/W	0h	Blanking time before current is sampled from the PWM Edge 0h = 0.25 µs 1h = 0.5 µs 2h = 0.75 µs 3h = 1 µs 4h = 1.25 µs 5h = 1.5 µs 6h = 1.75 µs 7h = 2 µs 8h = 2.25 µs 9h = 2.5 µs Ah = 2.75 µs Bh = 3 µs Ch = 3.5 µs Dh = 4 µs Eh = 5 µs Fh = 6 µs

Table 7-16. ISD_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16-13	BRK_TIME	R/W	0h	Brake time during MSS 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 s 9h = 2 s Ah = 3 s Bh = 4 s Ch = 5 s Dh = 7.5 s Eh = 10 s Fh = 15 s
12-9	HIZ_TIME	R/W	0h	Hi-Z time during MSS 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 s 9h = 2 s Ah = 3 s Bh = 4 s Ch = 5 s Dh = 7.5 s Eh = 10 s Fh = 15 s
8-6	STAT_DETECT_THR	R/W	0h	BEMF threshold to detect if motor is stationary 0h = 100 mV 1h = 150 mV 2h = 200 mV 3h = 500 mV 4h = 1000 mV 5h = 1500 mV 6h = 2000 mV 7h = 3000 mV
5-2	REV_DRV_HANDOFF_THR	R/W	0h	Speed threshold used to transition to open loop during reverse drive (% of MAX_SPEED) 0h = 2.5% 1h = 5% 2h = 7.5% 3h = 10% 4h = 12.5% 5h = 15% 6h = 20% 7h = 25% 8h = 30% 9h = 40% Ah = 50% Bh = 60% Ch = 70% Dh = 80% Eh = 90% Fh = 100%

Table 7-16. ISD_CONFIG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	REV_DRV_OPEN_LOOP_CURRENT	R/W	0h	Open loop current limit during reverse drive (% of BASE_CURRENT) 0h = 15% 1h = 25% 2h = 35% 3h = 50%

7.7.1.2 REV_DRIVE_CONFIG Register (Offset = 82h) [Reset = 00000000h]

REV_DRIVE_CONFIG is shown in Table 7-17.

Return to the Summary Table.

Register to configure reverse drive settings

Table 7-17. REV_DRIVE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-27	REV_DRV_OPEN_LOOP_ACCEL_A1	R/W	0h	Open loop acceleration coefficient A1 during reverse drive 0h = 0.01 Hz/s 1h = 0.05 Hz/s 2h = 1 Hz/s 3h = 2.5 Hz/s 4h = 5 Hz/s 5h = 10 Hz/s 6h = 25 Hz/s 7h = 50 Hz/s 8h = 75 Hz/s 9h = 100 Hz/s Ah = 250 Hz/s Bh = 500 Hz/s Ch = 750 Hz/s Dh = 1000 Hz/s Eh = 5000 Hz/s Fh = 10000 Hz/s
26-23	REV_DRV_OPEN_LOOP_ACCEL_A2	R/W	0h	Open loop acceleration coefficient A2 during reverse drive 0h = 0.0 Hz/s2 1h = 0.05 Hz/s2 2h = 1 Hz/s2 3h = 2.5 Hz/s2 4h = 5 Hz/s2 5h = 10 Hz/s2 6h = 25 Hz/s2 7h = 50 Hz/s2 8h = 75 Hz/s2 9h = 100 Hz/s2 Ah = 250 Hz/s2 Bh = 500 Hz/s2 Ch = 750 Hz/s2 Dh = 1000 Hz/s2 Eh = 5000 Hz/s2 Fh = 10000 Hz/s2
22-20	ACTIVE_BRAKE_CURRENT_LIMIT	R/W	0h	Bus current limit during active braking (% of BASE_CURRENT) 0h = 10% 1h = 20 % 2h = 30 % 3h = 40 % 4h = 50 % 5h = 60 % 6h = 70 % 7h = 80 %
19-10	ACTIVE_BRAKE_KP	R/W	0h	10-bit value for active braking PI loop Kp. Kp = ACTIVE_BRAKE_KP / 2^7
9-0	ACTIVE_BRAKE_KI	R/W	0h	10-bit value for active braking PI loop Ki. Ki = ACTIVE_BRAKE_KI / 2^9

7.7.1.3 MOTOR_STARTUP1 Register (Offset = 84h) [Reset = 00000000h]

MOTOR_STARTUP1 is shown in Table 7-18.

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Register to configure motor startup settings1

Table 7-18. MOTOR_STARTUP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	MTR_STARTUP	R/W	0h	Motor startup option 0h = Align 1h = Double Align 2h = IPD 3h = Slow first cycle
28-25	ALIGN_SLOW_RAMP_RATE	R/W	0h	Align, slow first cycle and open loop current ramp rate 0h = 1 A/s 1h = 5 A/s 2h = 10 A/s 3h = 25 A/s 4h = 50 A/s 5h = 100 A/s 6h = 150 A/s 7h = 250 A/s 8h = 500 A/s 9h = 1000 A/s Ah = 2000 A/s Bh = 5000 A/s Ch = 10000 A/s Dh = 20000 A/s Eh = 50000 A/s Fh = No Limit A/s
24-21	ALIGN_TIME	R/W	0h	Align time 0h = 10 ms 1h = 50 ms 2h = 100 ms 3h = 200 ms 4h = 300 ms 5h = 400 ms 6h = 500 ms 7h = 750 ms 8h = 1 s 9h = 1.5 s Ah = 2 s Bh = 3 s Ch = 4 s Dh = 5 s Eh = 7.5 s Fh = 10 s

Table 7-18. MOTOR_STARTUP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
20-17	ALIGN_OR_SLOW_CURRENT_ILIMIT	R/W	0h	Align or slow first cycle current limit (% of BASE_CURRENT) 0h = 5 % 1h = 10 % 2h = 15 % 3h = 20 % 4h = 25 % 5h = 30 % 6h = 40 % 7h = 50 % 8h = 60 % 9h = 65 % Ah = 70 % Bh = 75 % Ch = 80 % Dh = 85 % Eh = 90 % Fh = 95 %
16-14	IPD_CLK_FREQ	R/W	0h	IPD Clock Frequency 0h = 50 Hz 1h = 100 Hz 2h = 250 Hz 3h = 500 Hz 4h = 1000 Hz 5h = 2000 Hz 6h = 5000 Hz 7h = 10000 Hz
13-9	IPD_CURR_THR	R/W	0h	IPD Current Threshold (% of BASE_CURRENT) 0h = 2.5 % 1h = 5 % 2h = 7.5 % 3h = 10 % 4h = 12.5 % 5h = 15 % 6h = 20 % 7h = 25 % 8h = 30 % 9h = 36.67 % Ah = 40 % Bh = 46.67 % Ch = 53..33 % Dh = 60 % Eh = 66.67 % Fh = 72 % 10h = NA 11h = NA 12h = NA 13h = NA 14h = NA 15h = NA 16h = NA 17h = NA 18h = NA 19h = NA 1Ah = NA 1Bh = NA 1Ch = NA 1Dh = NA 1Eh = NA 1Fh = NA
8	RESERVED	R/W	0h	Reserved

Table 7-18. MOTOR_STARTUP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	IPD_ADV_ANGLE	R/W	0h	IPD advance angle 0h = 0° 1h = 30° 2h = 60° 3h = 90°
5-4	IPD_REPEAT	R/W	0h	Number of times IPD is executed 0h = 1 time 1h = average of 2 times 2h = average of 3 times 3h = average of 4 times
3	OL_ILIMIT_CONFIG	R/W	0h	Open loop current limit configuration 0h = Open loop current limit defined by OL_ILIMIT 1h = Open loop current limit defined by ILIMIT
2	IQ_RAMP_DOWN_EN	R/W	0h	Iq ramp down for transition from open loop to closed loop 0h = Disable Iq ramp down 1h = Enable Iq ramp down
1	ACTIVE_BRAKE_EN	R/W	0h	Enable active braking during deceleration 0h = Disable Active Brake 1h = Enable Active Brake
0	REV_DRV_CONFIG	R/W	0h	Open loop Configuration setting for reverse drive 0h = Open loop current, A1, A2 based on forward drive 1h = Open loop current, A1, A2 based on reverse drive

7.7.1.4 MOTOR_STARTUP2 Register (Offset = 86h) [Reset = 00000000h]

MOTOR_STARTUP2 is shown in Table 7-19.

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Register to configure motor startup settings2

Table 7-19. MOTOR_STARTUP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-27	OL_ILIMIT	R/W	0h	Open Loop current limit (% of BASE_CURRENT) 0h = 5 % 1h = 10 % 2h = 15 % 3h = 20 % 4h = 25 % 5h = 30 % 6h = 40 % 7h = 50 % 8h = 60 % 9h = 65 % Ah = 70 % Bh = 75 % Ch = 80 % Dh = 85 % Eh = 90 % Fh = 95 %
26-23	OL_ACC_A1	R/W	0h	Open loop acceleration coefficient A1 0h = 0.01 Hz/s 1h = 0.05 Hz/s 2h = 1 Hz/s 3h = 2.5 Hz/s 4h = 5 Hz/s 5h = 10 Hz/s 6h = 25 Hz/s 7h = 50 Hz/s 8h = 75 Hz/s 9h = 100 Hz/s Ah = 250 Hz/s Bh = 500 Hz/s Ch = 750 Hz/s Dh = 1000 Hz/s Eh = 5000 Hz/s Fh = 10000 Hz/s
22-19	OL_ACC_A2	R/W	0h	Open loop acceleration coefficient A2 0h = 0.0 Hz/s2 1h = 0.05 Hz/s2 2h = 1 Hz/s2 3h = 2.5 Hz/s2 4h = 5 Hz/s2 5h = 10 Hz/s2 6h = 25 Hz/s2 7h = 50 Hz/s2 8h = 75 Hz/s2 9h = 100 Hz/s2 Ah = 250 Hz/s2 Bh = 500 Hz/s2 Ch = 750 Hz/s2 Dh = 1000 Hz/s2 Eh = 5000 Hz/s2 Fh = 10000 Hz/s2
18	AUTO_HANDOFF_EN	R/W	0h	Auto Handoff Enable 0h = Disable Auto Handoff (and use OPN_CL_HANDOFF_THR) 1h = Enable Auto Handoff

Table 7-19. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-13	OPN_CL_HANDOFF_THR	R/W	0h	Open to Close loop Handoff Threshold (% of MAX_SPEED) 0h = 1% 1h = 2% 2h = 3% 3h = 4% 4h = 5% 5h = 6% 6h = 7% 7h = 8% 8h = 9% 9h = 10% Ah = 11% Bh = 12% Ch = 13% Dh = 14% Eh = 15% Fh = 16% 10h = 17% 11h = 18% 12h = 19% 13h = 20% 14h = 22.5% 15h = 25% 16h = 27.5% 17h = 30% 18h = 32.5% 19h = 35% 1Ah = 37.5% 1Bh = 40% 1Ch = 42.5% 1Dh = 45% 1Eh = 47.5% 1Fh = 50%

Table 7-19. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
12-8	ALIGN_ANGLE	R/W	0h	Align Angle 0h = 0 deg 1h = 10 deg 2h = 20 deg 3h = 30 deg 4h = 45 deg 5h = 60 deg 6h = 70 deg 7h = 80 deg 8h = 90 deg 9h = 110 deg Ah = 120 deg Bh = 135 deg Ch = 150 deg Dh = 160 deg Eh = 170 deg Fh = 180 deg 10h = 190 deg 11h = 210 deg 12h = 225 deg 13h = 240 deg 14h = 250 deg 15h = 260 deg 16h = 270 deg 17h = 280 deg 18h = 290 deg 19h = 315 deg 1Ah = 330 deg 1Bh = 340 deg 1Ch = 350 deg 1Dh = Reserved 1Eh = Reserved 1Fh = Reserved
7-4	SLOW_FIRST_CYC_FREQ	R/W	0h	Frequency of first cycle in slow first cycle startup (% of MAX_SPEED) 0h = 0.1% 1h = 0.2% 2h = 0.3% 3h = 0.4% 4h = 0.5% 5h = 0.7% 6h = 1.0% 7h = 1.2% 8h = 1.5% 9h = 2.0% Ah = 2.5% Bh = 3% Ch = 3.5% Dh = 4% Eh = 4.5% Fh = 5%
3	FIRST_CYCLE_FREQ_SEL	R/W	0h	First cycle frequency in open loop for align, double align and IPD startup options 0h = 0 Hz 1h = Defined by SLOW_FIRST_CYC_FREQ

Table 7-19. MOTOR_STARTUP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	THETA_ERROR_RAMP_RATE	R/W	0h	Ramp rate for reducing difference between estimated angle and open loop angle 0h = 0.01 deg/ms 1h = 0.05 deg/ms 2h = 0.1 deg/ms 3h = 0.15 deg/ms 4h = 0.2 deg / ms 5h = 0.5 deg/ms 6h = 1 deg/ms 7h = 2 deg/ms

7.7.1.5 CLOSED_LOOP1 Register (Offset = 88h) [Reset = 00000000h]

CLOSED_LOOP1 is shown in Table 7-20.

Return to the Summary Table.

Register to configure close loop settings1

Table 7-20. CLOSED_LOOP1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	RESERVED	R/W	0h	Reserved
29-25	CL_ACC	R/W	0h	Closed loop acceleration Speed Mode (Hz/s) Power Mode (W/s) Current Mode (A/s) Voltage Mode(0.1% modulation index per second) 0h = 0.5 1h = 1 2h = 2.5 3h = 5 4h = 7.5 5h = 10 6h = 20 7h = 40 8h = 60 9h = 80 Ah = 100 Bh = 200 Ch = 300 Dh = 400 Eh = 500 Fh = 600 10h = 700 11h = 800 12h = 900 13h = 1000 14h = 2000 15h = 4000 16h = 6000 17h = 8000 18h = 10000 19h = 20000 1Ah = 30000 1Bh = 40000 1Ch = 50000 1Dh = 60000 1Eh = 70000 1Fh = No limit
24	CL_DEC_CONFIG	R/W	0h	Closed loop deceleration configuration 0h = Closed loop deceleration defined by CL_DEC 1h = Closed loop deceleration defined by CL_ACC

Table 7-20. CLOSED_LOOP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
23-19	CL_DEC	R/W	0h	Closed loop deceleration. Speed Mode (Hz/s) Power Mode (W/s) Current Mode (A/s) Voltage Mode(0.1% modulation index per second) Note: This configuration bits are not used if AVS is enabled in speed mode or CL_DEC_CONFIG is set to '1' 0h = 0.5 1h = 1 2h = 2.5 3h = 5 4h = 7.5 5h = 10 6h = 20 7h = 40 8h = 60 9h = 80 Ah = 100 Bh = 200 Ch = 300 Dh = 400 Eh = 500 Fh = 600 10h = 700 11h = 800 12h = 900 13h = 1000 14h = 2000 15h = 4000 16h = 6000 17h = 8000 18h = 10000 19h = 20000 1Ah = 30000 1Bh = 40000 1Ch = 50000 1Dh = 60000 1Eh = 70000 1Fh = No limit
18-15	PWM_FREQ_OUT	R/W	0h	PWM output frequency 0h = 10 kHz 1h = 15 kHz 2h = 20 kHz 3h = 25 kHz 4h = 30 kHz 5h = 35 kHz 6h = 40 kHz 7h = 45 kHz 8h = 50 kHz 9h = 55 kHz Ah = 60 kHz Bh = 65 kHz Ch = 70 kHz Dh = 75 kHz Eh = Not Applicable Fh = Not Applicable
14	RESERVED	R/W	0h	Reserved
13-12	FG_SEL	R/W	0h	FG select 0h = Output FG in ISD, open loop and closed loop (HW config) 1h = Output FG in only closed loop 2h = Output FG in open loop for the first try. 3h = Not Defined

Table 7-20. CLOSED_LOOP1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11-8	FG_DIV	R/W	0h	FG Division factor 0h = Divide by 1 (2-pole motor mechanical speed) 1h = Divide by 1 (2-pole motor mechanical speed) 2h = Divide by 2 (4-pole motor mechanical speed) 3h = Divide by 3 (6-pole motor mechanical speed) 4h = Divide by 4 (8-pole motor mechanical speed) ... Fh = Divide by 15 (30-pole motor mechanical speed)
7	FG_CONFIG	R/W	0h	FG output configuration 0h = FG active as long as motor is driven 1h = FG active till BEMF drops below BEMF threshold defined by FG_BEMF_THR
6-4	FG_BEMF_THR	R/W	0h	FG output BEMF threshold, calculated as voltage at SHx pin divided by voltage gain. Voltage gain = 20 V/V, BUS_VOLT = 60 Voltage gain = 10 V/V, BUS_VOLT = 30 Voltage gain = 5 V/V, BUS_VOLT = 15 0h = +/- 1mV 1h = +/- 2mV 2h = +/- 5mV 3h = +/- 10mV 4h = +/- 20mV 5h = +/- 30mV 6h = Not Applicable 7h = Not Applicable
3	AVS_EN	R/W	0h	AVS enable 0h = Disable 1h = Enable
2	DEADTIME_COMP_EN	R/W	0h	Deadtime compensation enable 0h = Disable 1h = Enable
1	RESERVED	R/W	0h	Reserved
0	LOW_SPEED_RECIRC_BRAKE_EN	R/W	0h	Motor stop option applied when MTR_STOP is recirculation Mode and motor is running in align or open loop 0h = Hi-z 1h = Low Side Brake

7.7.1.6 CLOSED_LOOP2 Register (Offset = 8Ah) [Reset = 00000000h]

CLOSED_LOOP2 is shown in Table 7-21.

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Register to configure close loop settings2

Table 7-21. CLOSED_LOOP2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-28	MTR_STOP	R/W	0h	Motor stop option 0h = Hi-z 1h = Recirculation Mode 2h = Low side braking 3h = Low side braking 4h = Active spin down 5h = Not Defined 6h = Not Defined 7h = Not Defined
27-24	MTR_STOP_BRK_TIME	R/W	0h	Brake time during motor stop 0h = 1 ms 1h = 1 ms 2h = 1 ms 3h = 1 ms 4h = 1 ms 5h = 5 ms 6h = 10 ms 7h = 50 ms 8h = 100 ms 9h = 250 ms Ah = 500 ms Bh = 1000 ms Ch = 2500 ms Dh = 5000 ms Eh = 10000 ms Fh = 15000 ms
23-20	ACT_SPIN_THR	R/W	0h	Speed threshold for active spin down (% of MAX_SPEED) 0h = 100 % 1h = 90 % 2h = 80 % 3h = 70 % 4h = 60% 5h = 50 % 6h = 45 % 7h = 40 % 8h = 35 % 9h = 30 % Ah = 25 % Bh = 20 % Ch = 15 % Dh = 10 % Eh = 5 % Fh = 2.5 %

Table 7-21. CLOSED_LOOP2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
19-16	BRAKE_SPEED_THRESHOLD	R/W	0h	Speed threshold below which brake is applied for BRAKE pin and Motor stop options (Low side Braking) (% of MAX_SPEED) 0h = 100 % 1h = 90 % 2h = 80 % 3h = 70 % 4h = 60% 5h = 50 % 6h = 45 % 7h = 40 % 8h = 35 % 9h = 30 % Ah = 25 % Bh = 20 % Ch = 15 % Dh = 10 % Eh = 5 % Fh = 2.5 %
15-8	MOTOR_RES	R/W	0h	8-bit values for motor phase resistance
7-0	MOTOR_IND	R/W	0h	8-bit values for motor phase inductance

7.7.1.7 CLOSED_LOOP3 Register (Offset = 8Ch) [Reset = 00000000h]

CLOSED_LOOP3 is shown in Table 7-22.

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Register to configure close loop settings3

Table 7-22. CLOSED_LOOP3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-23	MOTOR_BEMF_CONST	R/W	0h	8-bit values for motor BEMF Constant
22-13	CURR_LOOP_KP	R/W	0h	10-bit Kp value for Iq and Id PI loop. CURR_LOOP_KP is divided in 2 sections. SCALE(9:8) and VALUE(7:0). Kp = VALUE / 10^SCALE Set to 0 for auto calculation of current Kp and Ki
12-3	CURR_LOOP_KI	R/W	0h	10-bit Ki value for Iq and Id PI loop. CURR_LOOP_KI is divided in 2 sections. SCALE(9:8) and VALUE(7:0). Ki = 1000 × VALUE / 10^SCALE Set to 0 for auto calculation of current Kp and Ki
2-0	SPD_LOOP_KP	R/W	0h	3 MSB bits for speed loop Kp. SPD_LOOP_KP is divided in 2 sections SCALE(9:8) and VALUE(7:0). Kp = 0.01 × VALUE / 10^SCALE.

7.7.1.8 CLOSED_LOOP4 Register (Offset = 8Eh) [Reset = 00000000h]

CLOSED_LOOP4 is shown in Table 7-23.

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Register to configure close loop settings4

Table 7-23. CLOSED_LOOP4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-24	SPD_LOOP_KP	R/W	0h	7 LSB bits for speed loop Kp. SPD_LOOP_KP is divided in 2 sections SCALE(10:9) and VALUE(8:0). Kp = 0.01 × VALUE / 10^SCALE.
23-14	SPD_LOOP_KI	R/W	0h	10 bit value for speed loop Ki. SPD_LOOP_KI is divided in 2 sections SCALE(9:8) and VALUE(7:0). Ki = 0.1 × VALUE / 10^SCALE.
13-0	MAX_SPEED	R/W	0h	14-bit value for setting maximum value of Speed in electrical Hz. 0 - 9600d = MAX_SPEED/6 9601d - 16383d = (MAX_SPEED/4 - 800) For example, if MAX_SPEED is 0x5DC(1500d), then maximum motor speed (Hz) is 1500/6 is equal to 250Hz If MAX_SPEED is 0x2710(10000d), then maximum motor speed (Hz) is (10000/4) - 800 is equal to 1700 Hz

7.7.1.9 REF_PROFILES1 Register (Offset = 94h) [Reset = 00000000h]

REF_PROFILES1 is shown in Table 7-24.

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Register to configure reference profile1

Table 7-24. REF_PROFILES1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	REF_PROFILE_CONFIG	R/W	0h	Configuration for Reference profiles 0h = Reference Mode 1h = Linear Mode 2h = Staircase Mode 3h = Forward Reverse Mode
28-21	DUTY_ON1	R/W	0h	Duty_ON1 Configuration Turn On Duty Cycle (%) = {(DUTY_ON1/255) × 100}
20-13	DUTY_OFF1	R/W	0h	Duty_OFF1 Configuration Turn Off Duty Cycle (%) = {(DUTY_OFF1/255) × 100}
12-5	DUTY_CLAMP1	R/W	0h	Duty_CLAMP1 Configuration Duty Cycle for clamping (%) = {(DUTY_CLAMP1/255) ×100}
4-0	DUTY_A	R/W	0h	5 MSB bits for Duty Cycle A

7.7.1.10 REF_PROFILES2 Register (Offset = 96h) [Reset = 00000000h]

REF_PROFILES2 is shown in Table 7-25.

Return to the Summary Table.

Register to configure reference profile2

Table 7-25. REF_PROFILES2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-28	DUTY_A	R/W	0h	3 LSB bits for Duty Cycle A Configuration Duty Cycle A (%) = {(DUTY_A/255) × 100}
27-20	DUTY_B	R/W	0h	Duty_B Configuration Duty Cycle B (%) = {(DUTY_B/255) × 100}
19-12	DUTY_C	R/W	0h	Duty_C Configuration Duty Cycle C (%) = {(DUTY_C/255) × 100}
11-4	DUTY_D	R/W	0h	Duty_D Configuration Duty Cycle D (%) = {(DUTY_D/255) × 100}
3-0	DUTY_E	R/W	0h	4 MSB bits for Duty Cycle E

7.7.1.11 REF_PROFILES3 Register (Offset = 98h) [Reset = 00000000h]

REF_PROFILES3 is shown in Table 7-26.

Return to the Summary Table.

Register to configure reference profile3

Table 7-26. REF_PROFILES3 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-27	DUTY_E	R/W	0h	4 LSB bits for Duty Cycle E Configuration Duty Cycle E (%) = {(DUTY_E/255) × 100}
26-19	DUTY_ON2	R/W	0h	Duty_ON2 Configuration Turn On Duty Cycle (%) = {(DUTY_ON2/255) × 100}
18-11	DUTY_OFF2	R/W	0h	Duty_OFF2 Configuration Turn Off Duty Cycle (%) = {(DUTY_OFF2/255) × 100}
10-3	DUTY_CLAMP2	R/W	0h	Duty_CLAMP2 Configuration Duty Cycle for clamping (%) = {(DUTY_CLAMP2/255) × 100}
2-1	DUTY_HYS	R/W	0h	Duty hysteresis 0h = 0% 1h = 0.8% 2h = 2% 3h = 4%
0	RESERVED	R/W	0h	Reserved

7.7.1.12 REF_PROFILES4 Register (Offset = 9Ah) [Reset = 00000000h]

REF_PROFILES4 is shown in Table 7-27.

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Register to configure reference profile4

Table 7-27. REF_PROFILES4 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-23	REF_OFF1	R/W	0h	Turn off ref Configuration Turn off reference (% of Maximum Reference) = {(REF_OFF1/255) × 100}
22-15	REF_CLAMP1	R/W	0h	Ref Clamp1 Configuration Clamp Ref (% of Maximum Reference) = {(REF_CLAMP1/255) × 100}
14-7	REF_A	R/W	0h	Ref A configuration Ref A (% of Maximum Reference) = {(REF_A/255) × 100}
6-0	REF_B	R/W	0h	7 MSB of REF_B configuration

7.7.1.13 REF_PROFILES5 Register (Offset = 9Ch) [Reset = 00000000h]

REF_PROFILES5 is shown in Table 7-28.

Return to the Summary Table.

Register to configure reference profile5

Table 7-28. REF_PROFILES5 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	REF_B	R/W	0h	1 LSB of REF_B configuration Ref B(% of Maximum Reference) = {(REF_B/255) × 100}
29-22	REF_C	R/W	0h	Ref C configuration Ref C (% of Maximum Reference) = {(REF_C/255) × 100}
21-14	REF_D	R/W	0h	Ref D configuration Ref D (% of Maximum Reference) = {(REF_D/255) × 100}
13-6	REF_E	R/W	0h	Ref E Configuration Ref E(% of Maximum Reference) = {(REF_E/255)*100}
5-0	RESERVED	R/W	0h	Reserved

7.7.1.14 REF_PROFILES6 Register (Offset = 9Eh) [Reset = 00000000h]

REF_PROFILES6 is shown in Table 7-29.

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Register to configure reference profile6

Table 7-29. REF_PROFILES6 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-23	REF_OFF2	R/W	0h	Turn off Ref Configuration Turn off Ref (% of Maximum Reference)) = {(REF_OFF2/255) × 100}
22-15	REF_CLAMP2	R/W	0h	Clamp Ref Configuration Clamp Ref (% of Maximum Reference) = {(REF_CLAMP2/255) ×100}
14-0	RESERVED	R/W	0h	Reserved

7.7.2 Internal_Algorithm_Configuration Registers

Table 7-30 lists the memory-mapped registers for the Internal_Algorithm_Configuration registers. All register offset addresses not listed in Table 7-30 should be considered as reserved locations and the register contents should not be modified.

Table 7-30. INTERNAL_ALGORITHM_CONFIGURATION Registers

Offset	Acronym	Register Name	Section
A0h	INT_ALGO_1	Internal Algorithm Configuration1	Section 7.7.2.1
A2h	INT_ALGO_2	Internal Algorithm Configuration2	Section 7.7.2.2

Complex bit access types are encoded to fit into small table cells. Table 7-31 shows the codes that are used for access types in this section.

Table 7-31. Internal_Algorithm_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.7.2.1 INT_ALGO_1 Register (Offset = A0h) [Reset = 00000000h]

INT_ALGO_1 is shown in Table 7-32.

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Table 7-32. INT_ALGO_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-29	ACTIVE_BRAKE_SPEED_DELTA_LIMIT_EXIT	R/W	0h	Speed Reference difference (% of MAX_SPEED) to come out of Active Brake state 0h = 2.5% 1h = 5% 2h = 7.5% 3h = 10%
28-27	SPEED_PIN_GLITCH_FILTER	R/W	0h	Glitch filter applied on SPEED/WAKE pin in PWM and Frequency input mode 0h = No Glitch Filter 1h = 0.2 µs 2h = 0.5 µs 3h = 1.0 µs
26	FAST_ISD_EN	R/W	0h	Enable fast speed detection during ISD 0h = Disable Fast ISD 1h = Enable Fast ISD
25-24	ISD_STOP_TIME	R/W	0h	Persistence time for declaring motor has stopped 0h = 1 ms 1h = 5 ms 2h = 50 ms 3h = 100 ms
23-22	ISD_RUN_TIME	R/W	0h	Persistence time for declaring motor is running 0h = 1 ms 1h = 5 ms 2h = 50 ms 3h = 100 ms
21-20	ISD_TIMEOUT	R/W	0h	Timeout in case ISD is unable to reliably detect speed or direction 0h = 500ms 1h = 750 ms 2h = 1000 ms 3h = 2000 ms
19-17	AUTO_HANDOFF_MIN_BEMF	R/W	0h	Minimum BEMF for auto handoff 0h = 0 mV 1h = 100 mV 2h = 200 mV 3h = 500 mV 4h = 1000 mV 5h = 2000 mV 6h = 2500 mV 7h = 3000 mV
16-15	RESERVED	R/W	0h	Reserved
14-13	RESERVED	R/W	0h	Reserved
12-11	RESERVED	R/W	0h	Reserved
10-8	MPET_OPEN_LOOP_CURR_REF	R/W	0h	Open Loop Current Reference for MPET (% of BASE_CURRENT) 0h = 10% 1h = 20% 2h = 30% 3h = 40% 4h = 50% 5h = 60% 6h = 70% 7h = 80%

Table 7-32. INT_ALGO_1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7-6	MPET_OPEN_LOOP_SPEED_REF	R/W	0h	Open Loop Speed Reference for MPET (% of MAXIMUM_SPEED) 0h = 15% 1h = 25% 2h = 35% 3h = 50%
5-3	MPET_OPEN_LOOP_SLEW_RATE	R/W	0h	Open loop acceleration for MPET 0h = 0.1 Hz/s 1h = 0.5 Hz/s 2h = 1 Hz/s 3h = 2 Hz/s 4h = 3 Hz/s 5h = 5 Hz/s 6h = 10 Hz/s 7h = 20 Hz/s
2-0	REV_DRV_OPEN_LOOP_DEC	R/W	0h	% of open loop acceleration to be applied during open loop deceleration in reverse drive 0h = 50% 1h = 60% 2h = 70% 3h = 80% 4h = 90% 5h = 100% 6h = 125% 7h = 150%

7.7.2.2 INT_ALGO_2 Register (Offset = A2h) [Reset = 00000000h]

INT_ALGO_2 is shown in Table 7-33.

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Register to configure internal algorithm parameters2

Table 7-33. INT_ALGO_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-21	FLUX_WEAKENING_KP	R/W	0h	10-bit value for flux weakening Kp FLUX_WEAKENING_KP is divided in 2 sections SCALE(9:8) and VALUE(7:0) Kp = 0.1 × VALUE / 10^SCALE.
20-11	FLUX_WEAKENING_KI	R/W	0h	10-bit value for flux weakening Ki FLUX_WEAKENING_KI is divided in 2 sections SCALE(9:8) and VALUE(7:0) Ki = 10.0 × VALUE / 10^SCALE).
10	FLUX_WEAKENING_EN	R/W	0h	Flux Weakening Enable 0h = Flux Weakening Disabled 1h = Flux Weakening Enabled
9-6	CL_SLOW_ACC	R/W	0h	Close loop acceleration when estimator is not yet fully aligned just after transition to closed loop Speed Mode (Hz/s) Power Mode (W/s) Current Mode (A/s) Voltage Mode(0.1% modulation index per second) 0h = 0.1 1h = 1 2h = 2 3h = 3 4h = 5 5h = 10 6h = 20 7h = 30 8h = 40 9h = 50 Ah = 100 Bh = 200 Ch = 500 Dh = 750 Eh = 1000 Fh = 2000
5-3	ACTIVE_BRAKE_BUS_CURRENT_SLEW_RATE	R/W	0h	Bus Current slew rate during active braking (A/s) 0h = 10 A/s 1h = 50 A/s 2h = 100 A/s 3h = 250 A/s 4h = 500 A/s 5h = 1000 A/s 6h = 5000 A/s 7h = No Limit
2	RESERVED	R/W	0h	Reserved
1	MPET_KE_MEAS_PARAMETER_SELECT	R/W	0h	MPET parameters selection 0h = Configured parameters for normal motor operation (OL_ACC_A1, OL_ACC_A2 for slew rate, OL_ILIMIT for current reference and OPN_CL_HANDOFF_THR for speed reference). 1h = MPET specific parameters (MPET_OPEN_LOOP_SLEW_RATE for slew rate, MPET_OPEN_LOOP_CURR_REF for current reference, MPET_OPEN_LOOP_SPEED_REF for speed reference).

Table 7-33. INT_ALGO_2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	IPD_HIGH_RESOLUTION_EN	R/W	0h	IPD high resolution enable 0h = Disable 1h = Enable

7.7.3 Hardware_Configuration Registers

Table 7-34 lists the memory-mapped registers for the Hardware_Configuration registers. All register offset addresses not listed in Table 7-34 should be considered as reserved locations and the register contents should not be modified.

Table 7-34. HARDWARE_CONFIGURATION Registers

Offset	Acronym	Register Name	Section
A4h	PIN_CONFIG	Hardware Pin Configuration	Section 7.7.3.1
A6h	DEVICE_CONFIG1	Device configuration1	Section 7.7.3.2
A8h	DEVICE_CONFIG2	Device configuration2	Section 7.7.3.3
AAh	PERI_CONFIG1	Peripheral Configuration1	Section 7.7.3.4
ACh	GD_CONFIG1	Gate Driver Configuration1	Section 7.7.3.5
AEh	GD_CONFIG2	Gate Driver Configuration2	Section 7.7.3.6

Complex bit access types are encoded to fit into small table cells. Table 7-35 shows the codes that are used for access types in this section.

Table 7-35. Hardware_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.7.3.1 PIN_CONFIG Register (Offset = A4h) [Reset = 00000000h]

PIN_CONFIG is shown in Table 7-36.

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Register to configure hardware pins

Table 7-36. PIN_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-28	FLUX_WEAKENING_CURRENT_RATIO	R/W	0h	Max value of Flux Weakening Current Reference as % of ILIMIT 0h = Only circular limit in place 1h = 80% 2h = 70% 3h = 60% 4h = 50% 5h = 40% 6h = 30% 7h = 20%
27	VdcFilterDisable	R/W	0h	Vdc filter disable 0h = Vdc filter Enable 1h = Vdc filter Disable
26-22	LEAD_ANGLE	R/W	0h	Lead Angle (deg) 0- 15 = 1 × Bit Value 15 - 31 = 2 × (Bit Value -15) + 15
21-11	MAX_POWER	R/W	0h	Maximum power (Watts) 0- 1023 = 1 × Bit Value 1024 - 2047 = 2 × (Bit Value -1024) + 1024
10-9	FG_IDLE_CONFIG	R/W	0h	FG Configuration During Stop 0h = FG continues and end state not defined, provided FG_CONFIG (defining FG during coasting) 1h = FG is Hi-Z (Externally Pulled up) 2h = FG is pulled to Low 3h = FG is Hi-Z (Externally Pulled up)
8-7	FG_FAULT_CONFIG	R/W	0h	FG signal behavior during fault 0h = FG is Hi-Z (Externally Pulled up) 1h = FG is Hi-Z (Externally Pulled up) 2h = FG is pulled to Low 3h = FG active till BEMF drops below BEMF threshold defined by FG_BEMF_THR if FG_CONFIG is1
6	RESERVED	R/W	0h	Reserved
5	BRAKE_PIN_MODE	R/W	0h	Brake Pin Mode 0h = Low side Brake 1h = Reserved
4	RESERVED	R/W	0h	Reserved
3-2	BRAKE_INPUT	R/W	0h	Brake pin override 0h = Hardware Pin BRAKE 1h = Override pin and brake according to BRAKE_PIN_MODE 2h = Override pin and do not brake / align 3h = Hardware Pin BRAKE
1-0	SPEED_MODE	R/W	0h	Configure Reference Command mode from Speed pin 0h = Analog Mode 1h = Controlled by Duty Cycle of SPEED Input Pin 2h = Register Override mode 3h = Controlled by Frequency of SPEED Input Pin

7.7.3.2 DEVICE_CONFIG1 Register (Offset = A6h) [Reset = 00000000h]

DEVICE_CONFIG1 is shown in Table 7-37.

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Register to configure device

Table 7-37. DEVICE_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	MTPA_EN	R/W	0h	Enable Maximum Torque Per Ampere Operation 0h = MTPA disabled 1h = MTPA enabled
29-28	DAC_SOX_ANA_CONFIG	R/W	0h	Pin 33 configuration 0h = DACOUT 1h = CSA_OUT 2h = ANA_ON_PIN 3h = CSA_OUT
27	RESERVED	R/W	0h	Reserved
26-20	I2C_SLAVE_ADDR	R/W	0h	I2C slave address
19-5	RESERVED	R/W	0h	Reserved
4-3	SLEW_RATE_I2C_PINS	R/W	0h	Slew Rate Control for I2C Pins 0h = 4.8 mA 1h = 3.9 mA 2h = 1.86 mA 3h = 30.8 mA
2	PULLUP_ENABLE	R/W	0h	Internal Pull up Enable for nFault and FG Pins 0h = Disable 1h = Enable
1-0	BUS_VOLT	R/W	0h	Maximum DC Bus Voltage Configuration (V) 0h = 15 V 1h = 30 V 2h = 60 V 3h = Not defined

7.7.3.3 DEVICE_CONFIG2 Register (Offset = A8h) [Reset = 00000000h]

DEVICE_CONFIG2 is shown in Table 7-38.

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Register to configure device

Table 7-38. DEVICE_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-16	INPUT_MAXIMUM_FREQ	R/W	0h	Input frequency on speed pin for control mode as "controlled by frequency speed pin input" that corresponds to 100% duty cycle Input duty cycle = Input frequency / INPUT_MAXIMUM_FREQ
15-14	SLEEP_ENTRY_TIME	R/W	0h	Device enters sleep mode when input source is held at or below the sleep entry threshold for SLEEP_ENTRY_TIME 0h = Sleep entry when SPEED pin remains low for 50µs 1h = Sleep entry when SPEED pin remains low for 200µs 2h = Sleep entry when SPEED pin remains low for 20ms 3h = Sleep entry when SPEED pin remains low for 200ms
13	RESERVED	R/W	0h	Reserved
12	DYNAMIC_VOLTAGE_GAIN_EN	R/W	0h	Adjust voltage gain at 1ms rate for optimal voltage resolution at all voltage levels 0h = Dynamic Voltage Gain is Disabled 1h = Dynamic Voltage Gain is Enabled
11	DEV_MODE	R/W	0h	Device mode select 0h = Standby Mode 1h = Sleep Mode
10-9	CLK_SEL	R/W	0h	Clock Source 0h = Internal Oscillator 1h = N/A 2h = NA 3h = External Clock input
8	EXT_CLK_EN	R/W	0h	Enable External Clock mode 0h = Disable 1h = Enable
7-5	EXT_CLK_CONFIG	R/W	0h	External Clock Configuration 0h = 8KHz 1h = 16KHz 2h = 32KHz 3h = 64KHz 4h = 128 KHz 5h = 256 KHz 6h = 512KHz 7h = 1024 KHz
4	EXT_WD_EN	R/W	0h	Enable external Watch Dog 0h = Disable 1h = Enable
3-2	EXT_WD_CONFIG	R/W	0h	External Watchdog Configuration in I2C mode 0h = 1s 1h = 2s 2h = 5s 3h = 10s
1	RESERVED	R/W	0h	Reserved
0	EXT_WD_FAULT_MODE	R/W	0h	External Watchdog Fault Mode 0h = Report Only 1h = Latch with Hi-z

7.7.3.4 PERI_CONFIG1 Register (Offset = AAh) [Reset = 40000000h]

PERI_CONFIG1 is shown in Table 7-39.

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Register to peripheral1

Table 7-39. PERI_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	SPREAD_SPECTRUM_MODULATION_DIS	R/W	1h	Spread Spectrum Modulation Disable 0h = SSM is Enabled 1h = SSM is Disabled
29-26	DIG_DEAD_TIME	R/W	0h	Dead time 0h = 0 1h = 50 ns 2h = 100 ns 3h = 150 ns 4h = 200 ns 5h = 250 ns 6h = 300 ns 7h = 350 ns 8h = 400 ns 9h = 450 ns Ah = 500 ns Bh = 600 ns Ch = 700 ns Dh = 800 ns Eh = 900 ns Fh = 1000 ns
25-22	BUS_CURRENT_LIMIT	R/W	0h	Bus Current Limit (% of BASE_CURRENT) 0h = 5 % 1h = 10 % 2h = 15 % 3h = 20 % 4h = 25 % 5h = 30 % 6h = 40 % 7h = 50 % 8h = 60 % 9h = 65 % Ah = 70 % Bh = 75 % Ch = 80 % Dh = 85 % Eh = 90 % Fh = 95 %
21	BUS_CURRENT_LIMIT_ENABLE	R/W	0h	Bus Current Limit Enable 0h = Disable 1h = Enable
20-19	DIR_INPUT	R/W	0h	DIR pin override 0h = Hardware Pin DIR 1h = Override DIR pin with clockwise rotation OUTA-OUTB-OUTC 2h = Override DIR pin with counter clockwise rotation OUTA-OUTC-OUTB 3h = Hardware Pin DIR
18	DIR_CHANGE_MODE	R/W	0h	Response to change of DIR pin status 0h = Follow motor stop options and ISD routine on detecting DIR change 1h = Change the direction through Reverse Drive while continuously driving the motor
17	RESERVED	R/W	0h	Reserved

Table 7-39. PERI_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16-13	ACTIVE_BRAKE_SPEED_DELTA_LIMIT_ENTRY	R/W	0h	Speed Reference difference(% of MAX_SPEED) to enter Active Brake state 0h = 2.5% 1h = 5% 2h = 10% 3h = 15% 4h = 20% 5h = 25% 6h = 30% 7h = 35% 8h = 40% 9h = 45% Ah = 50% Bh = 60% Ch = 70% Dh = 80% Eh = 90% Fh = 100%
12-10	ACTIVE_BRAKE_MOD_INDEX_LIMIT	R/W	0h	Modulation Index limit below which active braking will be applied 0h = 0% 1h = 40% 2h = 50% 3h = 60% 4h = 70% 5h = 80% 6h = 90% 7h = 100%
9	SPD_RANGE_SELECT	R/W	0h	SPEED/WAKE pin PWM input frequency selection 0h = 325Hz to 100KHz speed PWM input 1h = 10Hz to 325Hz speed PWM input
8	RESERVED	R/W	0h	Reserved
7-6	FLUX_WEAKENING_REFERENCE	R/W	0h	Modulation Index Reference to be tracked in Flux Weakening mode 0h = 70% 1h = 80% 2h = 90% 3h = 95%
5-4	CTRL_MODE	R/W	0h	Control mode 0h = Speed Control 1h = Power Control 2h = Current Control 3h = Modulation index Control
3-0	SALIENCY_PERCENTAGE	R/W	0h	Saliency Percentage calculated as ((Lq-Ld) × 100)/(4 × (Lq+Ld))

7.7.3.5 GD_CONFIG1 Register (Offset = ACh) [Reset = 00000000h]

GD_CONFIG1 is shown in Table 7-40.

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Register to configure gated driver settings1

Table 7-40. GD_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-26	RESERVED	R/W	0h	Reserved
25-24	BST_CHRG_TIME	R/W	0h	Bootstrap Capacitor Charging Time 0h = 0 ms 1h = 3 ms 2h = 6 ms 3h = 12 ms
23	SNS_FLT_MODE	R/W	0h	Sense Over Current Fault Mode 0h = Latch Mode 1h = Retry after tLCK_RETRY
22	VDS_FLT_MODE	R/W	0h	VDS Over Current Fault Mode 0h = Latch Mode 1h = Retry after tLCK_RETRY
21	BST_UV_MODE	R/W	0h	BST Under Voltage Fault Mode 0h = Latch Mode 1h = Retry after tLCK_RETRY
20	GVDD_UV_MODE	R/W	0h	GVDD Under Voltage Fault Mode 0h = Latch Mode 1h = Retry after tLCK_RETRY
19	RESERVED	R/W	0h	Reserved
18	RESERVED	R/W	0h	Reserved
17	RESERVED	R/W	0h	Reserved
16	DIS_BST_FLT	R/W	0h	Disable BST Fault 0h = Enable BST Fault 1h = Disable BST Fault
15	OTS_AUTO_RECOVERY	R/W	0h	OTS Auto recovery 0h = OTS Latched Fault 1h = OTS Auto Recovery
14-10	RESERVED	R/W	0h	Reserved
9	DIS_SNS_FLT	R/W	0h	Disable Sense Fault 0h = Enable SNS OCP Fault 1h = Disable SNS OCP Fault
8	DIS_VDS_FLT	R/W	0h	Disable VDS Fault 0h = Enable VDS Fault 1h = Disable VDS Fault
7	RESERVED	R/W	0h	Reserved

Table 7-40. GD_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-3	SEL_VDS_LVL	R/W	0h	Select the VDS_OCP Levels 0h = 0.06 V 1h = 0.12 V 2h = 0.18 V 3h = 0.24 V 4h = 0.3 V 5h = 0.36 V 6h = 0.42 V 7h = 0.48 V 8h = 0.6 V 9h = 0.8 V Ah = 1.0 V Bh = 1.2 V Ch = 1.4 V Dh = 1.6 V Eh = 1.8 V Fh = 2.0 V
2	RESERVED	R/W	0h	Reserved
1-0	CSA_GAIN	R/W	0h	Current Sense Amplifier (CSA) Gain 0h = 5 V/V 1h = 10 V/V 2h = 20 V/V 3h = 40 V/V

7.7.3.6 GD_CONFIG2 Register (Offset = AEh) [Reset = 00000000h]

GD_CONFIG2 is shown in Table 7-41.

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Register to configure gated driver settings2

Table 7-41. GD_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-15	RESERVED	R/W	0h	Reserved
14-0	BASE_CURRENT	R/W	0h	Base current (15 bit value) calculated based on gain settings Base Current in Ampere = 1.5/(RSENSE × CSA_GAIN) BASE_CURRENT = Base Current in Ampere × 32768/1200 Example: for 15A, enter 15 × 32768 / 1200

7.7.4 Fault_Configuration Registers

Table 7-42 lists the memory-mapped registers for the Fault_Configuration registers. All register offset addresses not listed in Table 7-42 should be considered as reserved locations and the register contents should not be modified.

Table 7-42. FAULT_CONFIGURATION Registers

Offset	Acronym	Register Name	Section
90h	FAULT_CONFIG1	Fault Configuration1	Section 7.7.4.1
92h	FAULT_CONFIG2	Fault Configuration2	Section 7.7.4.2

Complex bit access types are encoded to fit into small table cells. Table 7-43 shows the codes that are used for access types in this section.

Table 7-43. Fault_Configuration Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value

7.7.4.1 FAULT_CONFIG1 Register (Offset = 90h) [Reset = 00000000h]

FAULT_CONFIG1 is shown in Table 7-44.

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Register to configure fault settings1

Table 7-44. FAULT_CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30-27	ILIMIT	R/W	0h	Phase Current Peak Limit (% of BASE_CURRENT) 0h = 5 % 1h = 10 % 2h = 15 % 3h = 20 % 4h = 25 % 5h = 30 % 6h = 40 % 7h = 50 % 8h = 60 % 9h = 65 % Ah = 70 % Bh = 75 % Ch = 80 % Dh = 85 % Eh = 90 % Fh = 95 %
26-23	HW_LOCK_ILIMIT	R/W	0h	Comparator based lock detection current limit (% of BASE_CURRENT) 0h = 5 % 1h = 10 % 2h = 15 % 3h = 20 % 4h = 25 % 5h = 30 % 6h = 40 % 7h = 50 % 8h = 60 % 9h = 65 % Ah = 70 % Bh = 75 % Ch = 80 % Dh = 85 % Eh = 90 % Fh = 95 %
22-19	LOCK_ILIMIT	R/W	0h	ADC based lock detection current threshold (% of BASE_CURRENT) 0h = 5 % 1h = 10 % 2h = 15 % 3h = 20 % 4h = 25 % 5h = 30 % 6h = 40 % 7h = 50 % 8h = 60 % 9h = 65 % Ah = 70 % Bh = 75 % Ch = 80 % Dh = 85 % Eh = 90 % Fh = 95 %

Table 7-44. FAULT_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	LOCK_ILIMIT_MODE	R/W	0h	Lock current Limit Mode 0h = Ilimit lock detection causes latched fault; nfault active; Gate driver is tristated 1h = Ilimit lock detection causes latched fault; nfault active; Gate driver is tristated 2h = Ilimit lock detection causes latched fault; nfault active; Gate driver is in low side brake mode (All low side FETs are turned ON 3h = Ilimit lock detection causes latched fault; nfault active; Gate driver is in low side brake mode (All low side FETs are turned ON) 4h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFault active 5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFault active 6h = Fault automatically cleared for AUTO_RETRY_TIMES after LCK_RETRY time; Gate driver is in low side brake mode (All low side FETs are turned ON); nFault active 7h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in low side brake mode (All low side FETs are turned ON); nFault active 8h = Ilimit lock detection current limit is in report only but no action is taken; nFault active 9h = ILIMIT LOCK is disabled Ah = ILIMIT LOCK is disabled Bh = ILIMIT LOCK is disabled Ch = ILIMIT LOCK is disabled Dh = ILIMIT LOCK is disabled Eh = ILIMIT LOCK is disabled Fh = ILIMIT LOCK is disabled
14-11	LOCK_ILIMIT_DEG	R/W	0h	Lock detection current limit deglitch time 0h = No deglitch 1h = 0.1 ms 2h = 0.2 ms 3h = 0.5 ms 4h = 1 ms 5h = 2.5 ms 6h = 5 ms 7h = 7.5 ms 8h = 10 ms 9h = 25 ms Ah = 50 ms Bh = 75 ms Ch = 100 ms Dh = 200 ms Eh = 500 ms Fh = 1000 ms

Table 7-44. FAULT_CONFIG1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
10-7	LCK_RETRY	R/W	0h	Lock detection retry time 0h = 300 ms 1h = 500 ms 2h = 1 s 3h = 2 s 4h = 3 s 5h = 4 s 6h = 5 s 7h = 6 s 8h = 7 s 9h = 8 s Ah = 9 s Bh = 10 s Ch = 11 s Dh = 12 s Eh = 13 s Fh = 14 s
6-3	MTR_LCK_MODE	R/W	0h	Motor Lock Mode 0h = Motor lock detection causes latched fault; nfault active; Gate driver is tristated 1h = Motor lock detection causes latched fault; nfault active; Gate driver is tristated 2h = Motor lock detection causes latched fault; nfault active; Gate driver is in low side brake mode (All low side FETs are turned ON) 3h = Motor lock detection causes latched fault; nfault active; Gate driver is in low side brake mode (All low side FETs are turned ON) 4h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFault active 5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated; nFault active 6h = Fault automatically cleared for AUTO_RETRY_TIMES after LCK_RETRY time; Gate driver is in low side brake mode (All low side FETs are turned ON); nFault active 7h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in low side brake mode (All low side FETs are turned ON); nFault active 8h = Motor lock detection current limit is in report only but no action is taken; nFault active 9h = Motor lock detection is disabled Ah = Motor lock detection is disabled Bh = Motor lock detection is disabled Ch = Motor lock detection is disabled Dh = Motor lock detection is disabled Eh = Motor lock detection is disabled Fh = Motor lock detection is disabled
2	IPD_TIMEOUT_FAULT_EN	R/W	0h	IPD timeout fault Enable 0h = Disable 1h = Enable
1	IPD_FREQ_FAULT_EN	R/W	0h	IPD frequency fault Enable 0h = Disable 1h = Enable
0	SATURATION_FLAGS_EN	R/W	0h	Enable indication of current loop and speed loop saturation 0h = Disable 1h = Enable

7.7.4.2 FAULT_CONFIG2 Register (Offset = 92h) [Reset = 00000000h]

FAULT_CONFIG2 is shown in Table 7-45.

Return to the Summary Table.

Register to configure fault settings2

Table 7-45. FAULT_CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	PARITY	R/W	0h	Parity bit
30	LOCK1_EN	R/W	0h	Lock 1 (Abnormal Speed) Enable 0h = Disable 1h = Enable
29	LOCK2_EN	R/W	0h	Lock 2 (Abnormal BEMF) Enable 0h = Disable 1h = Enable
28	LOCK3_EN	R/W	0h	Lock 3 (No Motor) Enable 0h = Disable 1h = Enable
27-25	LOCK_ABN_SPEED	R/W	0h	Abnormal speed lock threshold (% of MAX_SPEED) 0h = 130% 1h = 140% 2h = 150% 3h = 160% 4h = 170% 5h = 180% 6h = 190% 7h = 200%
24-22	ABNORMAL_BEMF_THR	R/W	0h	Abnormal BEMF lock threshold (% of expected BEMF) Expected BEMF = MOTOR_BEMF_CONST × Estimated Speed 0h = 40% 1h = 45% 2h = 50% 3h = 55% 4h = 60% 5h = 65% 6h = 67.5% 7h = 70%
21-19	NO_MTR_THR	R/W	0h	No motor lock threshold (% of BASE_CURRENT) 0h = 1 % 1h = 2 % 2h = 3 % 3h = 4 % 4h = 5 % 5h = 7.5 % 6h = 10 % 7h = 20 %

Table 7-45. FAULT_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
18-15	HW_LOCK_ILIMIT_MODE	R/W	0h	Hardware Lock Detection current mode 0h = Hardware Ilimit lock detection causes latched fault; nfault active; Gate driver is tristated 1h = Hardware Ilimit lock detection causes latched fault; nfault active; Gate driver is tristated 2h = Hardware Ilimit lock detection causes latched fault; nfault active; Gate driver is in low side brake mode (All low side FETs are turned ON) 3h = Hardware Ilimit lock detection causes latched fault; nfault active; Gate driver is in low side brake mode (All low side FETs are turned ON) 4h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated 5h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is tristated 6h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in low side brake mode (All low side FETs are turned ON) 7h = Fault automatically cleared after LCK_RETRY time. Number of retries limited to AUTO_RETRY_TIMES. If number of retries exceed AUTO_RETRY_TIMES, fault is latched; Gate driver is in low side brake mode (All low side FETs are turned ON) 8h = Hardware ILIMIT lock detection is in report only but no action is taken 9h = Hardware ILIMIT lock detection is disabled Ah = Hardware ILIMIT lock detection is disabled Bh = Hardware ILIMIT lock detection is disabled Ch = Hardware ILIMIT lock detection is disabled Dh = Hardware ILIMIT lock detection is disabled Eh = Hardware ILIMIT lock detection is disabled Fh = Hardware ILIMIT lock detection is disabled
14-12	HW_LOCK_ILIMIT_DEG	R/W	0h	Hardware Lock Detection current limit deglitch time 0h = No Deglitch 1h = 1 us 2h = 2 us 3h = 3 us 4h = 4 us 5h = 5 us 6h = 6 us 7h = 7 us
11	VM_UV_OV_HYS	R/W	0h	Hysteresis for DC bus under voltage and over voltage auto recovery 0h = 0.5V for UV and 1V for OV 1h = 1V for UV and 2V for OV
10-8	MIN_VM_MOTOR	R/W	0h	DC Bus Undervoltage for running motor (V) 0h = No Limit 1h = 5.0 V 2h = 6.0 V 3h = 7.0 V 4h = 8.0 V 5h = 10.0 V 6h = 12.0 V 7h = 15.0 V
7	MIN_VM_MODE	R/W	0h	DC Bus Undervoltage Fault Recovery Mode 0h = Latch on Undervoltage 1h = Automatic clear if voltage in bounds

Table 7-45. FAULT_CONFIG2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6-4	MAX_VM_MOTOR	R/W	0h	DC Bus Overvoltage for running motor 0h = No Limit 1h = 10.0 V 2h = 15.0 V 3h = 22.0 V 4h = 32.0 V 5h = 40.0 V 6h = 50.0 V 7h = 60.0 V
3	MAX_VM_MODE	R/W	0h	DC Bus Overvoltage Fault Recovery Mode 0h = Latch on Overvoltage 1h = Automatic clear if voltage in bounds
2-0	AUTO_RETRY_TIMES	R/W	0h	Automatic retry attempts. This is used only if any of the fault mode is configured as "retry" 0h = No Limit 1h = 2 2h = 3 3h = 5 4h = 7 5h = 10 6h = 15 7h = 20

7.8 RAM (Volatile) Register Map

7.8.1 Fault_Status Registers

Table 7-46 lists the memory-mapped registers for the Fault_Status registers. All register offset addresses not listed in Table 7-46 should be considered as reserved locations and the register contents should not be modified.

Table 7-46. FAULT_STATUS Registers

Offset	Acronym	Register Name	Section
E0h	GATE_DRIVER_FAULT_STATUS	Fault Status Register	Section 7.8.1.1
E2h	CONTROLLER_FAULT_STATUS	Fault Status Register	Section 7.8.1.2

Complex bit access types are encoded to fit into small table cells. Table 7-47 shows the codes that are used for access types in this section.

Table 7-47. Fault_Status Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

7.8.1.1 GATE_DRIVER_FAULT_STATUS Register (Offset = E0h) [Reset = 00000000h]

GATE_DRIVER_FAULT_STATUS is shown in Table 7-48.

Return to the Summary Table.

Status of various gate driver faults

Table 7-48. GATE_DRIVER_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	DRIVER_FAULT	R	0h	Logic OR of driver fault registers 0h = No Gate Driver fault condition is detected 1h = Gate Driver fault condition is detected
30	RESERVED	R	0h	Reserved
29	OTS_FAULT	R	0h	Over Temperature Fault 0h = No overtemperature warning / shutdown is detected 1h = Overtemperature warning / shutdown is detected
28	OCP_VDS_FAULT	R	0h	Overcurrent VDS Fault status 0h = No overcurrent condition is detected 1h = Overcurrent condition is detected
27	OCP_SNS_FAULT	R	0h	Overcurrent Sense Fault status 0h = No overcurrent condition is detected 1h = Overcurrent condition is detected
26	BST_UV_FAULT	R	0h	Boot Strap UV protection status 0h = No BST undervoltage condition is detected on VM 1h = BST undervoltage condition is detected on VM
25	GVDD_UV_FLT	R	0h	GVDD UV fault status 0h = No GVDD undervoltage condition is detected on VM 1h = GVDD undervoltage condition is detected on VM
24	DRV_OFF	R	0h	DRV OFF STATUS 0h = DRV is ON 1h = DRVOff state detected
23-0	RESERVED	R	0h	Reserved

7.8.1.2 CONTROLLER_FAULT_STATUS Register (Offset = E2h) [Reset = 00000000h]

CONTROLLER_FAULT_STATUS is shown in Table 7-49.

Return to the Summary Table.

Status of various controller faults

Table 7-49. CONTROLLER_FAULT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31	CONTROLLER_FAULT	R	0h	Logic OR of Controller FAULT status registers
30	RESERVED	R	0h	Reserved
29	IPD_FREQ_FAULT	R	0h	Indicates IPD frequency fault
28	IPD_T1_FAULT	R	0h	Indicates IPD T1 fault
27	RESERVED	R	0h	Reserved
26	BUS_CURRENT_LIMIT_STATUS	R	0h	Indicates status of Bus Current limit
25	RESERVED	R	0h	Reserved
24	MPET_BEMF_FAULT	R	0h	Indicates error during BEMF constant measurement
23	ABN_SPEED	R	0h	Indicates Abnormal speed motor lock condition
22	ABN_BEMF	R	0h	Indicates Abnormal BEMF motor lock condition
21	NO_MTR	R	0h	Indicates No Motor fault
20	MTR_LCK	R	0h	Indicates when one of the motor lock is triggered
19	LOCK_LIMIT	R	0h	Indicates Lock Ilimit fault
18	HW_LOCK_LIMIT	R	0h	Indicates Hardware Lock Ilimit fault
17	DCBUS_UNDER_VOLTAGE	R	0h	Indicates DC bus undervoltage fault
16	DCBUS_OVER_VOLTAGE	R	0h	Indicates DC bus overvoltage fault
15	SPEED_LOOP_SATURATION	R	0h	Indicates speed loop saturation
14	CURRENT_LOOP_SATURATION	R	0h	Indicates current loop saturation
13-4	RESERVED	R	0h	Reserved
3	WATCHDOG_FAULT	R	0h	indicates Watchdog fault
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	RESERVED	R	0h	Reserved

7.8.2 Algorithm_Control Registers

Table 7-50 lists the memory-mapped registers for the Algorithm_Control registers. All register offset addresses not listed in Table 7-50 should be considered as reserved locations and the register contents should not be modified.

Table 7-50. ALGORITHM_CONTROL Registers

Offset	Acronym	Register Name	Section
ECh	ALGO_DEBUG1	Algorithm Control Register	Section 7.8.2.1
EEh	ALGO_DEBUG2	Algorithm Control Register	Section 7.8.2.2
F0h	CURRENT_PI	Current PI Controller used	Section 7.8.2.3
F2h	SPEED_PI	Speed PI controller used	Section 7.8.2.4
F4h	DAC_1	DAC1 Control Register	Section 7.8.2.5

Complex bit access types are encoded to fit into small table cells. Table 7-51 shows the codes that are used for access types in this section.

Table 7-51. Algorithm_Control Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.8.2.1 ALGO_DEBUG1 Register (Offset = ECh) [Reset = 00000000h]

ALGO_DEBUG1 is shown in Table 7-52.

Return to the Summary Table.

Algorithm control register for debug

Table 7-52. ALGO_DEBUG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	SPEED_OVER_RIDE	W	0h	Use to control the SPEED_MODE bits. If SPEED_OVER_RIDE = '1', Duty command can be written by the user through I2C serial interface. 0h = SPEED_MODE using Analog/PWM mode 1h = SPEED_MODE using DIGITAL_SPEED_CTRL
30-16	DIGITAL_SPEED_CTRL	W	0h	Digital Duty Command through I2C If OVERRIDE = 1, then SPEED_MODE is using DIGITAL_SPEED_CTRL
15	CLOSED_LOOP_DIS	W	0h	Use to disable Closed loop 0h = Enable Closed Loop 1h = Disable Closed loop, motor commutation in open loop
14	FORCE_ALIGN_EN	W	0h	Force Align State Enable 0h = Disable Force Align state, device comes out of align state if MTR_STARTUP is selected as ALIGN or DOUBLE ALIGN 1h = Enable Force Align state, device stays in align state if MTR_STARTUP is selected as ALIGN or DOUBLE ALIGN
13	FORCE_SLOW_FIRST_CYCLE_EN	W	0h	Force Slow First Cycle Enable 0h = Disable Force Slow First Cycle state, device comes out of slow first cycle state if MTR_STARTUP is selected as SLOW FIRST CYCLE 1h = Enable Force Slow First Cycle state, device stays in slow first cycle state if MTR_STARTUP is selected as SLOW FIRST CYCLE
12	FORCE_IPD_EN	W	0h	Force IPD Enable 0h = Disable Force IPD state, device comes out of IPD state if MTR_STARTUP is selected as IPD 1h = Enable Force IPD state, device stays in IPD state if MTR_STARTUP is selected as IPD
11	FORCE_ISD_EN	W	0h	Force ISD enable 0h = Disable Force ISD state, device comes out of ISD state if ISD_EN is set 1h = Enable Force ISD state, device stays in ISD state if ISD_EN is set
10	FORCE_ALIGN_ANGLE_SRC_SEL	W	0h	Force Align Angle State Source Select 0h = Force Align Angle defined by ALIGN_ANGLE 1h = Force Align Angle defined by FORCED_ALIGN_ANGLE
9-0	RESERVED	W	0h	Reserved

7.8.2.2 ALGO_DEBUG2 Register (Offset = EEh) [Reset = 00000000h]

ALGO_DEBUG2 is shown in Table 7-53.

Return to the Summary Table.

Algorithm control register for debug

Table 7-53. ALGO_DEBUG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	W	0h	Reserved
30-28	FORCE_RECIRCULATE_STOP_SECTOR	W	0h	use to do the recirculation at specific sector during force motor stop condition 0h = The last sector before stop condition 1h = Sector1 2h = Sector2 3h = Sector3 4h = Sector4 5h = Sector5 6h = Sector6 7h = The last sector before stop condition
27	FORCE_RECIRCULATE_STOP_EN	W	0h	Force recirculate stop Enable 0h = Enable Force recirculate stop 1h = Disable Force recirculate stop
26	CURRENT_LOOP_DIS	W	0h	Use to control the FORCE_VD_CURRENT_LOOP_DIS and FORCE_VQ_CURRENT_LOOP_DIS. If CURRENT_LOOP_DIS = '1', Current loop and speed loop are disabled 0h = Enable Current Loop 1h = Disable Current Loop
25-16	FORCE_VD_CURRENT_LOOP_DIS	W	0h	Sets Vd when current loop and speed loop are disabled If CURRENT_LOOP_DIS = 0b1, then Vd is control using FORCE_VD_CURRENT_LOOP_DIS mdRef = (FORCE_VD_CURRENT_LOOP_DIS /500) if FORCE_VD_CURRENT_LOOP_DIS < 500 (FORCE_VD_CURRENT_LOOP_DIS - 1024)/500 if FORCE_VD_CURRENT_LOOP_DIS > 524 Valid values: 0 to 500 and 524 to 1024
15-6	FORCE_VQ_CURRENT_LOOP_DIS	W	0h	Sets Vq when current loop and speed loop are disabled If CURRENT_LOOP_DIS = 0b1, then Vq is control using FORCE_VQ_CURRENT_LOOP_DIS mqRef = (FORCE_VQ_CURRENT_LOOP_DIS /500) if FORCE_VQ_CURRENT_LOOP_DIS < 500 (FORCE_VQ_CURRENT_LOOP_DIS - 1024)/500 if FORCE_VQ_CURRENT_LOOP_DIS > 524 Valid values: 0 to 500 and 524 to 1024
5	MPET_CMD	W	0h	Initiates motor parameter measurement routine when set to 1
4	RESERVED	W	0h	Reserved
3	RESERVED	W	0h	Reserved
2	MPET_KE	W	0h	Enables motor BEMF constant measurement during motor parameter measurement routine 0h = Disables Motor BEMF constant measurement during motor parameter measurement routine 1h = Enable Motor BEMF constant measurement during motor parameter measurement routine
1	MPET_MECH	W	0h	Enables motor mechanical parameter measurement during motor parameter measurement routine 0h = Disables Motor mechanical parameter measurement during motor parameter measurement routine 1h = Enable Motor mechanical parameter measurement during motor parameter measurement routine
0	MPET_WRITE_SHADOW	W	0h	Write measured parameters to shadow register when set to 1

7.8.2.3 CURRENT_PI Register (Offset = F0h) [Reset = 00000000h]

CURRENT_PI is shown in Table 7-54.

Return to the Summary Table.

Current PI controller used

Table 7-54. CURRENT_PI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	CURRENT_LOOP_KI	R	0h	10 bit for current loop ki Same Scaling as CURR_LOOP_KI
15-0	CURRENT_LOOP_KP	R	0h	10 bit for current loop kp Same Scaling as CURR_LOOP_KP

7.8.2.4 SPEED_PI Register (Offset = F2h) [Reset = 00000000h]

SPEED_PI is shown in Table 7-55.

Return to the Summary Table.

Speed PI controller used

Table 7-55. SPEED_PI Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	SPEED_LOOP_KI	R	0h	10 bit for speed loop ki Same Scaling as SPD_LOOP_KI
15-0	SPEED_LOOP_KP	R	0h	10 bit for speed loop kp Same Scaling as SPD_LOOP_KP

7.8.2.5 DAC_1 Register (Offset = F4h) [Reset = 00000000h]

DAC_1 is shown in Table 7-56.

Return to the Summary Table.

DAC1 Control Register

Table 7-56. DAC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31-21	RESERVED	R	0h	Reserved
20-17	DACOUT1_ENUM_SCALING	W	0h	Multiplication Factor for DACOUT1 Algorithm Variable extracted from the address contained in DACOUT1_VAR_ADDR multiplied with $2^{DACOUT1\_ENUM\_SCALING}$ DACOUT1_ENUM_SCALING comes into effect only if DACOUT1_SCALING is zero
16-13	DACOUT1_SCALING	W	0h	Scaling factor for DACOUT1 Algorithm Variable extracted from the address contained in DACOUT1_VAR_ADDR scaled with DACOUT1_SCALING / 8. Actual voltage depends on DACOUT1_UNIPOLAR If DACOUT1_UNIPOLAR = 1, 0V == 0pu of algorithm Variable * DACOUT1_SCALING / 8, 3V == 1pu of algorithm Variable * DACOUT1_SCALING / 8 If DACOUT1_UNIPOLAR = 0, 0V == -1pu of algorithm Variable * DACOUT1_SCALING / 8, 3V == 1pu of algorithm Variable * DACOUT1_SCALING / 8 0h = Treated s Enum with max value being 31 1h = 1 / 8 2h = 2 / 8 3h = 3 / 8 4h = 4 / 8 5h = 5 / 8 6h = 6 / 8 7h = 7 / 8 8h = 8 / 8 9h = 9 / 8 Ah = 10 / 8 Bh = 11 / 8 Ch = 12 / 8 Dh = 13 / 8 Eh = 14 / 8 Fh = 15 / 8
12	DACOUT1_UNIPOLAR	W	0h	Configures output of DACOUT1 If DACOUT1_UNIPOLAR = 1, 0V == 0pu of algorithm Variable * DACOUT1_SCALING / 16, 3V == 1pu of algorithm Variable * DACOUT1_SCALING / 16 If DACOUT1_UNIPOLAR = 0, 0V == -1pu of algorithm Variable * DACOUT1_SCALING / 16, 3V == 1pu of algorithm Variable * DACOUT1_SCALING / 16 0h = Bipolar (Offset of 1.5 V) 1h = Unipolar (No Offset)
11-0	DACOUT1_VAR_ADDR	R/W	0h	12-bit address of variable to be monitored

7.8.3 System_Status Registers

Table 7-57 lists the memory-mapped registers for the System_Status registers. All register offset addresses not listed in Table 7-57 should be considered as reserved locations and the register contents should not be modified.

Table 7-57. SYSTEM_STATUS Registers

Offset	Acronym	Register Name	Section
E4h	ALGO_STATUS	System Status Register	Section 7.8.3.1
E6h	MTR_PARAMS	System Status Register	Section 7.8.3.2
E8h	ALGO_STATUS_MPET	System Status Register	Section 7.8.3.3

Complex bit access types are encoded to fit into small table cells. Table 7-58 shows the codes that are used for access types in this section.

Table 7-58. System_Status Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

7.8.3.1 ALGO_STATUS Register (Offset = E4h) [Reset = 00000000h]

ALGO_STATUS is shown in Table 7-59.

Return to the Summary Table.

Status of various system and algorithm parameters

Table 7-59. ALGO_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	VOLT_MAG	R	0h	16-bit value indicating applied Modulation index Modulation index applied = VOLT_MAG * 100 / 32768 %
15-4	DUTY_CMD	R	0h	12-bit value indicating decoded Duty command in PWM/Analog mode DUTY_CMD (%) = DUTY_CMD/4096 * 100%.
3	RESERVED	R	0h	Reserved
2	SYS_ENABLE_FLAG	R	0h	1 indicates GUI can control the register 0 indicates GUI is still copying default parameters from shadow memory
1-0	RESERVED	R	0h	Reserved

7.8.3.2 MTR_PARAMS Register (Offset = E6h) [Reset = 00000000h]

MTR_PARAMS is shown in Table 7-60.

Return to the Summary Table.

Status of various motor parameters

Table 7-60. MTR_PARAMS Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	RESERVED	R	0h	Reserved
23-16	MOTOR_BEMF_CONST	R	0h	8-bit value indicating measured BEMF constant
15-8	RESERVED	R	0h	Reserved
7-0	RESERVED	R	0h	Reserved

7.8.3.3 ALGO_STATUS_MPET Register (Offset = E8h) [Reset = 00000000h]

ALGO_STATUS_MPET is shown in Table 7-61.

Return to the Summary Table.

Status of various MPET parameters

Table 7-61. ALGO_STATUS_MPET Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30	RESERVED	R	0h	Reserved
29	MPET_KE_STATUS	R	0h	Indicates status of BEMF constant measurement
28	MPET_MECH_STATUS	R	0h	Indicates status of mechanical parameter measurement
27-24	MPET_PWM_FREQ	R	0h	4-bit value indicating PWM frequency used during BEMF constant measurement
23-0	RESERVED	R	0h	Reserved

7.8.4 Device_Control Registers

Table 7-62 lists the memory-mapped registers for the Device_Control registers. All register offset addresses not listed in Table 7-62 should be considered as reserved locations and the register contents should not be modified.

Table 7-62. DEVICE_CONTROL Registers

Offset	Acronym	Register Name	Section
EAh	ALGO_CTRL1	Device Control Register	Section 7.8.4.1

Complex bit access types are encoded to fit into small table cells. Table 7-63 shows the codes that are used for access types in this section.

Table 7-63. Device_Control Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value

7.8.4.1 ALGO_CTRL1 Register (Offset = EAh) [Reset = 00000000h]

ALGO_CTRL1 is shown in Table 7-64.

Return to the Summary Table.

Control settings

Table 7-64. ALGO_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
31	EEPROM_WRT	R/W	0h	Write the configuration to EEPROM
30	EEPROM_READ	R/W	0h	Read the default configuration from EEPROM
29	CLR_FLT	W	0h	Clears all faults
28	CLR_FLT_RETRY_COUNT	W	0h	Clears fault retry count
27-20	EEPROM_WRITE_ACCESS_KEY	W	0h	EEPROM write access key
19-11	FORCED_ALIGN_ANGLE	W	0h	9-bit value (in degrees) used during forced Align state (FORCE_ALIGN_EN = 1) Angle applied = FORCED_ALIGN_ANGLE % 360deg
10	WATCHDOG_TICKLE	W	0h	RAM bit to tickle watchdog in I2C mode. This bit should be written to 1b by external controller with in every EXT_WD_CONFIG. MCF8329 will reset this bit to 0b.
9-0	FLUX_MODE_REFERENCE	W	0h	Sets ID Ref (% of BASE_CURRENT) when motor is in closed loop operation idRef = (FLUX_MODE_REFERENCE/500) * BASE_CURRENT if FLUX_MODE_REFERENCE < 500 idRef = (FLUX_MODE_REFERENCE - 1024)/500 * BASE_CURRENT if FLUX_MODE_REFERENCE > 524 Valid values are 0 to 500 and 524 to 1024

7.8.5 Algorithm_Variables Registers

Table 7-65 lists the memory-mapped registers for the Algorithm_Variables registers. All register offset addresses not listed in Table 7-65 should be considered as reserved locations and the register contents should not be modified.

Table 7-65. ALGORITHM_VARIABLES Registers

Offset	Acronym	Register Name	Section
196h	ALGORITHM_STATE	Current Algorithm State Register	Section 7.8.5.1
19Ch	FG_SPEED_FDBK	FG Speed Feedback Register	Section 7.8.5.2
40Eh	BUS_CURRENT	Calculated DC Bus Current Register	Section 7.8.5.3
43Ch	PHASE_CURRENT_A	Measured Current on Phase A Register	Section 7.8.5.4
43Eh	PHASE_CURRENT_B	Measured Current on Phase B Register	Section 7.8.5.5
440h	PHASE_CURRENT_C	Measured Current on Phase C Register	Section 7.8.5.6
450h	CSA_GAIN_FEEDBACK	CSA Gain Register	Section 7.8.5.7
458h	VOLTAGE_GAIN_FEEDBACK	Voltage Gain Register	Section 7.8.5.8
45Ch	VM_VOLTAGE	VM Voltage Register	Section 7.8.5.9
460h	PHASE_VOLTAGE_VA	Phase A Voltage Register	Section 7.8.5.10
462h	PHASE_VOLTAGE_VB	Phase B Voltage Register	Section 7.8.5.11
464h	PHASE_VOLTAGE_VC	Phase C Voltage Register	Section 7.8.5.12
4AAh	SIN_COMMUTATION_ANGLE	Sine of Commutation Angle	Section 7.8.5.13
4ACh	COS_COMMUTATION_ANGLE	Cosine of Commutation Angle	Section 7.8.5.14
4CCh	IALPHA	IALPHA Current Register	Section 7.8.5.15
4CEh	IBETA	IBETA Current Register	Section 7.8.5.16
4D0h	VALPHA	VALPHA Voltage Register	Section 7.8.5.17
4D2h	VBETA	VBETA Voltage Register	Section 7.8.5.18
4DCh	ID	Measured d-axis Current Register	Section 7.8.5.19
4DEh	IQ	Measured q-axis Current Register	Section 7.8.5.20
4E0h	VD	VD Voltage Register	Section 7.8.5.21
4E2h	VQ	VQ Voltage Register	Section 7.8.5.22
51Ah	IQ_REF_ROTOR_ALIGN	Align Current Reference	Section 7.8.5.23
532h	SPEED_REF_OPEN_LOOP	Open Loop Speed Register	Section 7.8.5.24
542h	IQ_REF_OPEN_LOOP	Open Loop Current Reference	Section 7.8.5.25
5D0h	SPEED_REF_CLOSED_LOOP	Speed Reference Register	Section 7.8.5.26
60Ah	ID_REF_CLOSED_LOOP	Reference for d-axis Current loop Register	Section 7.8.5.27
60Ch	IQ_REF_CLOSED_LOOP	Reference q-axis for Current loop Register	Section 7.8.5.28
6B0h	ISD_STATE	ISD State Register	Section 7.8.5.29
6BAh	ISD_SPEED	ISD Speed Register	Section 7.8.5.30
6E4h	IPD_STATE	IPD State Register	Section 7.8.5.31
71Ah	IPD_ANGLE	Calculated IPD Angle Register	Section 7.8.5.32
75Ch	ED	Estimated BEMF EQ Register	Section 7.8.5.33
75Eh	EQ	Estimated BEMF ED Register	Section 7.8.5.34
76Eh	SPEED_FDBK	Speed Feedback Register	Section 7.8.5.35
774h	THETA_EST	Estimated rotor Position Register	Section 7.8.5.36

Complex bit access types are encoded to fit into small table cells. Table 7-66 shows the codes that are used for access types in this section.

Table 7-66. Algorithm_Variables Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Reset or Default Value		
-n		Value after reset or the default value

7.8.5.1 ALGORITHM_STATE Register (Offset = 196h) [Reset = 0000h]

ALGORITHM_STATE is shown in Table 7-67.

Return to the Summary Table.

Current Algorithm State Register

Table 7-67. ALGORITHM_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ALGORITHM_STATE	R	0h	16-bit value indicating current state of device 0h = MOTOR_IDLE 1h = MOTOR_ISD 2h = MOTOR_TRISTATE 3h = MOTOR_BRAKE_ON_START 4h = MOTOR_IPD 5h = MOTOR_SLOW_FIRST_CYCLE 6h = MOTOR_ALIGN 7h = MOTOR_OPEN_LOOP 8h = MOTOR_CLOSED_LOOP_UNALIGNED 9h = MOTOR_CLOSED_LOOP_ALIGNED Ah = MOTOR_CLOSED_LOOP_ACTIVE_BRAKING Bh = MOTOR_SOFT_STOP Ch = MOTOR_RECIRCULATE_STOP Dh = MOTOR_BRAKE_ON_STOP Eh = MOTOR_FAULT Fh = MOTOR_MPET_MOTOR_STOP_CHECK 10h = MOTOR_MPET_MOTOR_STOP_WAIT 11h = MOTOR_MPET_MOTOR_BRAKE 12h = MOTOR_MPET_ALGORITHM_PARAMETERS_INIT 13h = MOTOR_MPET_RL_MEASURE 14h = MOTOR_MPET_KE_MEASURE 15h = MOTOR_MPET_STALL_CURRENT_MEASURE 16h = MOTOR_MPET_TORQUE_MODE 17h = MOTOR_MPET_DONE 18h = MOTOR_MPET_FAULT

7.8.5.2 FG_SPEED_FDBK Register (Offset = 19Ch) [Reset = 00000000h]

FG_SPEED_FDBK is shown in Table 7-68.

Return to the Summary Table.

Speed Feedback from FG

Table 7-68. FG_SPEED_FDBK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FG_SPEED_FDBK	R	0h	32-bit unsigned value indicating absolute value of estimated rotor speed Estimated Speed = (FG_SPEED_FDBK / 2^{27})*MAXIMUM_SPEED_HZ

7.8.5.3 BUS_CURRENT Register (Offset = 40Eh) [Reset = 00000000h]

BUS_CURRENT is shown in Table 7-69.

Return to the Summary Table.

Calculated Supply Current Register

Table 7-69. BUS_CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	BUS_CURRENT	R	0h	32-bit signed value indicating bus current. Negative value is represented in two's complement IBus = (BUS_CURRENT / 2^{27}) * Base_Current/($2^{CSA\_GAIN\_FEEDBACK}$)

7.8.5.4 PHASE_CURRENT_A Register (Offset = 43Ch) [Reset = 00000000h]

PHASE_CURRENT_A is shown in Table 7-70.

Return to the Summary Table.

Measured current on Phase A Register

Table 7-70. PHASE_CURRENT_A Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_CURRENT_A	R	0h	32-bit signed value indicating measured current on Phase A. Negative value is represented in two's complement Ia = (PHASE_CURRENT_A / 2^{27}) * Base_Current/ ($2^{CSA\_GAIN\_FEEDBACK}$)

7.8.5.5 PHASE_CURRENT_B Register (Offset = 43Eh) [Reset = 00000000h]

PHASE_CURRENT_B is shown in Table 7-71.

Return to the Summary Table.

Measured current on Phase B Register

Table 7-71. PHASE_CURRENT_B Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_CURRENT_B	R	0h	32-bit signed value indicating measured current on Phase B. Negative value is represented in two's complement IB = (PHASE_CURRENT_B / 2^{27}) * Base_Current/ ($2^{CSA\_GAIN\_FEEDBACK}$)

7.8.5.6 PHASE_CURRENT_C Register (Offset = 440h) [Reset = 00000000h]

PHASE_CURRENT_C is shown in Table 7-72.

Return to the Summary Table.

Measured current on Phase C Register

Table 7-72. PHASE_CURRENT_C Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_CURRENT_C	R	0h	32-bit signed value indicating measured current on Phase C. Negative value is represented in two's complement IC = (PHASE_CURRENT_C / 2^{27}) * Base_Current/ ($2^{CSA\_GAIN\_FEEDBACK}$)

7.8.5.7 CSA_GAIN_FEEDBACK Register (Offset = 450h) [Reset = 0000h]

CSA_GAIN_FEEDBACK is shown in Table 7-73.

Return to the Summary Table.

CSA Gain Register

Table 7-73. CSA_GAIN_FEEDBACK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CSA_GAIN_FEEDBACK	R	0h	16-bit value indicating current sense gain 0h = 40V/V 1h = 20V/V 2h = 10V/V 3h = 5V/V

7.8.5.8 VOLTAGE_GAIN_FEEDBACK Register (Offset = 458h) [Reset = 0000h]

VOLTAGE_GAIN_FEEDBACK is shown in Table 7-74.

Return to the Summary Table.

Voltage Gain Register

Table 7-74. VOLTAGE_GAIN_FEEDBACK Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VOLTAGE_GAIN_FEEDBACK	R	0h	16-bit value indicating voltage gain 0h = 15V 1h = 30V 2h = 60V

7.8.5.9 VM_VOLTAGE Register (Offset = 45Ch) [Reset = 00000000h]

VM_VOLTAGE is shown in Table 7-75.

Return to the Summary Table.

Supply voltage register

Table 7-75. VM_VOLTAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VM_VOLTAGE	R	0h	32-bit value indicating dc bus voltage DC Bus Voltage = VM_VOLTAGE * 60 / 2^{27}

7.8.5.10 PHASE_VOLTAGE_VA Register (Offset = 460h) [Reset = 00000000h]

PHASE_VOLTAGE_VA is shown in Table 7-76.

Return to the Summary Table.

Phase A Voltage Register

Table 7-76. PHASE_VOLTAGE_VA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_VOLTAGE_VA	R	0h	32-bit value indicating Phase Voltage Va during ISD Phase A voltage = PHASE_VOLTAGE_VA * 60 / (sqrt(3) * 2^{27})

7.8.5.11 PHASE_VOLTAGE_VB Register (Offset = 462h) [Reset = 00000000h]

PHASE_VOLTAGE_VB is shown in Table 7-77.

Return to the Summary Table.

Phase B Voltage Register

Table 7-77. PHASE_VOLTAGE_VB Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	PHASE_VOLTAGE_VB	R	0h	32-bit value indicating Phase Voltage Vb during ISD Phase B voltage = PHASE_VOLTAGE_VB * 60 / (sqrt(3) * 2^{27})

7.8.5.12 PHASE_VOLTAGE_VC Register (Offset = 464h) [Reset = 0h]

PHASE_VOLTAGE_VC is shown in Table 7-78.

Return to the Summary Table.

Phase C Voltage Register

Table 7-78. PHASE_VOLTAGE_VC Register Field Descriptions

Bit	Field	Type	Reset	Description
2	PHASE_VOLTAGE_VC	R	0h	32-bit value indicating Phase Voltage Vc during ISD Phase C voltage = PHASE_VOLTAGE_VC * 60 / (sqrt(3) * 2^{27})
1-0	RESERVED	R	0h	

7.8.5.13 SIN_COMMUTATION_ANGLE Register (Offset = 4AAh) [Reset = 00000000h]

SIN_COMMUTATION_ANGLE is shown in Table 7-79.

Return to the Summary Table.

Sine of Commutation Angle

Table 7-79. SIN_COMMUTATION_ANGLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SIN_COMMUTATION_ANGLE	R	0h	32-bit signed value indicating sine of commutation Angle. Negative value is represented in two's complement SinCommutationAngle = (SIN_COMMUTATION_ANGLE / 2^{27})

7.8.5.14 COS_COMMUTATION_ANGLE Register (Offset = 4ACh) [Reset = 00000000h]

COS_COMMUTATION_ANGLE is shown in Table 7-80.

Return to the Summary Table.

Cosine of Commutation Angle

Table 7-80. COS_COMMUTATION_ANGLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	COS_COMMUTATION_ANGLE	R	0h	32-bit signed value indicating cosine of commutation Angle. Negative value is represented in two's complement CosCommutationAngle = (COS_COMMUTATION_ANGLE / 2^{27})

7.8.5.15 IALPHA Register (Offset = 4CCh) [Reset = 00000000h]

IALPHA is shown in Table 7-81.

Return to the Summary Table.

IALPHA Current Register

Table 7-81. IALPHA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IALPHA	R	0h	32-bit signed value indicating calculated IALPHA. Negative value is represented in two's complement IAlpha = (IALPHA / 2^{27}) * Base_Current/($2^{CSA\_GAIN\_FEEDBACK}$)

7.8.5.16 IBETA Register (Offset = 4CEh) [Reset = 00000000h]

IBETA is shown in Table 7-82.

Return to the Summary Table.

IBETA Current Register

Table 7-82. IBETA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IBETA	R	0h	32-bit signed value indicating calculated IBETA. Negative value is represented in two's complement IBeta = (IBETA / 2^{27}) * Base_Current/($2^{CSA\_GAIN\_FEEDBACK}$)

7.8.5.17 VALPHA Register (Offset = 4D0h) [Reset = 00000000h]

VALPHA is shown in Table 7-83.

Return to the Summary Table.

VALPHA Voltage Register

Table 7-83. VALPHA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VALPHA	R	0h	32-bit signed value indicating calculated VALPHA. Negative value is represented in two's complement VAlpha = (VALPHA / 2^{27}) * 60 / sqrt(3)

7.8.5.18 VBETA Register (Offset = 4D2h) [Reset = 00000000h]

VBETA is shown in Table 7-84.

Return to the Summary Table.

VBETA Voltage Register

Table 7-84. VBETA Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VBETA	R	0h	32-bit signed value indicating calculated VBETA. Negative value is represented in two's complement VBeta = (VBETA / 2^{27}) * 60 / sqrt(3)

7.8.5.19 ID Register (Offset = 4DCh) [Reset = 00000000h]

ID is shown in Table 7-85.

Return to the Summary Table.

Measured d-axis Current Register

Table 7-85. ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ID	R	0h	32-bit signed value indicating estimated Id. Negative value is represented in two's complement Id = (ID / 2^{27}) * Base_Current/($2^{CSA\_GAIN\_FEEDBACK}$)

7.8.5.20 IQ Register (Offset = 4DEh) [Reset = 00000000h]

IQ is shown in Table 7-86.

Return to the Summary Table.

Measured q-axis Current Register

Table 7-86. IQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IQ	R	0h	32-bit signed value indicating estimated Iq. Negative value is represented in two's complement Iq = (IQ / 2^{27}) * Base_Current/($2^{CSA\_GAIN\_FEEDBACK}$)

7.8.5.21 VD Register (Offset = 4E0h) [Reset = 00000000h]

VD is shown in Table 7-87.

Return to the Summary Table.

VD Voltage Register

Table 7-87. VD Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VD	R	0h	32-bit signed value indicating applied Vd. Negative value is represented in two's complement Vd = (VD / 2^{27}) * 60 / sqrt(3)

7.8.5.22 VQ Register (Offset = 4E2h) [Reset = 00000000h]

VQ is shown in Table 7-88.

Return to the Summary Table.

VQ Voltage Register

Table 7-88. VQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	VQ	R	0h	32-bit signed value indicating applied Vq. Negative value is represented in two's complement Vq = (VQ / 2^{27}) * 60 / sqrt(3)

7.8.5.23 IQ_REF_ROTOR_ALIGN Register (Offset = 51Ah) [Reset = 00000000h]

IQ_REF_ROTOR_ALIGN is shown in Table 7-89.

Return to the Summary Table.

Align Current Reference

Table 7-89. IQ_REF_ROTOR_ALIGN Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IQ_REF_ROTOR_ALIGN	R	0h	32-bit signed value indicating Align Current Reference. Negative value is represented in two's complement IqRefRotorAlign = (IQ_REF_ROTOR_ALIGN / 2^{27}) * Base_Current/ ($2^{CSA\_GAIN\_FEEDBACK}$)

7.8.5.24 SPEED_REF_OPEN_LOOP Register (Offset = 532h) [Reset = 00000000h]

SPEED_REF_OPEN_LOOP is shown in Table 7-90.

Return to the Summary Table.

Speed at which motor transitions to close loop

Table 7-90. SPEED_REF_OPEN_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPEED_REF_OPEN_LOOP	R	0h	32-bit signed value indicating Open Loop Speed. The value is positive for OUTA-OUTB-OUTC and Negative and represented in two's complement for OUTA-OUTC-OUTB OpenLoopSpeedRef = (SPEED_REF_OPEN_LOOP / 2^{27}) * max_Speed- In Hz

7.8.5.25 IQ_REF_OPEN_LOOP Register (Offset = 542h) [Reset = 00000000h]

IQ_REF_OPEN_LOOP is shown in Table 7-91.

Return to the Summary Table.

Open Loop Current Reference

Table 7-91. IQ_REF_OPEN_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IQ_REF_OPEN_LOOP	R	0h	32-bit signed value indicating Open Loop Current Reference. Negative value is represented in two's complement IqRefOpenLoop = (IQ_REF_OPEN_LOOP / 2^{27}) * Base_Current/ ($2^{CSA\_GAIN\_FEEDBACK}$)

7.8.5.26 SPEED_REF_CLOSED_LOOP Register (Offset = 5D0h) [Reset = 00000000h]

SPEED_REF_CLOSED_LOOP is shown in Table 7-92.

Return to the Summary Table.

Speed Reference Register

Table 7-92. SPEED_REF_CLOSED_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPEED_REF_CLOSED_LOOP	R	0h	32-bit signed value indicating reference for closed loop. Negative and represented in two's complement In Speed Control mode, Speed Reference in closed loop (Hz) = (SPEED_REF_CLOSED_LOOP/ 2^{27}) * MAX_SPEED (Hz) In Power Control mode, Power Reference in closed loop (watts) = (SPEED_REF_CLOSED_LOOP/ 2^{27}) * MAX_POWER (Watts) In Current Control mode, IQ current reference in closed loop (A) = (SPEED_REF_CLOSED_LOOP / 2^{27}) * Base_Current/ ($2^{CSA\_GAIN\_FEEDBACK}$)

7.8.5.27 ID_REF_CLOSED_LOOP Register (Offset = 60Ah) [Reset = 00000000h]

ID_REF_CLOSED_LOOP is shown in Table 7-93.

Return to the Summary Table.

Reference for Current Loop Register

Table 7-93. ID_REF_CLOSED_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ID_REF_CLOSED_LOOP	R	0h	32-bit signed value indicating Id_ref for flux loop. Negative value is represented in two's complement IdRefClosedLoop = (ID_REF_CLOSED_LOOP / 2^{27}) * Base_Current/($2^{CSA\_GAIN\_FEEDBACK}$)

7.8.5.28 IQ_REF_CLOSED_LOOP Register (Offset = 60Ch) [Reset = 00000000h]

IQ_REF_CLOSED_LOOP is shown in Table 7-94.

Return to the Summary Table.

Reference for Current Loop Register

Table 7-94. IQ_REF_CLOSED_LOOP Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IQ_REF_CLOSED_LOOP	R	0h	32-bit signed value indicating Iq_ref for torque loop. Negative value is represented in two's complement IqRefClosedLoop = (IQ_REF_CLOSED_LOOP / 2^{27}) * Base_Current/($2^{CSA\_GAIN\_FEEDBACK}$)

7.8.5.29 ISD_STATE Register (Offset = 6B0h) [Reset = 0000h]

ISD_STATE is shown in Table 7-95.

Return to the Summary Table.

ISD state Register

Table 7-95. ISD_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ISD_STATE	R	0h	16-bit value indicating current ISD state 0h = ISD_INIT 1h = ISD_MOTOR_STOP_CHECK 2h = ISD_ESTIM_INIT 3h = ISD_RUN_MOTOR_CHECK 4h = ISD_MOTOR_DIRECTION_CHECK 5h = ISD_COMPLETE 6h = ISD_FAULT

7.8.5.30 ISD_SPEED Register (Offset = 6BAh) [Reset = 00000000h]

ISD_SPEED is shown in Table 7-96.

Return to the Summary Table.

ISD Speed Register

Table 7-96. ISD_SPEED Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ISD_SPEED	R	0h	32-bit value indicating calculated absolute speed during ISD state Isd speed = (ISD_SPEED / 2^{27}) * max_Speed- In Hz

7.8.5.31 IPD_STATE Register (Offset = 6E4h) [Reset = 0000h]

IPD_STATE is shown in Table 7-97.

Return to the Summary Table.

IPD state Register

Table 7-97. IPD_STATE Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	IPD_STATE	R	0h	16-bit value indicating current IPD state 0h = IPD_INIT 1h = IPD_VECTOR_CONFIG 2h = IPD_RUN 3h = IPD_SLOW_RISE_CLOCK 4h = IPD_SLOW_FALL_CLOCK 5h = IPD_WAIT_CURRENT_DECAY 6h = IPD_GET_TIMES 7h = IPD_SET_NEXT_VECTOR 8h = IPD_CALC_SECTOR_RISE 9h = IPD_CALC_ROTOR_POSITION Ah = IPD_CALC_ANGLE Bh = IPD_COMPLETE Ch = IPD_FAULT

7.8.5.32 IPD_ANGLE Register (Offset = 71Ah) [Reset = 00000000h]

IPD_ANGLE is shown in Table 7-98.

Return to the Summary Table.

Calculated IPD Angle Register

Table 7-98. IPD_ANGLE Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	IPD_ANGLE	R	0h	32-bit value indicating measured IPD angle IpdAngle = (IPD_ANGLE / 2^{27}) * 360 (Degree)

7.8.5.33 ED Register (Offset = 75Ch) [Reset = 00000000h]

ED is shown in Table 7-99.

Return to the Summary Table.

Estimated BEMF EQ Register

Table 7-99. ED Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	ED	R	0h	32-bit signed value indicating estimated ED. Negative value is represented in two's complement Ed = (ED / 2^{27}) * 60 / sqrt(3)

7.8.5.34 EQ Register (Offset = 75Eh) [Reset = 00000000h]

EQ is shown in Table 7-100.

Return to the Summary Table.

Estimated BEMF ED Register

Table 7-100. EQ Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	EQ	R	0h	32-bit signed value indicating estimated EQ. Negative value is represented in two's complement Eq = (EQ / 2^{27}) * 60 / sqrt(3)

7.8.5.35 SPEED_FDBK Register (Offset = 76Eh) [Reset = 00000000h]

SPEED_FDBK is shown in Table 7-101.

Return to the Summary Table.

Speed Feedback Register

Table 7-101. SPEED_FDBK Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	SPEED_FDBK	R	0h	32-bit signed value indicating estimated rotor speed. The value is positive for OUTA-OUTB-OUTC and Negative and represented in two's complement for OUTA-OUTC-OUTB Estimated speed = (SPEED_FDBK / 2^{27})*MAXIMUM_SPEED_HZ

7.8.5.36 THETA_EST Register (Offset = 774h) [Reset = 00000000h]

THETA_EST is shown in Table 7-102.

Return to the Summary Table.

Estimated rotor Position Register

Table 7-102. THETA_EST Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	THETA_EST	R	0h	32-bit signed value indicating estimated rotor angle. Negative value is represented in two's complement Estimated angle = (THETA_EST / 2^{27})*360 (Degree)

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The MCF8329A is used in 3-phase sensorless trapezoidal motor control applications such as Cordless vacuum cleaners, HVAC blowers and ventilators, Appliance fans, pumps and Medical CPAP blowers.

8.2 Typical Applications

Figure 8-1 shows the typical schematic of MCF8329A. Table 7-1 shows the recommended values of the external components for the driver.

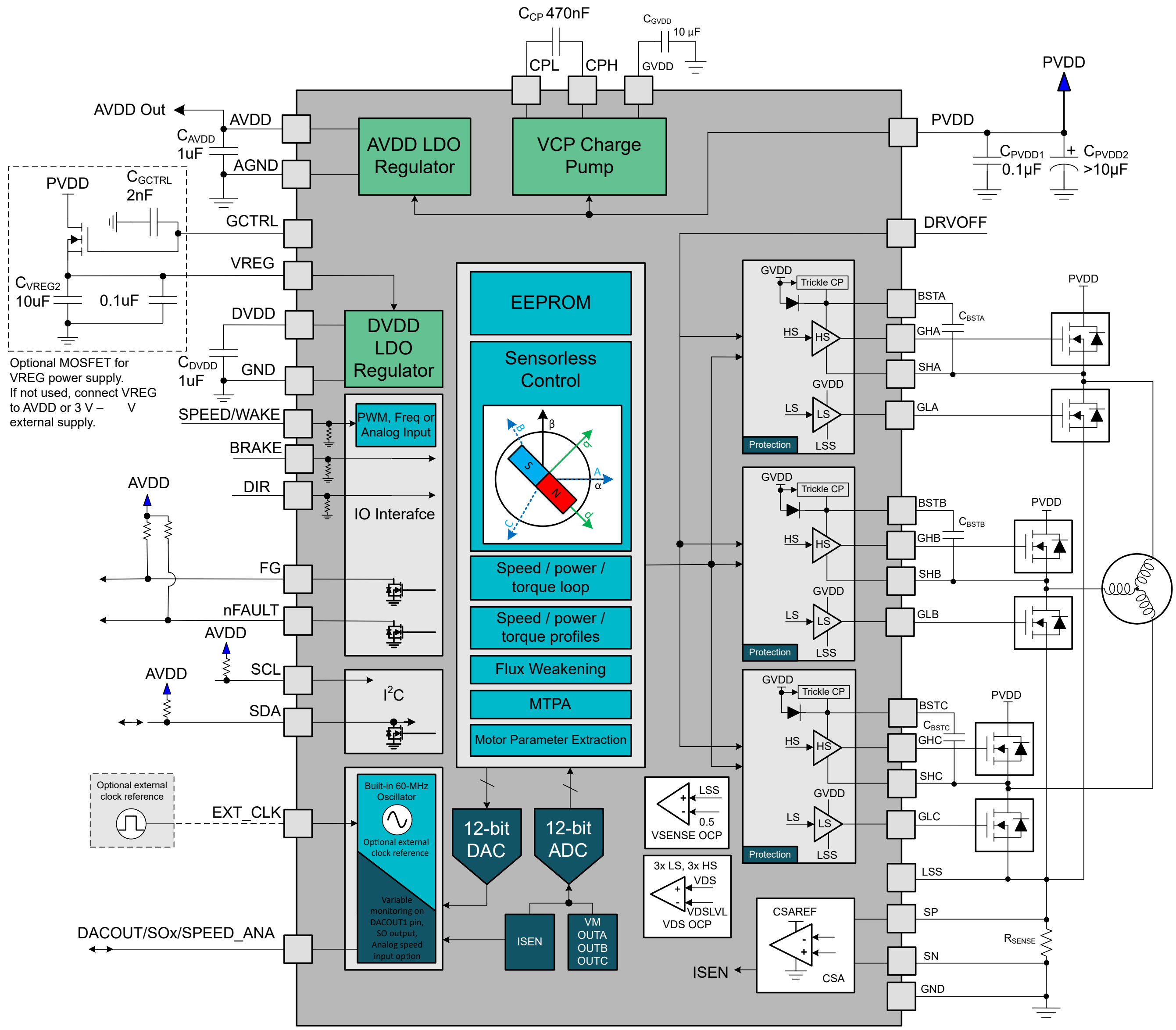


Figure 8-1. Typical Schematic of MCF8329A

Default EEPROM configuration for MCF8329A is listed in Table 8-1. Default values are chosen for reliable motor start-up and closed loop operation.

Table 8-1. Recommended Default Values

Address Name	Address	Recommended Value
ISD_CONFIG	0x00000080	0x64A2D4A1
REV_DRIVE_CONFIG	0x00000082	0x48300000
MOTOR_STARTUP1	0x00000084	0x10A64CC0
MOTOR_STARTUP2	0x00000086	0x2D81C007
CLOSED_LOOP1	0x00000088	0x1D7181B8
CLOSED_LOOP2	0x0000008A	0x0AAD0000
CLOSED_LOOP3	0x0000008C	0x00000000
CLOSED_LOOP4	0x0000008E	0x000004B0
REF_PROFILES1	0x00000094	0x00000000

Table 8-1. Recommended Default Values (continued)

Address Name	Address	Recommended Value
REF_PROFILES2	0x00000096	0x00000000
REF_PROFILES3	0x00000098	0x00000004
REF_PROFILES4	0x0000009A	0x00000000
REF_PROFILES5	0x0000009C	0x00000000
REF_PROFILES6	0x0000009E	0x00000000
FAULT_CONFIG1	0x00000090	0x465A31A6
FAULT_CONFIG2	0x00000092	0x71422888
PIN_CONFIG	0x000000A4	0x40032309
DEVICE_CONFIG1	0x000000A6	0x00100002
DEVICE_CONFIG2	0x000000A8	0x03E8C00C
PERI_CONFIG1	0x000000AA	0x69845CC0
GD_CONFIG1	0x000000AC	0x0000807B
GD_CONFIG2	0x000000AE	0x00000400
INT_ALGO_1	0x000000A0	0x0946027D
INT_ALGO_2	0x000000A2	0x020082E3

Detailed Design Procedure

Table below lists the example input parameters for the system design.

Table 8-2. Design parameters

DESIGN PARAMETERS	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{PVDD}	24 V
Motor peak current	I_{PEAK}	20 A
PWM Frequency	f_{PWM}	20 kHz
MOSFET VDS Slew Rate	SR	120 V/us
MOSFET input gate capacitance	Q_G	54 nC
MOSFET input gate capacitance	Q_{GD}	14 nC
Dead time	t_{dead}	200 ns
Overcurrent protection	I_{OCP}	30 A

Bootstrap Capacitor and GVDD Capacitor Selection

The bootstrap capacitor must be sized to maintain the bootstrap voltage above the undervoltage lockout for normal operation. Equation 13 calculates the maximum allowable voltage drop across the bootstrap capacitor:

$$\Delta V_{BSTX} = V_{GVDD} - V_{BOOTD} - V_{BSTUV} \tag{13}$$

ΔV_{BSTX}=12 V – 0.85 V – 4.45 V = 6.7 V

where

- V_{GVDD} is the supply voltage of the gate drive
- V_{BOOTD} is the forward voltage drop of the bootstrap diode
- V_{BSTUV} is the threshold of the bootstrap undervoltage lockout

In the example, allowed voltage drop across bootstrap capacitor is 6.7 V. It is generally recommended that ripple voltage on both the bootstrap capacitor and GVDD capacitor should be minimized as much as possible. Many of commercial, industrial, and automotive applications use ripple value between 0.5 V to 1 V.

The total charge needed per switching cycle can be estimated with Equation 14:

$$Q_{TOT} = Q_G + \frac{IL_{BS\_TRAN}}{f_{SW}} \quad (14)$$

Q_{TOT}=54 nC + 115 µA/20 kHz = 54 nC + 5.8 nC = 59.8nC

where

- Q_G is the total MOSFET gate charge
- IL_{BS_TRAN} is the bootstrap pin leakage current
- f_{SW} is the is the PWM frequency

The minimum bootstrap capacitor can then be estimated as below assuming 1V of ΔV_{BSTx}:

$$C_{BST\_MIN} = {}^{Q_{TOT}}/_{\Delta V_{BSTX}} \quad (15)$$

C_{BST_MIN}= 59.8 nC / 1 V = 59.8 nF

The calculated value of minimum bootstrap capacitor is 59.8 nF. It should be noted that, this value of capacitance is needed at full bias voltage. In practice, the value of the bootstrap capacitor must be greater than calculated value to allow for situations where the power stage may skip pulse due to various transient conditions. It is recommended to use a 100 nF bootstrap capacitor in this example. It is also recommenced to include enough margin and place the bootstrap capacitor as close to the BSTx and SHx pins as possible.

$$C_{GVDD} \geq 10 \times C_{BSTX} \quad (16)$$

C_{GVDD}= 10*100 nF= 1 µF

For this example application, choose a 1-µF C_{GVDD} capacitor. Choose a capacitor with a voltage rating at least twice the maximum voltage that it will be exposed to because most ceramic capacitors lose significant capacitance when biased. This value also improves the long-term reliability of the system.

Note

For higher power system requiring 100% duty cycle support for longer duration it is recommended to use C_{BSTx} of ≥1µF and C_{GVDD} of ≥10 µF.

8.2.1 Selection of External MOSFET for VREG Power Supply

The MCF8329A device provides option to drive external MOSFET (using GCTRL pin) which can act as regulator to power internal digital circuitry through VREG pin, as explained in Section 7.3.4.3. Select the external MOSFET to make sure that the VREG pin voltage is between 2.2 V to 5.5 V across operating conditions. As an example calculation, use Equation 17 for the MOSFET selection to get a minimum VREG pin voltage of 2.4 V at a minimum GCTRL pin voltage of 4.9V ($V_{GCTRL(min)}$ - $V_{VREG(min)}$ = 2.5 V). Use Equation 18 to design for the maximum voltage at VREG pin is less than 5.5 V at maximum GCTRL pin voltage.

$$V_{GS(th)\_max} + V_{PVDD}\left(\frac{C_{GD}}{C_{GD} + C_{GCTRL}}\right) + \left(1.3 \times I_{GATE\_LEAK} \times 10^6\right) < 2.5\,V \quad (17)$$

$$V_{GCTRL(\max)} - V_{GS(th)\_min} < 5.5\,V \quad (18)$$

where,

$V_{GS(th)\_max}$ is the maximum gate to source threshold voltage of the external MOSFET across operating condition

$V_{GS(th)\_min}$ is the minimum gate to source threshold voltage of the external MOSFET across operating condition

V_{PVDD} is the voltage at the drain of the external MOSFET

C_{GD} is the gate to drain capacitance of the external MOSFET

C_{GCTRL} is the capacitance connected between GCTRL pin and GND

I_{GATE_LEAK} is the maximum gate leakage of the external MOSFET

$V_{GCTRL(max)}$ is the maximum voltage at GCTRL pin

The external MOSFET has to be selected so that the GCTRL pin voltage does not peak more than 0.5V from operating maximum value of GCTRL pin voltage and use Equation 19 for the MOSFET selection.

$$V_{PVDD}\left(\frac{C_{GD}}{C_{GD}+C_{GCTRL}}\right) + \left(1.3 \times I_{GATE\_LEAK} \times 10^{6}\right) < 0.5\,V \quad (19)$$

Table 8-3. Example External MOSFET

Part Number	V_{DS}(V)	Max $V_{GS(TH)}$ (V)	C_{ISS} (pF)	GCTRL-GND Cap (nF)	GCTRL Start up time (ms)
CSD18534Q5A	60	2.3	1770	2	20

Gate Drive Current

Selecting an appropriate gate drive current is essential when turning on or off power MOSFETs gates to switch motor current. The amount of gate drive current and input capacitance of the MOSFETs determines the drain-to-source voltage slew rate (V_{DS}). Gate drive current can be sourced from GVDD into the MOSFET gate (I_{SOURCE}) or sunk from the MOSFET gate into SHx or LSS (I_{SINK}).

Using too high of a gate drive current can turn on MOSFETs too quickly which may cause excessive ringing, dV/dt coupling, or cross-conduction from switching large amounts of current. If parasitic inductances and capacitances exist in the system, voltage spiking or ringing may occur which can damage the MOSFETs or MCF8329A device.

On the other hand, using too low of a gate drive current causes long V_{DS} slew rates. Turning on the MOSFETs too slowly may heat up the MOSFETs due to $R_{DS,on}$ switching losses.

The relationship between gate drive current I_{GATE}, MOSFET gate-to-drain charge Q_{GD}, and V_{DS} slew rate switching time $t_{rise,fall}$ are described by the following equations:

$$SR_{DS} = \frac{V_{DS}}{t_{rise,fall}} \quad (20)$$

$$I_{GATE} = \frac{Q_{gd}}{t_{rise,fall}} \quad (21)$$

It is recommend to evaluate at lower gate drive currents and increase gate drive current settings to avoid damage from unintended operation during initial evaluation.

Gate Resistor Selection

The slew rate of the SHx connection will be dependent on the rate at which the gate of the external MOSFETs is controlled. The pull-up/pull-down strength of MCF8329A is fixed internally, hence the slew rate of gate voltage can be controlled with an external series gate resistor. In some applications, the gate charge of the MOSFET, which is the load on gate driver device, is significantly larger than the gate driver peak output current capability. In such applications, external gate resistors can limit the peak output current of the gate driver. External gate resistors are also used to dampen ringing and noise.

The specific parameters of the MOSFET, system voltage, and board parasitics will all affect the final SHx slew rate, so generally selecting an optimal value or configuration of external gate resistor is an iterative process.

To lower the gate drive current, a series resistor R_{GATE} can be placed on the gate drive outputs to control the current for the source and sink current paths. A single gate resistor will have the same gate path for source and sink gate current, so larger R_{GATE} values will yield similar SHx slew rates. Note that gate drive current varies by PVDD voltage, junction temperature, and process variation of the device.

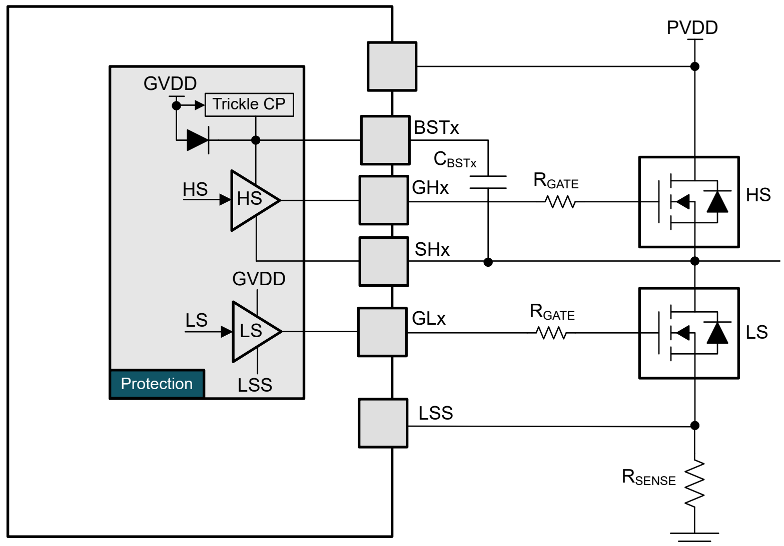


Figure 8-2. Gate driver outputs with series resistors

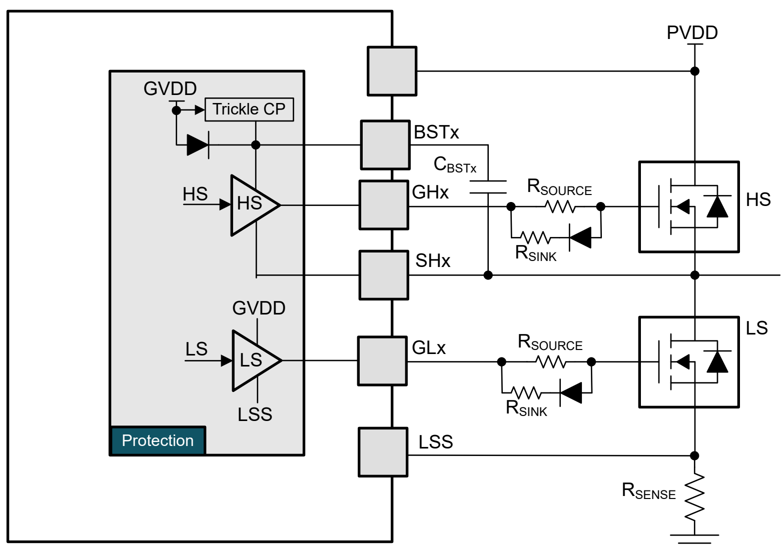


Figure 8-3. Gate driver outputs with separate source and sink current paths

Typically, it is recommended to have the sink current be twice the source current to implement a strong pull-down from gate to the source to ensure the MOSFET stays off while the opposite FET is switching. This can be implemented discretely by providing a separate path through a resistor for the source and sink currents by placing a diode and sink resistor (R_{SINK}) in parallel to the source resistor (R_{SOURCE}). Using the same value of source and sink resistors results in half the equivalent resistance for the sink path. This yields twice the gate drive sink current compared to the source current, and SHx will slew twice as fast when turning off the MOSFET.

System Considerations in High Power Designs

Higher power system designs can require design and application considerations by implementing troubleshooting guidelines, external components and circuits, driver product features, or layout techniques. For more information, visit the System Design Considerations for High-Power Motor Driver Applications application note.

Capacitor Voltage Ratings

Use capacitors with voltage ratings that are 2x the supply voltage (PVDD, GVDD, AVDD, etc). Capacitors can experience up to half the rated capacitance due to poor DC voltage rating performance.

For example, since the bootstrap voltage is around 12 to 13-V with respect to SHx (BSTx-SHx) then the BSTx-SHx capacitor should be rated for 25-V or greater.

External Power Stage Components

External components in the power stage are not required by design but are helpful in suppressing transients, managing inductor coil energy, mitigating supply pumping, dampening phase ringing, or providing strong gate-to-source pulldown paths. These components are used for system tuning and debuggability so the BLDC motor system is robust while avoiding damage to the MCF8329A device or external MOSFETs.

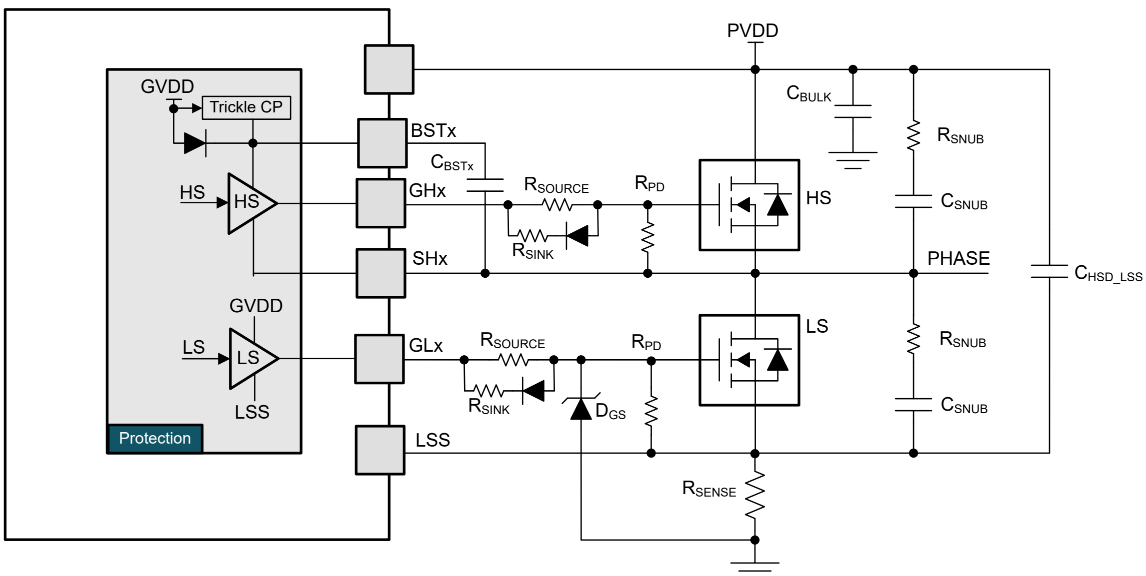


Figure 8-4. Optional external power stage components

Some examples of issues and external components that can resolve those issues are found in table below.

Table 8-4. Common issues and resolutions for power stage debugging

Issue	Resolution	Components
Gate drive current required is too large, resulting in very fast MOSFET V_{DS} slew rate	Series resistors required for gate drive current adjustability	0-100 Ω series resistors (RGATE/RSOURCE) at gate driver outputs (GHx/GLx), optional sink resistor (RSINK) and diode in parallel with gate resistor for adjustable sink current
Ringing at phase's switch node (SHx) resulting in high EMI emissions	RC snubbers placed in parallel to each HS/LS MOSFET to dampen oscillations	Resistor (RSNUB) and Capacitor (CSNUB) placed parallel to the MOSFET, calculate RC values based on ringing frequency using Proper RC Snubber Design for Motor Drivers
Negative transients at low-side source (LSS) below minimum specification	HS drain to LS source capacitor to suppress negative bouncing	0.01uF-1uF, PVDD-rated capacitor from PVDD-LSS (CHSD_LSS) placed near LS MOSFET's source

Table 8-4. Common issues and resolutions for power stage debugging (continued)

Issue	Resolution	Components
Negative transient at low-side gate (GLx) below minimum specification	Gate-to-ground Zener diode to clamp negative voltage	GVDD voltage rated Zener diode (DGS) with anode connected to GND and cathode connected to GLx
Extra protection required to ensure MOSFET is turned off if gate drive signals are Hi-Z	External gate-to-source pulldown resistors (after series gate resistors)	10 kΩ to 100 kΩ resistor (RPD) connected from gate to source for each MOSFET

8.2.2 Application curves

8.2.2.1 Motor startup

Figure 8-5 shows the FG waveform and the phase current waveform at different motor operations.

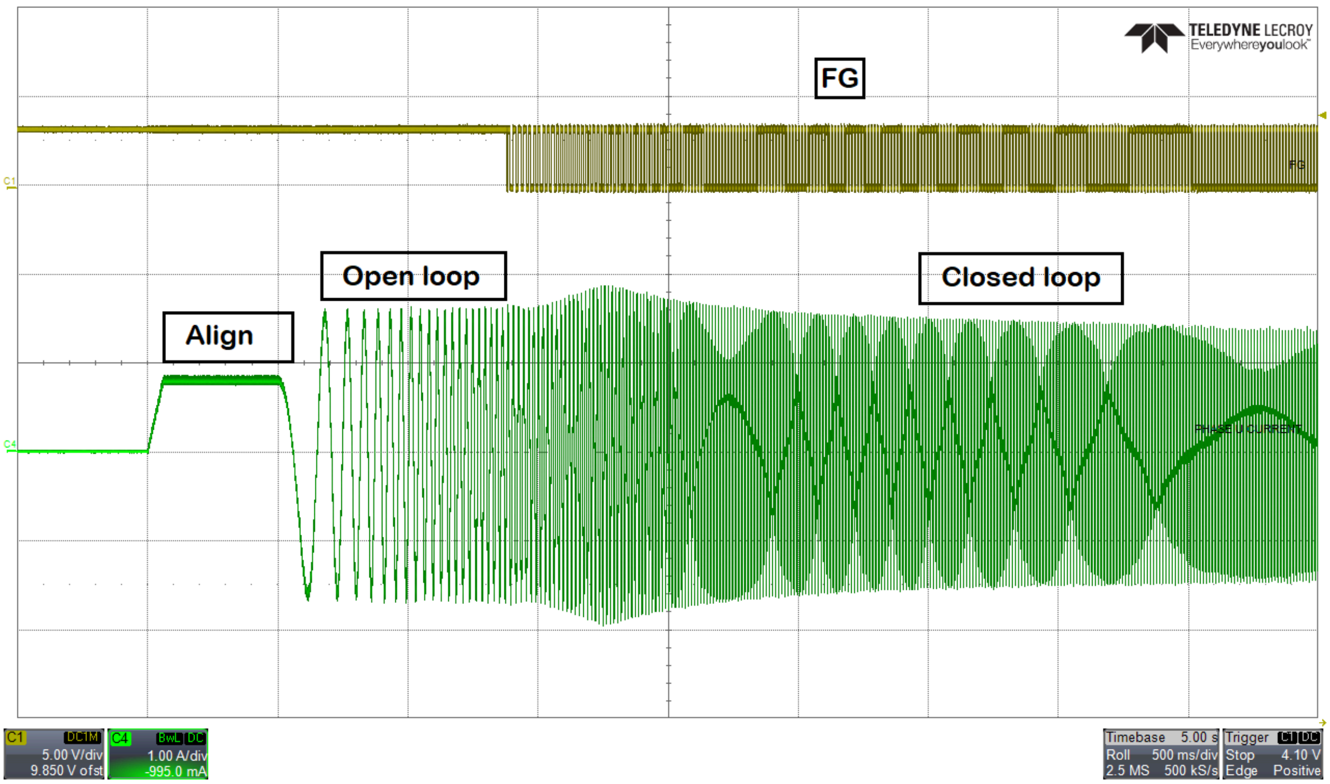


Figure 8-5. Motor Startup - FG and Phase current

High speed (1.8 kHz) operation

Figure 8-6 shows the phase current waveform and FG signal for a high speed motor at 1.8 kHz speed (2-pole, 108 kRPM).

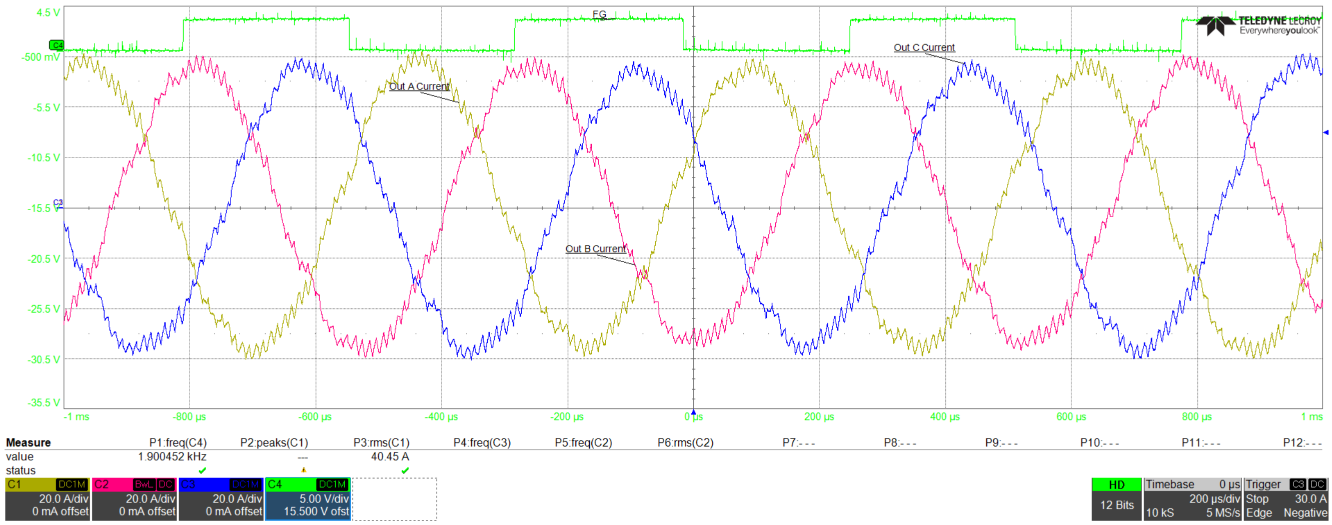


Figure 8-6. Phase currents at 1.8 kHz motor speed

Active Braking for faster deceleration

When motor speed decelerates at a very high deceleration rate, mechanical energy from the motor returns to the power supply which can result in pumping up the DC supply voltage. The active braking feature helps to achieve faster deceleration without energy going back to DC bus. Figure 8-7 shows overshoot in power supply voltage when active braking is disabled and motor decelerates from 100% speed to 20% speed at a deceleration rate of 500 Hz/sec. Figure 8-8 shows no overshoot in power supply voltage when active braking is enabled.

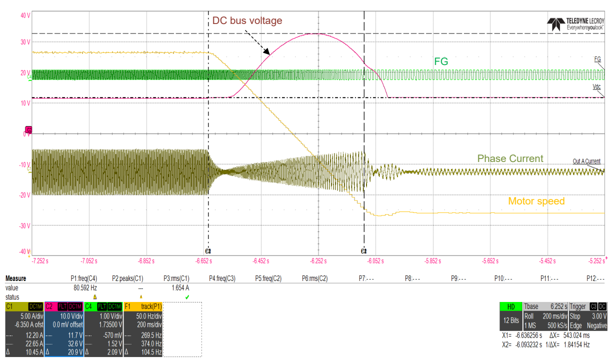


Figure 8-7. DC bus spike with active braking disabled and AVS disabled

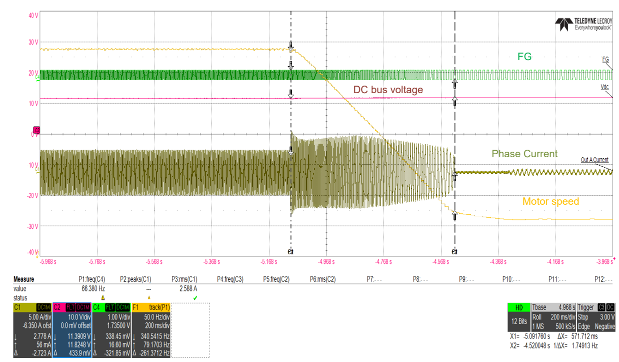


Figure 8-8. DC bus voltage with active braking enabled and AVS disabled

8.2.2.2 Dead Time compensation

Figure 8-9 shows the phase current waveform when dead time compensation is disabled. Fundamental frequency of phase current is 40 Hz. Fast Fourier transform (FFT) of phase current plot shows harmonics at 160 Hz and 220 Hz. Figure 8-10 shows the phase current waveform when dead time compensation is enabled. Phase current looks more sinusoidal and the FFT of phase current plot does not have any harmonics.

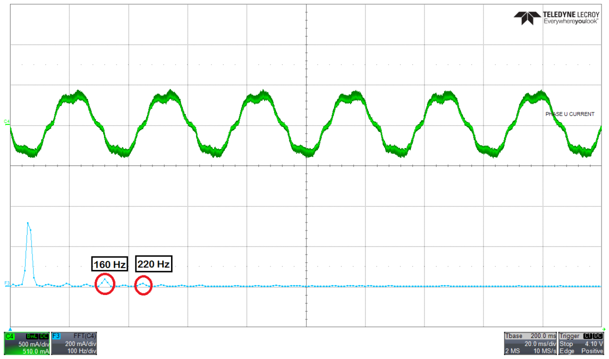


Figure 8-9. Phase current and FFT - Dead time compensation disabled

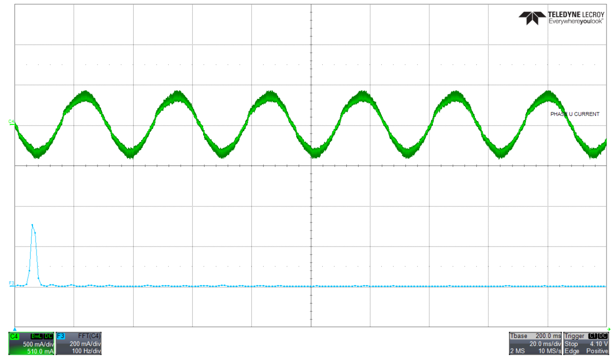


Figure 8-10. Phase current and FFT - Dead time compensation enabled

9 Power Supply Recommendations

The MCF8329A is designed to operate from an input voltage supply (PVDD) range from 4.5 V to 60 V. A 10-μF and 0.1-μF ceramic capacitor rated for PVDD must be placed as close to the device as possible. In addition, a bulk capacitor must be included on the PVDD pin but can be shared with the bulk bypass capacitance for the external power MOSFETs. Additional bulk capacitance is required to bypass the external half-bridge MOSFETs and should be sized according to the application requirements.

9.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed DC, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate at which current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in PVDD voltage. When adequate bulk capacitance is used, the PVDD voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate bulk capacitor. The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

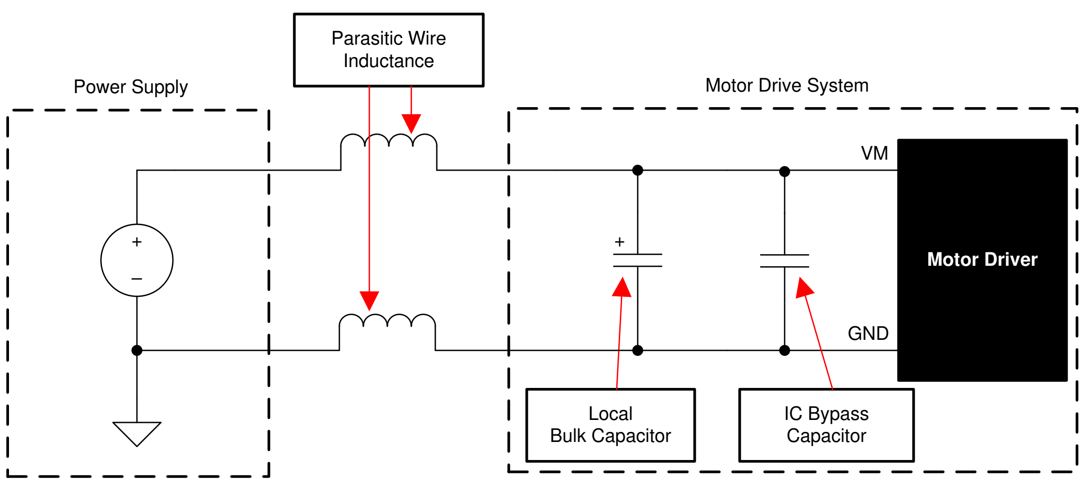


Figure 9-1. Example Setup of Motor Drive System With External Power Supply

10 Layout

10.1 Layout Guidelines

Bypass the PVDD pin to the GND (PGND) pin using a low-ESR ceramic bypass capacitor with a recommended value of 0.1 µF. Place this capacitor as close to the PVDD pin as possible with a thick trace or ground plane connected to the PGND pin. Additionally, bypass the PVDD pin using a bulk capacitor rated for PVDD. This component can be electrolytic. This capacitance must be at least 10 µF.

Additional bulk capacitance is required to bypass the high current path on the external MOSFETs. This bulk capacitance should be placed such that it minimizes the length of any high current paths through the external MOSFETs. The connecting metal traces should be as wide as possible, with numerous vias connecting PCB layers. These practices minimize inductance and let the bulk capacitor deliver high current.

Place a low-ESR ceramic capacitor between the CPL and CPH pins. This capacitor should be 470 nF, rated for PVDD, and be of type X5R or X7R.

The bootstrap capacitors (BSTx-SHx) should be placed closely to device pins to minimize loop inductance for the gate drive paths.

Bypass the AVDD pin to the AGND pin with a 1-µF low-ESR ceramic capacitor rated for 6.3 V and of type X5R or X7R. Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the AGND pin.

Bypass the DVDD pin to the GND pin with a 1-µF low-ESR ceramic capacitor rated for ≥ 4 V and of type X5R or X7R. Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the GND pin.

Bypass the VREG pin with an adequate low-ESR ceramic capacitor rated of type X5R or X7R.

Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the GHx pin of the device to the high-side power MOSFET gate, then follows the high-side MOSFET source back to the SHx pin. The low-side loop is from the GLx pin of the device to the low-side power MOSFET gate, then follows the low-side MOSFET source back to the PGND pin.

When designing higher power systems, physics in the PCB layout can cause parasitic inductance, capacitance, and impedance that deter the performance of the system. Understanding the parasitic that are present in a higher power motor drive system can help designers mitigate their effects through good PCB layout. For more information, visit the System Design Considerations for High-Power Motor Driver Applications and Best Practices for Board Layout of Motor Drivers application notes.

Gate drive traces (BSTx, GHx, SHx, GLx, LSS) should be at least 15-20mil wide and as short as possible to the MOSFET gates to minimize parasitic inductance and impedance. This helps supply large gate drive currents, turn MOSFETs on efficiently, and improves VGS and VDS monitoring. Ensure that the shunt resistor selected to monitor the low-side current from LSS to GND, is wide to minimize inductance introduced at the low-side source LSS.

Ensure grounds are connected through net-ties or wide resistors to reduce voltage offsets and maintain gate driver performance. The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the heat that is generated in the device. To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

10.2 Layout Example

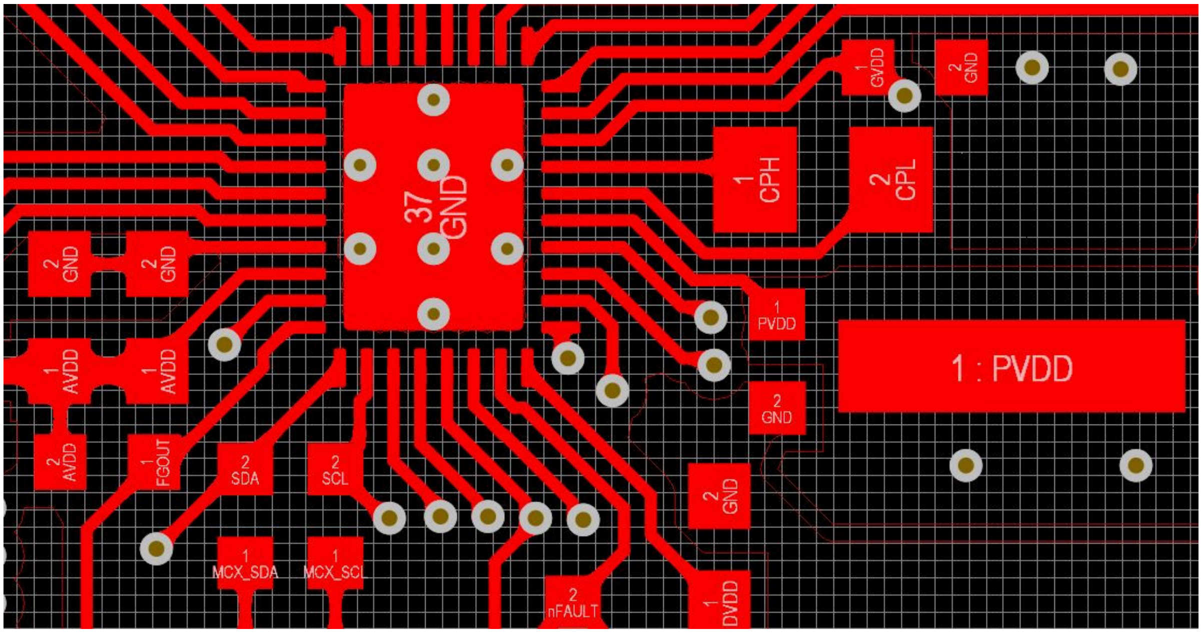


Figure 10-1. Layout example of MCF8329A device

10.3 Thermal Considerations

The MCF8329A has thermal shutdown (TSD) as previously described. A die temperature in excess of 150°C (minimally) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heat-sinking, or too high an ambient temperature.

10.3.1 Power Dissipation

The MCF8329A integrates a variety of circuits that contribute to total power losses. These power losses include standby power losses, GVDD power losses, AVDD power losses, DVDD power losses. At start-up and fault conditions, this current is much higher than normal running current; remember to take these peak currents and their duration into consideration. The maximum amount of power that the device can dissipate depends on ambient temperature and heat-sinking.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

- Refer to the application note Power Delivery in Cordless Power Tools Using DRV8329
- Refer to the application note System Design Considerations for High-Power Motor Driver Applications
- Refer to the E2E FAQ How to Conduct a BLDC Schematic Review and Debug
- Refer to the application note Best Practices for Board Layout of Motor Drivers
- Refer to the application note QFN and SON PCB Attachment
- Refer to the application note Cut-Off Switch in High-Current Motor-Drive Applications

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

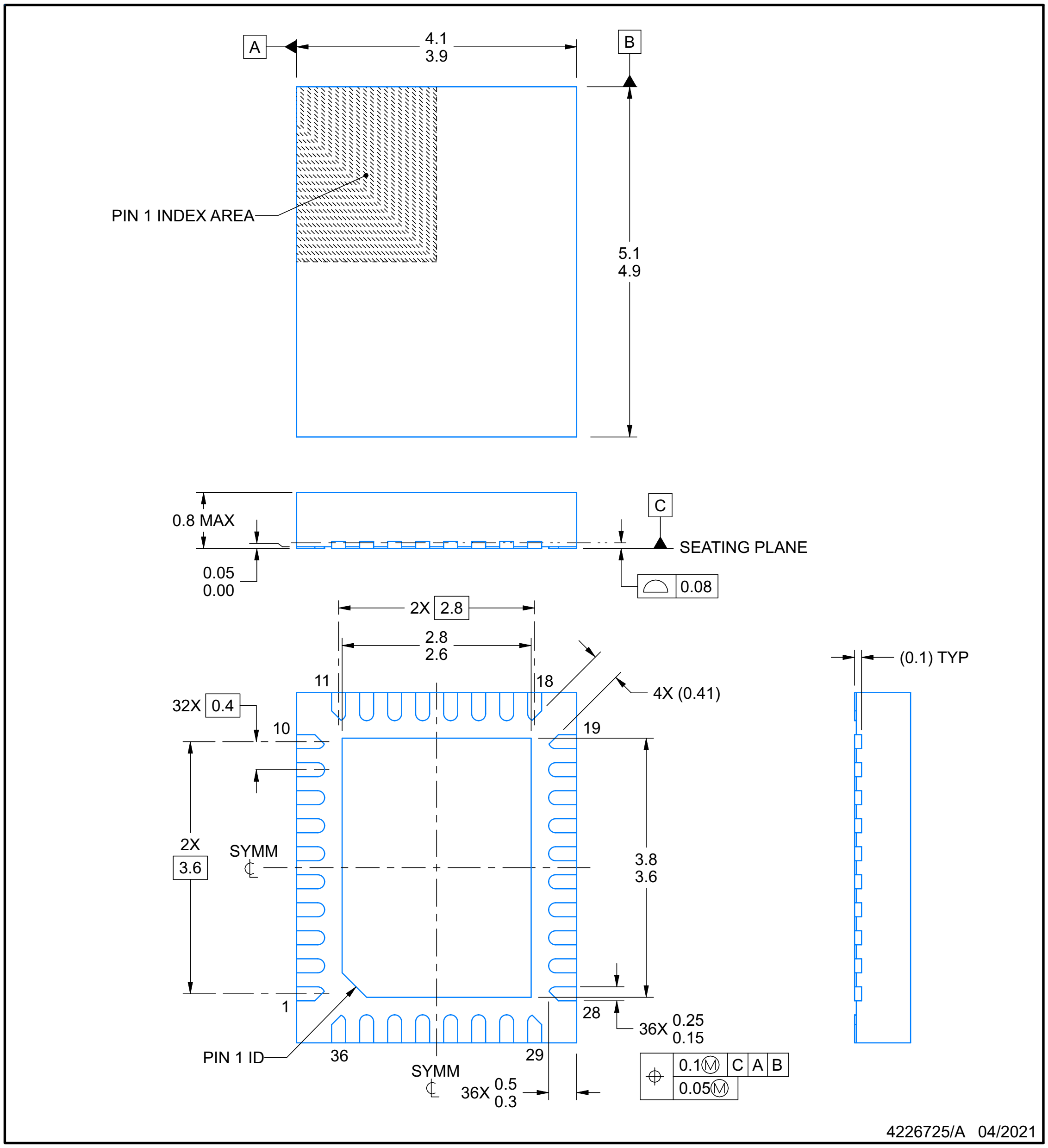
The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGE OUTLINE

REE0036A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

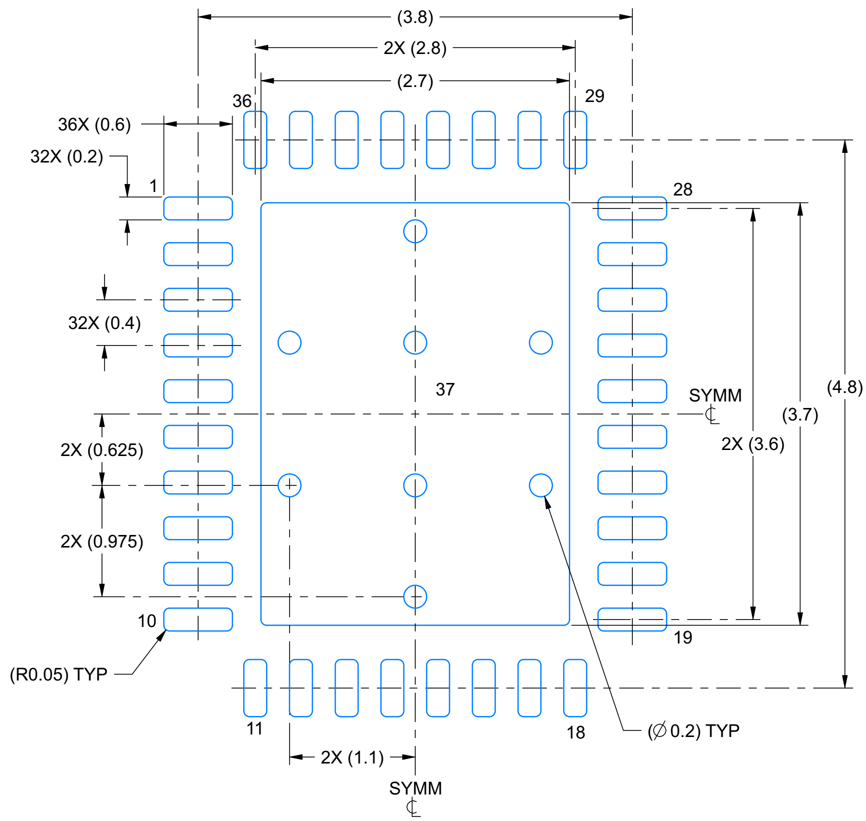
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

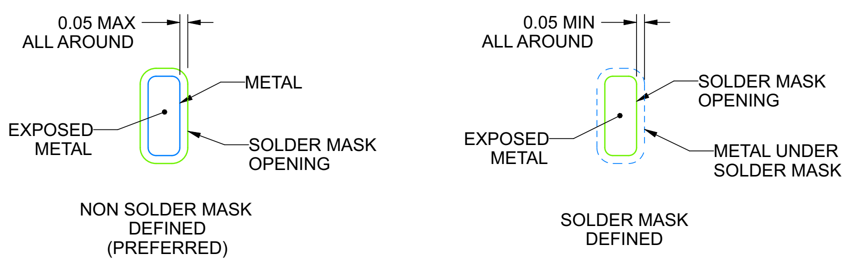
REE0036A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

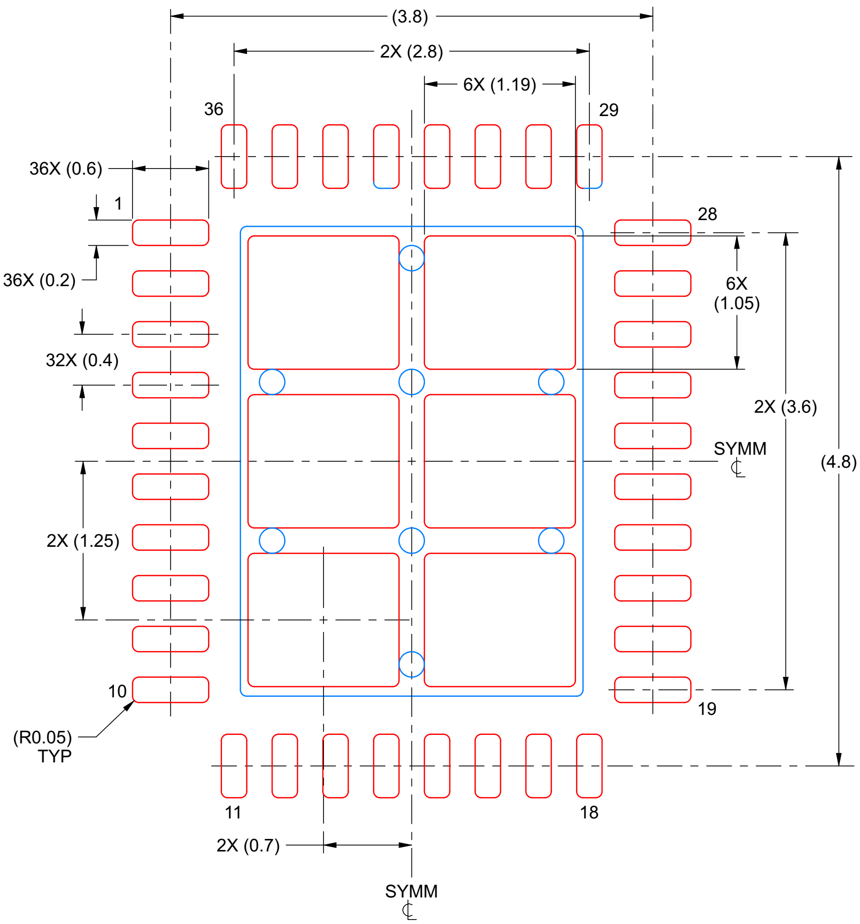
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

REE0036A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4226725/A 04/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MCF8329A1IREER	ACTIVE	WQFN	REE	36	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	MCF8329 A1I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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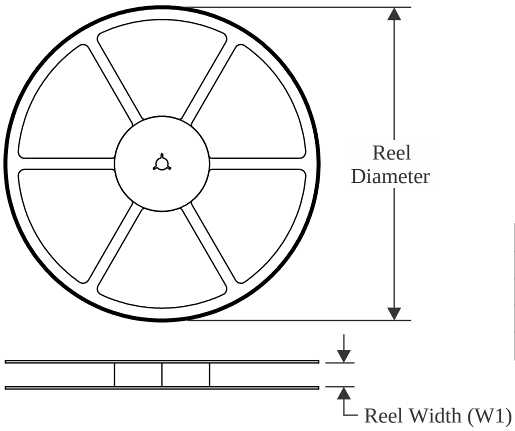
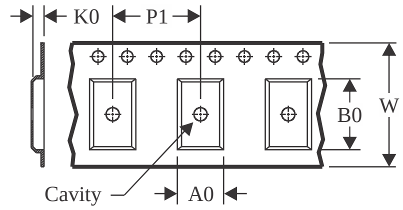
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

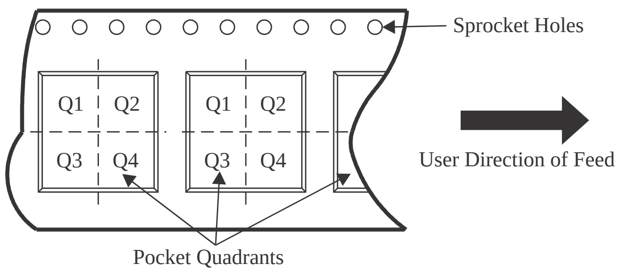


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

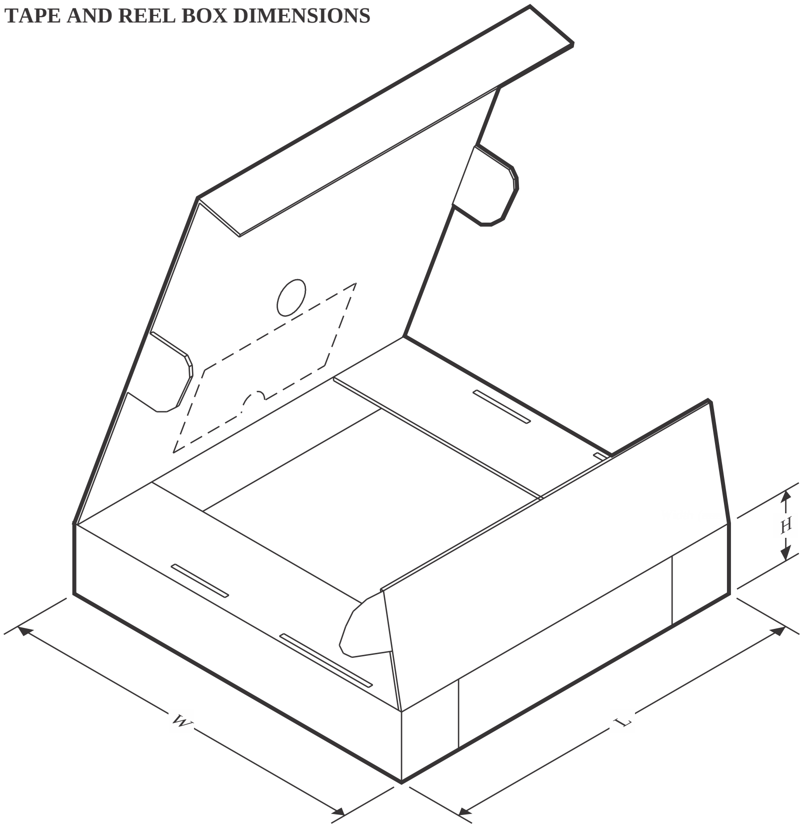
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

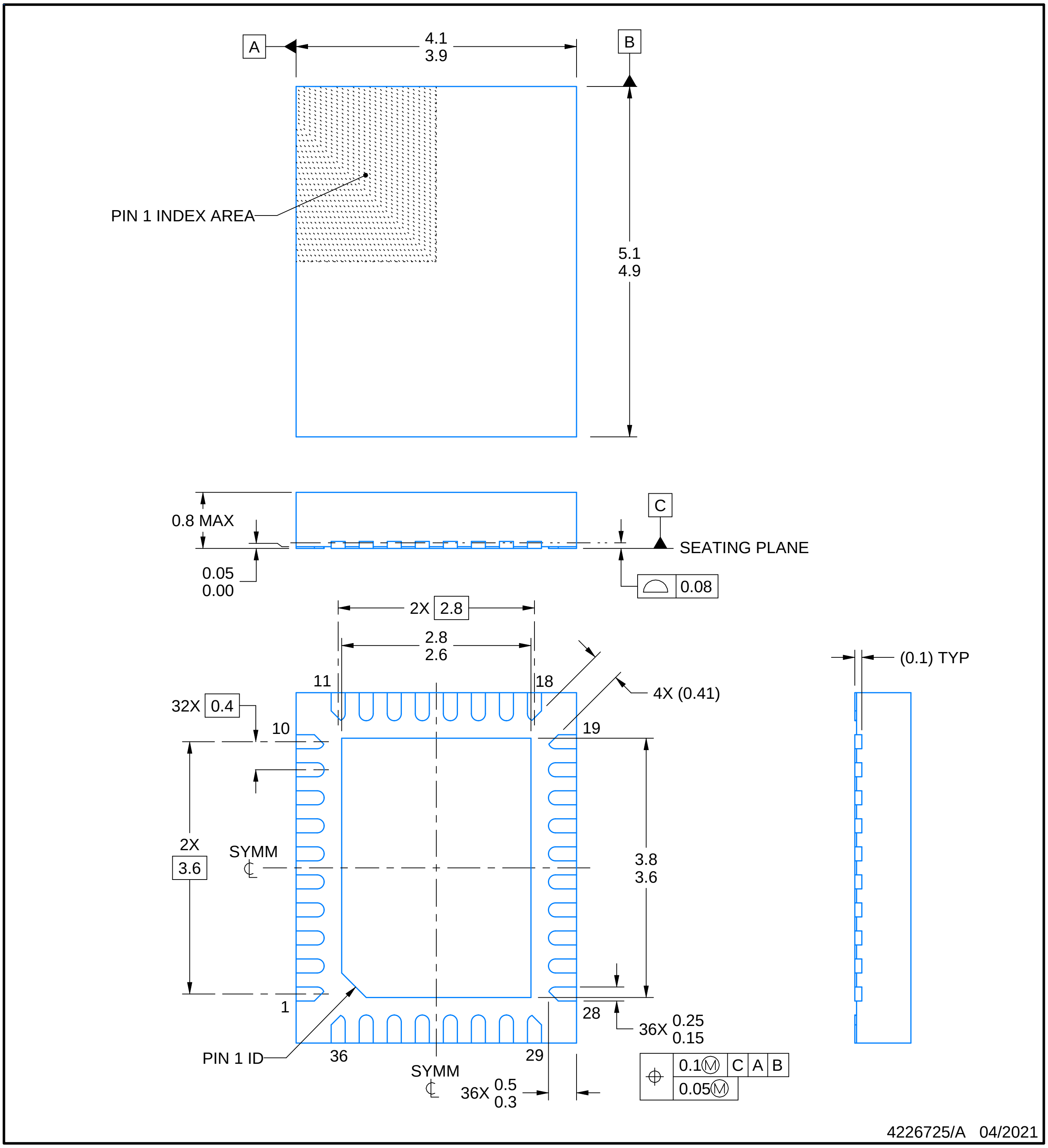
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MCF8329A1IREER	WQFN	REE	36	5000	330.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



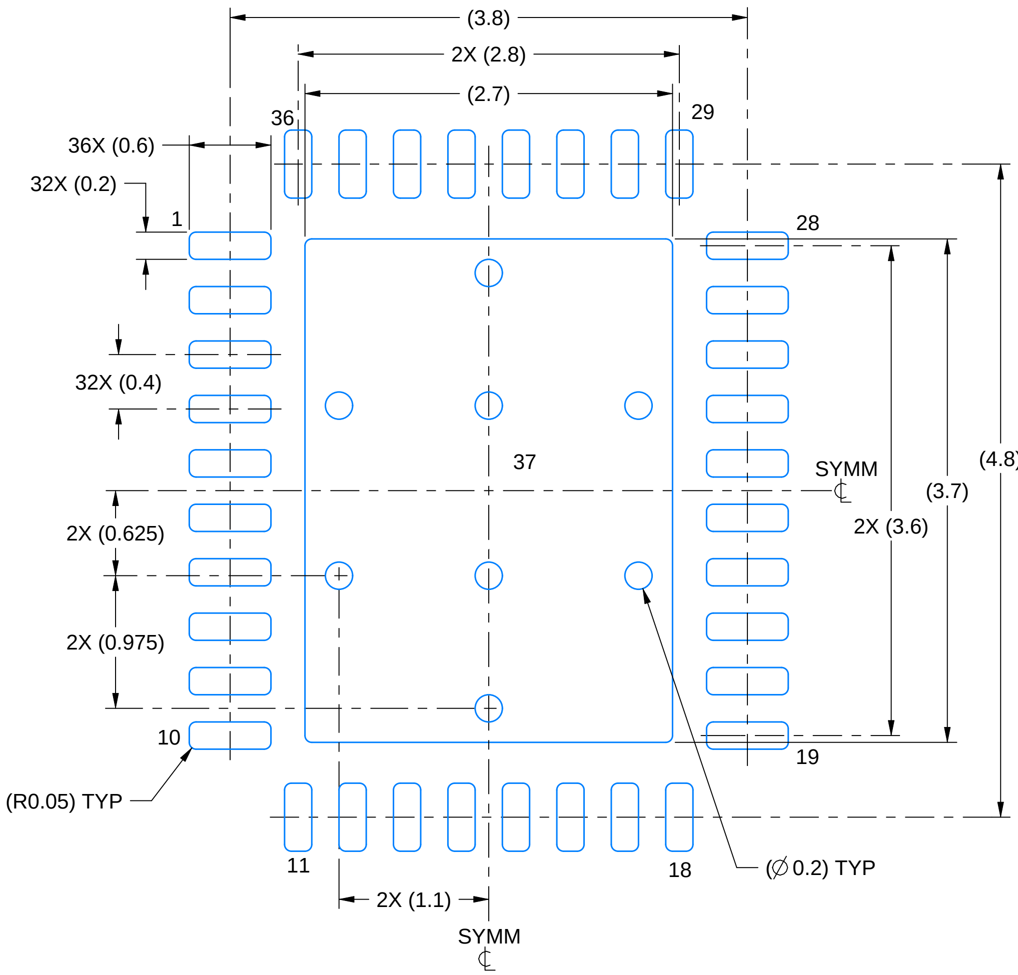
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MCF8329A1IREER	WQFN	REE	36	5000	367.0	367.0	35.0

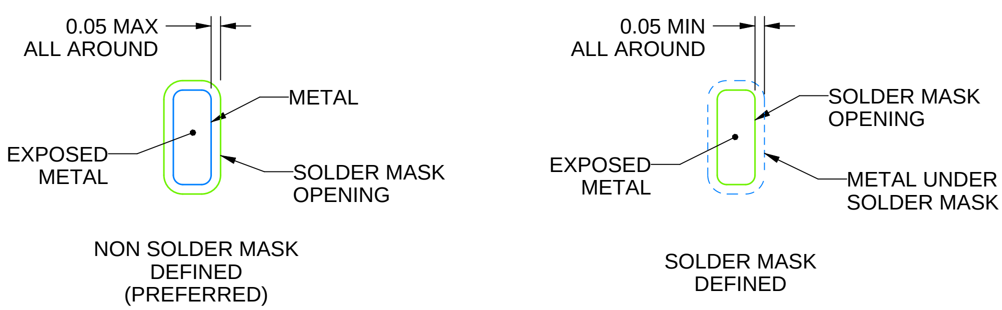


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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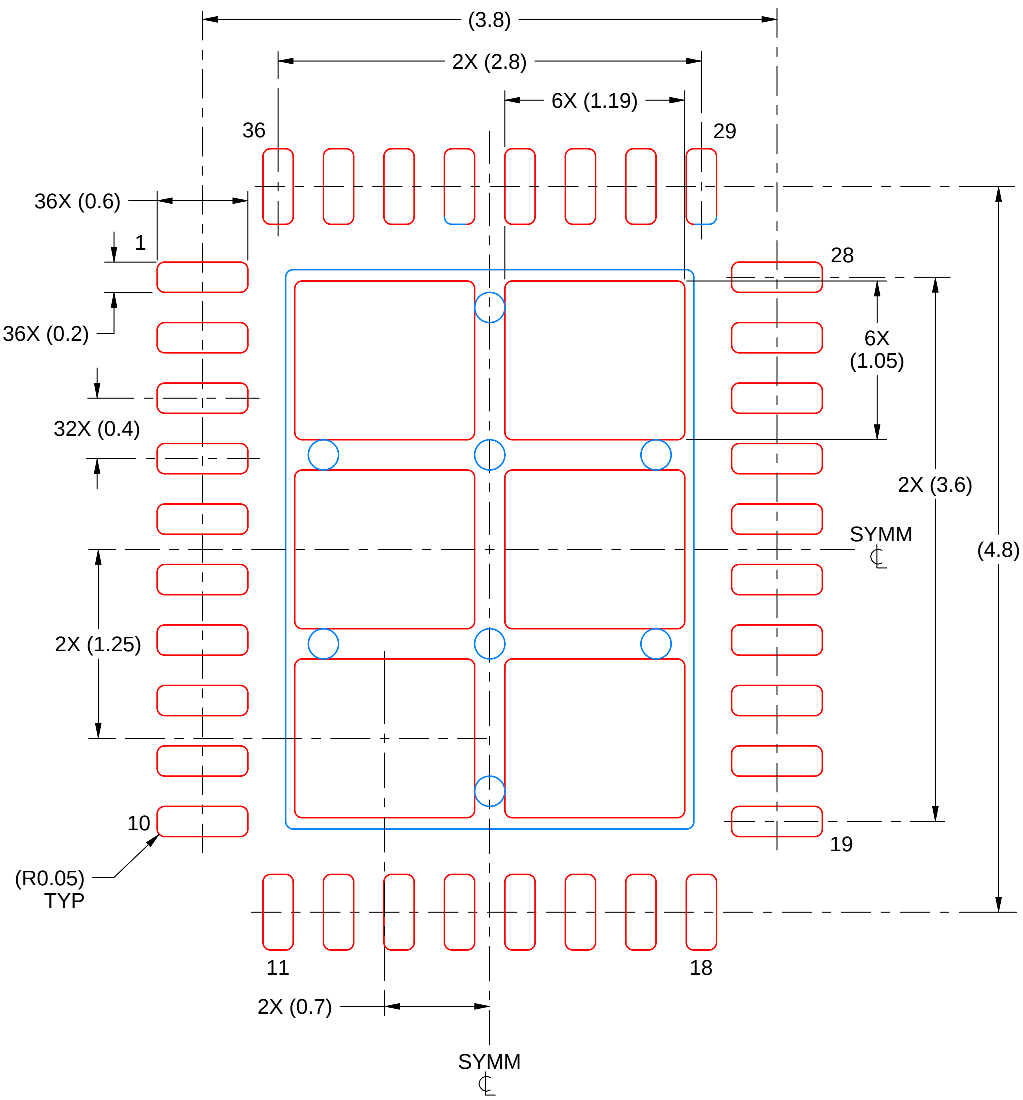
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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