GENERAL DESCRIPTION

OB2009 is a high performance and highly integrated secondary side synchronous rectification controller used for secondary side rectification in switch mode power supply system. It drives a much lower voltage drop N-channel MOSFET to emulate the traditional diode rectifier at the secondary side of flyback converter, which can reduce heat dissipation, increase output current capability and efficiency, and simplify thermal design. It can support wide range of system output voltage 3V~28V.

It is suitable for multiple mode applications including discontinuous conduction mode (DCM), quasi-resonant mode (QR) and continuous conduction mode (CCM). The drain-to-source voltage of SR MOSFET is sensed to control the turn on and off of the SR MOSFET. In addition, to reduce SR falling time further, soft gate is implemented in OB2009, which would pull down the gate voltage level before being turned off thoroughly.

OB2009 is offered in SOT23-6 package.

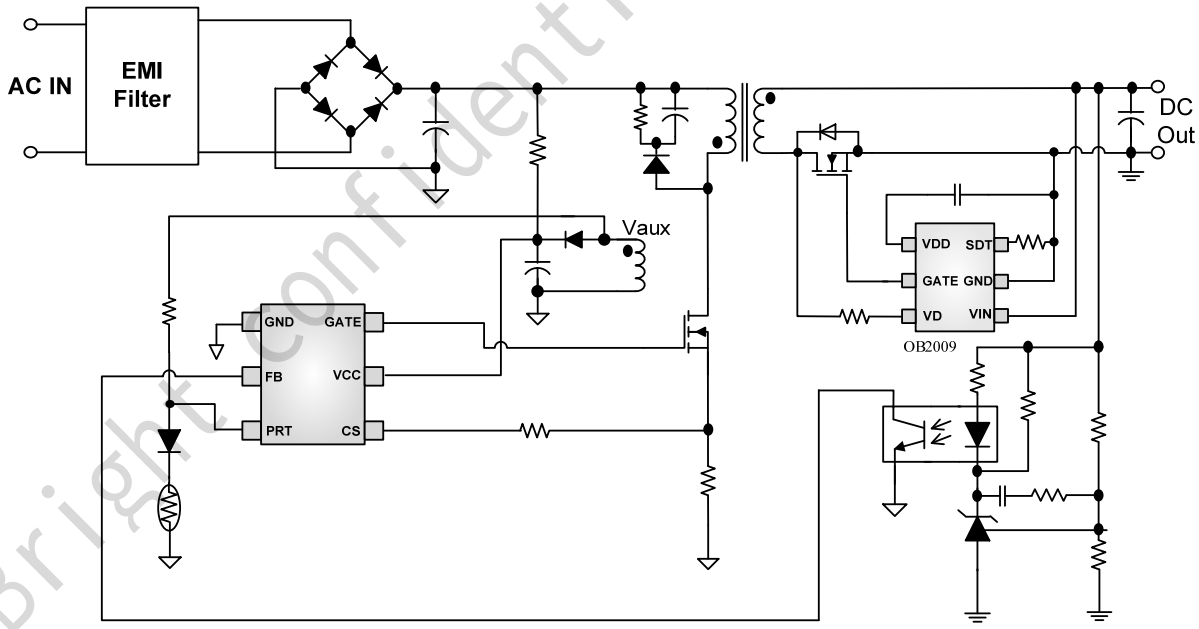
FEATURES

- Secondary-side synchronous rectification controller for 3V~28V output system
- Up to 150V VD and VIN pin high voltage tolerance
- Self-supplying for operation without the use of an auxiliary winding
- Suitable for DCM, QR and CCM operation
- Soft gate drive for fast turn-off
- Accurate secondary side MOSFET Vds sensing
- Adaptive off time control effectively avoid the ring impact induced by parasitic elements
- 3A/1A peak current sink/source driver capability
- VDD UVLO protection

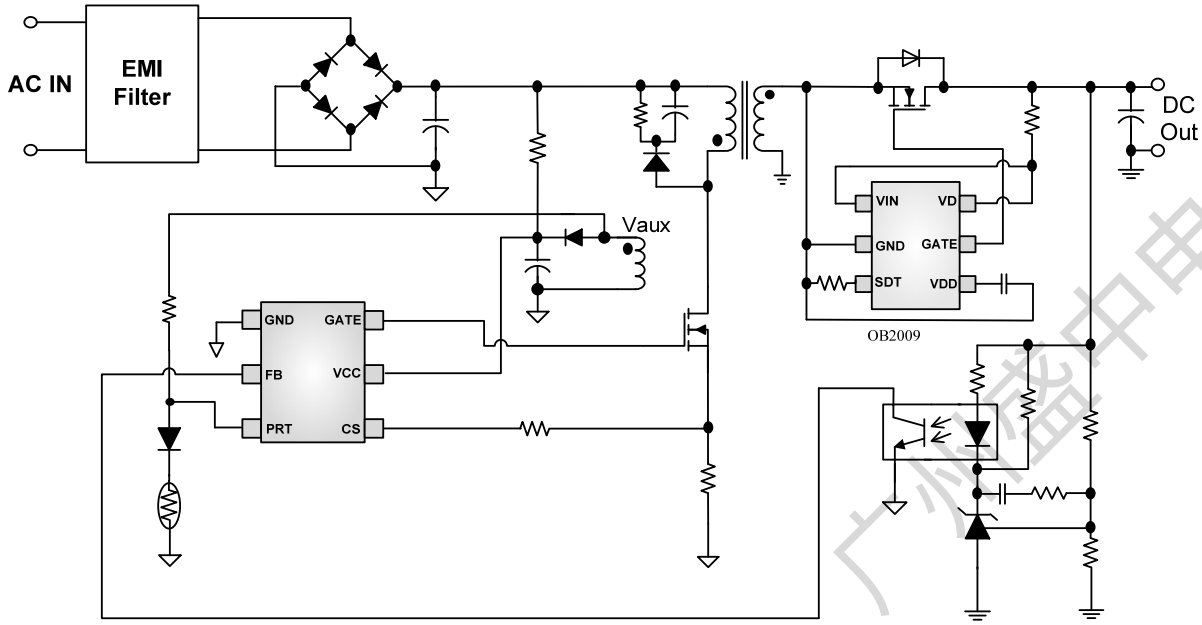
APPLICATIONS

- AC/DC 3V~28V adaptors
- Low voltage rectification circuits

TYPICAL APPLICATION



Flyback low side synchronous rectification

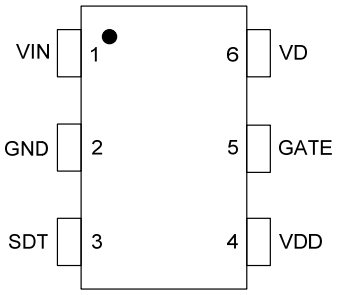


Flyback high side synchronous rectification

GENERAL INFORMATION

Pin Configuration

The OB2009 is offered in SOT23-6 package, shown as below.



Ordering Information

Part Number	Description
OB2009MP	SOT23-6, Halogen-free in T&R

Package Dissipation Rating

Package	RθJA(℃/W)	RθJC(℃/W)
SOT23-6	200	60

Recommended Operating Range

Symbol	Parameter	Min/Max
VDD	VDD Supply Voltage	5.5V to 6.5V

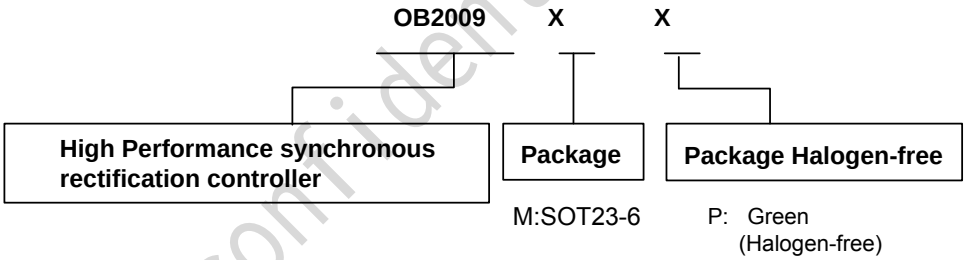
Absolute Maximum Ratings

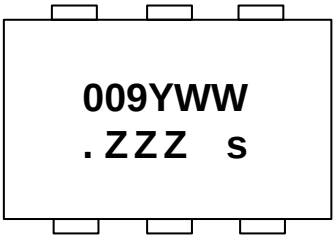
Parameter	Value
VIN pin	-2.5V to 150V Note2
VD pin	-2.5V to 150V Note2
SDT pin	-0.6V to 5V
VDD pin	-0.6V to 12V
Gate pin	-0.6V to 12V
Min/Max Operating Junction Temperature TJ	-40 to 150 ℃
Min/Max Storage Temperature Tstg	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Note2: -2.5V applies to minimum duty cycle during normal operation only.

Marking Information



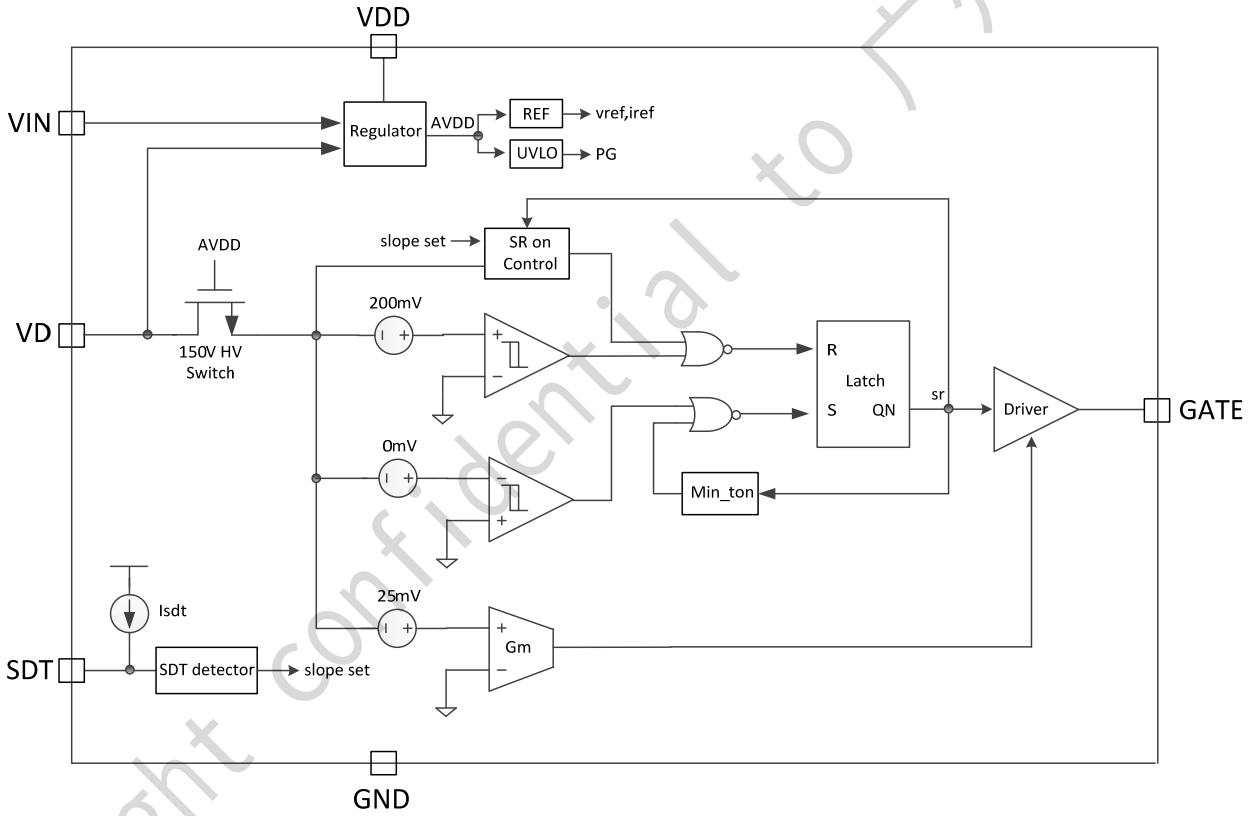


Y:Year Code
WW:Week Code(01-52)
ZZZ: Lot code
s: Internal code

TERMINAL ASSIGNMENTS

Pin Name	I/O	Description
VIN	I	System output voltage detection
GND	P	Ground
SDT	I	SDT is used to adjust the threshold of Vds falling edge slope sensing. If not otherwise stated, being floating.
VDD	P	Power Supply
GATE	O	Driver output for external N-channel MOSFET
VD	I	This pin is connected to external n-channel MOSFET drain, no more than 50ohm resistor is recommended to connect between VD and MOS drain.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

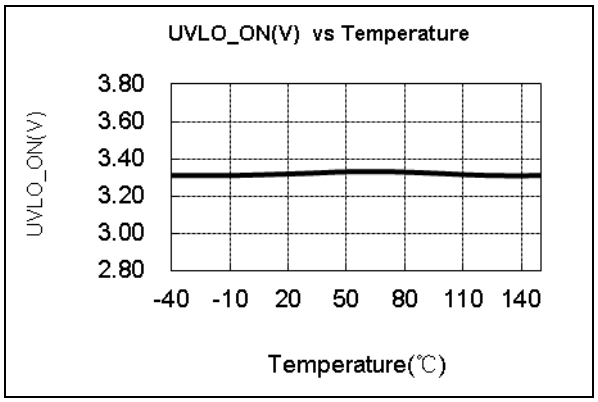
(T_A = 25℃, VDD=6.5V, unless otherwise noted)

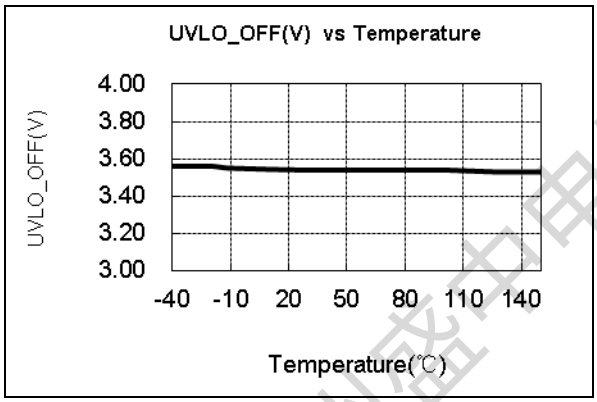
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
Supply Voltage (VDD)						
I_Vdd_operation	Operation current	Frequency@VD=65kHz, VDH=10V, VDL=-0.5V, VDD=6.5V, Vin=5V, 1nF Cap load at GATE.		1.2		mA
		Frequency@VD=2kHz, VDH=10V, VDL=-0.5V, VDD=6.5V, Vin=5V, No load at GATE.		0.4		mA
Vdd_regulation	Vdd regulation voltage	Frequency@VD=65kHz, VDH=10V, VDL=-0.5V, VIN floating, 1uF Cap load at VDD.		5.5		V
		Frequency@VD=65kHz, VDH=10V, VDL=-0.5V, VIN=12V, 1uF Cap load at VDD.		6.5		V
UVLO_OFF	VDD Under Voltage Lockout Exit			3.6		V
UVLO_ON	VDD Under Voltage Lockout Enter			3.3		V
VD Detection Section						
Vth_SR_act	SR MOSFET turn on threshold voltage detection at VD			-200		mV
Vth_SR_deact	Adjustable SR MOSFET turn off threshold voltage detection at VD, Which is 0.2*Rd mV, and Rd is the resistor connected to VD. (Note1)	Rd=0ohm		0		mV
Tdelay_on	SR MOSFET fast path turn-on propagation delay			25		ns
	SR MOSFET slow path turn-on propagation delay			225		ns
Tdelay_off	SR MOSFET turn-off propagation delay			15		ns
T_minimum_on	SR MOSFET minimum on time		1.2	1.35	1.5	us
Vth_reg	Vds regulation voltage	Rd=0ohm		-25		mV
Vth_fast_off	SR MOSFET fast turn off threshold voltage detection at VD, during min on time			1		V
VD Falling Edge Slop Detection(SDT)						
I_{SDT}	SDT sourcing current			20		uA
T_{SDT1}	Vds falling time threshold1	SDT open		150		ns
T_{SDT2}	Vds falling time threshold2	SDT connected to GND		120		ns
T_{SDT3}	Vds falling time threshold3	R_{SDT}=50k ohm		180		ns
GATE Driver Section						
VOH	Output high level @ VDD=6.5V		6			V

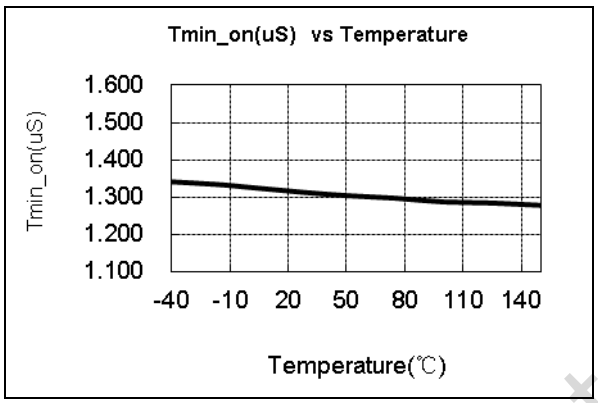
VOL	Output low level @ VDD=6.5V				0.5	V
Tf	Falling time	Gate voltage falling from 6V to 1V @ C_L=1nF		10		ns
Tr	Rising time	Gate voltage rising from 1V to 6V @ C_L=1nF		20		ns

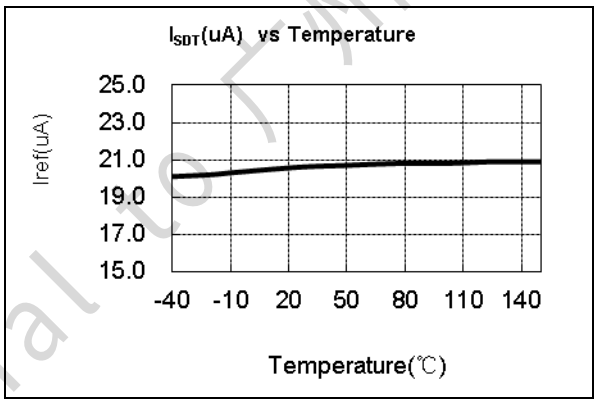
Note1： Rd can be chosen between 10~50 Ω

CHARACTERIZATION PLOTS









Operation Description

OB2009 is a high performance and highly integrated secondary side synchronous rectification controller in switch mode power supply system. It drives a much lower voltage drop N-channel MOSFET to emulate the traditional diode rectifier, which can reduce heat dissipation, increase output current capability and efficiency, and simplify the thermal design.

Startup and under voltage lockout (UVLO)

Whether OB2009 can operate normally or not depends on UVLO function implemented on chip. When power system is plugged in, VDD cap is charged from transformer secondary winding. When VDD rises above UVLO(off), the IC wakes up from under voltage lock out state, refer to Fig.1.

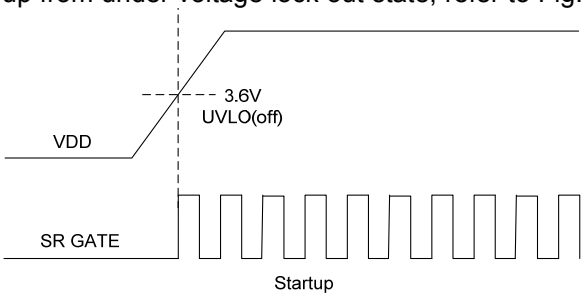


Fig.1 System start up timing diagram

With enough high Vin, OB2009 would be powered from VDD and system output (Vin), which can lead to better system efficiency. When VDD drops below UVLO(on),SR would be disable. Refer to the following timing diagram.

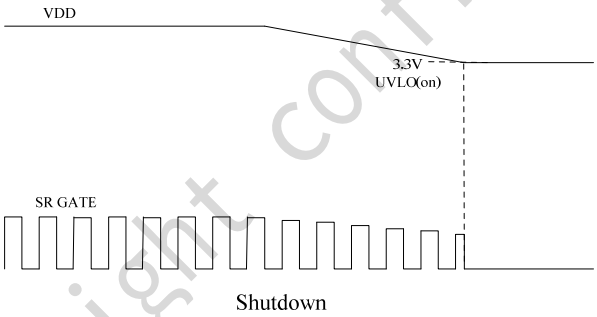


Fig.2 System shut down timing diagram

Besides, a hysteresis window between UVLO(off) and UVLO(on) makes system work reliably.

Turn-on and Turn-off Phase

OB2009 controls the turn-on and turn-off of synchronization rectifier MOSFET (SR MOSFET) by detection of drain-source voltage of SR MOSFET. When demagnetization of transformer starts, the secondary-side current will flow through the body diode of SR MOSFET and the voltage at the drain will drop to below -200mV (typical). As soon as OB2009 detects this negative voltage and the VD falling time is lower than T_{SDT}, the driver voltage is pulled high to turn on the SR MOSFET after variable delay time depending on input line voltage and loading condition, refer to Fig.3. This variable delay time can improve system immunity to noise.

After the SR MOSFET is turned on, the drain voltage of SR MOSFET begins to rise based on its Rdson and secondary-side current. The drain voltage becomes higher with demagnetization goes on. For reliable operation,OB2009 generates an adjustable SR turn-off threshold voltage based on resistor Rd on VD pin, which is determined by 0.2*Rd mV. When the drain voltage rises above SR turn off threshold, the gate of SR MOSFET will be pulled down to ground very quickly after turn-off delay, refer to Fig.3.

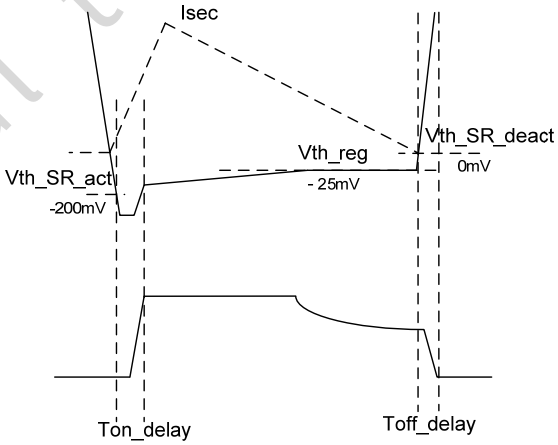


Fig.3 Synchronous Rectification Operation

Conduction Phase

Once the SR MOSFET is turned on, the gate drive voltage will remain at the high level during minimum on time. With the decrease of the switching current, the VDS will rise above Vth_reg(typ. -25mV), then the soft gate control is implemented. The gate voltage is pulled lower to enlarge the Rds(on) of the synchronous MOSFET, therefore VDS is adjusted to remain at -25mV during the rest of demagnetization time. The low level gate voltage saves the pull-down time, resulting in higher turn-off speed, which is very important in CCM mode.

Minimum on time

To avoid effectively false turn-off due to high frequency interference caused by parasitic

element at the start of secondary-side demagnetization, OB2009 offers a blanking time(minimum turn-on time) of 1.35μs.

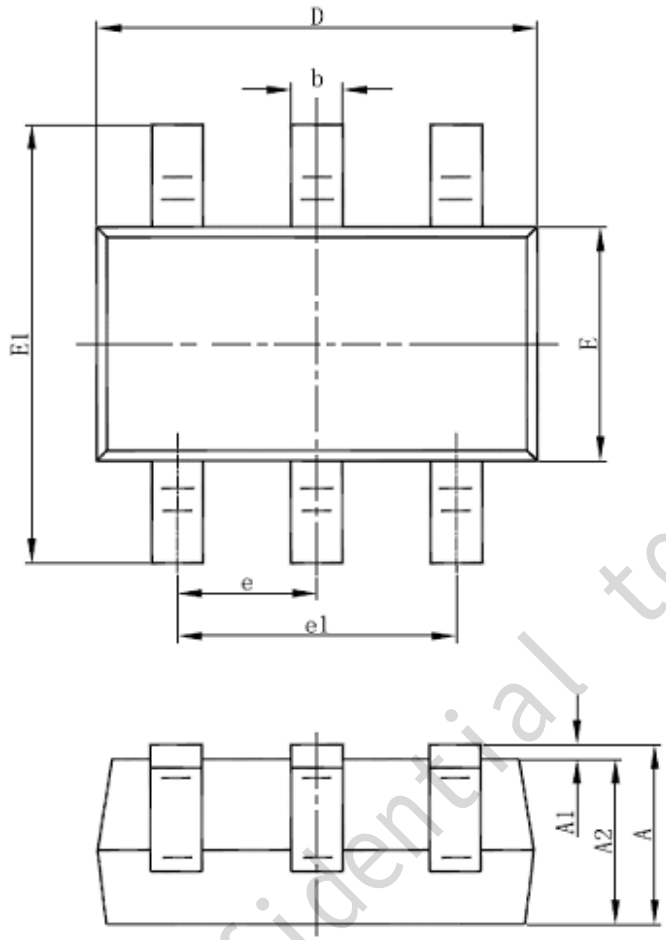
Adaptive minimum off time

At the end of demagnetization, SR MOSFET will be turn off. The remaining current may flow through body diode again, which may result in negative voltage (about -700mV) appears at drain and SR MOSFET will turn on again. In addition, the resonance oscillation between the magnetization inductance and parasitic capacitance after demagnetization may cause negative drain voltage. These may turn on SR MOSFET unexpectedly. To avoid above mis-turn-on of SR MOSFET, constant minimum off time can be used to screen it. But it may disturb SR MOSFET operation. For reliable SR operation achieve reliable SR operation, an adaptive minimum off time control is implemented in OB2009, which can guarantee reliable synchronous rectification operation.

Gate driver

For good and efficient synchronous rectification operation, the SR MOSFET should be turned on/off in very short time. Therefore strong driver capability is needed. OB2009 can offer typical source capability 1A and typical sink capability 3A. This guarantees fast turn-on and turn-off of SR MOSFET. In addition, in order to further speed up gate turn off, soft gate control is implemented. Refer to Conduction Phase section for soft gate control.

PACKAGE MECHANICAL DATA



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.450	0.039	0.057
A1	0.000	0.150	0.000	0.006
A2	0.900	1.300	0.035	0.051
b	0.300	0.500	0.012	0.020
c	0.080	0.220	0.003	0.009
D	2.800	3.020	0.110	0.119
E	1.500	1.726	0.059	0.068
E1	2.600	3.000	0.102	0.118
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

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