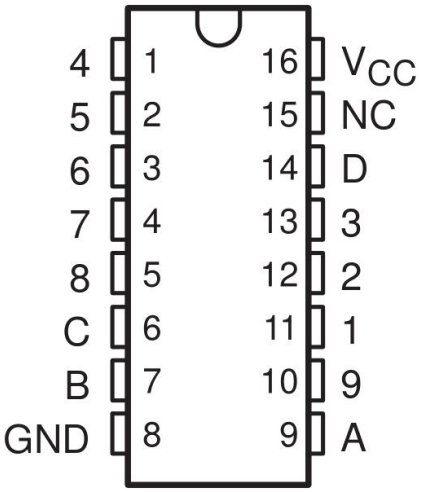
1. DESCRIPTION

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The ’LS147 devices encode nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition, as zero is encoded when all nine data lines are at a high logic level. The ’LS148 devices encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level. All inputs are buffered to represent one normalized Series 74LS load, respectively.

2. PIN CONFIGURATIONS

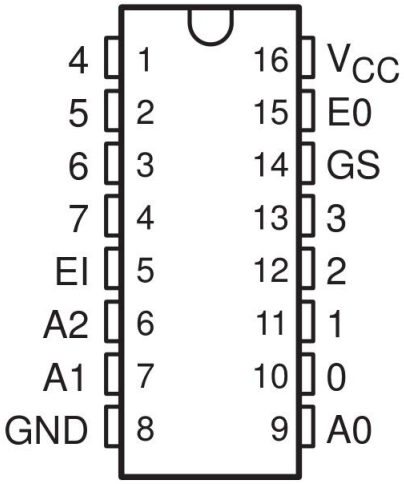
XD74LS147

(TOP VIEW)

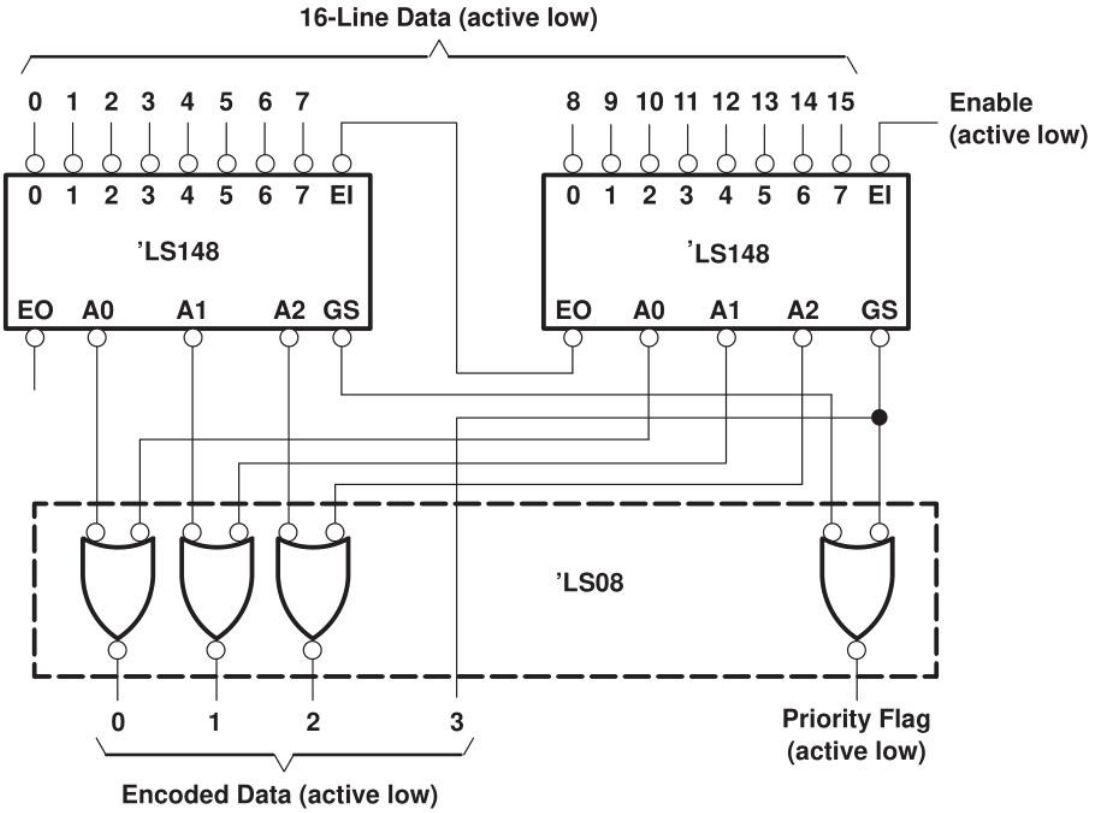


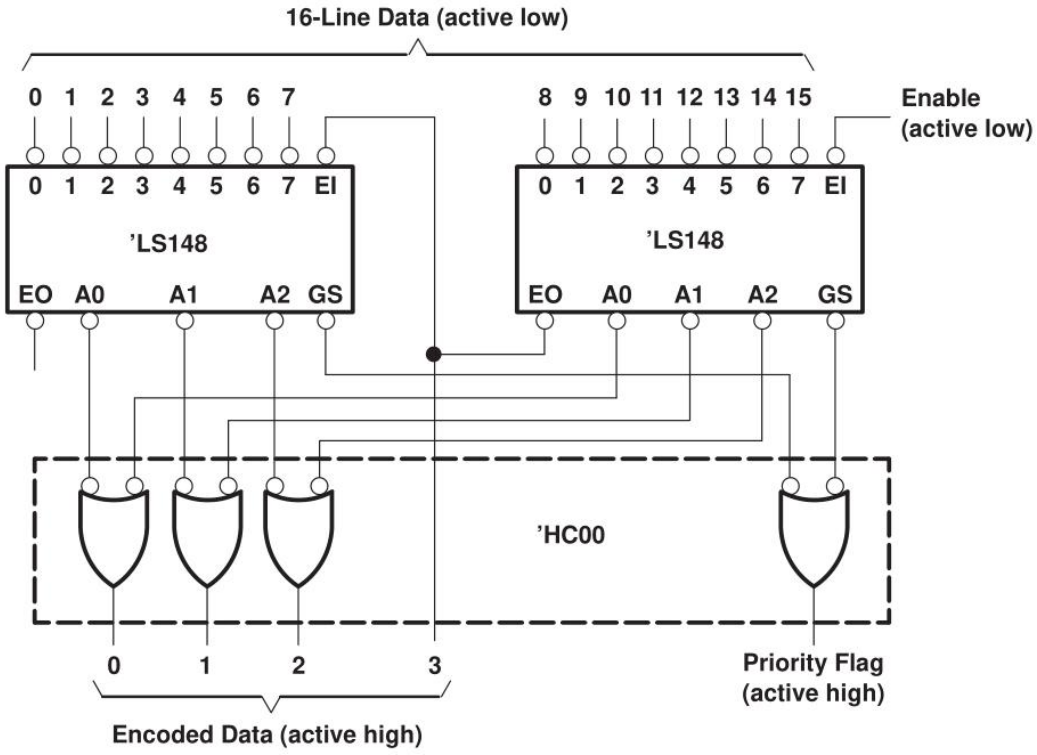
XL/XD74LS148

(TOP VIEW)



3. APPLICATION INFORMATION

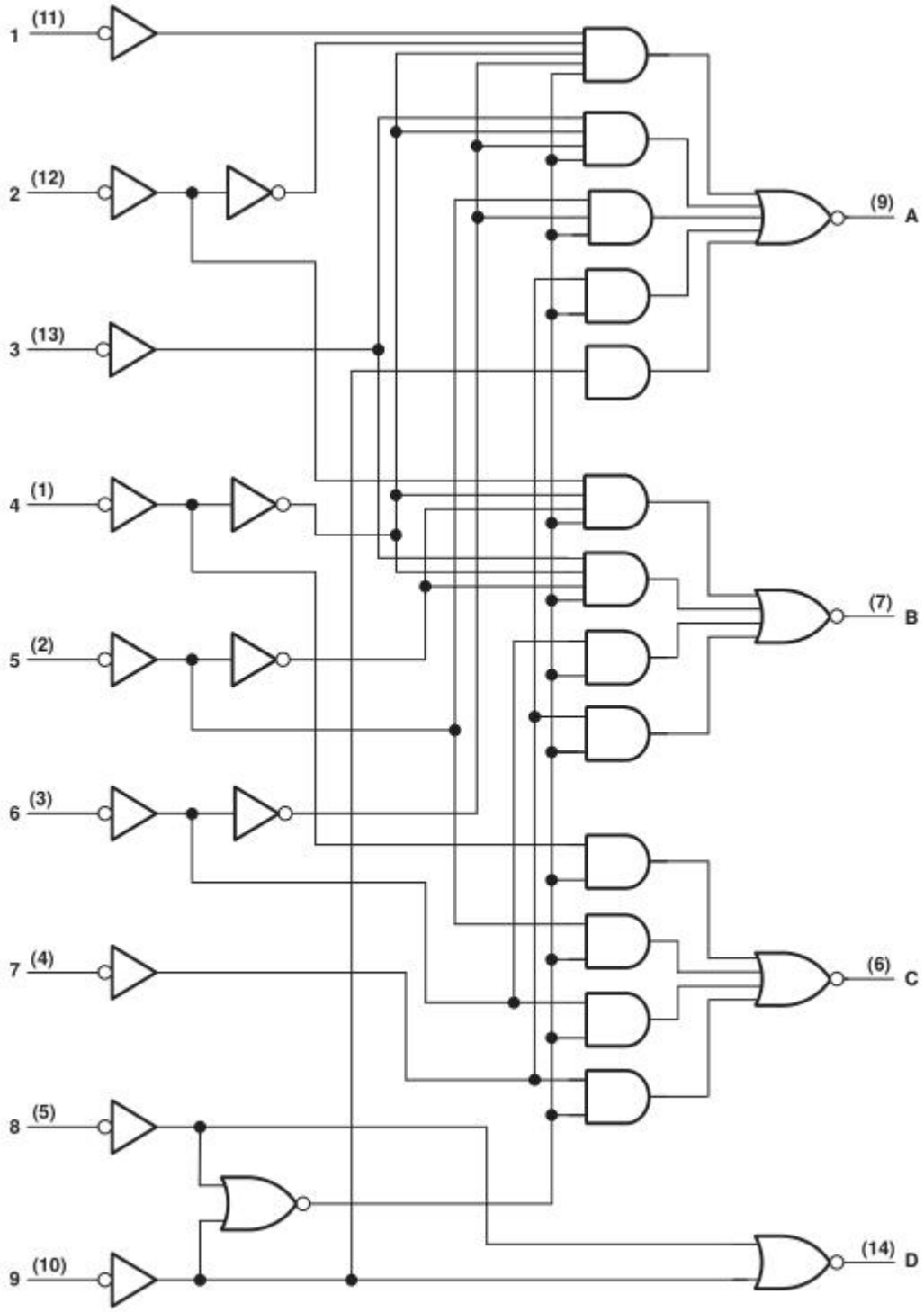




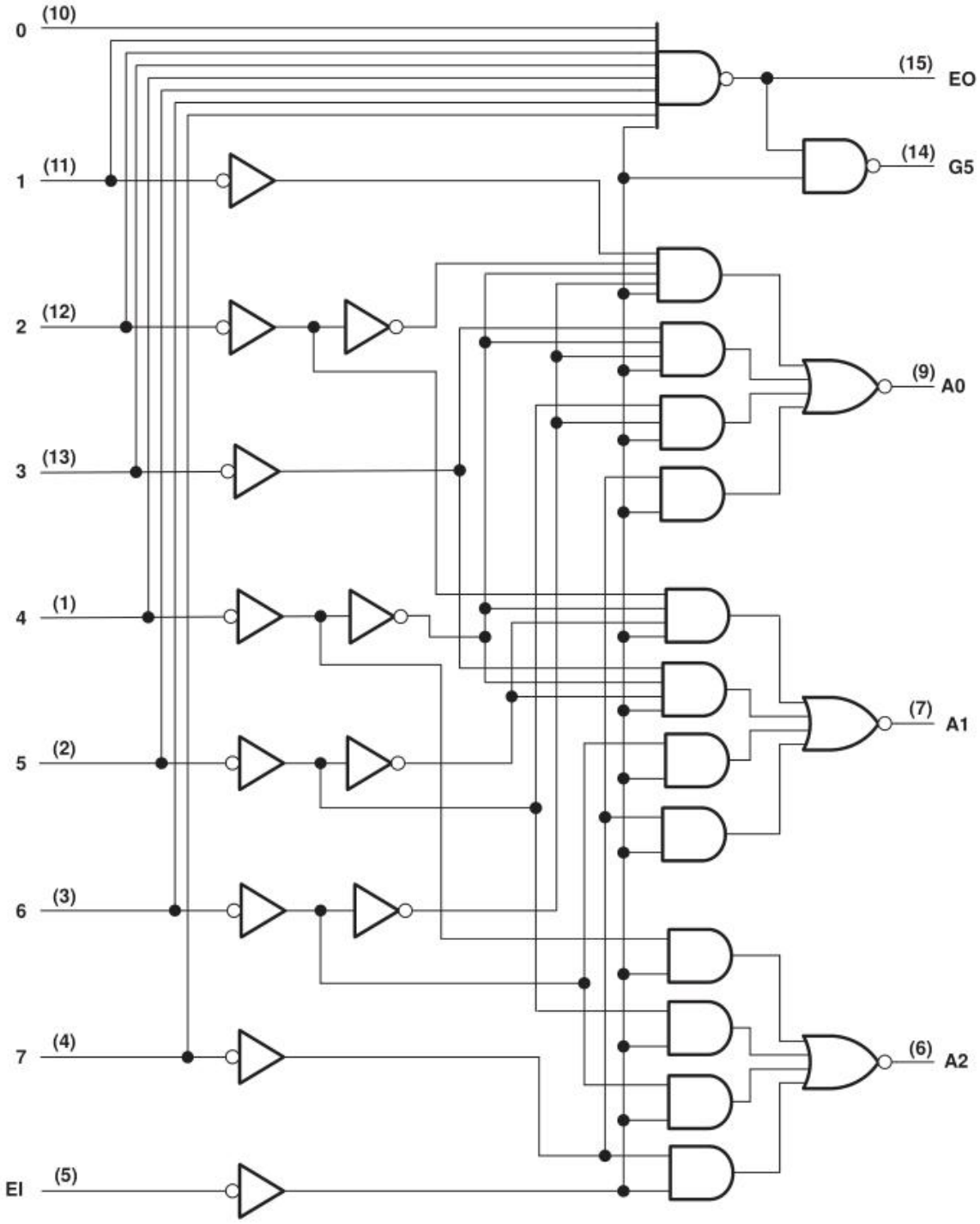
Because the ’LS147 and ’LS148 devices are combinational logic circuits, wrong addresses can appear during input transients. Moreover, for the ’LS148 devices, a change from high to low at EI can cause a transient low on GS when all inputs are high. This must be considered when strobing the outputs.

4. LOGIC DIAGRAM

'LS147 logic diagram (positive logic)



'LS148 logic diagram (positive logic)



FUNCTION TABLE – 74LS147

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = high logic level, L = low logic level, X = irrelevant

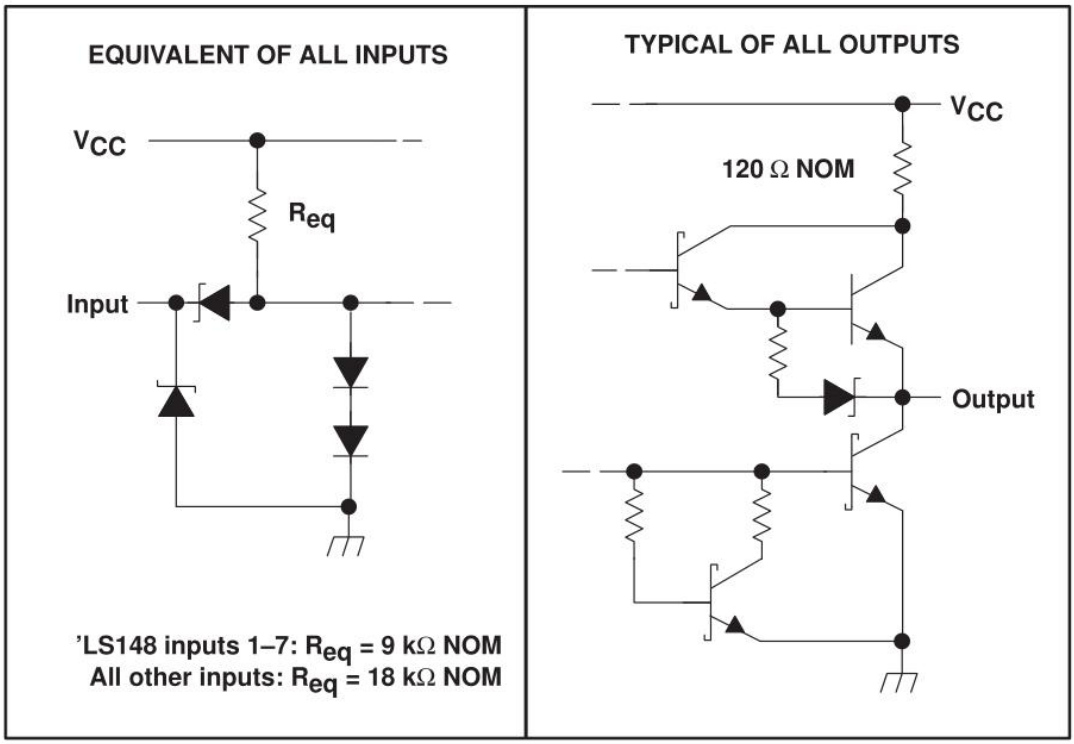
FUNCTION TABLE – 74LS148

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = high logic level, L = low logic level, X = irrelevant

5. SCHEMATICS OF INPUTS AND OUTPUTS

'LS147, 'LS148



6. ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTES)

Supply voltage, V_{CC} (see Note 1)..... 7V

Input voltage, VI: 74LS148/ 74LS147..... 7V

Operating free-air temperature range: SOP package..... 0°C to 70°C

DIP package..... 0°C to 70°C

Storage temperature range, Tstg..... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES:
1. Voltage values, except inter-emitter voltage, are with respect to the network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

7. RECOMMENDED OPERATING CONDITIONS

		74LS'			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.75	5	5.25	V
I_{OH}	High-level output current			−400	mA
I_{OL}	Low-level output current			8	mA
T_A	Operating free-air temperature	0		70	°C

8. ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR RANGE (UNLESS OTHERWISE NOTED)

PARAMETER			TEST CONDITIONS†		74LS'			UNIT
					MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −400 μA	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} MAX	I_{OL} = 4 mA		0.25	0.4	V
				I_{OL} = 8 mA		0.35	0.5	
I_I	Input current at maximum input voltage	'LS148 inputs 1–7	V_{CC} = MAX,	V_I = 7 V			0.2	mA
		All other inputs					0.1	
I_{IH}	High-level input current	'LS148 inputs 1–7	V_{CC} = MAX,	V_I = 2.7 V			40	μA
		All other inputs					20	
I_{IL}	Low-level input current	'LS148 inputs 1–7	V_{CC} = MAX,	V_I = 0.4 V			−0.8	mA
		All other inputs					−0.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX (See Note 6)	Condition 1		12	20	mA
				Condition 2		10	17	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 4: For 'LS147, I_{CC} (Condition 1) is measured with input 7 grounded, other inputs and outputs open; I_{CC} (Condition 2) is measured with all inputs and outputs open. For 'LS148, I_{CC} (Condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open; I_{CC} (Condition 2) is measured with all inputs and outputs open.

9. SWITCHING CHARACTERISTICS,VCC = 5 V, TA = 25℃

SN74LS147 switching characteristics, VCC = 5 V, TA = 25°C (see Figure 1)

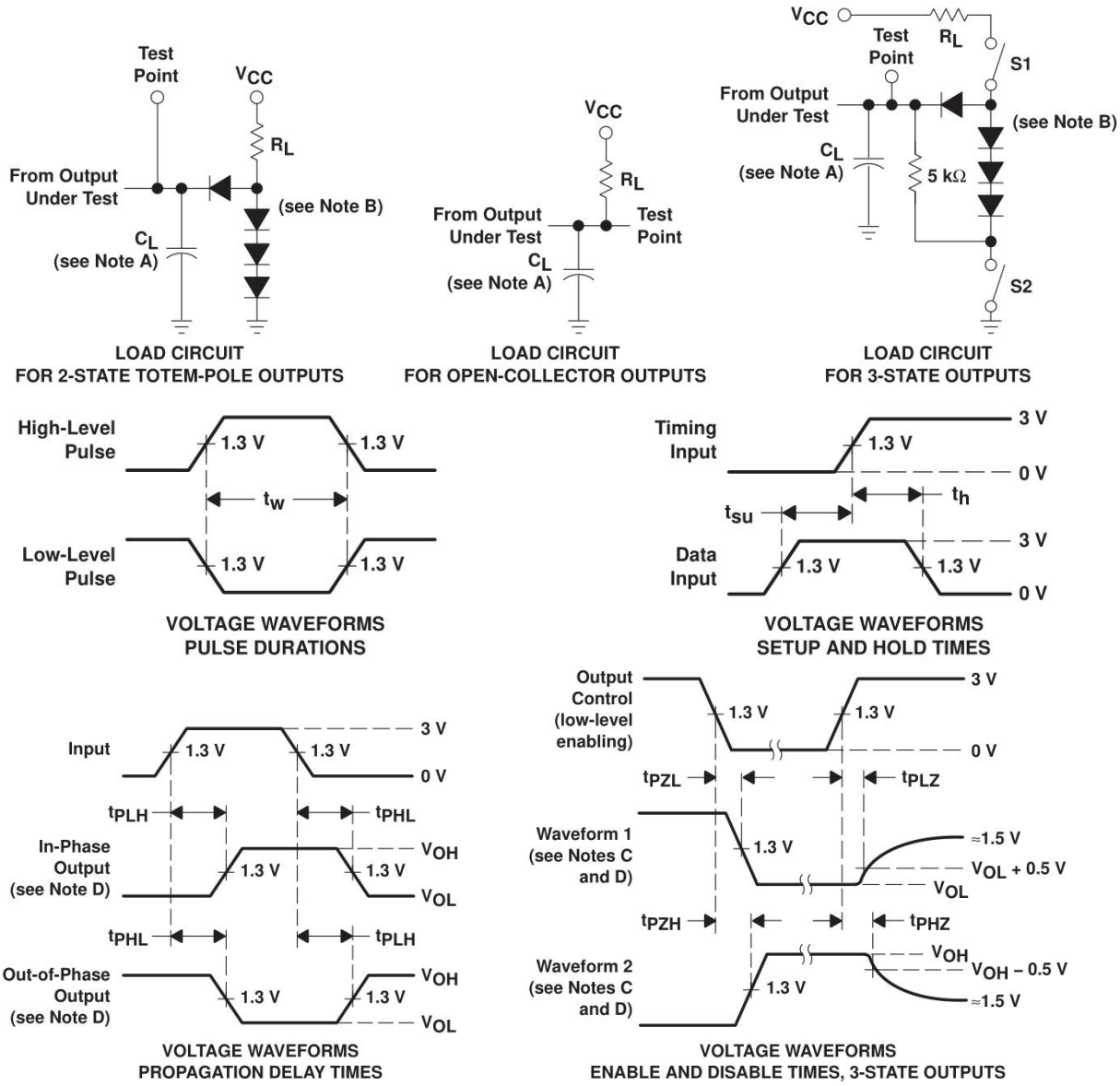
PARAMETER	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Any	In-phase output	C_L = 15 pF, R_L = 2 kΩ		12	18	ns
t_{PHL}						12	18	
t_{PLH}	Any	Any	Out-of-phase output			21	33	ns
t_{PHL}						15	23	

SN74LS148 switching characteristics, V_{CC} = 5 V, T_A = 25°C (see Figure 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	1–7	A0, A1, or A2	In-phase output	C_L = 15 pF, R_L = 2 kΩ		14	18	ns
t_{PHL}						15	25	
t_{PLH}	1–7	A0, A1, or A2	Out-of-phase output			20	36	ns
t_{PHL}						16	29	
t_{PLH}	0–7	EO	Out-of-phase output			7	18	ns
t_{PHL}						25	40	
t_{PLH}	0–7	GS	In-phase output			35	55	ns
t_{PHL}						9	21	
t_{PLH}	EI	A0, A1, or A2	In-phase output			16	25	ns
t_{PHL}						12	25	
t_{PLH}	EI	GS	In-phase output			12	17	ns
t_{PHL}						14	36	
t_{PLH}	EI	EO	In-phase output			12	21	ns
t_{PHL}						23	35	

† t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

10. PARAMETER MEASUREMENT INFORMATION SERIES 74LS DEVICES



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064 or equivalent.
C. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open, and S2 is closed for t_{PZH}; S1 is closed, and S2 is open for t_{PZL}.
E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, $t_r \le 1.5$ ns, $t_f \le 2.6$ ns.
G. The outputs are measured one at a time, with one input transition per measurement.

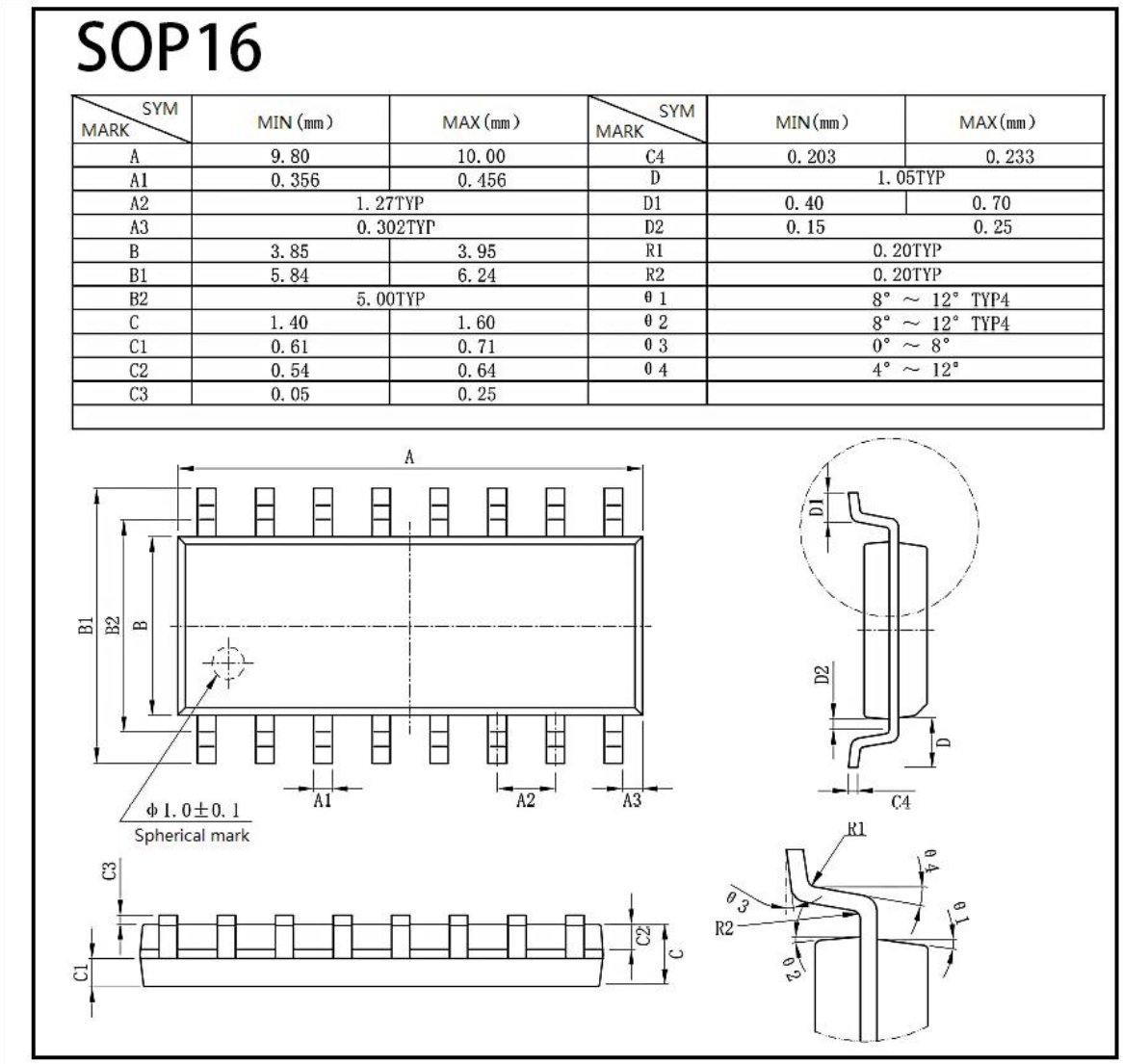
Figure 1. Load Circuits and Voltage Waveforms

11. ORDERING INFORMATION

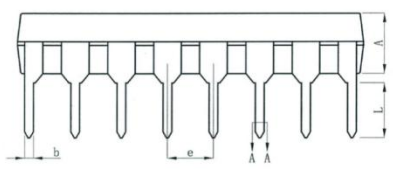
Ordering Information

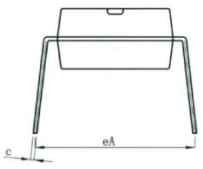
Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL74LS148	XL74LS148	SOP16	10.00 * 3.95	-0 to 70	MSL3	T&R	2500
XD74LS148	XD74LS148	DIP16	19.05 * 6.35	-0 to 70	MSL3	Tube 25	1000
XD74LS147	XD74LS147	DIP16	19.05 * 6.35	-0 to 70	MSL3	Tube 25	1000

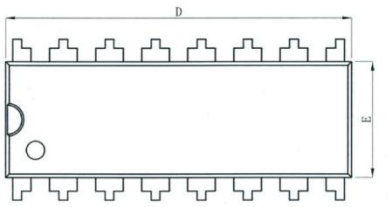
12. DIMENSIONAL DRAWINGS

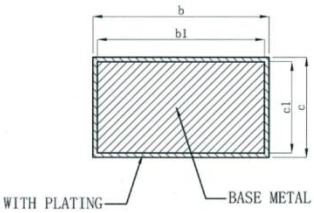


DIP16









symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	---	0.53
b1	0.43	0.46	0.49
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	---	---