1. DESCRIPTION

Each circuit in XL/XD74LS14 functions as an inverter. However, because of the Schmitt-Trigger action, they have different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

These circuits are temperature compensated and can be triggered from the slowest of input ramps and still give clean, jitter-free output signals.

2. FEATURES

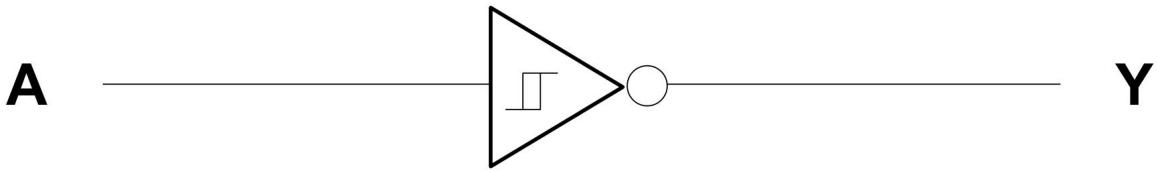
- Operation From Very Slow Edges
- Improved Line-Receiving Characteristics
- High Noise Immunity

3. APPLICATIONS

- HVAC Gateways
- Residential Ductless Air Conditioning Outdoor Units
- Robotic Controls
- Industrial Stepper Motors
- Power Meter and Power Analyzers
- Digital Input Modules for Factory Automation

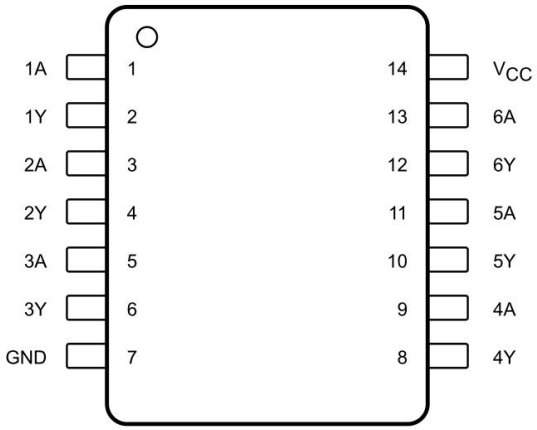
4. LOGIC DIAGRAM

Logic Diagram (Positive Logic)



5. PIN CONFIGURATIONS AND FUNCTIONS

Top View



PIN		I/O	DESCRIPTION
NAME	SOP, DIP		
1A	1	I	Channel 1 input
1Y	2	O	Channel 1 output
2A	3	I	Channel 2 input
2Y	4	O	Channel 2 output
3A	5	I	Channel 3 input
3Y	6	O	Channel 3 output
4A	9	I	Channel 4 input
4Y	8	O	Channel 4 output
5A	11	I	Channel 5 input
5Y	10	O	Channel 5 output
6A	13	I	Channel 6 input
6Y	12	O	Channel 6 output
GND	7	—	Ground
NC	—	—	No internal connection
V_{CC}	14	—	Power supply

6. SPECIFICATIONS

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CC}(2)			7	V
Input voltage	XL/XD74LS14		7	V
Junction temperature, T_J			150	℃
Storage temperature, T_{stg}		–65	150	℃

[1] Stressesbeyondthoselistedunder AbsoluteMaximumRatingsmaycausepermanentdamagetothedevice. Thesearestress ratingsonly, whichdonotimplyfunctionaloperationofthedeviceattheseoranyotherconditionsbeyondthoseindica ted underRecommendedOperatingConditions. Exposuretoabsolute-maximum-ratedconditionsforextendedperiodsmayaf fect devicereliability.

[2] Voltagevaluesarewithrespecttonetworkgroundterminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	XL/XD74LS14	4.75	5	5.25	V
I_{OH}	High-level output current	XL/XD74LS14			–0.4	mA
I_{OL}	Low-level output current	XL/XD74LS14			8	mA
T_A	Operating free-air temperature	XL/XD74LS14	0		70	℃

6.4 Thermal Information

THERMAL METRIC(1)		XL/XD74LS14 SOP,DIP 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	54.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.6	°C/W

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
V_{T+}	V_{CC} = 5 V	XL/XD74LS14	1.4	1.6	1.9	V
; 、 V_{T-}	V_{CC} = 5 V	XL/XD74LS14	0.5	0.8	1	V
Hysteresis (V_{T+} – V_{T-})	V_{CC} = 5 V		0.4	0.8		V
V_{IK}	V_{CC} = MIN, I_I = –18 mA, XL/XD74LS14				–1.5	V
V_{OH}	V_{CC} = MIN, V_I = 0.5 V, I_{OH} = –0.4 mA, XL/XD74LS14		2.4	3.4		V
V_{OL}						V
	V_{CC} = MIN, V_I = 1.9 V	I_{OL} = 4 mA, XL/XD74LS14		0.25	0.4	
		I_{OL} = 8 mA, XL/XD74LS14		0.35	0.5	
I_{T+}	V_{CC} = 5 V, V_I = V_{T+}	XL/XD74LS14		0.14		mA
I_{T-}	V_{CC} = 5 V, V_I = V_{T-}	XL/XD74LS14		0.18		mA
I_I	V_{CC} = MAX, V_I = 7 V, XL/XD74LS14				0.1	mA
I_{IH}	V_{CC} = MAX, V_{IH} = 2.7 V, XL/XD74LS14				20	µA
I_{IL}	V_{CC} = MAX, V_{IL} = 0.4 V	XL/XD74LS14			–0.4	mA
I_{OS}(3)	V_{CC} = MAX	XL/XD74LS14	–20		–100	mA
I_{CCH}	V_{CC} = MAX	XL/XD74LS14		8.6	16	mA
I_{CCL}	V_{CC} = MAX	XL/XD74LS14		12	21	mA

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(3) Not more than one output should be shorted at a time.

6.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C, and over operating free-air temperature range (unless otherwise noted; see Figure 20)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A	Y	R_L = 400 Ω and C_L = 15 pF, or R_L = 2 kΩ and C_L = 15 pF		15	22	ns
t_{PHL}	A	Y	R_L = 400 Ω and C_L = 15 pF, or R_L = 2 kΩ and C_L = 15 pF		15	22	ns

6.7 Typical Characteristics

Data for temperatures below 0°C and above 70°C and supply voltage below 4.75 V and above 5.25 V are applicable for XL/XD74LS14 only.

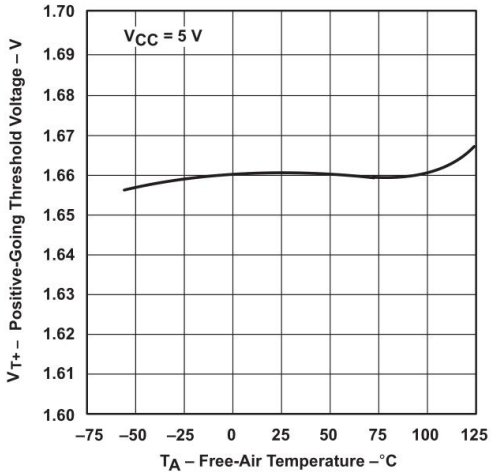


Figure 8. Positive-Going Threshold Voltage vs Free-Air Temperature

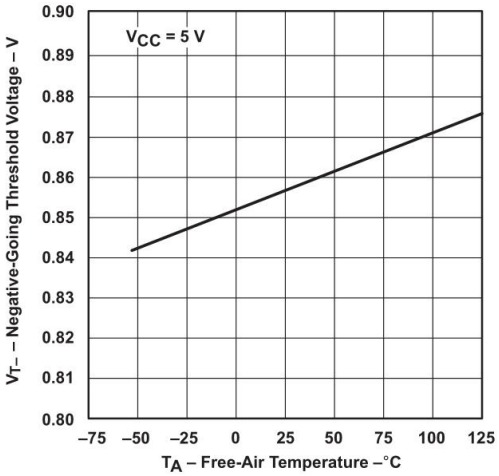


Figure 9. Negative-Going Threshold Voltage vs Free-Air Temperature

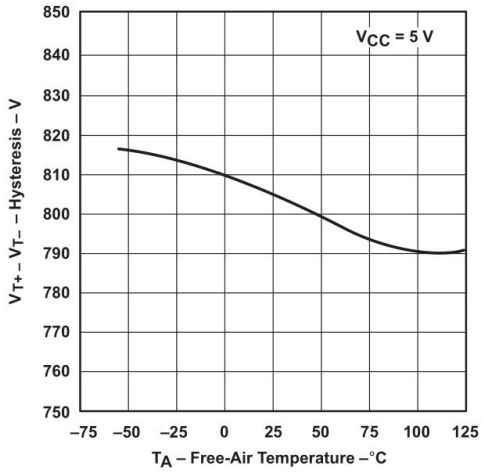


Figure 10. Hysteresis vs Free-Air Temperature

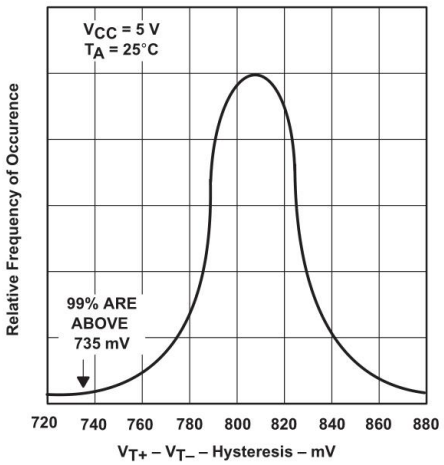


Figure 11. Distribution of Units for Hysteresis

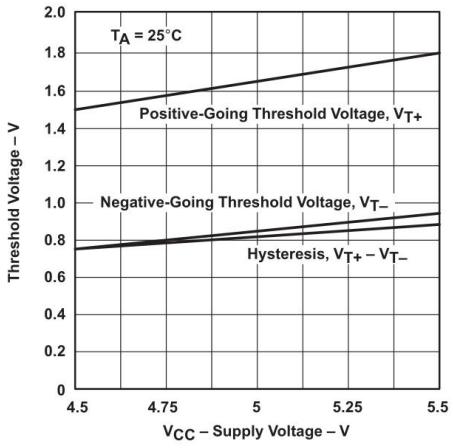


Figure 12. Threshold Voltages and Hysteresis vs Supply Voltage

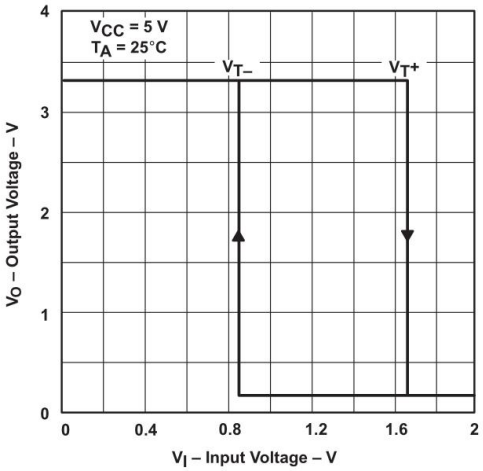


Figure 13. Output Voltage vs Input Voltage

7. PARAMETER MEASUREMENT INFORMATION

Series XL/XD74LS14 Devices

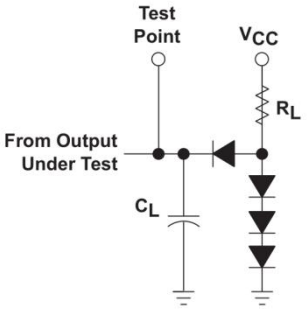


Figure 21. Load Circuit For 2-State Totem-Pole Outputs

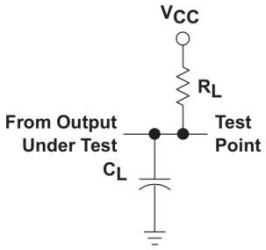


Figure 22. Load Circuit For Open-Collector Outputs

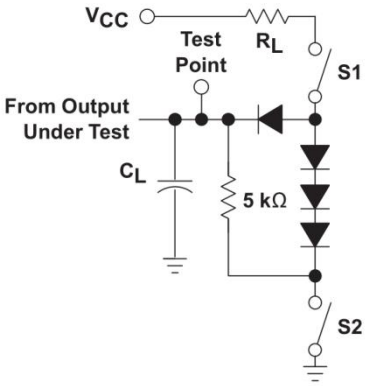


Figure 23. Load Circuit For 3-State Outputs

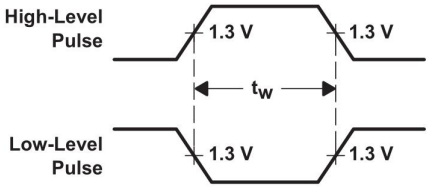


Figure 24. Voltage Waveforms Pulse Durations

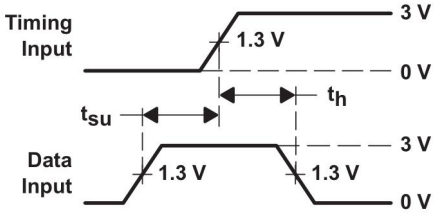


Figure 25. Voltage Waveforms Setup and Hold Times

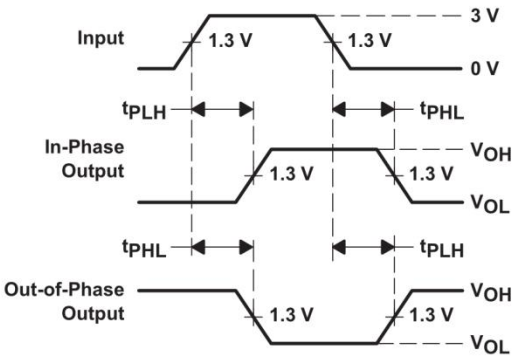
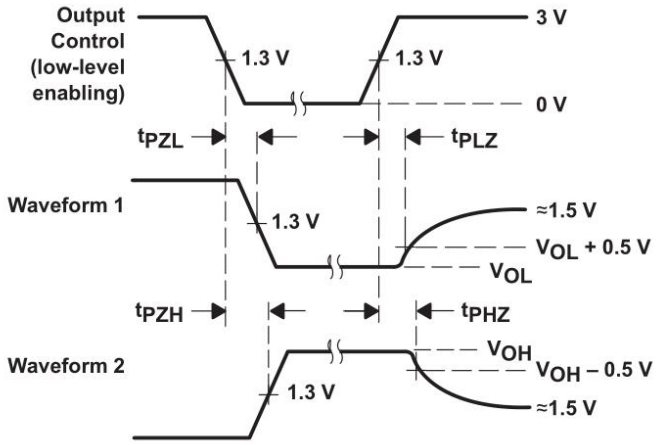


Figure 26. Voltage Waveforms Propagation Delay Times

Series XL/XD74LS14 Devices (continued)



A. C_L includes probe and jig capacitance.

B. All diodes are 1N3064 or equivalent.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. S1 and S2 are closed for t_{PLH}, t_{PHL}, t_{PHZ}, and t_{PLZ}; S1 is open and S2 is closed for t_{PZH}; S1 is closed and S2 is open for t_{PZL}.

E. Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.

F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O \approx 50\ \Omega$, $t_r \leq 1.5$ ns, $t_f \leq 2.6$ ns.

G. The outputs are measured one at a time with one input transition per measurement.

Figure 27. Voltage Waveforms Enable and Disable Times, 3-State Outputs

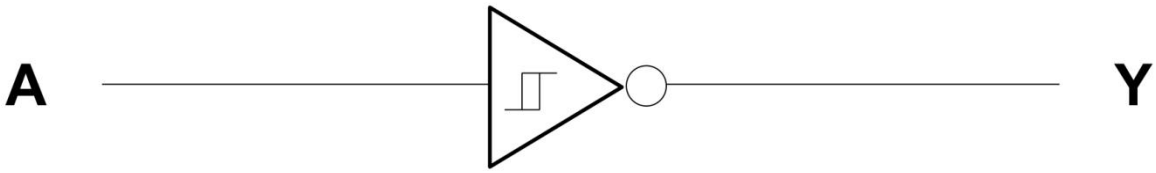
8. DETAILED DESCRIPTION

8.1. Overview

The XL/XD74LS14 Schmitt-Trigger devices contain six independent inverters. They perform the Boolean function Y = A in positive logic.

Schmitt-Trigger inputs are designed to provide a minimum separation between positive and negative switching thresholds. This allows for noisy or slow inputs that would cause problems such as oscillation or excessive current draw with normal CMOS inputs.

8.2. Functional Block Diagram



8.3. Feature Description

The device can operate from very slow transition edge inputs. This device has high noise immunity.

8.4. Device Functional Modes

Table 1 lists the functional modes of the XL/XD74LS14.

Table 1. Function Table

INPUT A	OUTPUT Y
H	L
L	H

9. APPLICATION AND IMPLEMENTATION

Note

Information in the following applications sections is not part of the Xinluda component specification, and Xinluda does not warrant its accuracy or completeness. Xinluda's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1. Application Information

The XL/XD74LS14 device is a Schmitt-Trigger input CMOS device that can be used for a multitude of inverting buffer type functions. The application shown here takes advantage of the Schmitt-Trigger inputs to produce a delay for a logic input.

9.2. Typical Application

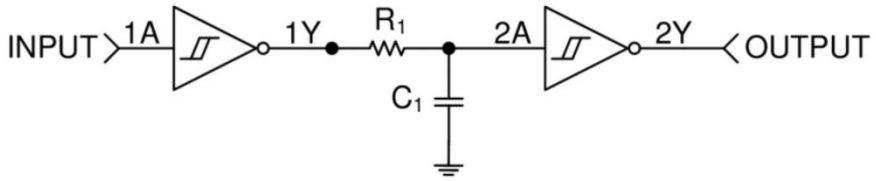


Figure 28. Simplified Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Parallel output drive can create fast edges into light loads, so consider routing and load conditions to prevent ringing.

9.2.2 Detailed Design Procedure

This circuit is designed around an RC network that produces a slow input to the second inverter. The RC time constant (τ) is calculated from: $\tau = RC$.

The delay time for this circuit is from $t_{delay(min)} = -\ln |1 - V_{T+(min)} / V_{CC}| \tau$ to $t_{delay(max)} = -\ln |1 - V_{T+(max)} / V_{CC}| \tau$. It must be noted that the delay is consistent for each device, but because the switching threshold is only ensured between the minimum and maximum value, the output pulse length varies between devices. These values must be calculated by using the minimum and maximum ensured V_{T+} values in the *Electrical Characteristics*.

The resistor value must be chosen such that the maximum current to and from the SNx414/SNx4LS14 is 8 mA at 5-V V_{CC}.

Typical Application (continued)

9.2.3 Application Curves

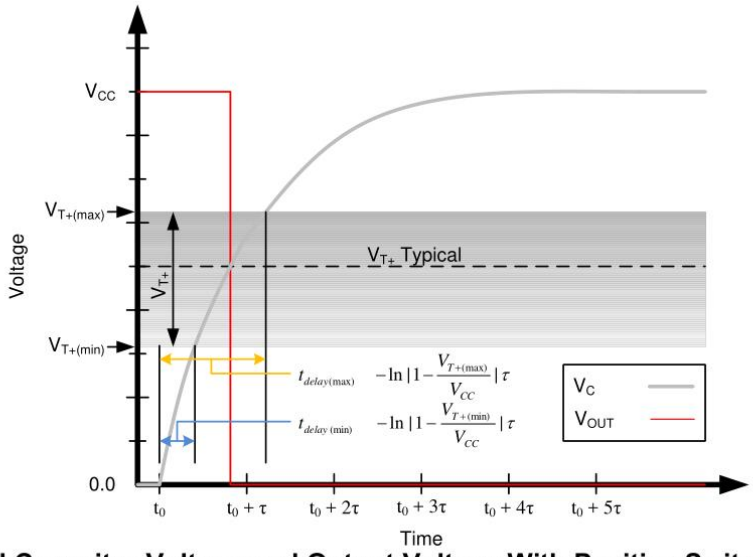


Figure 29. Ideal Capacitor Voltage and Output Voltage With Positive Switching Threshold

9.3. System Examples

Here are some examples of various applications using the XL/XD74LS14 device.

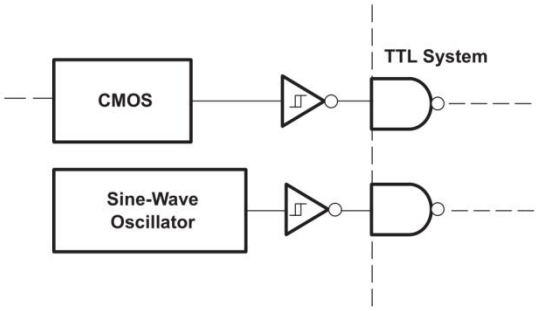


Figure 30. TTL System Interface For Slow Input Waveforms

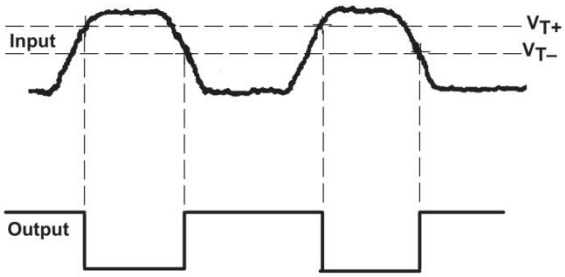


Figure 31. Pulse Shaper

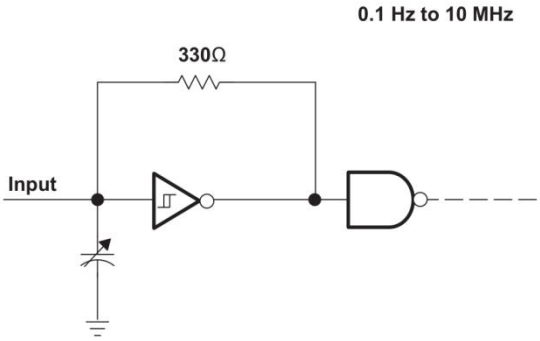


Figure 32. Multivibrator

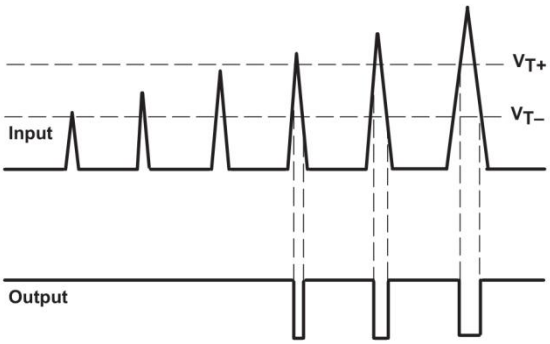
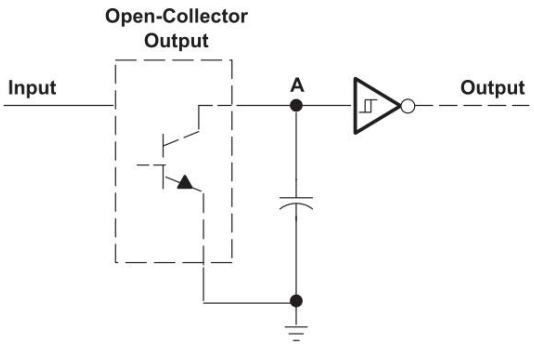


Figure 33. Threshold Detector



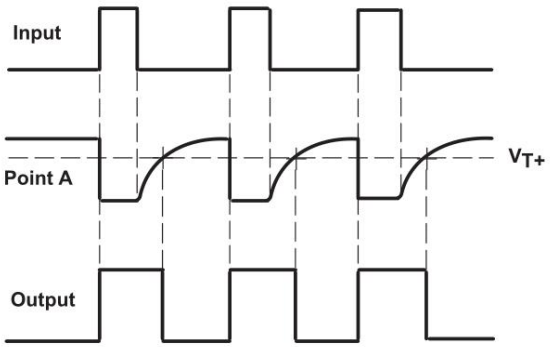


Figure 34. Pulse Stretcher

10. POWER SUPPLY RECOMMENDATIONS

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. The V_{CC} terminal must have a good bypass capacitor to prevent power disturbance. TI recommends using a 0.1-µF capacitor on the V_{CC} terminal, and must be placed as close as possible to the pin for best results.

11. LAYOUT

11.1. Layout Guidelines

When using multiple bit logic devices, inputs must never float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such inputs must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or V_{CC}, whichever makes more sense or is more convenient. Floating outputs are generally acceptable, unless the part is a transceiver.

11.2. Layout Example

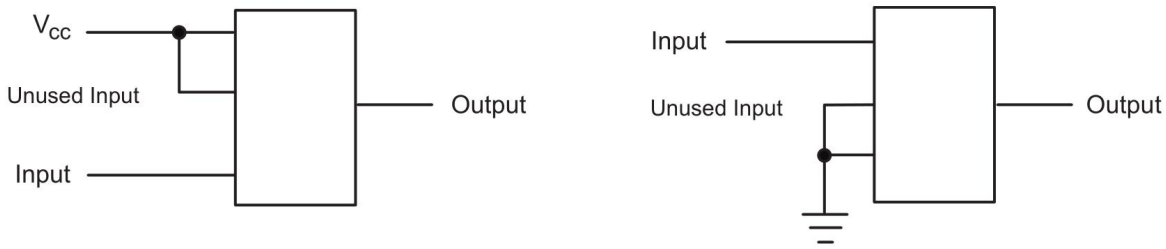


Figure 35. Layout Diagram

12. ORDERING INFORMATION

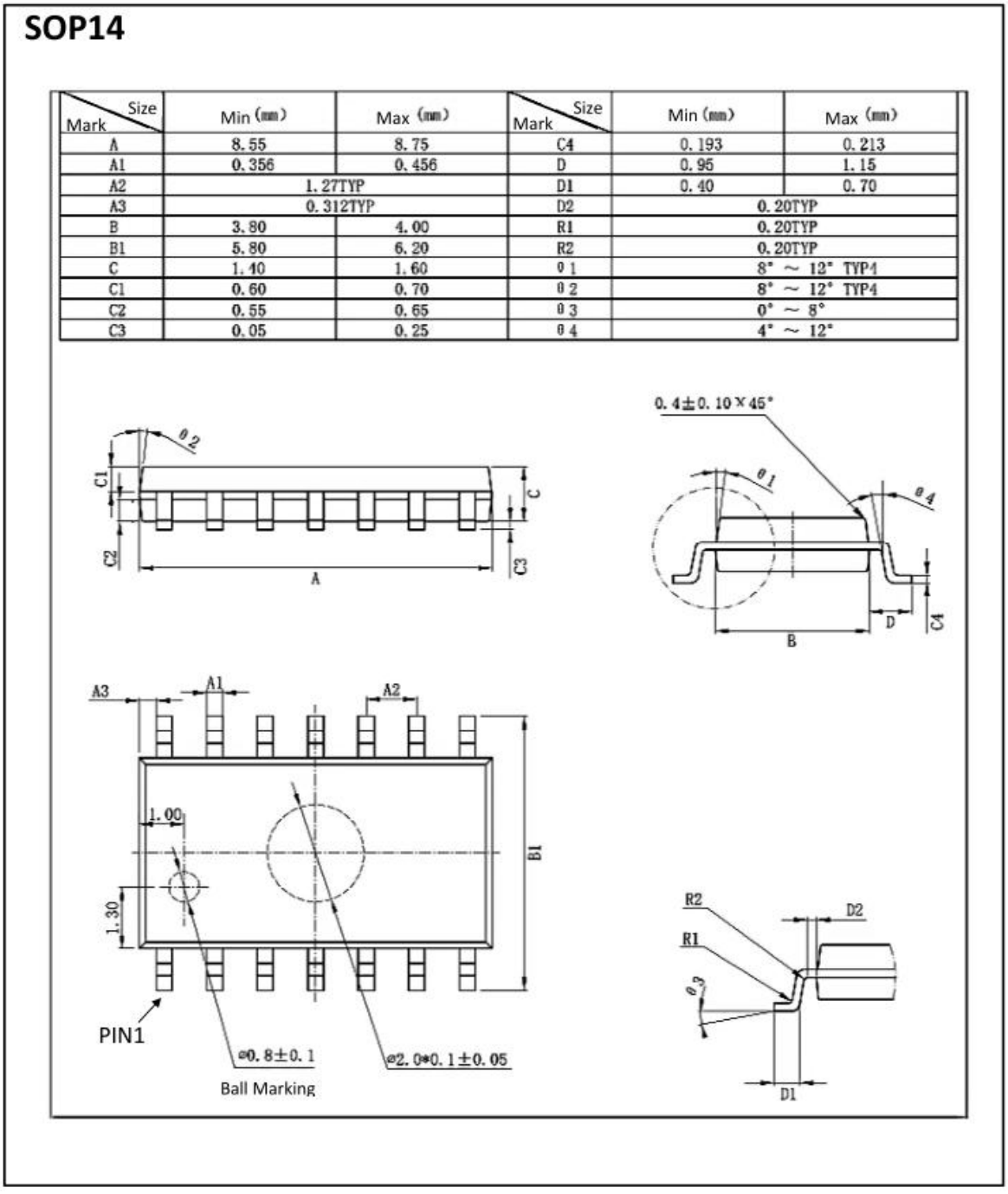
Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL74LS14	XL74LS14	SOP14	8.75 * 4.00	-0 to 70	MSL3	T&R	2500
XD74LS14	XD74LS14	DIP14	19.05 * 6.35	-0 to 70	MSL3	Tube 25	1000

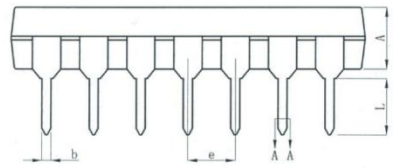
13. DIMENSIONAL DRAWINGS

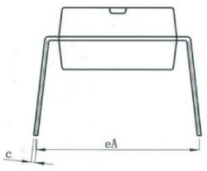
SOP14

Mark \ Size	Min (mm)	Max (mm)	Mark \ Size	Min (mm)	Max (mm)
A	8.55	8.75	C4	0.193	0.213
A1	0.356	0.456	D	0.95	1.15
A2	1.27TYP		D1	0.40	0.70
A3	0.312TYP		D2	0.20TYP	
B	3.80	4.00	R1	0.20TYP	
B1	5.80	6.20	R2	0.20TYP	
C	1.40	1.60	θ1	8° ~ 12° TYP4	
C1	0.60	0.70	θ2	8° ~ 12° TYP4	
C2	0.55	0.65	θ3	0° ~ 8°	
C3	0.05	0.25	θ4	4° ~ 12°	

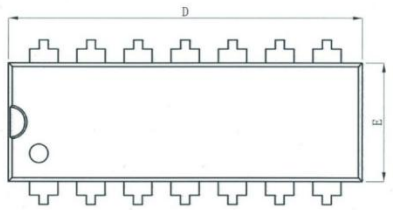


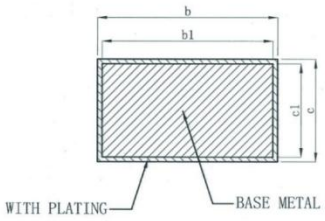
DIP14





symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	----	0.53
b1	0.43	0.46	0.49
c	0.25	----	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	----	----





SECTION A-A