TPS51386 4.5-V to 24-V Input, 8-A Synchronous Buck Converter With Latched OVP/ UVP, Adjustable Soft Start, and PSM/OOA Modes

1 Features

- 4.5-V to 24-V input voltage range
- 0.6-V to 5.5-V output voltage range
- Integrated 22-mΩ and 11-mΩ MOSFETs
- Support 8-A continuous I_{OUT}
- 84-µA low quiescent current
- ±1% reference voltage (0.6 V) at 25°C
- ±1.5% reference voltage (0.6 V) at –40°C to 125°C
- 600-kHz switching frequency
- D-CAP3™ control mode for fast transient response
- Supports POSCAP and all MLCC output capacitor
- Adjustable soft start and internal 1-ms soft start
- Selectable PSM and Out-of-Audio™ (OOA) mode under light load and supports on-the-fly change
- Large duty operation support
- Power-good indicator to monitor output voltage
- Latched output OV and UV protection
- Non-latched UVLO and OT protection
- Cycle-by-cycle overcurrent protection
- Built-in output discharge feature
- Small 2.00-mm × 3.00-mm HotRod™ QFN package

2 Applications

- Notebook and PC computers
- Ultrabook, tablet computers
- TV and STB, point-of-load (POL)
- Distributed power systems

3 Description

The TPS51386 is a monolithic, 8-A, synchronous buck converter with adaptive on-time D-CAP3 control mode. Integrated low $R_{DS(on)}$ power MOSFETs enable high efficiency and offer ease-of-use with minimum external component count for space-constrained power systems. Features include an accurate reference voltage, fast load transient response, auto-skip mode operation for light load efficiency, OOA light load operation with > 25-kHz switching frequency, D-CAP3 control mode with good line, load regulation, and does not require external compensation.

The TPS51386 provides complete protection OVP, UVP, OCP, OTP, and UVLO. The device is a combined power-good signal and output discharge function.

The TPS51386 supports both internal and external soft-start time option. The device has the internal fixed soft-start time 1 ms. If the application needs longer soft-start time, the external SS pin can be used to achieve longer soft-start time by connecting the external capacitor.

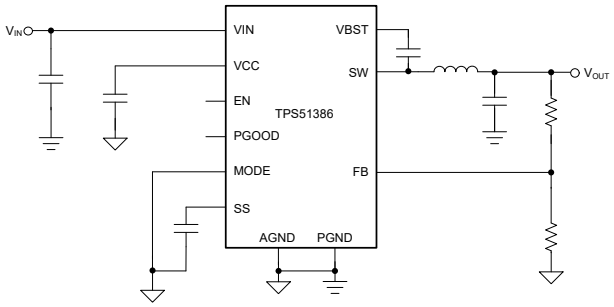
The TPS51386 are available in a thermally enhanced 12-pin QFN package and are designed to operate from –40°C to 125°C junction temperature.

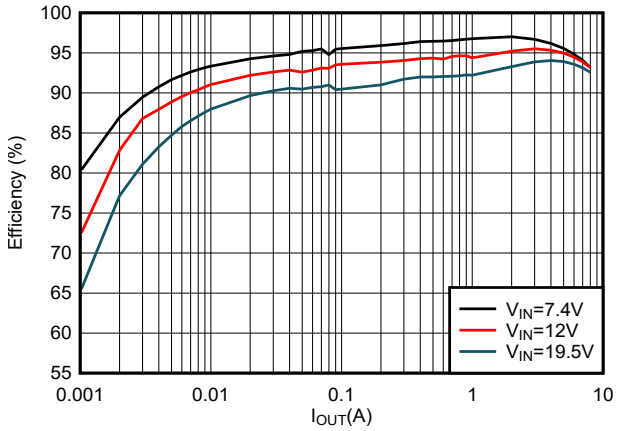
Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS51386	RJN (VQFN-HR, 12)	2.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

Typical Application





Efficiency Curve, V_{OUT} = 5.1 V, PSM Mode

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4 Revision History

DATE	REVISION	NOTES
August 2023	*	Initial release

5 Pin Configuration and Functions

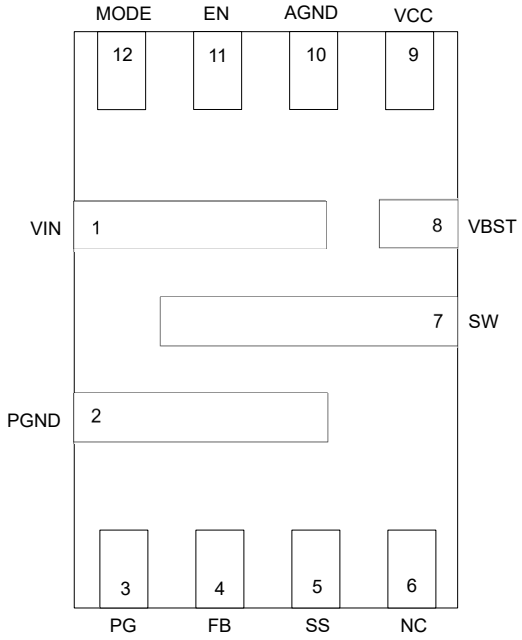


Figure 5-1. RJN Package 12-Pin VQFN-HR Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	1	P	Input voltage supply pin for the control circuitry. Connect the input decoupling capacitors between VIN and PGND.
PGND	2	G	Power ground terminal for the internal power FET.
PG	3	O	Open Drain Power-Good Indicator. This pin is asserted low if output voltage is out of PG threshold, overvoltage or if the device is under thermal shutdown, EN shutdown or during soft start.
FB	4	I	TPS51386 uses FB pin to regulate output voltage via feedback resistor divider network.
SS	5	O	Soft-start time selection pin for TPS51386. Connecting an external capacitor sets the soft-start time and if no external capacitor is connected, the soft-start time is approximately 1 ms.
NC	6	-	No connect pin
SW	7	O	Switch node terminal. Connect the output inductor to this pin.
VBST	8	I	Supply input for the high-side MOSFET gate drive. Connect the bootstrap capacitor between VBST and SW.
VCC	9	O	5-V internal VCC LDO output. This pin supplies voltage to the internal circuitry and gate driver. Bypass this pin with a 1-µF capacitor.
AGND	10	G	Ground of internal analog circuitry. Connect AGND to PGND at a single point close to AGND.
EN	11	I	Enable pin of buck converter. EN pin is a digital input pin, pull up to enable the converter, pull down to disable. Internal pulldown if EN pin is floating.
MODE	12	I	Mode selection pin. Connect MODE pin to VCC, or pull above 0.8 V for OOA mode operation, connect MODE to AGND or float for Power Save Mode. Internal pulldown if MODE pin is floating.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	28	V
Input voltage	VBST	–0.3	34	
Input voltage	VBST - SW	–0.3	6	V
Input voltage	EN, FB, MODE, SS	–0.3	6	V
Output voltage	SW (10ns transient)	–4	28	
Output voltage	SW	–1.0	28	V
Output voltage	PG	–0.3	6	V
Output voltage	VCC	–0.3	6	V
Voltage	PGND, AGND	–0.3	0.3	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage range	VIN	4.5		24	V
Input voltage range	VBST	–0.1		29.5	V
Input voltage range	VBST – SW	–0.1		5.5	V
Input voltage range	EN, FB, MODE, SS	–0.3		5.5	V
Output voltage range	SW	–1.0		24	V
Output voltage range	PG, VCC	–0.1		5.5	V
Output current	IOUT			8	A
T_J		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		DEVICE		UNIT
		RJNR (QFN, JEDEC)	RJNR (QFN, TI EVM)	
		12 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.7	37.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.1	Not Applicable (2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.7	Not Applicable (2)	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	3.7	°C/W

6.4 Thermal Information (continued)

THERMAL METRIC[1]		DEVICE		UNIT
		RJNR (QFN, JEDEC)	RJNR (QFN, TI EVM)	
		12 PINS	12 PINS	
ψ_{JB}	Junction-to-board characterization parameter	18.4	18.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The thermal simulation setup is not applicable to a TI EVM layout.

6.5 Electrical Characteristics

MODE connected to AGND, V_{EN} = 3.3V; T_J = –40°C to +125°C, Typical values are at T_J = 25°C and V_{VIN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (VIN)						
VIN	Input voltage range	VIN	4.5		24	V
I_{VIN}	VIN Supply Current (Quiescent)	No load, V_{EN} = 3.3 V, non-switching		84		µA
I_{INSDN}	VIN Shutdown Current	No load, V_{EN}= 0 V, PG open		3.7		µA
UVLO						
$V_{VCC\ UVLO\_R}$	V_{CC} Under-Voltage Lockout	V_{VCC} rising		4.2	4.42	V
$V_{VCC\ UVLO\_F}$	V_{CC} Under-Voltage Lockout	V_{VCC} falling	3.65	3.85		V
$V_{VCC\ UVLO\_H}$	V_{CC} Under-Voltage Lockout	Hysteresis V_{CC} voltage		350	650	mV
ENABLE (EN), MODE						
V_{EN_R}	EN Threshold High-level	V_{EN} rising		1.31	1.5	V
V_{EN_F}	EN Threshold Low-level	V_{EN} falling	1.0	1.13		V
V_{EN_H}	EN Threshold Low-level	Hysteresis		180		mV
I_{EN}	EN Pull down Current	V_{EN} = 0.8 V	1.3	2.3		uA
$V_{IL;MODE}$	Low-Level Input Voltage at MODE Pin		0.4			V
$V_{IH;MODE}$	High-Level Input Voltage at MODE Pin				0.8	V
I_{MODE}	MODE Pull down Current	V_{MODE} = 0.8 V	1.3	2.3	3.5	uA
VCC						
V_{VCC}	VCC Output Voltage	V_{VIN} > 5.2 V, I_{VCC} ≤ 1 mA	4.85	5	5.15	V
FEEDBACK VOLTAGE (FB)						
V_{FB_REG}	Feedback regulation voltage	T_J= 25 °C	594	600	606	mV
	Feedback regulation voltage	–40 °C ≤ T_J ≤ 125°C	591	600	609	mV
DUTY CYCLE and FREQUENCY CONTROL						
f_{SW}	Switching frequency	CCM operation		600		kHz
$t_{ON(min)}$	Minimum ON pulse width[1]	T_J = 25°C		65	75	ns
$t_{OFF(min)}$	Minimum OFF pulse width[1]	T_J = 25°C			190	ns
OOA FUNCTION						
t_{OOA}	OOA operation period	V_{MODE} = V_{VCC}		30	50	µs
SOFT-START (SS)						
t_{SS}	Internal fixed soft start		0.55	1	1.35	ms
I_{SS}	Soft Start Charge Current		4	5	6	µA
POWER SWITCHES (SW)						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	T_J = 25°C		22		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	T_J = 25°C		11		mΩ
CURRENT LIMIT						
I_{OCL}	Low-side valley current limit	Valley current limit on LS FET	9.5	11	12.5	A
I_{NOCL}	Low-side negative current limit	Sinking current limit on LS FET, OOA operation		3.9		A
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						

6.5 Electrical Characteristics (continued)

MODE connected to AGND, V_{EN} = 3.3V; T_J = –40°C to +125°C, Typical values are at T_J = 25°C and V_{VIN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP}	OVP Trip Threshold		117	120	123	%
t_{OVPDLY}	OVP Prop deglitch			20		µs
t_{OVPDLY}	OVP latch-off Prop deglitch			256		µs
V_{UVP}	UVP Trip Threshold		55	60	65	%
t_{UVPDLY}	UVP Prop deglitch			256		µs
POWER GOOD (PG)						
t_{PGDLY}	PG Start-Up delay	PG from low to high		500		µs
t_{PGDLY}	PG delay time when V_{FB} rising (fault)	PG from high to low		20		µs
t_{PGDLY}	PG delay time when V_{FB} falling (fault)	PG from high to low		28		µs
V_{PGTH}	PG Threshold when V_{FB} falling (fault)	V_{FB} falling (fault), percentage of V_{FB}	79	85	89	%
V_{PGTH}	PG Threshold when V_{FB} rising (good)	V_{FB} rising (good), percentage of V_{FB}	86	90	94	%
V_{PGTH}	PG Threshold when V_{FB} rising (fault)	V_{FB} rising (fault), percentage of V_{FB}	116	120	124	%
V_{PGTH}	PG Threshold when V_{FB} falling (good)	V_{FB} falling (good), percentage of V_{FB}	109	115	119	%
I_{PGMAX}	PG Sink Current	V_{PG} = 0.5 V		50		mA
I_{PGLK}	PG Leak Current	V_{PG} = 5.5 V			1	µA
OUTPUT DISCHARGE						
R_{DIS}	Discharge resistance	T_J = 25 °C, V_{EN} = 0 V		160		Ω
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold(1)			165		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis (1)			20		°C

(1) Specified by design. Not production tested

6.6 Typical Characteristics

V_{IN} = 12 V, T_J = –40°C to 125°C, unless otherwise specified.

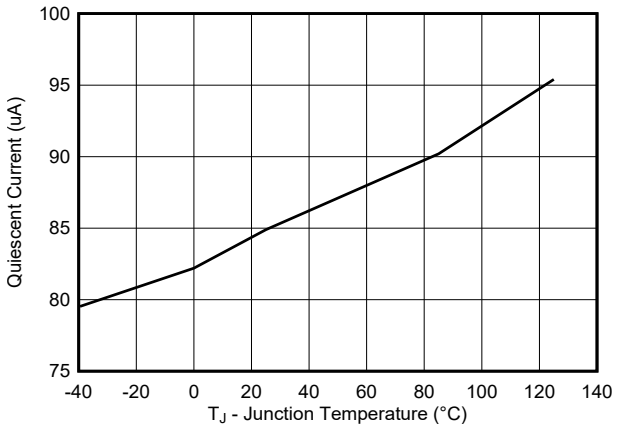


Figure 6-1. Quiescent Current vs Temperature

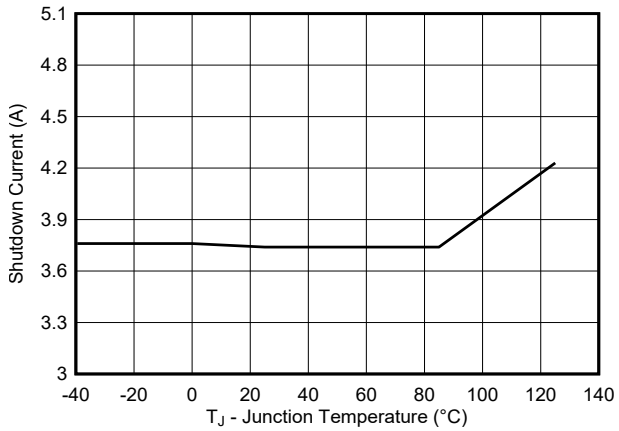


Figure 6-2. Shutdwon Current vs Temperature

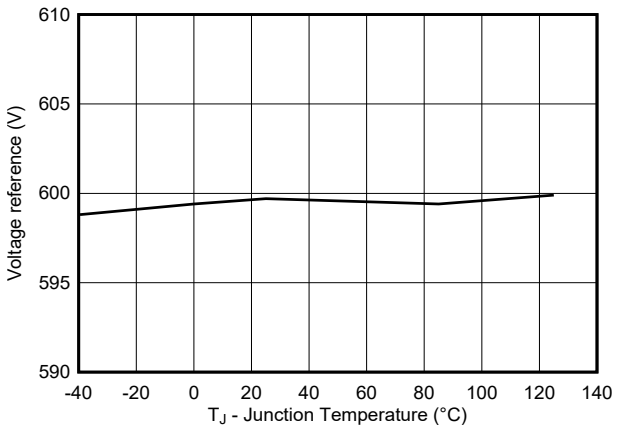


Figure 6-3. Voltage Reference vs Temperature

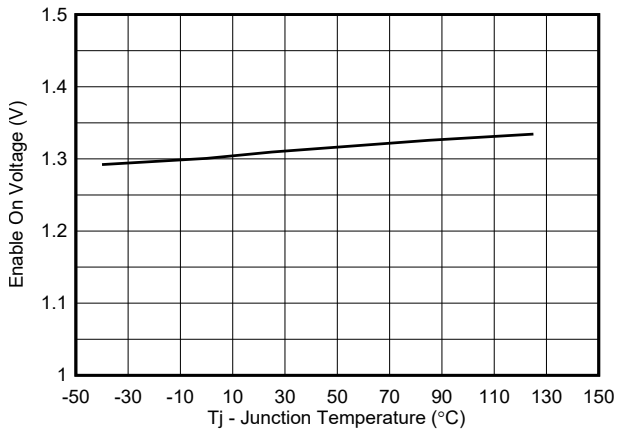


Figure 6-4. Enable On Voltage vs Temperature

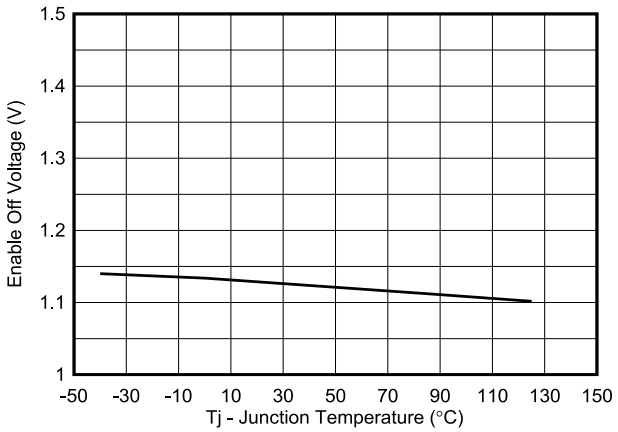


Figure 6-5. Enable Off Voltage vs Temperature

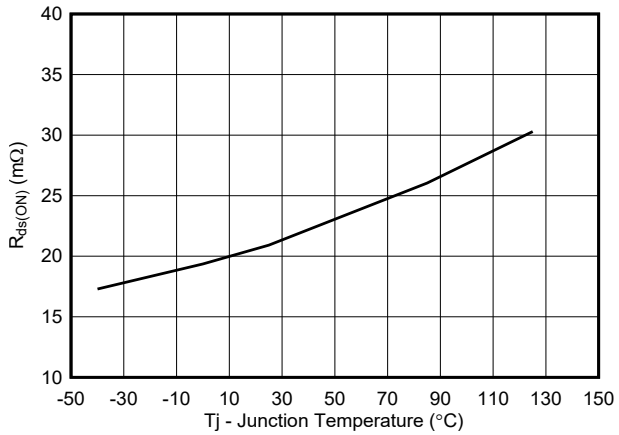


Figure 6-6. High-side $R_{DS(on)}$ vs Temperature

6.6 Typical Characteristics (continued)

V_{IN} = 12 V, T_J = –40°C to 125°C, unless otherwise specified.

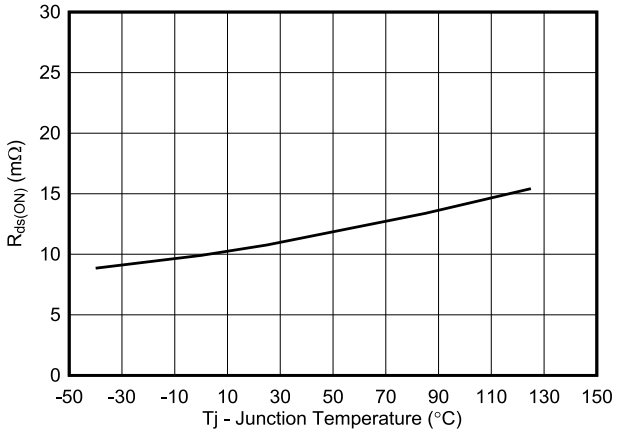


Figure 6-7. Low-side $R_{DS(on)}$ vs Temperature

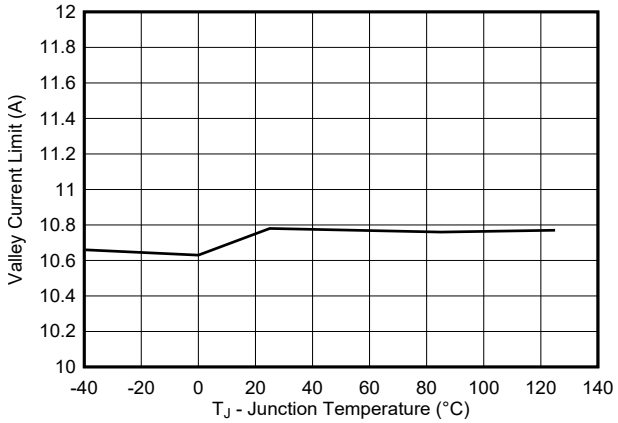


Figure 6-8. Valley Current Limit vs Temperature

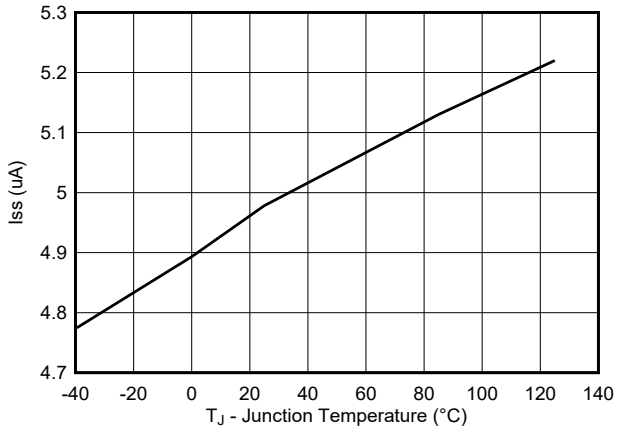


Figure 6-9. Iss vs Temperature

7 Detailed Description

7.1 Overview

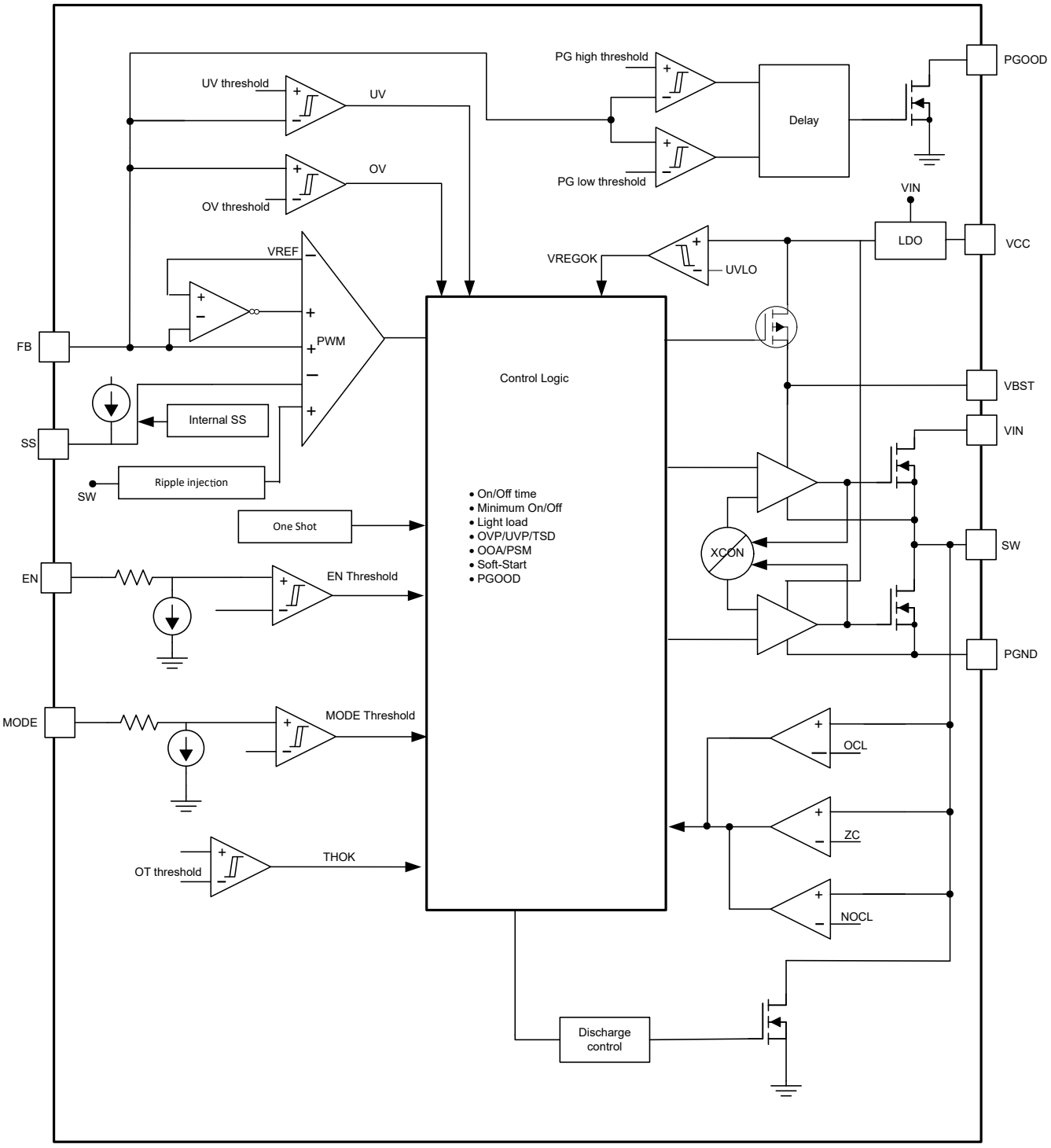
The TPS51386 is an 8-A, integrated FET, synchronous buck converter which operates from 4.5-V to 24-V input voltage (VIN), and the output is from 0.6 V to 5.5 V. The proprietary D-CAP3 control mode enables low external component count, ease of design, optimization of the power design for cost, size and efficiency.

The key feature of the TPS51386 is the ULQ™ (Ultra Low Quiescent) extended battery life feature to enable low-bias current DC/DC converter. The ULQ extended battery life feature is extremely beneficial for long battery life in low power operation.

The device employs D-CAP3 control mode control that provides fast transient response with no external compensation components and an accurate feedback voltage. The control topology provides seamless transition between CCM operating mode at higher load condition and DCM operation at lighter load condition. Eco-mode allows the TPS51386 to maintain high efficiency at light load. OOA (Out-of-Audio™) mode makes switching frequency above audible frequency larger than 25 kHz, even there is no loading at output side.

The TPS51386 is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Operation and D-CAP3™ Control Mode

The TPS51386 operates using the adaptive on-time PWM control with a proprietary D-CAP3 control mode, which enables low external component count with a fast load transient response while maintaining a good output voltage accuracy. At the beginning of each switching cycle, the high side MOSFET is turned on for an on-time set by an internal one shot timer. This on-time is set based on the converter input voltage, output voltage, and

the pseudo-fixed frequency, hence this type of control topology is called an adaptive on-time control. The one shot timer resets and turns on again after the feedback voltage (V_{FB}) falls below the internal reference voltage (V_{REF}). An internal ramp is generated which is fed to the FB pin to simulate the output voltage ripple. This action enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for D-CAP3 control mode topology.

The TPS51386 includes an error amplifier that makes the output voltage very accurate. For any control topology that is compensated internally, there is a range of the output filter it can support. The output filter used is a low pass L-C circuit. This L-C filter has double pole that is described in the following equation.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain. The low frequency L-C double pole has a 180 degree in phase. At the output filter frequency, the gain rolls off at a –40dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40dB to –20dB per decade and increases the phase to 90 degree one decade above the zero frequency. The internal ripple injection high frequency zero is optimized to provide fast transient response performance and also give an consideration to meet the stability requirement with typical external L-C filter. The inductor and capacitor selected for the output filter must be such that the double pole is located close enough to the high-frequency zero so that the phase boost provided by this high-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system must usually be targeted to be less than one-fifth of the switching frequency (F_{SW}).

7.3.2 VCC LDO

The VCC pin is the output of the internal 5-V linear regulator that creates the bias for all the internal circuitry and MOSFET gate drivers. The VCC pin must be bypassed with a minimum 1-µF, 10-V X5R rated capacitor. The UVLO circuit monitors the VCC pin voltage and disables the output when VCC falls below the UVLO threshold.

7.3.3 Soft Start

The TPS51386 has an internal 1-ms soft start, and also an external SS pin is provided for setting higher soft-start time if needed. When the EN pin becomes high, the soft-start function begins ramping up the reference voltage to the PWM comparator.

If the application needs a larger soft-start time, this soft-start time can be set by connecting a capacitor on SS pin. When the EN pin becomes high, the soft-start charge current (I_{SS}) begins charging the external capacitor (C_{SS}) connected between SS and AGND. The devices tracks the lower of the internal soft-start voltage or the external soft-start voltage as the reference. The equation for the soft-start time (T_{SS}) is shown in the following equation:

$$T_{SS} = \frac{C_{SS}(nF) \times V_{REF}(V) \times 1.4}{I_{SS(\mu A)}} \quad (2)$$

where

- V_{ref} is 0.6 V and I_{SS} is 5 µA
- 1.4 is typical value of correlation factor

7.3.4 Enable Control

The EN pin controls the turn-on and turn-off of the device. When EN pin voltage is above the turn-on threshold which is around 1.31 V, the device starts switching and when the EN pin voltage falls below the turn-off threshold which is around 1.13V it stops switching.

7.3.5 Power Good

The Power Good (PGOOD) pin is an open drain output. After the FB pin voltage is between 90% and 115% of the internal reference voltage (V_{REF}) the PGOOD is de-asserted and floats after a 500-µs de-glitch time. TI recommends a pullup resistor of 100 kΩ to pull it up to VCC. The PGOOD pin is pulled low when the FB pin

voltage is lower than V_{UVP} or greater than V_{OVP} threshold or in an event of thermal shutdown or during the soft-start period.

7.3.6 Overcurrent Protection and Undervoltage Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. During the on time of the high-side FET switch, the switch current increases at a linear rate determined by input voltage, output voltage, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the measured drain to source voltage of the low-side FET is above the voltage proportional to current limit, the low side FET stays on until the current level becomes lower than the OCL level which reduces the output current available. When the current is limited the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 60% of the target voltage, the UVP comparator detects it and shuts down the device after a wait time of 256 us. In this type of valley detect control, the load current is higher than the OCL threshold by one half of the peak to peak inductor ripple current. This protection is a latch function, fault latching can be re-set by EN going low or VIN power cycling.

7.3.7 UVLO Protection

Undervoltage Lock Out protection (UVLO) monitors the internal VCC regulator voltage. When the VCC voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.8 Overvoltage Protection

TPS51386 detects overvoltage and undervoltage conditions by monitoring the feedback voltage (VFB). When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and output is discharged after a wait time of 20 us. When the OV fault comparator has been tripped for 256 us, the part latches off. When the overvoltage condition is removed, output remains latched until EN is toggled to low then high, or the power cycling VIN.

7.3.9 Output Voltage Discharge

TPS51386 has a 160-ohm discharge switch that discharges the output V_{OUT} through the SW pin during any event of fault like output overvoltage, output undervoltage, TSD, or if VCC voltage is below the UVLO and when the EN pin voltage (V_{EN}) is below the turn-on threshold.

7.3.10 Thermal Shutdown

The device monitors the internal die temperature. If this temperature exceeds the thermal shutdown threshold value (T_{SDN} typically 165°C) the device shuts off. This protection is a non-latch protection. The device re-starts switching when the temperature goes below the thermal shutdown threshold and 20°C hysterisis.

7.4 Device Functional Modes

7.4.1 MODE Pin

TPS51386 has a MODE pin that can be used to toggle mode of the device by pulling it high (> 0.8 V) or low (< 0.4 V). When the MODE pin is pulled high, the pin enables the converter to operate in Out-of-Audio (OOA) mode. When the MODE pin is pulled low or float, the converter goes into Power Save Mode (PSM). The MODE pin can be toggled dynamically, even when the converter is in operation.

7.4.2 Out-of-Audio™ Mode

Out-of-Audio (OOA) mode is a unique control feature, If the MODE pin is selected to operate in OOA mode, when the device works at light load, the minimum switching frequency is above 25 kHz which avoids the audible noise in the system.

7.4.3 Power Save Mode (PSM)

The TPS51386 can be placed in power save mode by floating the MODE pin or pulling the MODE pin low (< 0.4 V), which is helpful to improve efficiency at light load.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The schematic shows a typical application for TPS51386. This design converts an input voltage range of 6 V to 24 V down to 5.1 V with a maximum output current of 8 A.

8.2 Typical Application

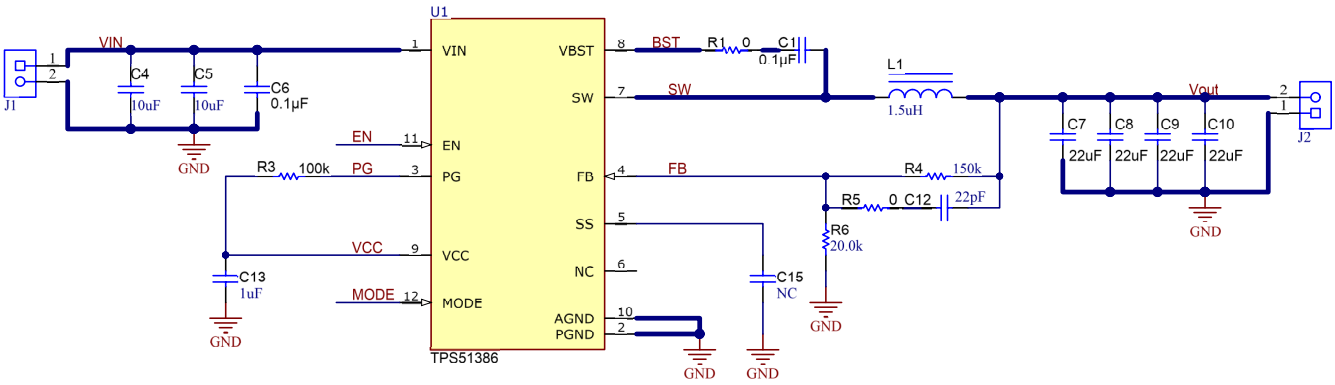


Figure 8-1. Application Schematic

8.2.1 Design Requirements

Table 8-1. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage			5.1		V
I_{OUT}	Output current				8	A
V_{IN}	Input voltage		6	19.5	24	V
$V_{OUT(ripple)}$	Output voltage ripple	V_{IN} = 19.5 V, I_{OUT} = 8 A		50		$mV_{(P-P)}$
F_{SW}	Switching frequency	V_{IN} = 19.5 V, I_{OUT} = 8 A		600		kHz
Operating Mode		Float MODE pin (default)		PSM		
T_A	Ambient temperature			25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 External Component Selection

8.2.2.1.1 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor must have a ripple current rating higher than the inductor ripple current. See Table 8-2 for recommended inductor values.

The RMS and peak currents through the inductor can be calculated using Equation 3 and Equation 4. Make sure that the inductor is rated to handle these currents.

$$I_{L(rms)} = \sqrt{\left(I_{OUT}^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times L_{OUT} \times F_{SW}}\right)\right)} \quad (3)$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{OUT(ripple)}}{2} \quad (4)$$

During transient, short-circuit conditions the inductor current can increase up to the current limit of the device, so choose an inductor with a saturation current higher than the peak current under current limit condition.

8.2.2.1.2 Output Capacitor Selection

After selecting the inductor the output capacitor must be optimized. In D-CAP3 control mode, the regulator reacts within one cycle to the change in the duty cycle so the good transient performance can be achieved without needing large amounts of output capacitance. Table 8-2 lists the recommended output capacitance range.

Ceramic capacitors have very low ESR, otherwise the maximum ESR of the capacitor must be less than $V_{OUT(ripple)}/I_{OUT(ripple)}$

Table 8-2. Recommended Component Values

V_{OUT} (V)	R_{LOWER} (Kohm)	R_{UPPER} (Kohm)	F_{sw} (kHz)	Typical L_{OUT} (µH)	$C_{OUT(Range)}$ (µF)	$C_{FF(Range)}$ (pF)
1	30	20	600	0.68/0.82	44-500	-
1.8	20	40	600	1.0/1.2	44-500	0-100
3.3	20	90	600	1.5/2.2	44-500	0-100
5	20	147	600	1.5/2.2	44-500	0-100

8.2.2.1.3 Input Capacitor Selection

The minimum input capacitance required is given in Equation 5.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{INripple} \times V_{IN} \times F_{SW}} \quad (5)$$

TI recommends using a high quality X5R or X7R input decoupling capacitors of 22 µF on the input voltage pin. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. The input ripple current is calculated by Equation 6 below:

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{\left(V_{IN(min)} - V_{OUT}\right)}{V_{IN(min)}}} \quad (6)$$

8.2.3 Application Curves

V_{IN} = 19.5 V, T_a = 25°C unless otherwise specified.

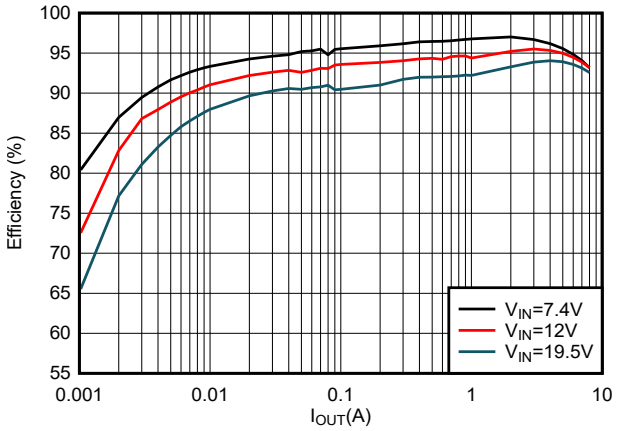


Figure 8-2. Efficiency, PSM Mode

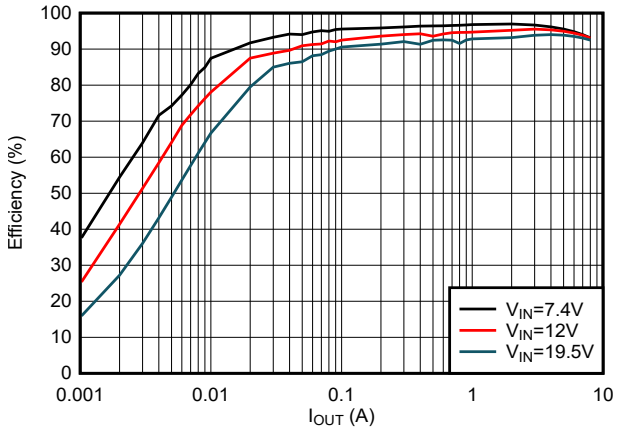


Figure 8-3. Efficiency, OOA Mode

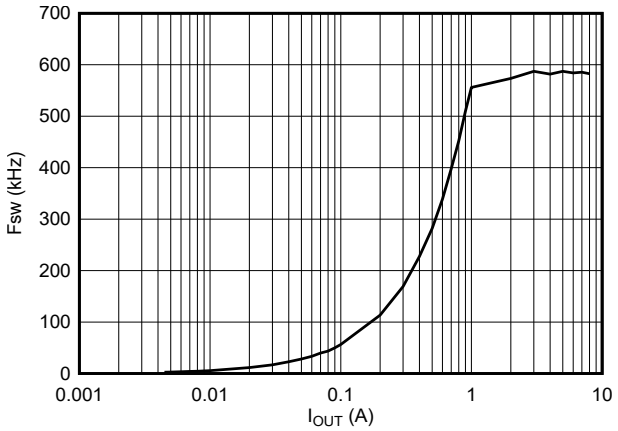


Figure 8-4. Switching Frequency, PSM Mode

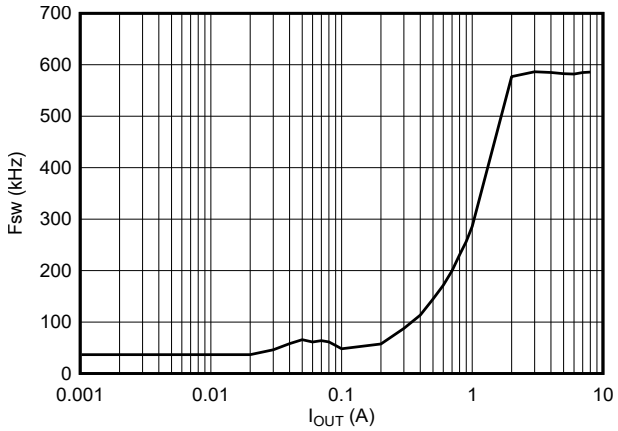


Figure 8-5. Switching Frequency, OOA Mode

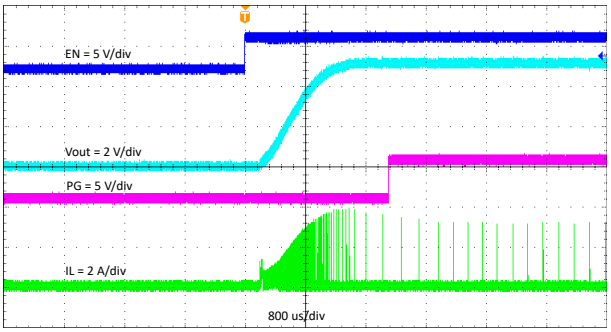


Figure 8-6. Start-Up Relative to EN Rising, Iout = 0.01 A, PSM Mode

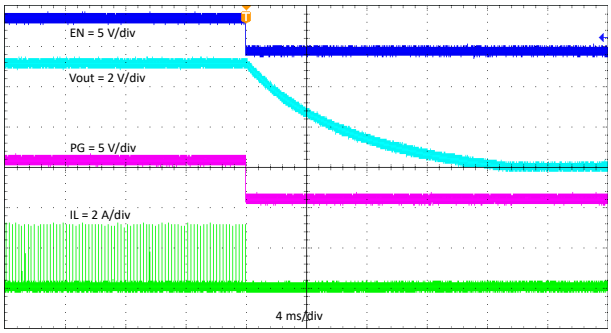


Figure 8-7. Shutdown Relative to EN Falling, Iout = 0.01 A, PSM Mode

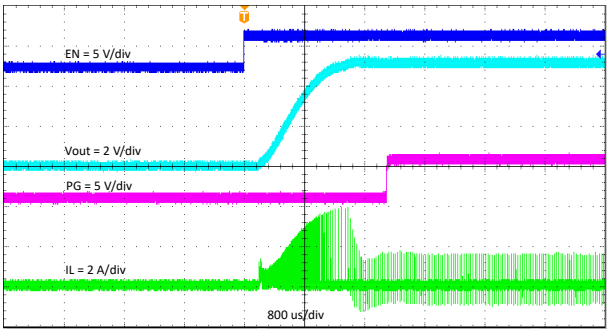


Figure 8-8. Start-Up Relative to EN Rising, Iout = 0.01 A, OOA Mode

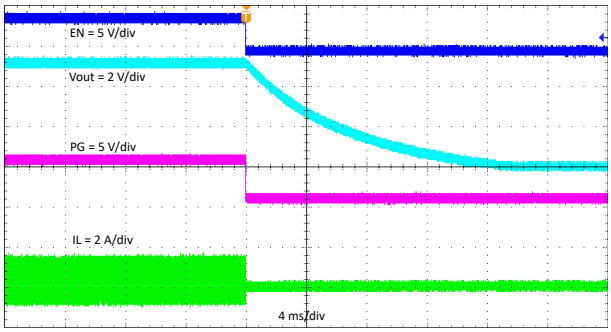


Figure 8-9. Shutdown Relative to EN Falling, Iout = 0.01 A, OOA Mode

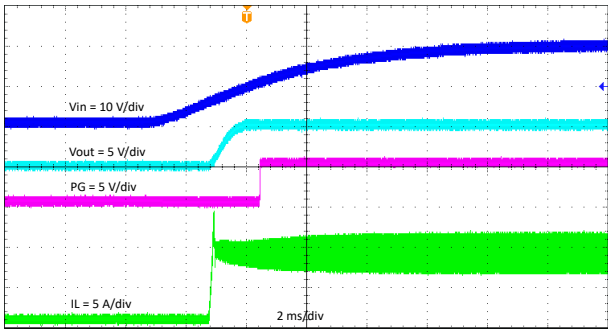


Figure 8-10. Start-Up Relative to Vin Rising, Iout = 8 A

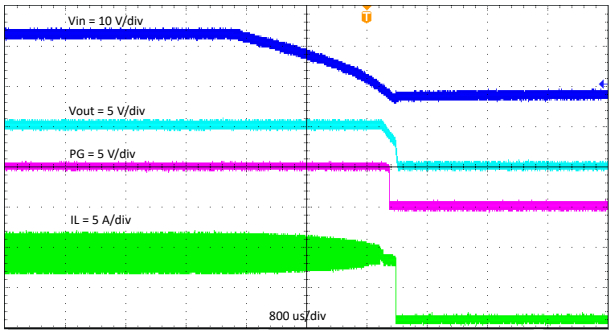


Figure 8-11. Shutdown Relative to Vin Falling, Iout = 8 A

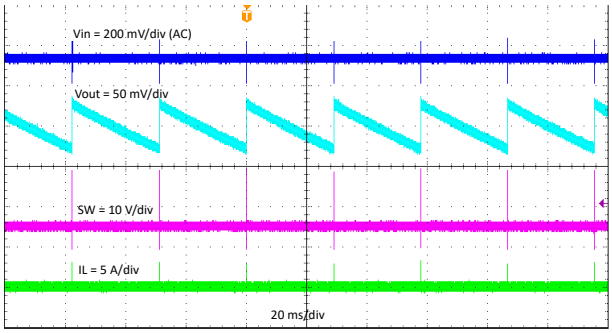


Figure 8-12. Output Voltage Ripple, Iout = 0 A, PSM Mode

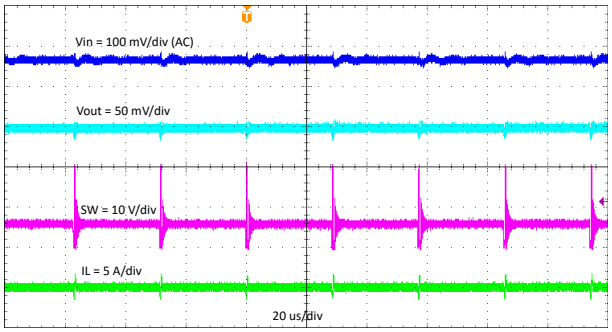


Figure 8-13. Output Voltage Ripple, Iout = 0 A, OOA Mode

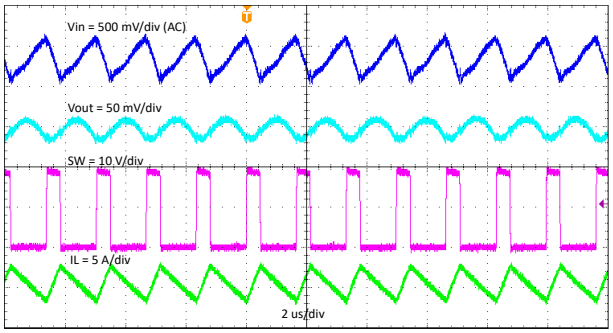


Figure 8-14. Output Voltage Ripple, Iout = 8 A

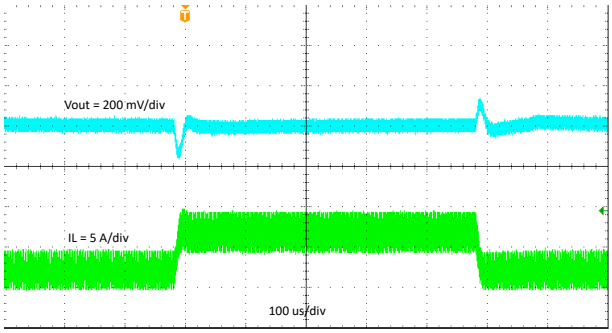


Figure 8-15. Transient Response, 1.6 A to 6.4 A with 2.5 A/us SR

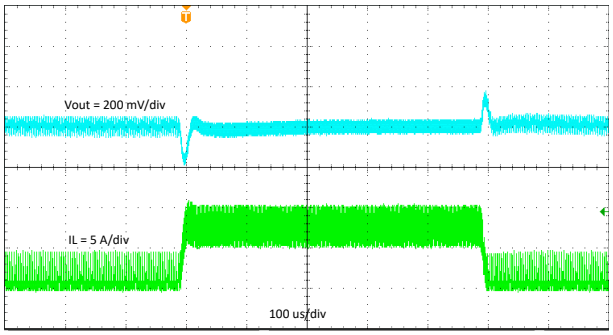


Figure 8-16. Transient Response, 0.8 A to 7.2 A with 2.5 A/us SR

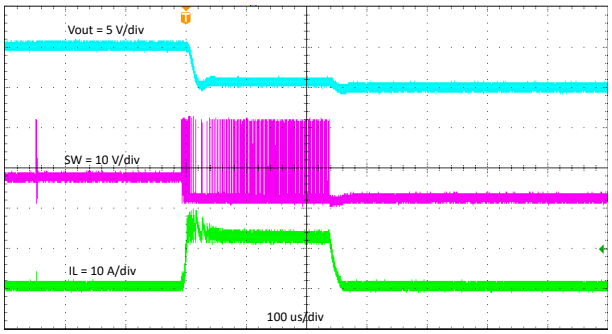


Figure 8-17. Normal Operation to Output Hard Short

8.3 Power Supply Recommendations

The TPS51386 are intended to be powered by a well regulated DC voltage. The input voltage range is 4.5 V to 24 V. TPS51386 are buck converters. The input supply voltage must be greater than the desired output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far from the TPS51386 circuit, TI recommends some additional input bulk capacitance. Typical values are 100 µF to 470 µF.

8.4 Layout

8.4.1 Layout Guidelines

Layout is a critical portion of good power supply design. Key guidelines to follow for the layout are:

- Make VIN, PGND, and SW traces as wide as possible to reduce trace impedance and improve heat dissipation. Use vias and traces on others layers to reduce VIN and PGND trace impedance.
- Use multiple vias near the PGND pins and use the layer directly below the device to connect them together, which helps to minimize noise and can help heat dissipation
- Use vias near both VIN pins and provide a low impedance connection between them through an internal layer.
- Place the smaller value high frequency bypass ceramic capacitors from each VIN to PGND pins and place them as close as possible to the device on the same side of the PCB. Place the remaining ceramic input capacitance next to these high frequency bypass capacitors. The remaining input capacitance can be placed on the other side of the board but use as many vias as possible to minimize impedance between the capacitors and the pins of the IC.
- Route FB traces away from the noisy switch node. Place the bottom resistor in the FB divider as close as possible to the FB pin of the IC. Also keep the upper feedback resistor and the feedforward capacitor near the IC. Connect the FB divider to the output voltage at the desired point of regulation.
- Place the BOOT-SW capacitor as close as possible to the BOOT and SW pins.

8.4.2 Layout Example

The following figure shows the recommended top side layout.

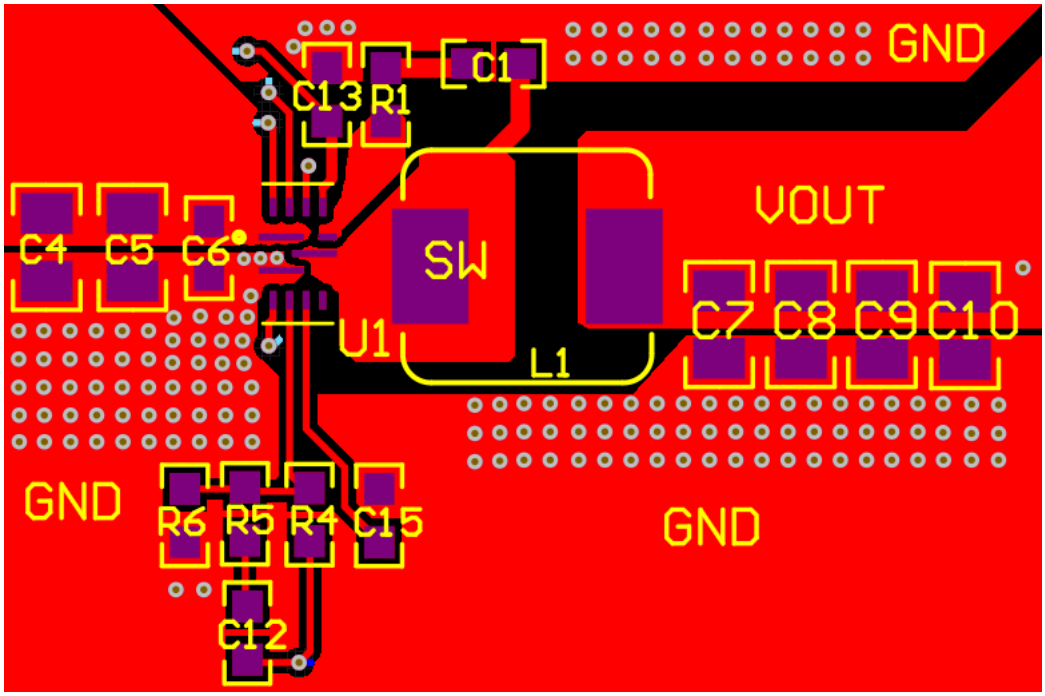


Figure 8-18. Top Side Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS51386RJNR	ACTIVE	VQFN-HR	RJN	12	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	51386	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

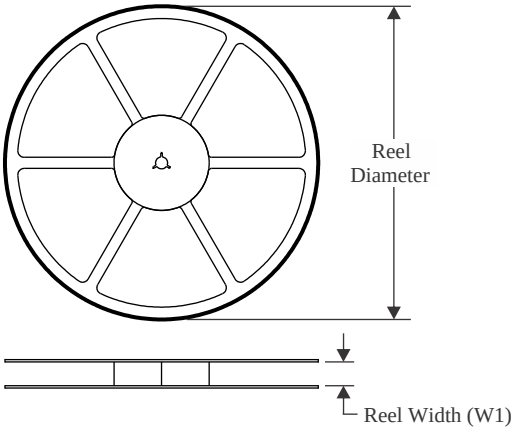
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

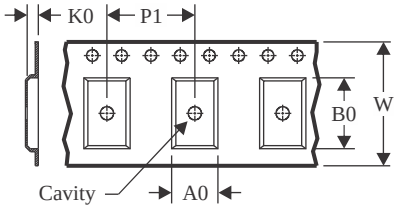
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

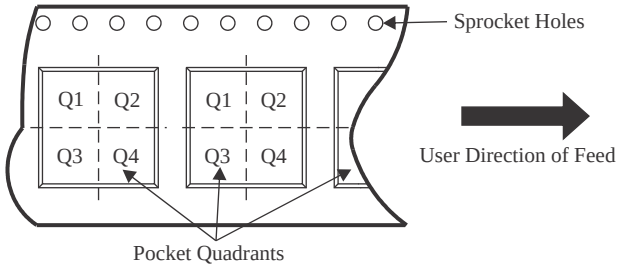


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

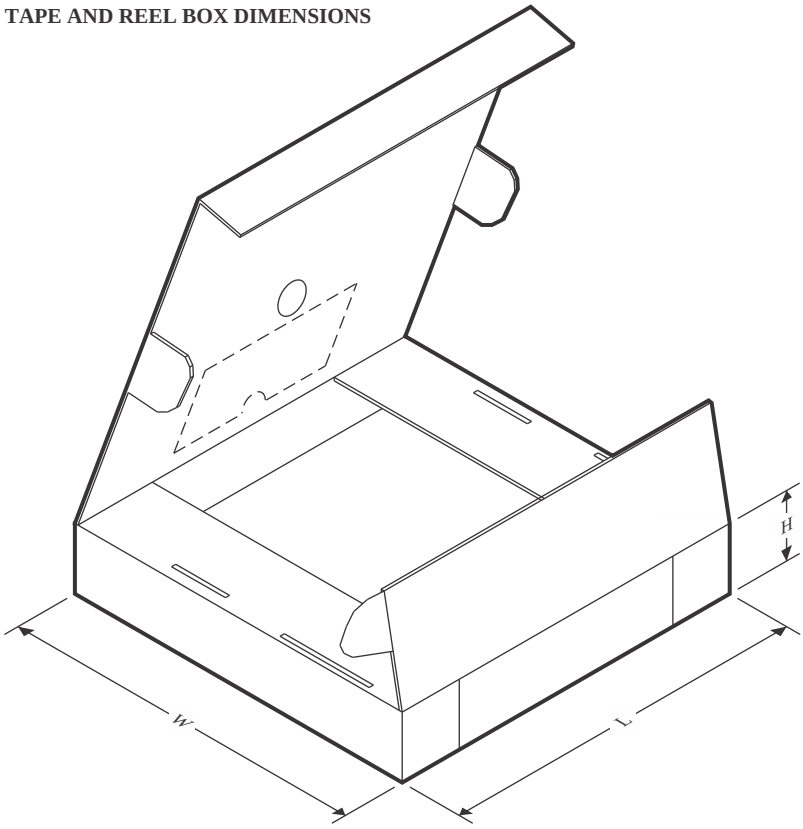
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51386RJNR	VQFN-HR	RJN	12	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

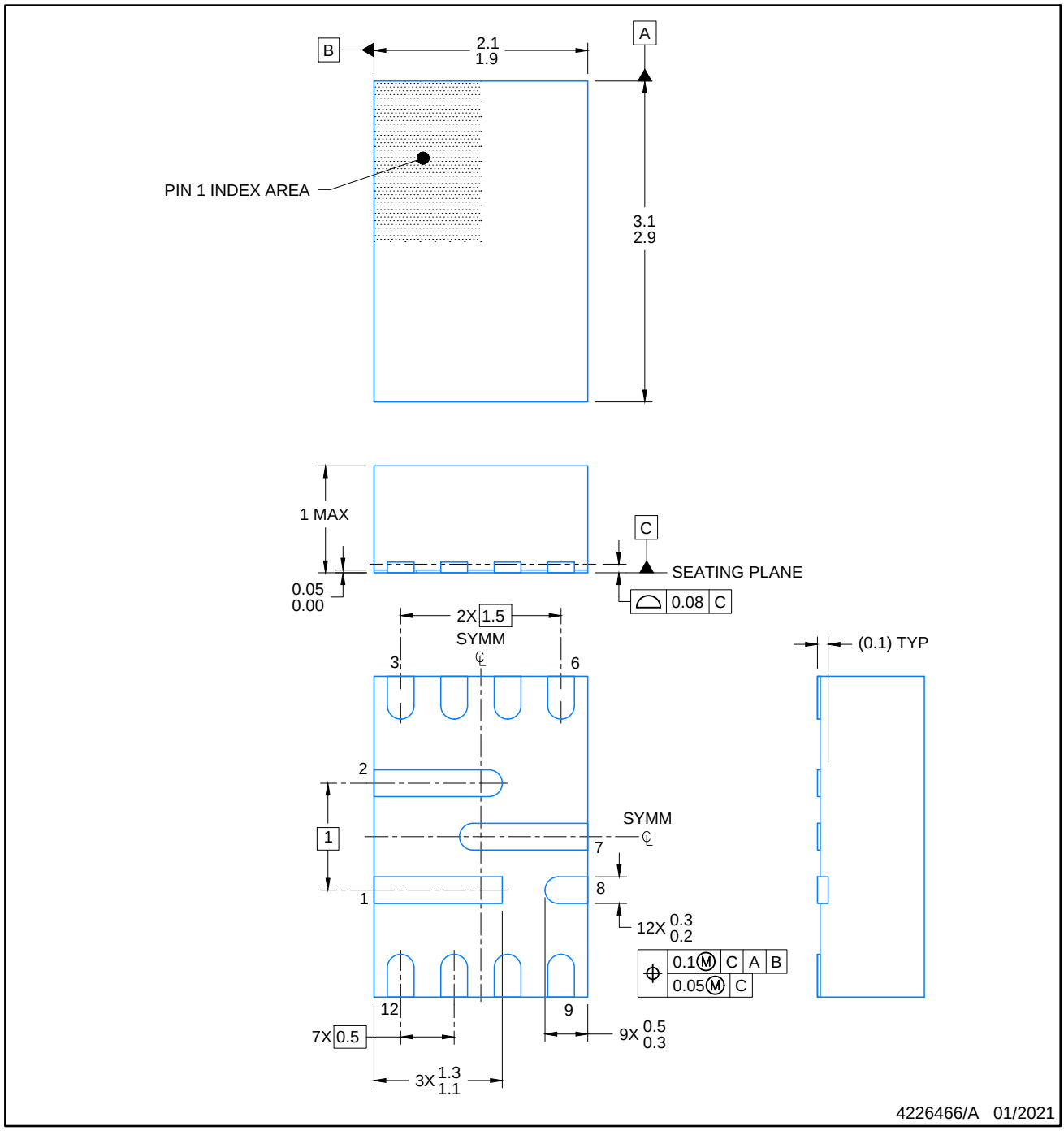
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51386RJNR	VQFN-HR	RJN	12	3000	210.0	185.0	35.0

PACKAGE OUTLINE

RJN0012A

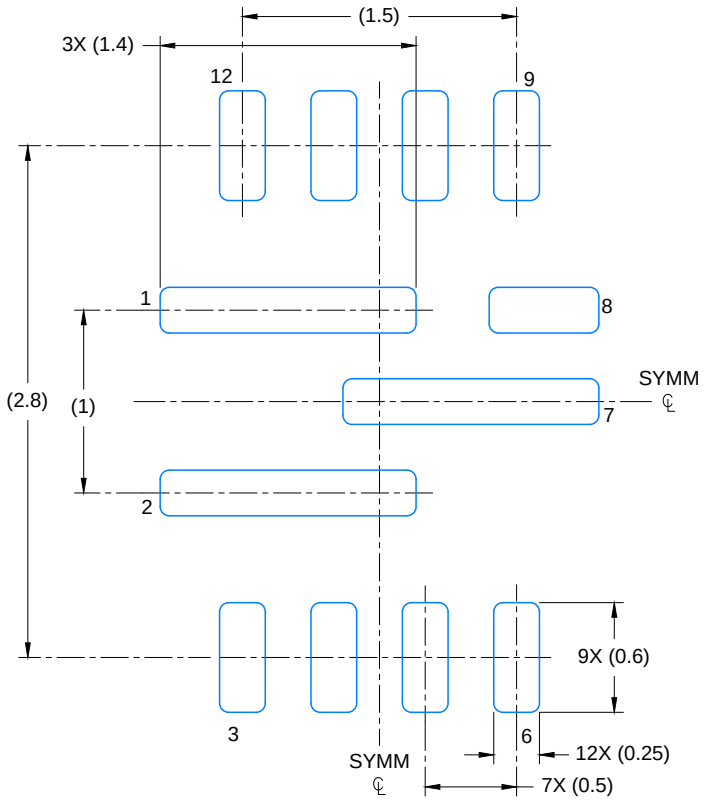
VQFN-HR - 1 mm max height

PLASTIC SMALL OUTLINE- NO LEAD

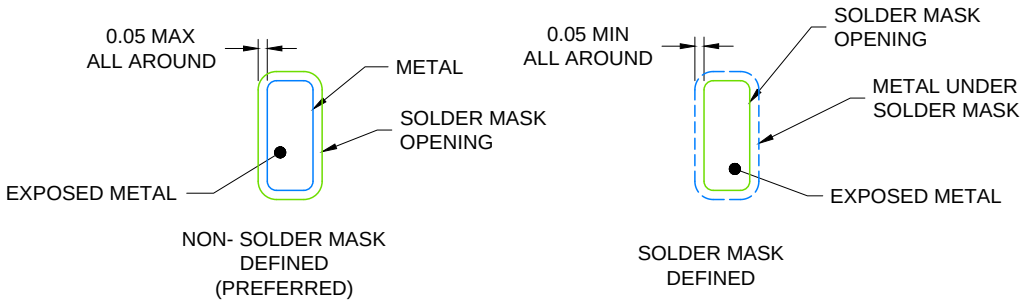


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

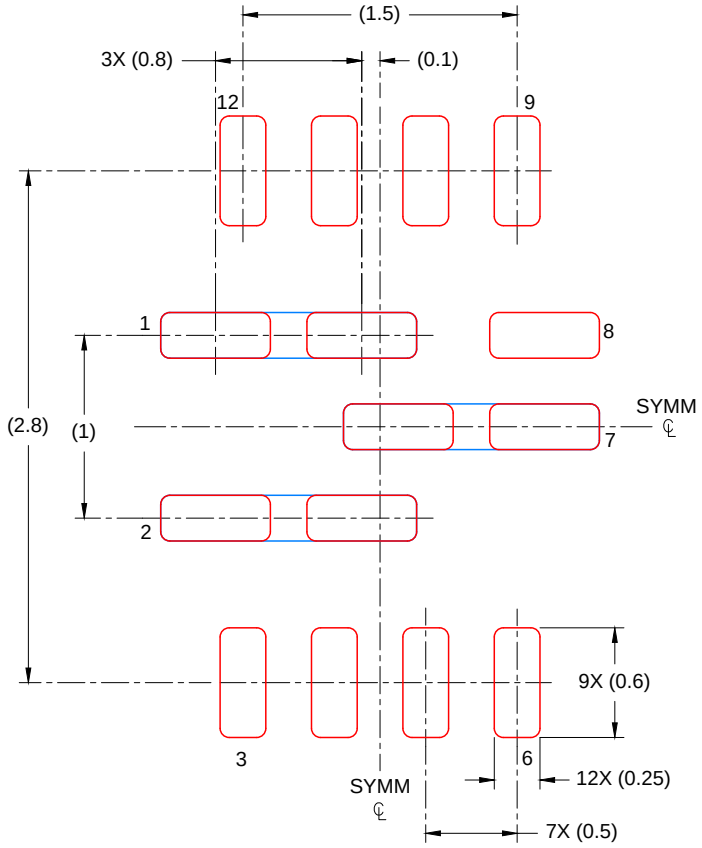


SOLDER MASK DETAILS

4226466/A 01/2021

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

EXPOSED PAD
PINS 1,2,7: 86%
SCALE: 25X

4226466/A 01/2021

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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