1. DESCRIPTION

The XL5615 and XD5615 are 10-bit voltage output digital-to-analog converter (DAC) with a buffered reference input (high impedance). The DAC has an output voltage range that is two times the reference voltage, and the DAC is monotonic. The device is simple to use, running from a single supply of 5V. A power-on-reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the XL5615 and XD5615 are over a three-wire serial bus that is CMOS compatible and easily interfaced to industry standard microprocessor and microcontroller devices. The device receives a 16-bit data word to produce the analog output. The digital inputs feature Schmitt triggers for high noise immunity. Digital communication protocols include the SPI™, QSPI™, and Microwire™ standards.

The 8-terminal small-outline D package allows digital control of analog functions in space-critical applications. The XL5615 and XD5615 are characterized for operation from –40°C to +85°C.

2. FEATURES

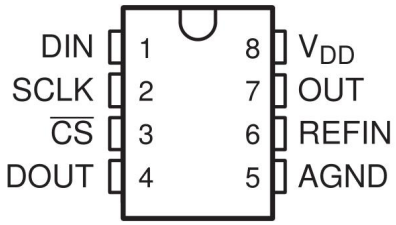
- 10-Bit CMOS Voltage Output DAC in an 8-Terminal Package
- 5V Single Supply Operation
- 3-Wire Serial Interface
- High-Impedance Reference Inputs
- Voltage Output Range: 2 Times the Reference Input Voltage
- Internal Power-On Reset
- Low Power Consumption: 1.75mW Max
- Update Rate of 1.21MHz
- Settling Time to 0.5LSB: 12.5µs Typ
- Monotonic Over Temperature

3. TYPICAL APPLICATION

- Battery-Powered Test Instruments
- Digital Offset and Gain Adjustment
- Battery Operated/Remote Industrial Controls
- Machine and Motion Control Devices
- Cellular Telephones

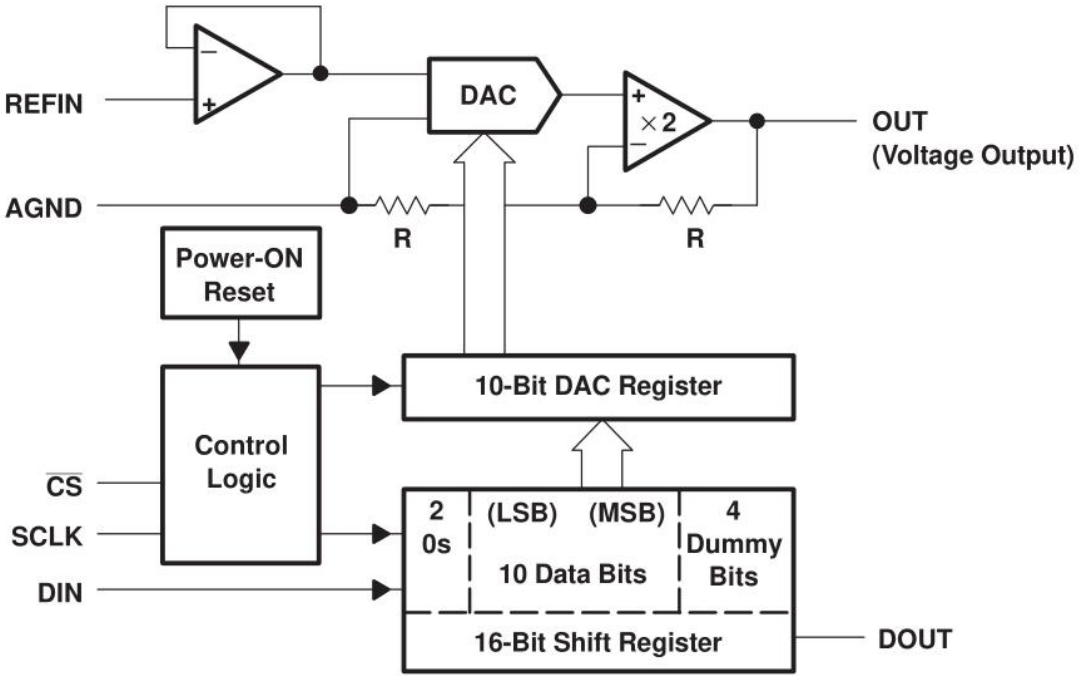
4. PIN CONFIGURATIONS AND FUNCTIONS

(TOP VIEW)



TERMINAL NAME	NO.	I/O	DESCRIPTION
DIN	1	I	Serial data input
SCLK	2	I	Serial clock input
CS	3	I	Chip select, active low
DOUT	4	O	Serial data output for daisy chaining
AGND	5		Analog ground
REFIN	6	I	Reference input
OUT	7	O	DAC analog voltage output
V_{DD}	8		Positive power supply

5. BLOCK DIAGRAM



6. ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
Supply voltage (V_{DD} to AGND)		7V
Digital input voltage range to AGND		–0.3V to VDD + 0.3V
Reference input voltage range to AGND		–0.3V to VDD + 0.3V
Output voltage at OUT from external source		VDD + 0.3V
Continuous current at any terminal		20mA
Operating free-air temperature range, T_A	XL5615	–40 °C to +85 °C
	XD5615	–40°C to +85°C
Storage temperature range, T_{stg}		–65°C to +150°C
Lead temperature 1,6mm (1/16 inch) from case for 10 seconds		+260°C

Stressesbeyondthoselistedunder AbsoluteMaximumRatingsmaycausepermanentdamagetothedevice.Thesearestress ratingsonly,andfunctionaloperationofthedeviceattheseoranyotherconditionsbeyondthoseindicatedunder RecommendedOperatingConditionsisnotimplied.Exposuretoabsolute-maximum-ratedconditionsforextendedperiods may affectdevicereliability.

7. RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		4.5	5	5.5	V
High-level digital input voltage, V_{IH}		2.4			V
Low-level digital input voltage, V_{IL}				0.8	V
Reference voltage, V_{ref} to REFIN terminal		2	2.048	V_{DD}–2	V
Load resistance, R_L		2			kΩ
Operating free-air temperature, T_A	XL5615	–40		85	°C
	XD5615	–40		85	°C

8. ELECTRICAL CHARAC TERISTICS

over recommended operating free-air temperature range, V_{DD} = 5V ± 5%, V_{ref} = 2.048V (unless otherwise noted)

STATIC DAC SPECIFICATIONS						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			10			bits
Integral nonlinearity, end point adjusted (INL)		V_{ref} = 2.048V, See (1)			±1	LSB
Differential nonlinearity (DNL)		V_{ref} = 2.048V, See (2)		±0.1	±0.5	LSB
E_{ZS} Zero-scale error (offset error at zero scale)		V_{ref} = 2.048V, See (3)			±3	LSB
Zero-scale-error temperature coefficient		V_{ref} = 2.048V, See (4)		3		ppm/°C
E_G Gain error		V_{ref} = 2.048V, See (5)			±3	LSB
Gain-error temperature coefficient		V_{ref} = 2.048V, See (6)		1		ppm/°C
PSRR Power-supply rejection ratio	Zero scale	See (7)(8)	80			dB
	Gain		80			
Analog full scale output		R_L = 100kΩ		$2V_{ref}$(1023/1024)		V

(1) The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors (see text). Tested from code 3 to code 1024.

(2) The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code. Tested from code 3 to code 1024.

(3) Zero-scale error is the deviation from zero-voltage output when the digital input code is zero (see text).

(4) Zero-scale-error temperature coefficient is given by:EZS TC = [EZS (Tmax) – EZS (Tmin)]/Vref × 106/(Tmax– Tmin).

(5) Gain error is the deviation from the ideal output (Vref – 1LSB) with an output load of 10kΩ excluding the effects of the zero-scale error.

(6) Gain temperature coefficient is given by:E_G TC = [$E_G(T_{max})$ – E_G (T_{min})]/V_{ref} × 10^6/(T_{max}– T_{min}).

(7) Zero-scale-error rejection ratio (EZS-RR) is measured by varying the VDD from 4.5V to 5.5V dc and measuring the proportion of this signal imposed on the zero-code output voltage.

(8) Gain-error rejection ratio (EG-RR) is measured by varying the VDD from 4.5V to 5.5V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero-scale change.

9. VOLTAGE OUTPUT(OUT)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Voltage output range	R_L= 10kΩ		0		V_{DD}–0.4	V
	Output load regulation accuracy	$V_{O(OUT)}$ = 2V,	R_L = 2kΩ			0.5	LSB
I_{OSC}	Output short circuit current	OUT to V_{DD} or AGND			20		mA
$V_{OL(low)}$	Output voltage, low-level	$I_{O(OUT)}$≤ 5mA				0.25	V
$V_{OH(high)}$	Output voltage, high-level	$I_{O(OUT)}$≤– 5mA		4.75			V
REFERENCE INPUT (REFIN)							
V_I	Input voltage			0		V_{DD}–2	V
r_i	Input resistance			10			MΩ
C_i	Input capacitance				5		pF
DIGITAL INPUTS (DIN, SCLK, CS)							
V_{IH}	High-level digital input voltage			2.4			V
V_{IL}	Low-level digital input voltage					0.8	V
I_{IH}	High-level digital input current	$V_I = V_{DD}$				±1	μA
I_{IL}	Low-level digital input current	V_I = 0				±1	μA
C_i	Input capacitance				8		pF
DIGITAL OUTPUT (DOUT)							
V_{OH}	Output voltage, high-level	I_O = –2mA		V_{DD}–1			V
V_{OL}	Output voltage, low-level	I_O = 2mA				0.4	V
POWER SUPPLY							
V_{DD}	Supply voltage			4.5	5	5.5	V
I_{DD}	Power supply current	V_{DD} = 5.5V, No load, All inputs = 0V or V_{DD}	V_{ref} = 0		150	250	μA
		V_{DD}= 5.5V, No load, All inputs = 0V or V_{DD}	V_{ref} = 2.048V		230	350	μA
ANALOG OUTPUT DYNAMIC PERFORMANCE							
	Signal-to-noise + distortion, S/(N+D)	V_{ref} = 1V_{PP} at 1kHz + 2.048Vdc, code = 11 1111 1111[1]		60			dB

[1] The limiting frequency value at 1V_{PP} is determined by the output-amplifier slew rate.

10. DIGITAL INPUT TIMING REQUIREMENTS (See Figure 1)

PARAMETER		MIN	NOM	MAX	UNIT
$t_{su(DS)}$	Setup time, DIN before SCLK high	45			ns
$t_{h(DH)}$	Hold time, DIN valid after SCLK high	0			ns
$t_{su(CSS)}$	Setup time, CS low to SCLK high	1			ns
$t_{su(CS1)}$	Setup time, CS high to SCLK high	50			ns
$t_{h(CSH0)}$	Hold time, SCLK low to CS low	1			ns
$t_{h(CSH1)}$	Hold time, SCLK low to CS high	0			ns
$t_{w(CS)}$	Pulse duration, minimum chip select pulse width high	20			ns
$t_{w(CL)}$	Pulse duration, SCLK low	25			ns
$t_{w(CH)}$	Pulse duration, SCLK high	25			ns

11. OUTPUT SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{pd(DOUT)}$	Propagation delay time, DOUT	C_L = 50pF			50	ns

12. OPERATING CHARACTERISTICS

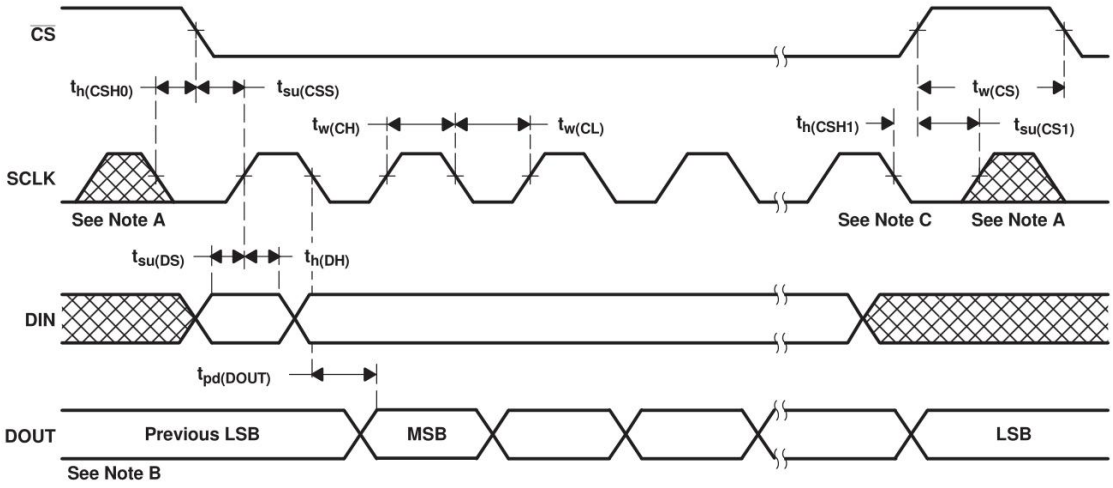
over recommended operating free-air temperature range, VDD = 5V ±5%, Vref = 2.048V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG OUTPUT DYNAMIC PERFORMANCE							
SR	Output slew rate	C_L = 100pF, T_A= +25°C	R_L = 10kΩ,	0.3	0.5		V/μs
t_s	Output settling time	To 0.5LSB, R_L = 10kΩ,	C_L = 100pF, [1]		12.5		μs
	Glitch energy	DIN = All 0s to all 1s			5		nV-s
REFERENCE INPUT (REFIN)							
	Reference feedthrough	REFIN = $1V_{PP}$ at 1kHz + 2.048Vdc [2]			–80		dB
	Reference input bandwidth (f–3dB)	REFIN = $0.2V_{PP}$ + 2.048Vdc			30		kHz

[1] Settling time is the time for the output signal to remain within ±0.5LSB of the final measured value for a digital input code change of 000 hex to 3FF hex or 3FF hex to 000 hex.

[2] Reference feedthrough is measured at the DAC output with an input code = 000 hex and a V_{ref} input = 2.048Vdc + $1V_{pp}$ at 1kHz.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input clock, applied at the SCLK terminal, should be inhibited low when $\overline{CS}$ is high to minimize clock feedthrough.
B. Data input from preceeding conversion cycle.
C. Sixteenth SCLK falling edge

Figure 1. Timing Digram

TYPICAL CHARACTERISTICS

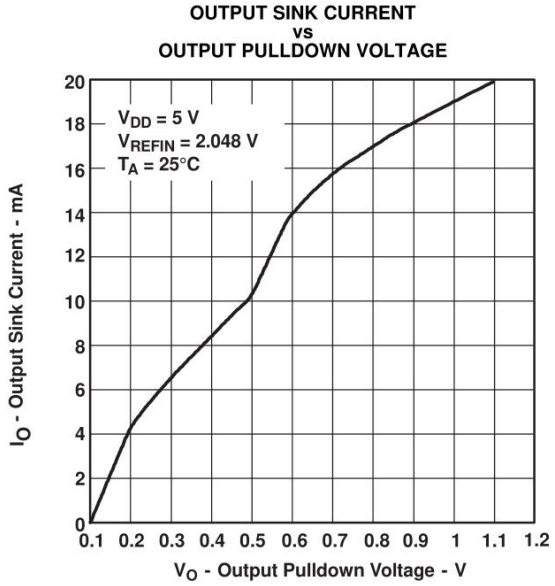


Figure 2.

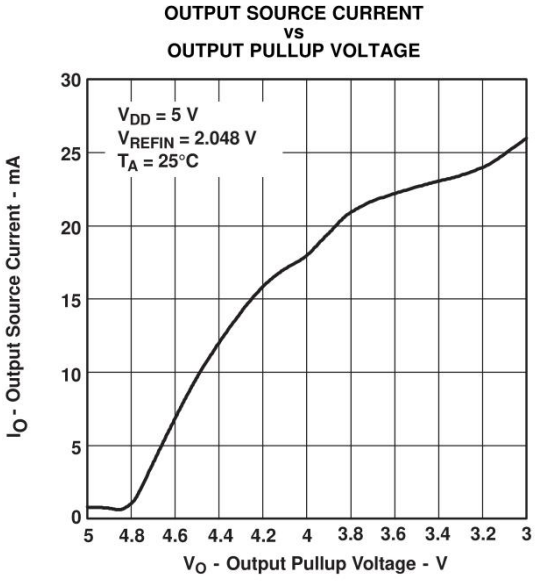


Figure 3.

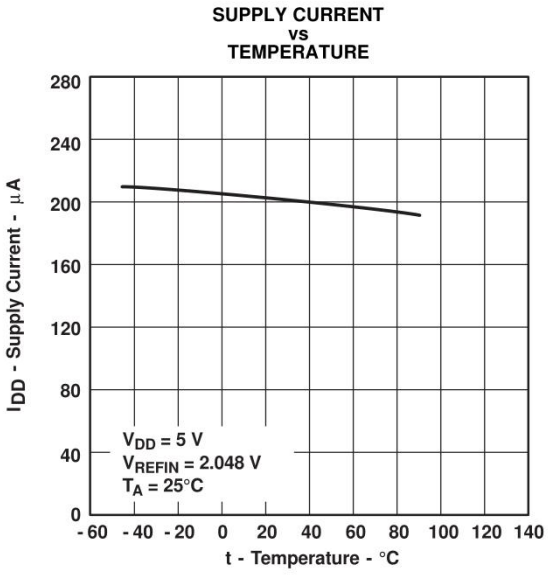


Figure 4.

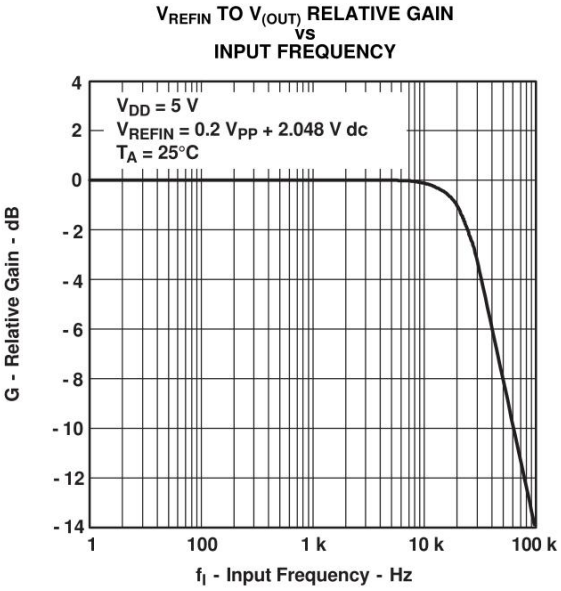


Figure 5.

TYPICAL CHARACTERISTICS (continued)

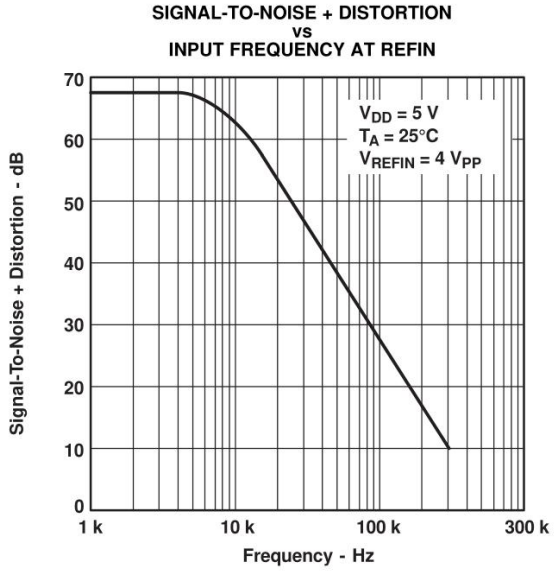


Figure 6.

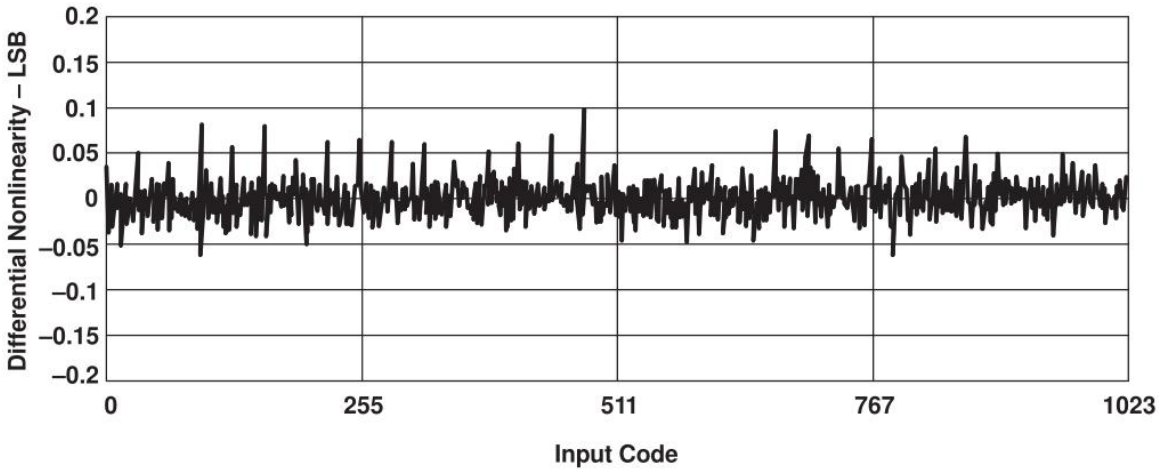


Figure 7. Differential Nonlinearity With Input Code

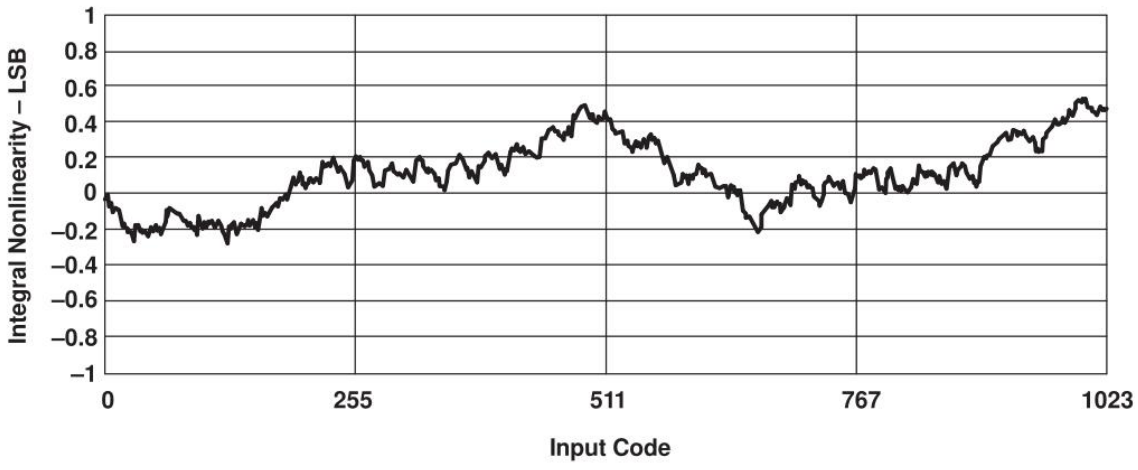


Figure 8. Integral Nonlinearity With Input Code

APPLICATION INFORMATION

GENERAL FUNCTION

The XL5615 uses a resistor string network buffered with an op amp in a fixed gain of 2 to convert 10-bit digital data to analog voltage levels (see functional block diagram and Figure 9). The output of the XL5615 is the same polarity as the reference input (see Table 1).

An internal circuit resets the DAC register to all zeros on power up.

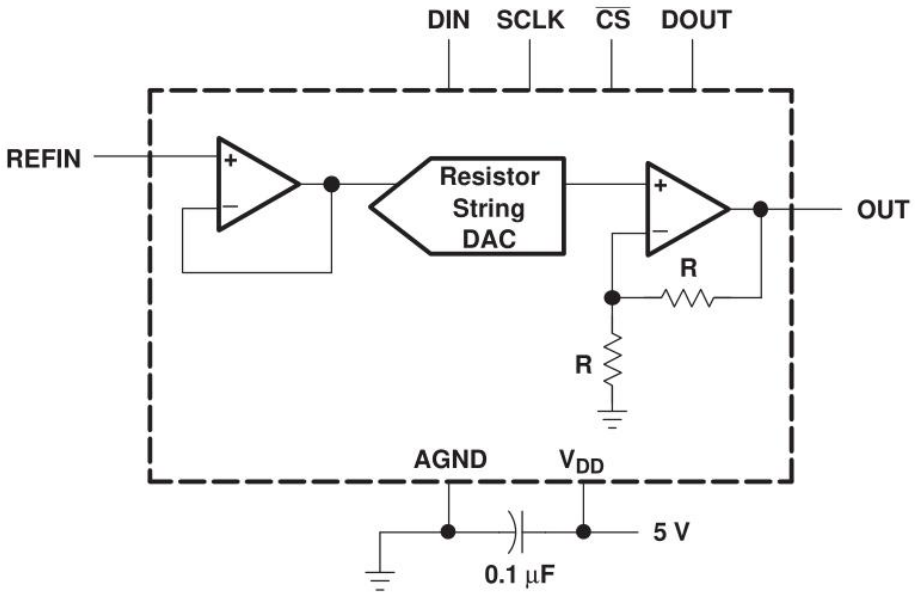


Figure 9. XL5615 Typical Operating Circuit

Table 1. Binary Code Table (0V to 2V_{REFIN}Output), Gain = 2

INPUT(1)			OUTPUT
1111	1111	11(00)	$2(V_{REFIN})\,^{1023}/_{1024}$
	:		:
1000	0000	01(00)	$2(V_{REFIN})\,^{513}/_{1024}$
1000	0000	00(00)	$2(V_{REFIN})^{512}/_{1024} = V_{REFIN}$
0111	1111	11(00)	$2(V_{REFIN})^{511}/_{1024}$
	:		:
0000	0000	01(00)	$2(V_{REFIN})\,^{1}/_{1024}$
0000	0000	00(00)	0 V

(1) A 10-bit data word with two bits below the LSB bit (sub-LSB) with 0 values must be written since the DAC input latch is 12 bits wide.

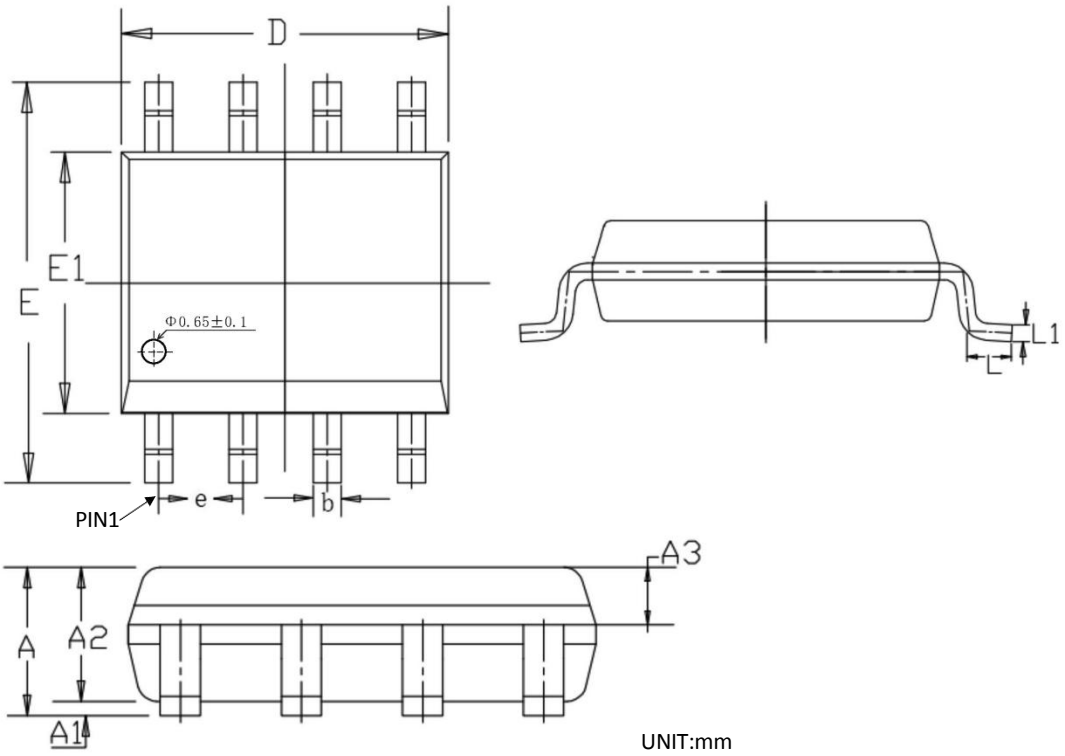
13. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL5615	XL5615	SOP8	4.90 * 3.90	- 40 to 85	MSL3	T&R	2500
XD5615	XD5615	DIP8	9.25 * 6.38	- 40 to 85	MSL3	Tube 50	2000

14. DIMENSIONAL DRAWINGS

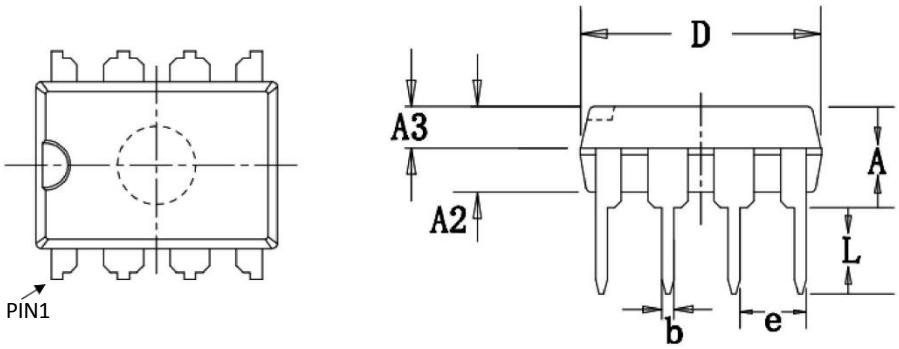
SOP8

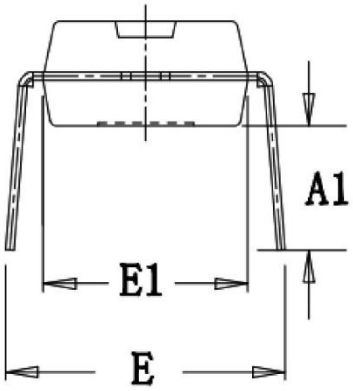


UNIT:mm

	MIN	NOM	MAX
A	1.450	1.550	1.650
A1	0.100	0.150	0.200
A2	1.300	1.400	1.500
A3	0.600	0.650	0.700
b	0.380	–	0.510
e	1.240	1.270	1.300
D	4.800	4.900	5.000
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.450	0.600	0.750
L1	—	0.25BSC	—

DIP8





UNIT:mm

	MIN	NOM	MAX
A	3.600	3.800	4.000
A1	3.786	3.886	3.986
A2	3.200	3.300	3.400
A3	1.550	1.600	1.650
b	0.440	–	0.490
e	2.510	2.540	2.570
D	9.150	9.250	9.350
E	7.800	8.500	9.200
E1	6.280	6.380	6.480
L	3.000	–	–