



DESCRIPTION

The HSN75LBC184 and HSN65LBC184 are differential data line transceivers in the trade-standard footprint of the SN75176 with built-in protection against high-energy noise transients. This feature provides a substantial increase in reliability for better immunity to noise transients coupled to the data cable over most existing devices. Use of these circuits provides a reliable low-cost direct-coupled (with no isolation transformer) data line interface without requiring any external components.

The HSN75LBC184 and HSN65LBC184 can withstand overvoltage transients of 400-W peak (typical). The conventional combination wave called out in IEC 61000-4-5 simulates the overvoltage transient and models a unidirectional surge caused by overvoltages from switching and secondary lightning transients.

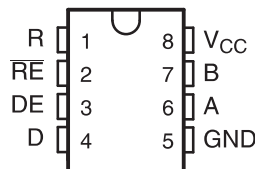
APPLICATIONS

- Industrial Networks
- Utility Meters
- Motor Control

FEATURES

- Integrated Transient Voltage Suppression
- ESD Protection for Bus Terminals Exceeds: ± 30 kV IEC 61000-4-2, Contact Discharge ± 15 kV IEC 61000-4-2, Air-Gap Discharge ± 15 kV EIA/JEDEC Human Body Model
- Circuit Damage Protection of 400-W Peak (Typical) Per IEC 61000-4-5
- Controlled Driver Output-Voltage Slew Rates Allow Longer Cable Stub Lengths
- 250-kbps in Electrically Noisy Environments
- Open-Circuit Fail-Safe Receiver Design
- 1/4 Unit Load Allows for 128 Devices Connected on Bus
- Thermal Shutdown Protection
- Power-Up/-Down Glitch Protection
- Each Transceiver Meets or Exceeds the Requirements of TIA/EIA-485 (RS-485) and ISO/IEC 8482:1993(E) Standards
- Low Disabled Supply Current 300 μ A Max
- Pin Compatible With SN75176

PIN CONFIGURATION



SOP-8, DIP-8

Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----------------|-----|---------------------|--|
| NAME | NO. | | |
| A | 6 | Bus input/output | Driver output or receiver input (complementary to B) |
| B | 7 | Bus input/output | Driver output or receiver input (complementary to A) |
| D | 4 | Digital input | Driver data input |
| DE | 3 | Digital input | Active-HIGH driver enable |
| GND | 5 | Reference potential | Local device ground |
| R | 1 | Digital output | Receiver data output |
| \overline{RE} | 2 | Digital input | Active-LOW receiver enable |
| V _{CC} | 8 | Supply | 4.75-V to 5.25-V supply |



BLOCK DIAGRAM

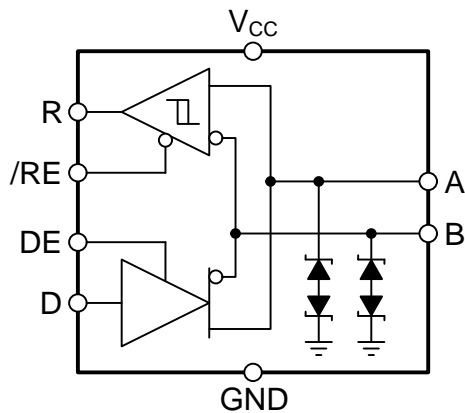
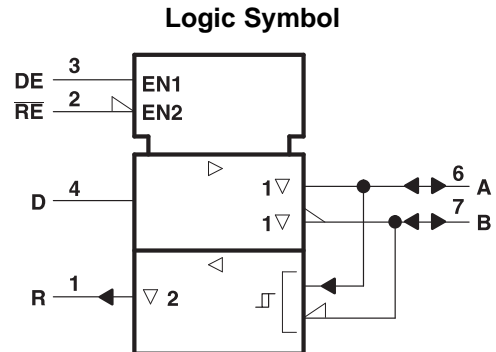


Figure 13. Functional Logic Diagram

LOGIC SYMBOL



OVERVIEW

The HSNx5LBC184 device is a 5-V, half-duplex, RS-485 transceiver with integrated transient voltage suppressors that prevent circuit damage in the presence of high-energy transients of up to 400-W peak power. This transceiver has an active-HIGH driver enable and active-LOW receiver enable. The differential driver is suitable for data transmission up to 250 kbps.

FEATUER DESCRIPTION

Integrated transient voltage suppressors protect the transceiver against Electrostatic Discharges (ESD) according to IEC 61000-4-2 of up to ± 30 kV and surge transients according to IEC 61000-4-5 of up to 400-W peak.

The differential driver incorporates slew-rate controlled outputs sufficient to transmit data up to 250 kbps. Slew-rate control allows for longer unterminated cable runs and longer stub lengths from the main cable trunk than with faster voltage transitions. A unique receiver design provides a high level failsafe output when the inputs are left floating.

The HSN65LBC184 is characterized from -40°C to 85°C and the HSN75LBC184 is characterized from 0°C to 70°C .

DRIVER FUNCTION TABLE

| INPUT | ENABLE | OUTPUTS | |
|-------|--------|---------|---|
| D | DE | A | B |
| H | H | H | L |
| L | H | L | H |
| X | L | Z | Z |

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

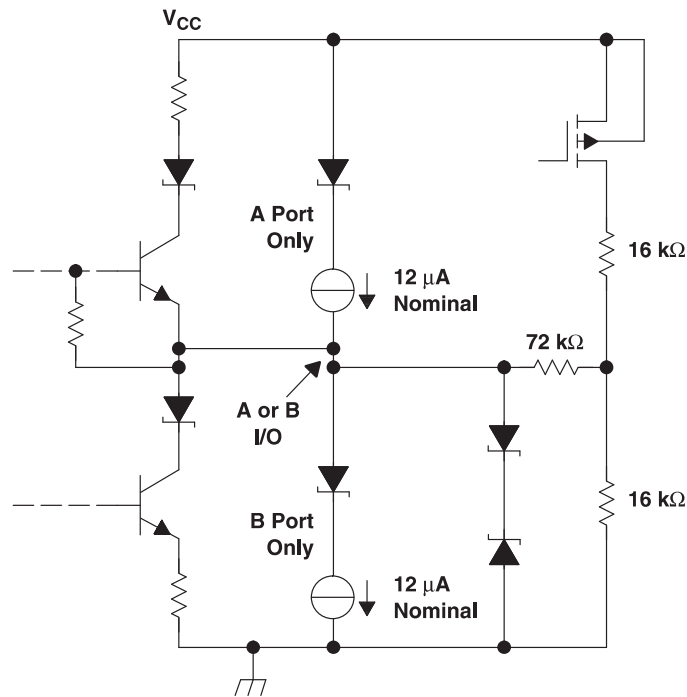
RECEIVER FUNCTION TABLE

| DIFFERENTIAL INPUTS | ENABLE | OUTPUT |
|--|------------------------|--------|
| A - B | $\overline{\text{RE}}$ | R |
| $V_{\text{ID}} \geq 0.2 \text{ V}$ | L | H |
| $-0.2 \text{ V} < V_{\text{ID}} < 0.2 \text{ V}$ | L | ? |
| $V_{\text{ID}} \leq -0.2 \text{ V}$ | L | L |
| X | H | Z |
| Open | L | H |

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)



Schematic of Inputs and Outputs



SPECIFICATIONS

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| SYMBOL | PARAMETER | MIN | MAX | UNIT |
|------------------|---|--------------------|-----|------|
| V _{CC} | Supply voltage ⁽²⁾ | -0.5 | 7 | V |
| | Continuous voltage range at any bus terminal | -15 | 15 | V |
| | Data input/output voltage | -0.3 | 7 | V |
| I _O | Receiver output current | -20 | 20 | mA |
| | Continuous total power dissipation ⁽³⁾ | Internally Limited | | |
| T _{stg} | Storage temperature | | 160 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
- (3) The driver shuts down at a junction temperature of approximately 160°C. To operate below this temperature, see the Dissipation Ratings.

ESD Ratings

| SYMBOL | PARAMETER | VALUE | UNIT |
|--|---|--------------------------|--------|
| V _(ESD) Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | A, B, GND | ±15000 |
| | | All pins | ±3000 |
| | Contact discharge (IEC61000-4-2) | A, B, GND ⁽²⁾ | ±30000 |
| | | A, B, GND ⁽³⁾ | ±15000 |
| | All pins (Class 3A) | | ±8000 |
| | All pins (Class 3B) | | ±200 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) GND and bus pin ESD protection is beyond readily available test equipment capabilities for IEC 61000-4-2, EIA/JEDEC test method A114-A and MIL-STD-883C method 3015. Ratings listed are limits of test equipment; device performance exceeds these limits.



Recommended Operating Conditions

over operating free-air temperature range

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT |
|-----------------------------------|---|-------------|-----|------|------|
| V _{CC} | Supply voltage | 4.75 | 5 | 5.25 | V |
| V _I or V _{IC} | Voltage at any bus terminal (separately or common mode) | -7 | | 12 | V |
| V _{IH} | High-level input voltage | 2 | | | V |
| V _{IL} | Low-level input voltage | | | 0.8 | V |
| V _{ID} | Differential input voltage | | | 12 | V |
| I _{OH} | High-level output current | Driver | | | mA |
| | | Receiver | -60 | | |
| I _{OL} | Low-level output current | Driver | | | mA |
| | | Receiver | -8 | | |
| T _A | Operating free-air temperature | HSN75LBC184 | 0 | 70 | °C |
| | | HSN65LBC184 | -40 | 85 | |

Thermal Information

| SYMBOL | THERMAL METRIC | HSNx5LBC184 | | UNIT |
|-----------------------|--|-------------|-----------|------|
| | | P [DIP-8] | D [SOP-8] | |
| | | 8 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 108.7 | 172.4 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 34.8 | 42.5 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 23.6 | 41.4 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 12 | 4.6 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 23.5 | 40.7 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | N/A | N/A | °C/W |

Driver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--------------------|--|--|-----|------|-----|------|----|
| t _{d(DH)} | Differential output delay time, low-to-high-level output | R _L = 54 Ω C _L = 50 pF See Figure 9 | | | 1.3 | μs | |
| t _{d(DL)} | Differential output delay time, high-to-low-level output | | | | 1.3 | μs | |
| t _{PLH} | Propagation delay time, low-to-high-level output | | | 0.5 | 1.3 | μs | |
| t _{PHL} | Propagation delay time, high-to-low-level output | | | 0.5 | 1.3 | μs | |
| t _{sk(p)} | Pulse skew (t _{d(DH)} - t _{d(DL)}) | | | 75 | 150 | ns | |
| t _r | Rise time, single-ended | | | 0.25 | | 1.2 | μs |
| t _f | Fall time, single-ended | | | 0.25 | | 1.2 | μs |
| t _{PZH} | Output enable time to high level | R _L = 110 Ω See Figure 6 | | | 3.5 | μs | |
| t _{PZL} | Output enable time to low level | R _L = 110 Ω See Figure 7 | | | 3.5 | μs | |
| t _{PHZ} | Output disable time from high level | R _L = 110 Ω See Figure 6 | | | 2 | μs | |
| t _{PLZ} | Output disable time from low level | R _L = 110 Ω See Figure 7 | | | 2 | μs | |

Dissipation Ratings

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE T _A = 25°C | T _A = 70°C POWER RATING | T _A = 85°C POWER RATING |
|---------|---------------------------------------|--|---------------------------------------|---------------------------------------|
| D | 725 mW | 5.8 mW/°C | 464 mW | 377 mW |
| P | 1150 mW | 9.2 mW/°C | 736 mW | 598 mW |



Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

| SYMBOL | PARAMETER | ALTERNATE SYMBOLS | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|----------------------|--|------------------------------------|---|------|--------------------|-----------------|------|
| I _{CC} | Supply current | NA | DE = \overline{RE} = 5 V No Load | | 12 | 25 | mA |
| | | | DE = 0 V \overline{RE} = 5 V No Load | | 175 | 300 | μA |
| I _{IH} | High-level input current (D, DE, \overline{RE}) | NA | V _I = 2.4 V | | | 50 | μA |
| I _{IL} | Low-level input current (D, DE, \overline{RE}) | NA | V _I = 0.4 V | -50 | | | μA |
| I _{OS} | Short-circuit output current OS ⁽²⁾ | NA | V _O = -7 V | -250 | -120 | | mA |
| | | | V _O = V _{CC} | | | 250 | |
| | | | V _O = 12 V | | | 250 | |
| I _{OZ} | High-impedance output current | NA | See Receiver I _I | | | | mA |
| V _O | Output voltage | V _{oa} , V _{ob} | I _O = 0 | 0 | | V _{CC} | V |
| V _{OC(PP)} | Peak-to-peak change in common-mode output voltage during state transitions | NA | See Figure 9 and Figure 10 | | 0.8 | | V |
| V _{OC} | Common-mode output voltage | V _{os} | See Figure 8 | 1 | | 3 | V |
| ΔV _{OC(SS)} | Magnitude of change, common-mode steady-state output voltage | V _{os} - V _{os} | See Figure 10 | | | 0.1 | V |
| V _{OD} | Magnitude of differential output voltage V _A - V _B | V _O | I _O = 0 | 1.5 | | 6 | V |
| | | | R _L = 54 Ω, See Figure 8 | 1.5 | | | V |
| Δ V _{OD} | Change in differential voltage magnitude between logic states | V _I - V _I | R _L = 54 Ω | | | 0.1 | V |

(1) All typical values are measured with T_A = 25°C and V_{CC} = 5 V.

(2) This parameter is measured with only one output being driven at a time.

Electrical Characteristics: Receiver

over recommended operation conditions (unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX | UNIT | |
|------------------|--|--|--|--------------------|------|------|----|
| I _{CC} | Supply current (total package) | DE = \overline{RE} = 0 V, No Load | | | 3.9 | mA | |
| | | \overline{RE} = 5 V, DE = 0 V, No Load | | | 300 | μA | |
| I _I | Input current | Other input = 0 V | V _I = 12 V | | | 250 | μA |
| | | | V _I = 12 V, V _{CC} = 0 | | | 250 | |
| | | | V _I = -7 V | -200 | | | |
| | | | V _I = -7 V, V _{CC} = 0 | -200 | | | |
| I _{OZ} | High-impedance-state output current | V _O = 0.4 V to 2.4 V | | | ±100 | μA | |
| V _{hys} | Input hysteresis voltage | | | 70 | | mV | |
| V _{IT+} | Positive-going input threshold voltage | | | | 200 | V | |
| V _{IT-} | Negative-going input threshold voltage | | -200 | | | mV | |
| V _{OH} | High-level output voltage | I _{OH} = -8 mA, See Figure 11 | 2.8 | | | V | |
| V _{OL} | Low-level output voltage | I _{OL} = 4 mA, See Figure 11 | | | 0.4 | V | |

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.



Receiver Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------|--|---------------------------------------|-----|-----|-----|------|
| t_{PLH} | Propagation delay time, low-to-high-level output | $C_L = 50 \text{ pF}$, See Figure 11 | | | 150 | ns |
| t_{PHL} | Propagation delay time, high-to-low-level output | | | | 150 | ns |
| $t_{sk(p)}$ | Pulse skew ($t_{PHL} - t_{PLH}$) | | | | 50 | ns |
| t_r | Rise time, single-ended | See Figure 11 | | 20 | | ns |
| t_f | Fall time, single-ended | | | 20 | | ns |
| t_{PZH} | Output enable time to high level | See Figure 12 | | | 100 | ns |
| t_{PZL} | Output enable time to low level | | | | 100 | ns |
| t_{PHZ} | Output disable time from high level | | | | 100 | ns |
| t_{PLZ} | Output disable time from low level | | | | 100 | ns |

TYPICAL CHARACTERISTICS

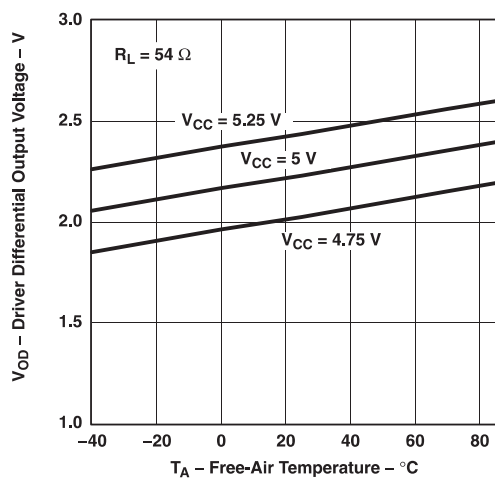


Figure 1. Driver Differential Output Voltage vs Free-Air Temperature

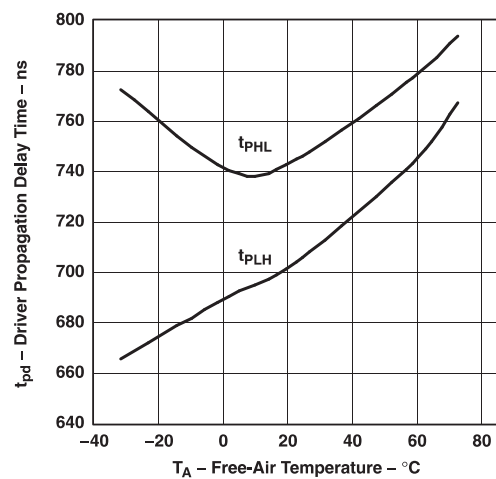


Figure 2. Driver Propagation Delay Time vs Free-Air Temperature

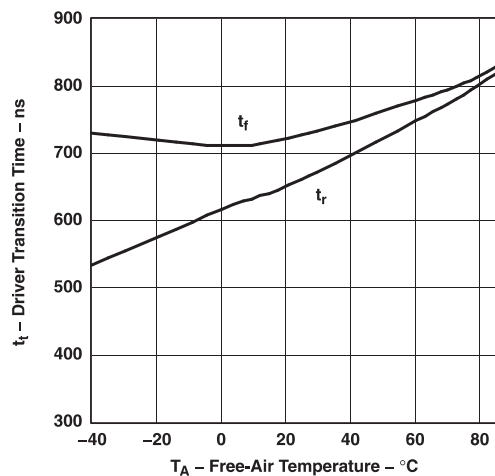


Figure 3. Driver Transition Time vs Free-Air Temperature

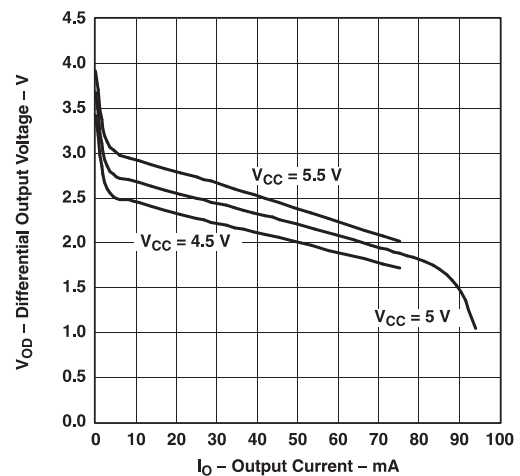


Figure 4. Differential Output Voltage vs Output Current

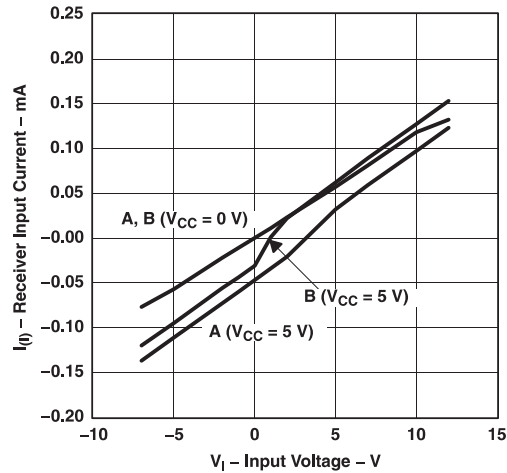
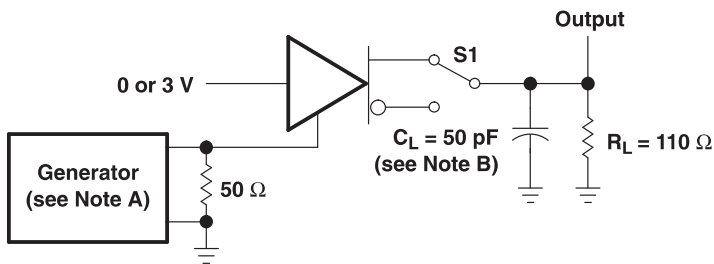
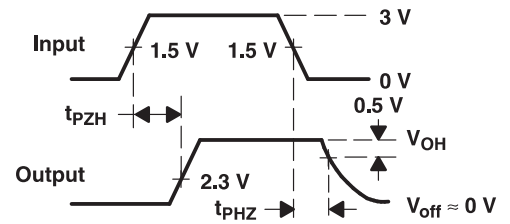


Figure 5. Receiver Input Current vs Input Voltage

PARAMETER MEASUREMENT INFORMATION



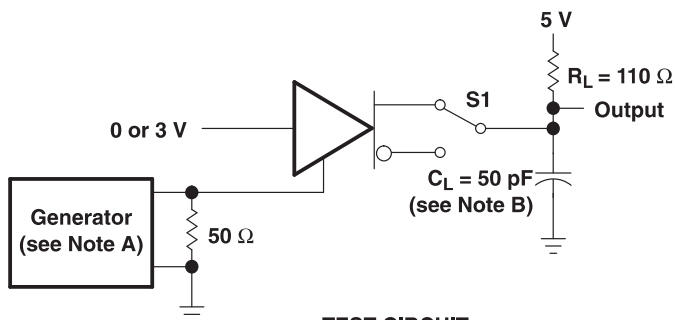
TEST CIRCUIT



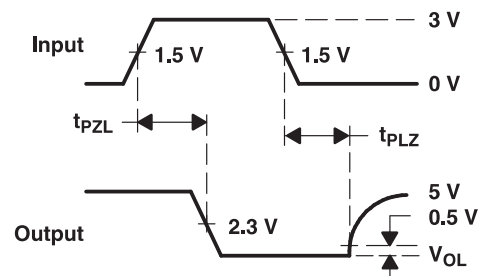
VOLTAGE WAVEFORMS

- The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50 \Omega$.
- C_L includes probe and jig capacitance.

Figure 6. Driver t_{PZH} and t_{PHZ} Test Circuit and Voltage Waveforms



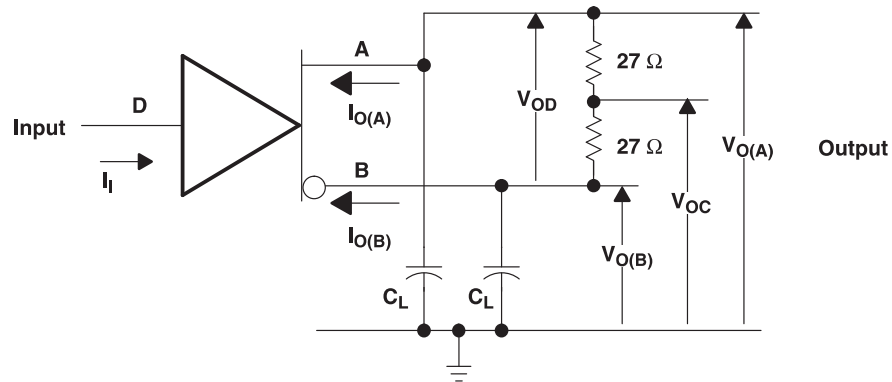
TEST CIRCUIT



VOLTAGE WAVEFORMS

- The input pulse is supplied by a generator having the following characteristics: PRR = 1.25 kHz, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O = 50 \Omega$.
- C_L includes probe and jig capacitance.

Figure 7. Driver t_{PZL} and t_{PLZ} Test Circuit and Voltage Waveforms



- A. Resistance values are in ohms and are 1% tolerance.
- B. C_L includes probe and jig capacitance.

Figure 8. Driver Test Circuit, Voltage, and Current Definitions

PARAMETER MEASUREMENT INFORMATION(CONTINUED)

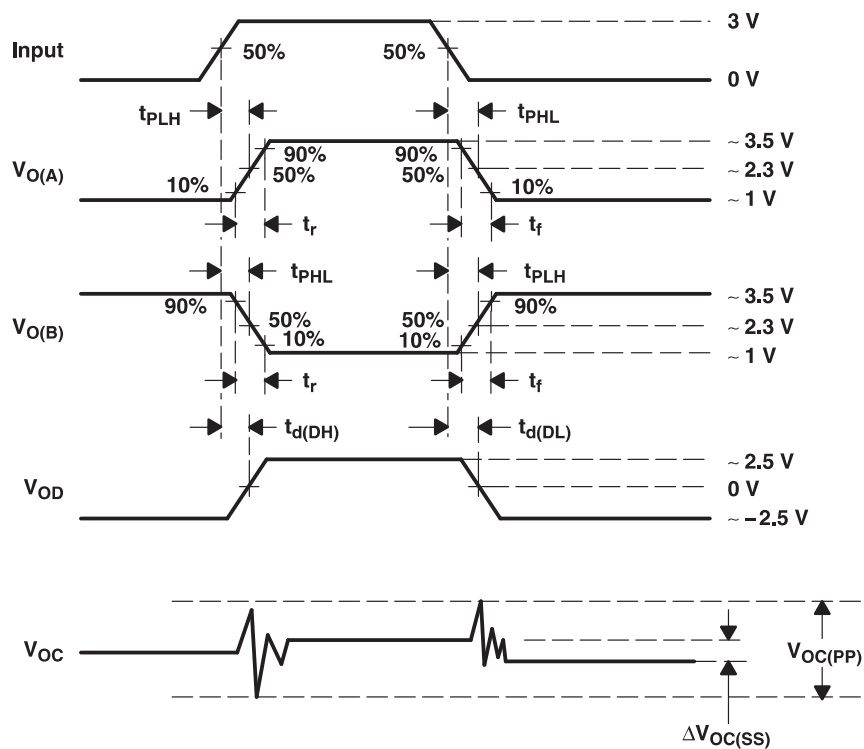
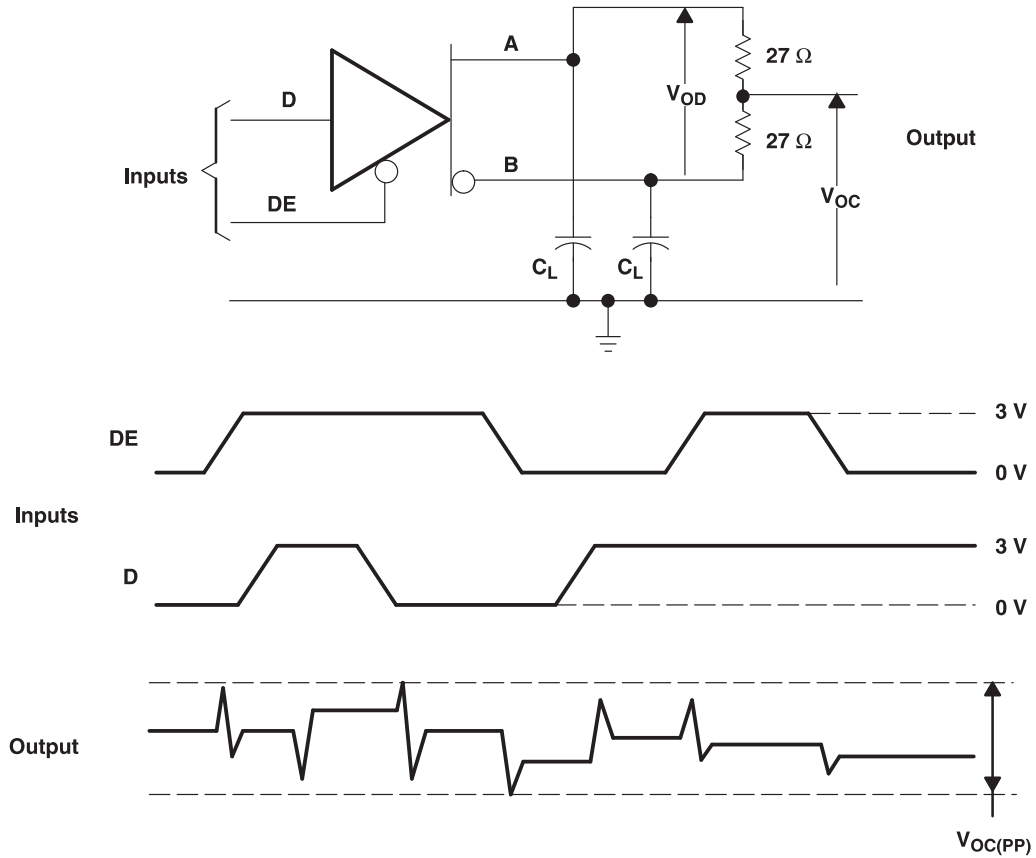


Figure 9. Driver Timing, Voltage, and Current Waveforms

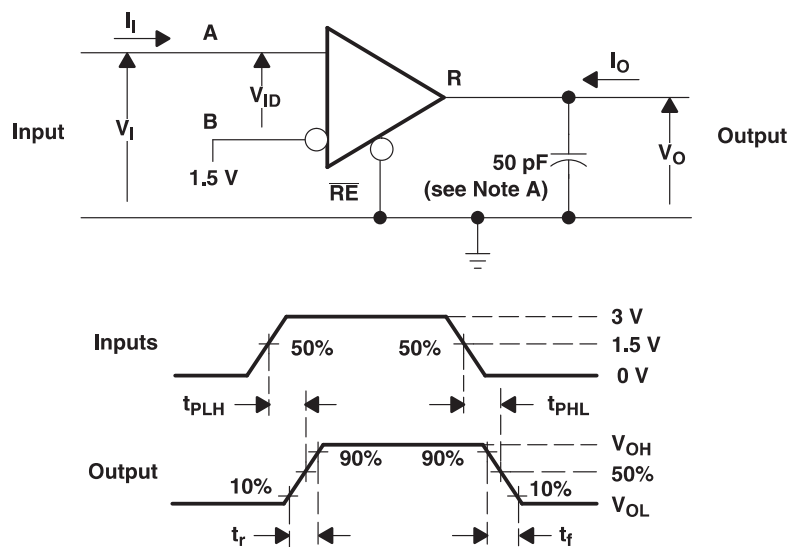


PARAMETER MEASUREMENT INFORMATION(CONTINUED)



- A. Resistance values are in ohms and are 1% tolerance.
- B. C_L includes probe and jig capacitance ($\pm 10\%$).

Figure 10. Driver $V_{OC(PP)}$ Test Circuit and Waveforms

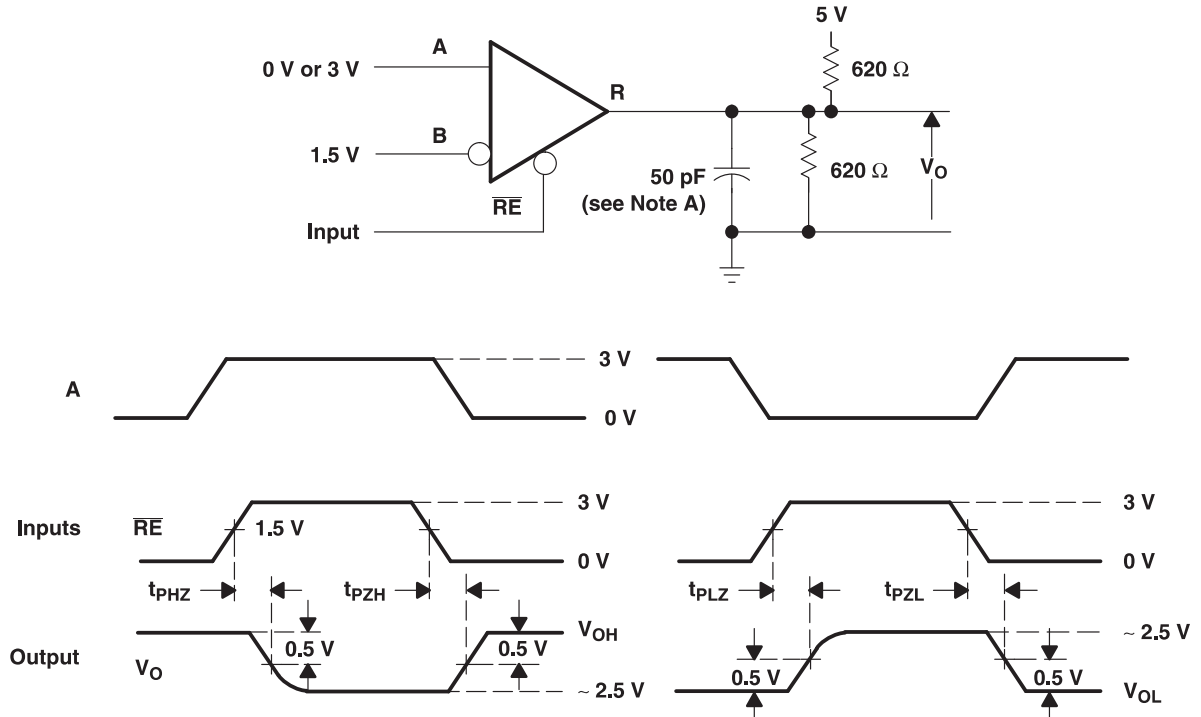


- A. This value includes probe and jig capacitance ($\pm 10\%$).

Figure 11. Receiver t_{PLH} and t_{PHL} Test Circuit and Voltage Waveforms



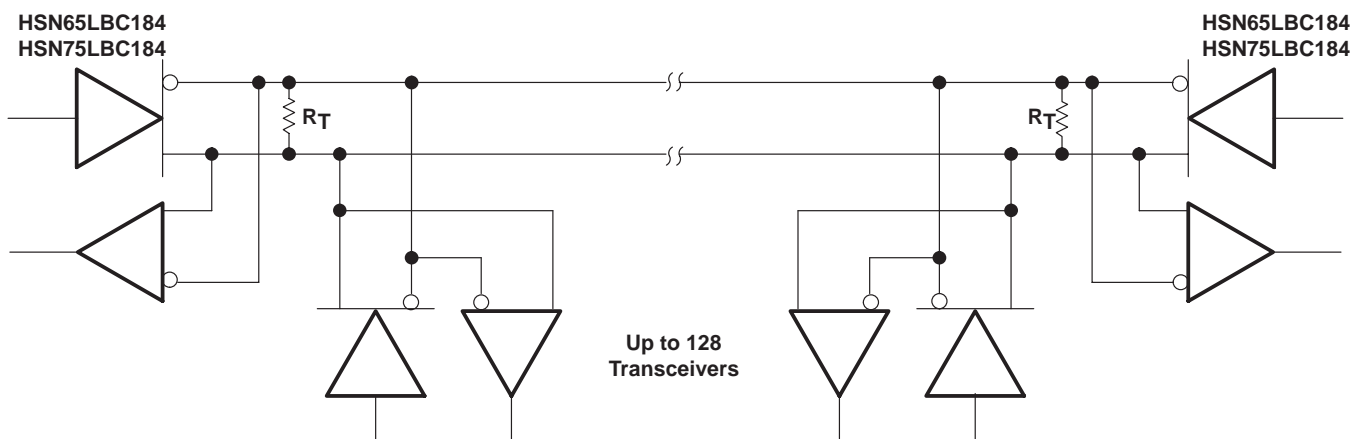
PARAMETER MEASUREMENT INFORMATION(CONTINUED)



A. This value includes probe and jig capacitance ($\pm 10\%$).

Figure 12. Receiver t_{PZL} , t_{PLZ} , t_{PZH} , and t_{PHZ} Test Circuit and Voltage Waveforms

APPLICATION INFORMATION



NOTE A: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

Figure 13. Typical Application Circuit



HSN65LBC184 TEST DESCRIPTION

The HSN65LBC184 is tested against the IEC 61000-4-5 recommended transient identified as the combination wave. The combination wave provides a 1.2-/50- μ s open-circuit voltage waveform and a 8-/20- μ s short-circuit current waveform shown in Figure 14. The testing is performed with a combination/hybrid pulse generator with an effective output impedance of 2 Ω . The setup for the overvoltage stress is shown in Figure 15 with all testing performed with power applied to the HSN65LBC184 circuit.

NOTE

High voltage transient testing is done on a sampling basis.

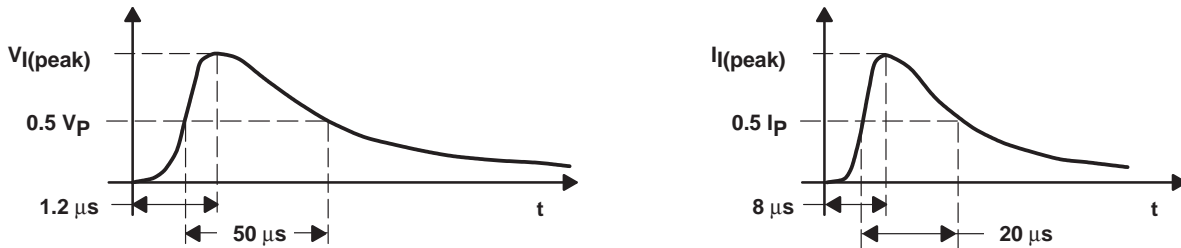


Figure 14. Short-Circuit Current Waveforms

The HSN65LBC184 is tested and evaluated for both maximum (single pulse) as well as life test (multiple pulse) capabilities. The HSN65LBC184 is evaluated against transients of both positive and negative polarity and all testing is performed with the worst-case transient polarity. Transient pulses are applied to the bus pins (A & B) across ground as shown in Figure 15.

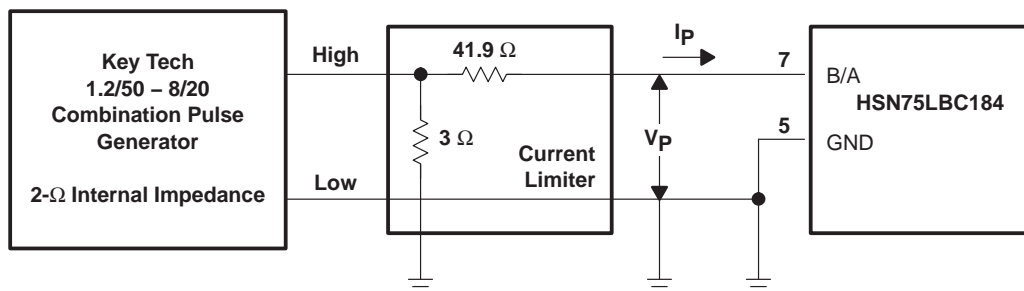


Figure 15. Overvoltage-Stress Test Circuit

An example waveform as seen by the HSN65LBC184 is shown in Figure 16. The bottom trace is current, the middle trace shows the clamping voltage of the device and the top trace is power as calculated from the voltage and current waveforms. This example shows a peak clamping voltage of 16 V, peak current of 33.6 A yielding an absorbed peak power of 538 W.

NOTE

A circuit reset may be required to ensure normal data communications following a transient noise pulse of greater than 250 W peak.

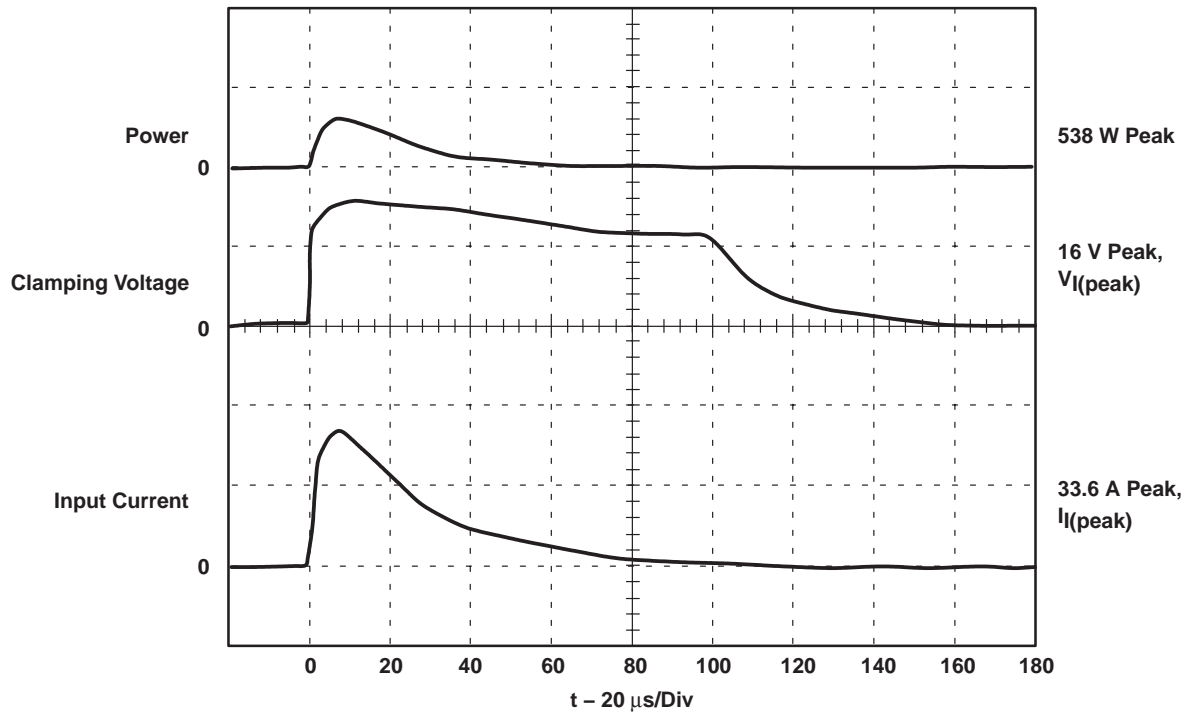


Figure 16. Typical Surge Waveform Measured At Terminals 5 and 7

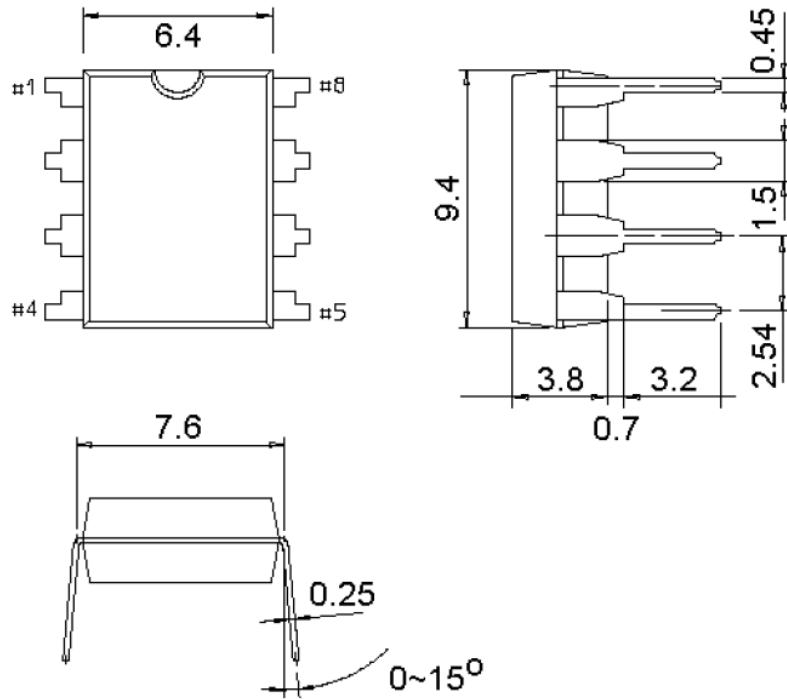
ORDERING INFORMATION

| Package | Oder No. | Compliance | Operating temperature | Supplied As |
|---------|---------------|-------------|-----------------------|-------------|
| SOP-8 | HSN65LBC184DR | RoHS, Green | -40°C to +85°C | Tube |
| DIP-8 | HSN65LBC184N | RoHS, Green | -40°C to +85°C | Tube |
| SOP-8 | HSN75LBC184DR | RoHS, Green | -0°C to +70°C | Tube |
| DIP-8 | HSN75LBC184N | RoHS, Green | -0°C to +70°C | Tube |

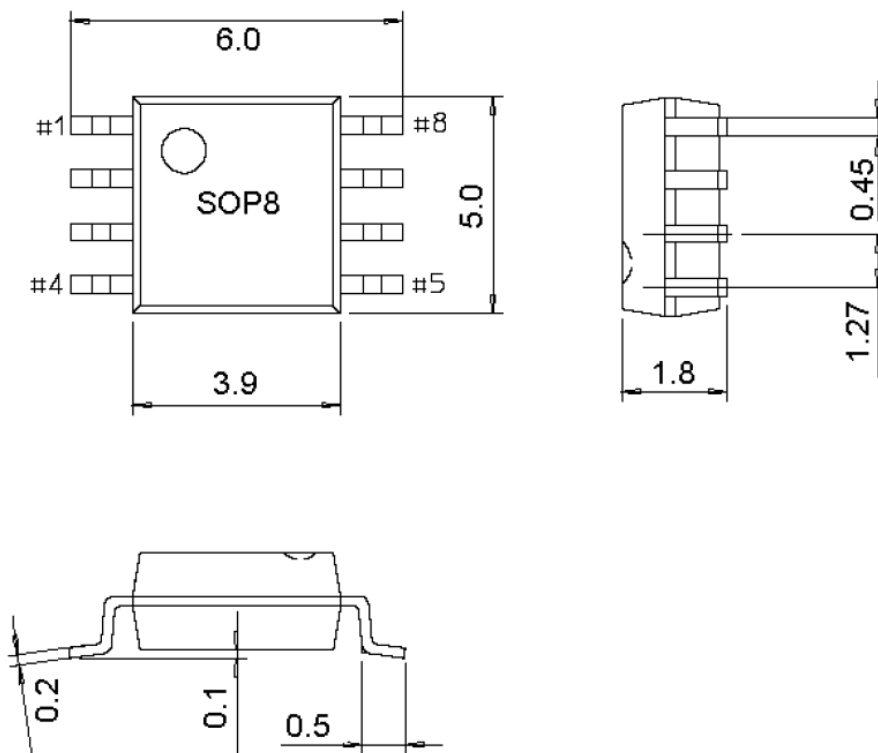


PACKAGE OUTLINE DIMENSIONS

DIP-8



SOP-8





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