RTL8822BS-CG

Single-Chip 802.11ac/a/b/g/n 2T2R WLAN with Integrated Bluetooth Smart Ready Controller With SDIO/HS-UART Mixed Interface

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.1	2015/02/24	Preliminary release.
0.2	2015/09/14	1.) Add WLAN feature
0.3	2015/09/15	1.) Add MU-MIMO description
0.4	2015/10/19	1.) Modify RF-related pin description 2.) Modify Mechanical Dimensions
0.5	2015/10/20	1.) Modify bt features description
0.6	2015/10/20	1.) Modify general description
0.7	2016/01/05	1.) Modify SDIO word
0.8	2016/03/24	1) Modify the RF block diagram 2) Modify the RF pin description 3) Add CHIP_EN, WL_DIS# power sequence timing

Notice:

Please handle the chipset with care to prevent any damage from ESD (electrostatic discharge) and EOS (electrical overstress).

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1. General Description

The Realtek RTL8822BS-CG is a highly integrated single-chip that support 2-stream 802.11ac solutions with Multi-user MIMO (Multiple-Input, Multiple-Output) with integrated Bluetooth 2.1/3.0/4.1 controller, SDIO (SDIO 1.1/2.0/3.0) interface, and HS-UART mixed interface. It combines a WLAN MAC, a 2T2R capable WLAN baseband, and RF in single chip. The RTL8822BS-CG provides a complete solution for a high-performance integrated wireless and Bluetooth device.

The RTL8822BS-CG baseband implements Multi-user Multiple Input, Multiple Output (MU MIMO) Orthogonal Frequency Division Multiplexing (OFDM) with two transmit and two receive paths (2T2R). Features include two spatial stream transmissions, short Guard Interval (GI) of 400ns, spatial spreading, and support for variant channel bandwidth. Moreover, RTL8822BS-CG provides one spatial stream space-time block code (STBC), Transmit Beamforming (TxBF) and Low Density Parity Check (LDPC) to extend the range of transmission. At the receiver, extended range and good minimum sensitivity is achieved by having receiver diversity up to 2 antennas. As the recipient, the RTL8822BS-CG also supports explicit sounding packet feedback that helps senders with beamforming capability.

For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all IEEE 802.11b, 802.11g and 802.11a data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability are available, and CCK provides support for legacy data rates, with long or short preamble. The high speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation of the individual subcarriers, and rate compatible coding rate of 1/2, 2/3, 3/4, and 5/6, provide up to 866.7Mbps for IEEE 802.11ac MIMO OFDM.

The RTL8822BS-CG builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate severe multi-path effects and mutual interference in the reception of multiple streams. For better detection quality, receive diversity with Maximal-Ratio-Combine (MRC) applying up to two receive paths is implemented. Robust interference detection and suppression are provided to protect against Bluetooth, cordless phone, and microwave oven interference.

Receive vector diversity for multi-stream application is implemented for efficient utilization of the MIMO channel. Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for the radio frequency front-end.

The RTL8822BS-CG supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control functions to obtain better performance in the analog portions of the transceiver.

The RTL8822BS-CG MAC supports 802.11e for multimedia applications, 802.11i and WAPI (Wireless Authentication Privacy Infrastructure) for security, and 802.11n/802.11ac for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, U-APSD, and MIMO power saving reduce the power wasted during idle time, and compensate for the extra power required to transmit MIMO OFDM. The RTL8822BS-CG provides simple legacy, 20MHz/40MHz/80MHz co-existence mechanisms to ensure backward and network compatibility.

2. Features

General

- TFBGA 6.5x6.5mm package
- CMOS MAC, Baseband PHY and RF in a single chip for IEEE 802.11a/b/g/n/ac compatible WLAN
- Support 802.11ac 2x2,Wave-2 compliant with MU-MIMO
- Complete 802.11n MIMO solution for 2.4GHz and 5Ghz band
- Maximum PHY data rate up to 173.3 Mbps using 20MHz bandwidth, 400Mbps using 40MHz bandwidth, and 866.7Mbps using 80MHz bandwidth.
- Backward compatible with 802.11a/b/g devices while operating at 802.11n data rates
- Backward compatible with 802.11a/n devices while operating at 802.11ac data rates.

Host Interface

- Complies with SDIO 1.1/2.0/3.0 for WLAN with clock rate up to 183MHz
- Complies with HS-UART with configurable baud rate for Bluetooth

Standards Supported

- IEEE 802.11a/b/g/n/ac compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- IEEE 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- IEEE 802.11h DFS, TPC, Spectrum Measurement
- IEEE 802.11k Radio Resource Measurement
- WAPI (Wireless Authentication Privacy Infrastructure) certified.
- Cisco Compatible Extensions (CCX) for WLAN devices

MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate Block Acknowledgement (BA)
- Long NAV for media reservation with CF-End for NAV release
- PHY-level spoofing to enhance legacy compatibility
- MIMO power saving mechanism
- Channel management and co-existence
- Multiple BSSID feature allows the RTL8822BS-CG to assume multiple MAC identities when used as a wireless bridge
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth

- WiFi Direct supports wireless peer to peer applications

Other Features

- Supports Wake-On-WLAN via Magic Packet and Wake-up frame
- Transmit Beamforming
- CCA on secondary through RTS/CTS handshake.
- Support TCP/UDP/IP checksum offload

Peripheral Interfaces

- Up to 15 General Purpose Input/Output pins
- Three configurable LED pins (mux with GPIO pins)
- Generates 40MHz clock for peripheral chip.
- Single external power source 3.3V only

PHY Features

- IEEE 802.11ac MIMO OFDM
- IEEE 802.11n MIMO OFDM
- Two Transmit and Two Receive paths
- 5MHz / 10MHz / 20MHz / 40MHz / 80MHz bandwidth transmission
- Support 2.4Ghz and 5Ghz band channels
- Short Guard Interval (400ns)
- Sounding packet.
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g, 300Mbps in 802.11n and 866.7Mbps in 802.11ac.
- OFDM receive diversity with MRC using up to 2 receive paths. Switch diversity used for DSSS/CCK
- Support STBC
- Support LDPC
- Hardware antenna diversity
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC
- Build-in both 2.4GHz and 5GHz PA
- Build-in both 2.4GHz and 5GHz LNA

Bluetooth Controller

- Compatible with Bluetooth v2.1 and v3.0 systems
- Support Bluetooth 4.1 features

- Support Bluetooth 4.2 LE Secure Connection by upper layer software upgrade
  - HS-UART interface for Bluetooth data transmission compliant with H4 and H5 specification
  - PCM interface for audio data transmission via Bluetooth controller
  - Integrated MCU to execute Bluetooth protocol stack
  - Supports all packet types in basic rate and enhanced data rate
  - Supports SCO/eSCO link (allows one link for PCM interface and three links for HS-UART)
  - Supports piconets in a scatternet
  - Supports Secure Simple Pairing
  - Supports Low Power Mode (Sniff/Sniff Sub-rating)
  - Enhanced BT/WLAN Coexistence Control to improve transmission quality in different profiles
  - Bluetooth 4.0 Dual Mode support: Simultaneous LE and BR/EDR
  - Supports multiple Low Energy states

Bluetooth Transceiver

- Fast AGC control to improve receiving dynamic range
- Supports AFH to dynamically detect channel quality to improve transmission quality
- Integrated internal Class 1, Class 2, and Class 3 PA
- Supports Enhanced Power Control
- Supports Bluetooth Low Energy
- Integrated 32K oscillator for power management

Peripheral Interfaces

- General Purpose Input/Output (8 pins)
- 4-wire EEPROM control interface (93C46)
- Three configurable LED pins
- Flexible CRYSTAL frequency selection(52, 48, 40, 38.4, 27, 26, 25, 24, 20, 19.2, 17.664, 16, 14.318, 13 and 12MHz)
- Support CRYSTAL or external clock input

3. Application Diagrams

3.1. 11ac Dual-Band 2x2 RF Application

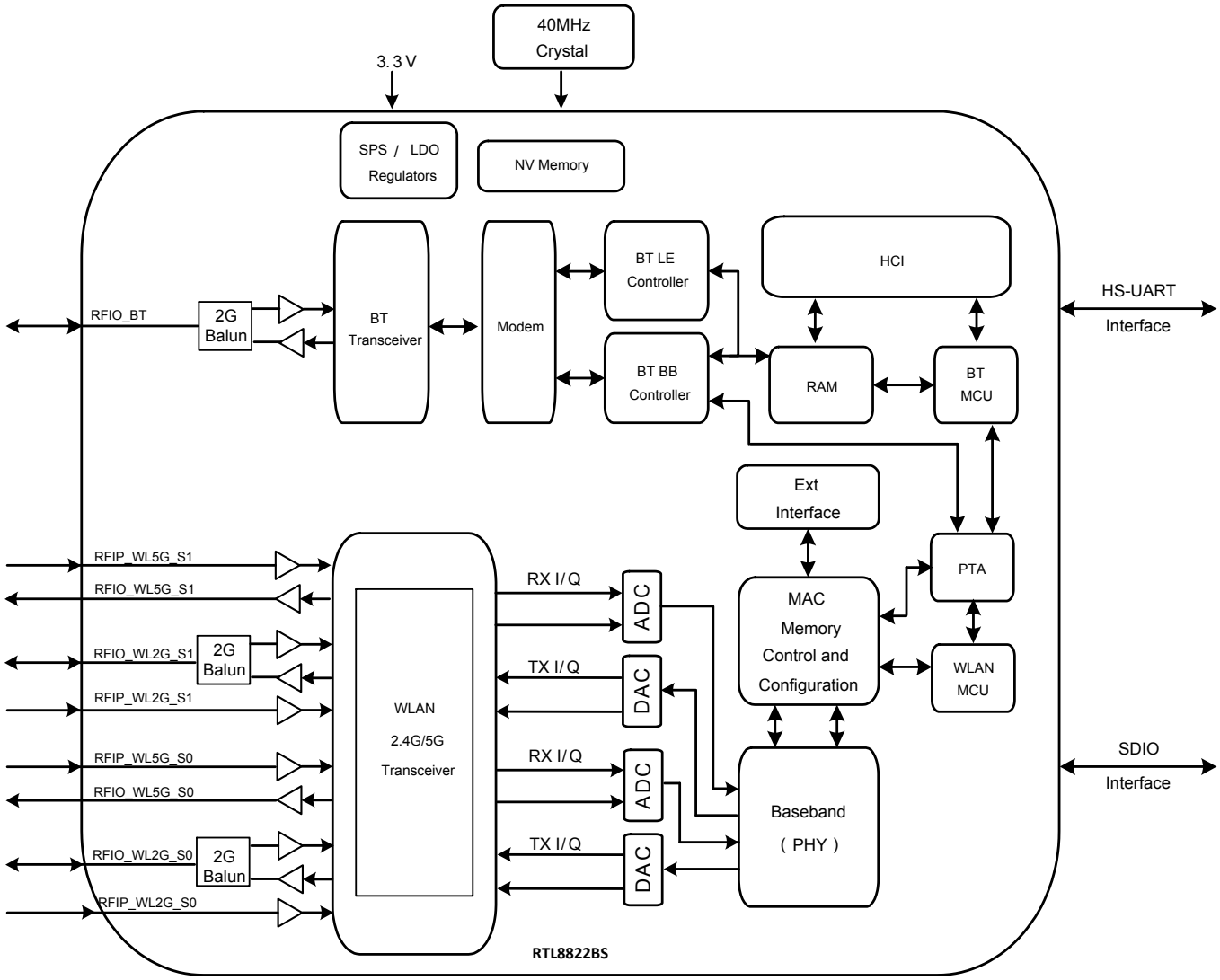


Figure 1. Dual-Band MIMO 2x2 Solution(11ac 2x2 MAC/BB/RF + PA) and Integrated Bluetooth Controller Solution --- RTL8822BS-CG

4. TFPGA Ball Assignments

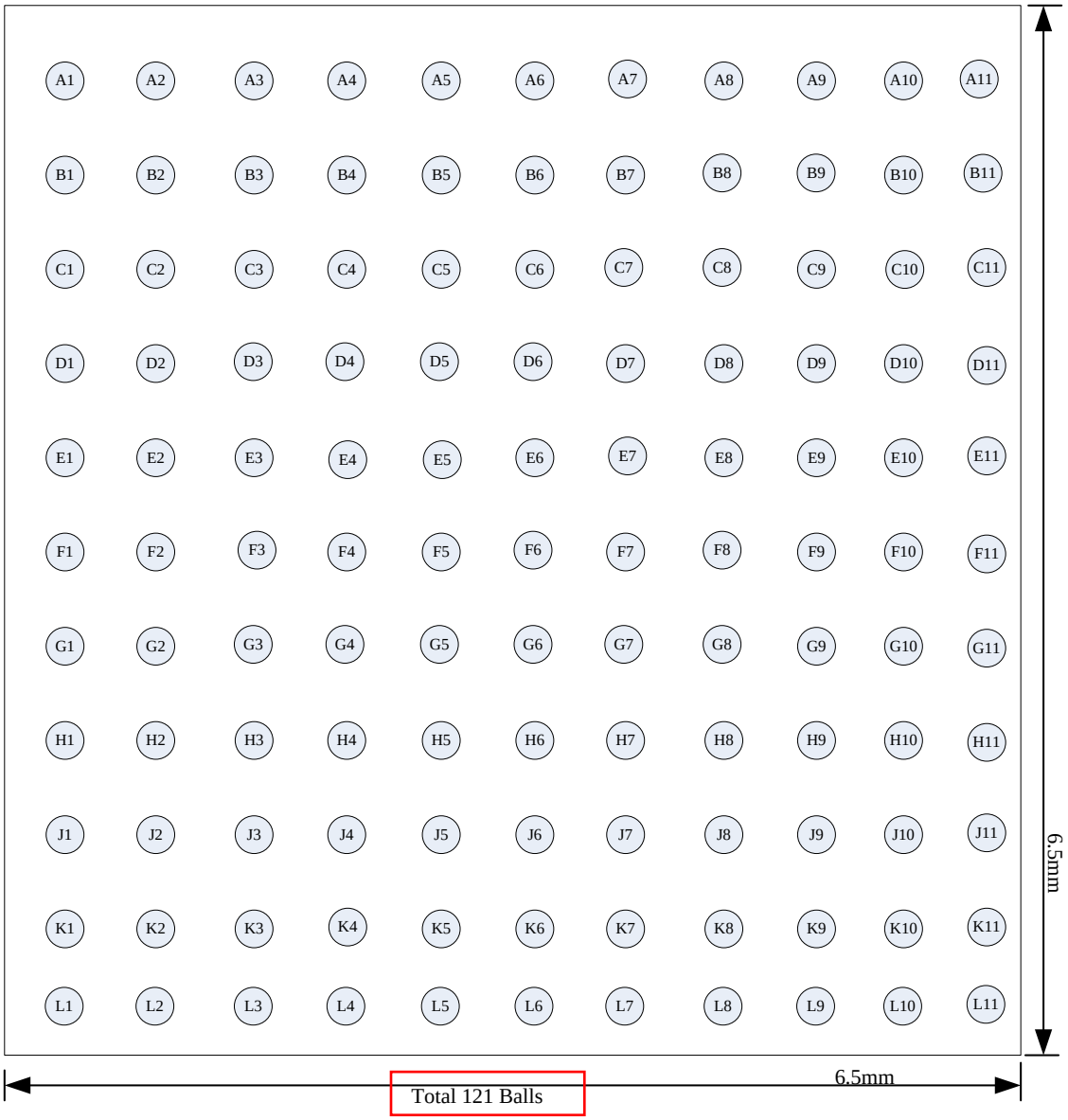


Figure 2. TFBGA Ball Assignments

4.1. Package Identification & Mark Information

Green package is indicated by a 'G' in the location marked 'T' in

Figure 2.

Mark Item	Body (mm^2)	LOGO FONT / LOGO SIZE	2.7 x 2.2 mm^2	Mark Example					備註 Remark
T69	6x6								Pin1 位置在正印的左下 Pin1 mark orientation：bottom left
	Line	Item	FONT	a (mm)	b (mm)	c (mm)	d (mm)	e (mm)	對齊 Alignment
	1	Part no.	Realtek standard	0.50	0.40	0.1	0.1	-	Left
	2	Lot no.	Realtek standard	0.50	0.40	0.1	0.1	-	Left
	3	Date Code (BDC/ADC)	Realtek standard	0.50	0.40	0.1	0.1	-	Right

5. Ball Descriptions

The following signal type codes are used in the tables:

I:	Input	O:	Output
T/S:	Tri-State bi-directional input/output pin	S/T/S:	Sustained Tri-State
O/D:	Open Drain	P:	Power pin
N/A:	No Bonding pin		

5.1. Power On Trap Pin

Table 1. Power-On Trap Pins

Symbol	Type	Ball No	Description
TEST_MODE_SEL	I	H7	Shared with GPIO4 0: Normal operation mode 1: Test/debug mode
SPS_LDO_SEL	I	J9	Shared with GPIO5 0: Internal switching regulator select 1: Internal LDO select

Symbol	Type	Ball No	Description
EEPROM_SEL	I	J10	Shared with EESK pin 0: Internal NV memory select 1: External EEPROM select

5.2. SDIO Interface

Table 2. SDIO Interface

Symbol	Type	Ball No	Description
SD_CLK	I	B11	SDIO Clock Input
SD_CMD	IO	C11	SDIO Command Input
SD_D0	IO	D11	SDIO Data Line 0
SD_D1	IO	E11	SDIO Data Line 1
SD_D2	IO	F11	SDIO Data Line 2
SD_D3	IO	G11	SDIO Data Line 3

5.3. G-SPI Interface

Table 3. G-SPI Interface

Symbol	Type	Pin No	Description
SPI_CLK	I	B11	Serial clock (output from master)
SPI_OUT (MOSI)	I	C11	Output from Master and input to slave
SPI_IN (MISO)	O	D11	Input to Master and output from slave
SPI_INT	O	E11	Active low output(output from slave)
SPI_CS (SCSn)	I	G11	Active low (output from master)

5.4. HS-UART Transceiver Interface

Table 4. HS-UART Interface

Symbol	Type	Ball No	Description
UART_TX	O	B10	High-Speed UART Data Out
UART_CTS	I	A11	High-Speed UART CTS
UART_RTS	O	A9	High-Speed UART RTS
UART_RX	I	A10	High-Speed UART Data In

5.5. EEPROM Interface

Table 5. EEPROM Interface

Symbol	Type	Ball No	Description
EECS	O	C9	External EEPROM Chip Select
EESK	O	J10	External EEPROM Clock

5.6. PCM Interface

Table 6. PCM Interface

Symbol	Type	Pin No	Description
PCM_IN	I	J8	PCM data Input, shared with GPIO0
PCM_OUT	O	H8	PCM data Out, shared with GPIO1
PCM_SYNC	O	H9	PCM Synchronization control, shared with GPIO2
PCM_CLK	IO	H10	PCM Clock, shared with GPIO3

5.7. RF Interface

Table 7. RF Interface

Symbol	Type	Ball No	Description
BT RFIO	I/O	A2	BT RF I/O
RFIP_WL5G_S1	I	C1	WLAN 5G RF input
RFIO_WL5G_S1	O	D1	WLAN 5G RF output
RFIO_WL2G_S1	I/O	F1	WLAN 2G RF input/output
RFIP_WL2G_S1	I	G1	WLAN 2G RF input (efuse configuration needed)
RFIP_WL5G_S0	I	H1	WLAN 5G RF input
RFIO_WL5G_S0	O	J1	WLAN 5G RF output
RFIO_WL2G_S0	I/O	L1	WLAN 2G RF input/output
RFIP_WL2G_S0	I	L2	WLAN 2G RF input (efuse configuration needed)
S1_TSSI	I	D5	TSSI input from external PA
S0_PAPE_5G	I	G6	GPIO for RF switch control. (refer to HDK for actual assignment)
ANTSW	O	D4	GPIO for RF switch control. (refer to HDK for actual assignment)
ANTSWB	O	E4	GPIO for RF switch control. (refer to HDK for actual assignment)
S1_PAPE_2G	O	E5	GPIO for RF switch control. (refer to HDK for actual assignment)
S1_PAPE_5G	O	D6	GPIO for RF switch control. (refer to HDK for actual assignment)
S1_TRSW	O	F6	GPIO for RF switch control. (refer to HDK for actual assignment)
S1_TRSWB	O	F5	GPIO for RF switch control. (refer to HDK for actual assignment)
S0_TSSI	I	G5	TSSI input from external PA
S0_PAPE_2G	O	H5	GPIO for RF switch control. (refer to HDK for actual assignment)
S0_TRSW	O	K7	GPIO for RF switch control. (refer to HDK for actual assignment)
S0_TRSWB	O	H6	GPIO for RF switch control. (refer to HDK for actual assignment)

5.8. LED Interface

Table 8. LED Interface

Symbol	Type	Ball No	Description
LED0	O	E6	LED Pin (Active Low)
LED1	O	E8	LED Pin (Active Low)
LED2	O	E7	LED Pin (Active Low), shared with GPIO8

5.9. Power Management Handshake Interface

Table 9. Power Management Handshake Interface

Symbol	Type	Ball No	Description
SD_RESET	I	C8	Shared with GPIO9. This pin can externally shut down the RTL8822BS-CG WLAN function when SD_RESET is pulled low. When this pin is pulled low, SDIO/G-SPI interface will be disabled.
BT_DIS#	I	C7	Shared with GPIO11. This pin can externally shut down the RTL8822BS-CG BT function when BT_DIS# is pulled Low. When this pin is pulled low, UART interface will be also disabled. This pin can be also defined as the BT Radio-off function with host interface remaining connected.
CHIP_EN	I	F9	This Pin Can externally shut down the RTL8822BS-CG (No Extra Power Switch Required). When this function is not required, external pull high is required.
WL_DIS_N	I	F10	Shared with GPIO15. This pin can be defined as the WLAN Radio-off function with host interface remaining connected. When this pin is pulled low, WLAN Radio will be disabled.

5.10. Clock and Other Pins

Table 10. Clock and Other Pins

Symbol	Type	Ball No	Description
XI	I	L5	40MHz OSC Input 40MHz crystal reference clock input
XO	O	L6	40MHz crystal reference clock output
SUS_CLK	I	C9	Shared with EECS. External 32K or RTC clock input.
GPIO0	IO	J8	General Purpose Input/ Output Pin
GPIO1	IO	H8	General Purpose Input/ Output Pin
GPIO2	IO	H9	General Purpose Input/ Output Pin
GPIO3	IO	H10	General Purpose Input/ Output Pin
GPIO4	IO	H7	General Purpose Input/ Output Pin
GPIO5	IO	J9	General Purpose Input/ Output Pin
GPIO6	IO	D7	General Purpose Input/ Output Pin
GPIO7	IO	D8	General Purpose Input/ Output Pin

Symbol	Type	Ball No	Description
GPIO8	IO	E7	General Purpose Input/ Output Pin
GPIO9	IO	C8	General Purpose Input/ Output Pin
GPIO10	IO	E10	General Purpose Input/ Output Pin
GPIO11	IO	C7	General Purpose Input/ Output Pin
GPIO12	IO	D9	General Purpose Input/ Output Pin
GPIO13	IO	D10	General Purpose Input/ Output Pin
GPIO14	IO	E9	General Purpose Input/ Output Pin
GPIO15	IO	F10	General Purpose Input/ Output Pin
RSVD		B8.B9,C10 ,F7,F8,G7, G8	Reserved

5.11. Power Pins

Table 11. Power Pins

Symbol	Type	Ball No	Description
LX_SPS	P	K10,K11	Switching Regulator Output
VD33_SPS	P	L11	Switching Regulator Input Or Linear Regulator input from 3.3V to 1.5V
VD33_IO	P	L10	VDD3.3V for Digital IO
VD33_IO	P	A7	VDD3.3V for Digital IO
VDD_IO_2	P	L8	VDD for GPIO0 to GPIO5 and EESK
VDD_IO_1	P	B7	VDD for GPIO6,GPIO7,GPIO9,GPIO11,GPIO12 and EECS.
VD10D_WL	P	H11	1.05V for WLAN digital power
VD10D_FB_WL	P	L9	1.05V for WLAN digital power
VD10D_BT	P	A6	1.05V for BT digital power
GND_SPS	P	J11	Switching Regulator Ground
VDDIO_HOST	P	A8	supply voltage for SDIO IO
GND_CORE	P	B6,C6,G10,G9, K8,K9	Digital GND
VD1_BT	P	A1	VDD 1.05V for BT RF
VD33_PA_BT	P	A3	VDD 3.3V for BT PA
VD1_SYN_BT	P	A4	VDD 1.05V for BT synthesizer
VD33_SYN_BT	P	C4	VDD 3.3V for BT synthesizer
VD1_AFE_BT	P	A5	VDD 1.05V for BT AFE
VD33_AFE_BT	P	C5	VDD 3.3VV for BT AFE
GND_RF_BT	P	B2	Ground for BT RF
GND_BALUN_B T	P	B3	Ground for BT RF
GND_SYN_BT	P	B4	Ground for BT RF
GND_AFE_BT	P	B5	Ground for BT AFE
VD1_RF_WLS1	P	B1	VDD 1.05V for WLAN RF
VD33_PA_WLS1	P	E1	VDD 3.3V for WLAN PA
VD33_PAD_WLS 1	P	E2	VDD 3.3V for WLAN PAD

Symbol	Type	Ball No	Description
VD1_RF_WLS0	P	G2	VDD 1.05V for WLAN RF
VD33_PA_WLS0	P	K1	VDD 3.3V for WLAN PA
VD33_PAD_WLS0	P	J2	VDD 3.3V for WLAN PAD
GND_RF1_WL	P	C2,C3	Ground of WLAN RF
GND_RF2_WL	P	D2,D3,E3,F2,F3,F4,G4	Ground of WLAN RF
GND_RF3_WL	P	G3	Ground of WLAN RF
GND_RF4_WL	P	H2,H3,H4,J3,J4,K2 K3	Ground of WLAN RF
VD1_SYN_WL	P	L3	VDD 1.05V for WLAN synthesizer
VD33_SYN_WL	P	L4	VDD 3.3V for WLAN synthesizer
GND_SYN_WL	P	K4	Ground for WLAN synthesizer
VD1_AFE_WL	P	L7	VDD 1.05V for WLAN AFE
GND_AFE_WL	P	J6,J7	Ground for WLAN AFE
VD33X	P	K6	VDD 3.3V for crystal
GND_XTAL	P	K5	Ground for crystal
CAP_XTAL	P	J5	LDO output . External CAP 1uF is needed.

6. Electrical and Thermal Characteristics

6.1. Temperature Limit Ratings

Table 12. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

6.2. DC Characteristics

6.2.1. Power Supply Characteristics

Table 13. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VD33	3.3V I/O Supply Voltage	3.0	3.3	3.6	V
VD10	1.05V Core Supply Voltage	0.945	1.05	1.155	V

6.2.2. Digital IO Pin DC Characteristics

Table 14. 3.3V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	2.0	3.3	3.6	V
V_{IL}	Input low voltage	--	0	0.9	V
V_{OH}	Output high voltage	2.97	--	3.3	V
V_{OL}	Output low voltage	0	--	0.33	V

PS. 3.3V and 1.2V ripple < 100mV

7. Interface Timing Specification

7.1. SDIO Interface AC Characteristics

For timing criteria, please check “SD specifications Part1 Physical Layer Specification Version 3.01”

7.2. SDIO/G-SPI Interface Signal Levels

The SDIO and G-SPI signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8822BS-CG SDIO and G-SPI interfaces via the VDDIO_HOST pin (Ball A8).

7.2.1. SDIO/G-SPI Interface Characteristics

■ SDIO Interface Timing

For timing criteria, please check specification in "SD specifications Part1 Physical Layer Specification Version 3.01"

■ G-SPI Interface Timing

A high-to-low transition on the SPI_CS pin is required to start a SPI bus transaction, and a low-to-high transition is required at the end the transaction.

SPI_IN and SPI_OUT data transient are driven by the falling edge of the SPI_CLK and latch the data at the rising edge of the SPI_CLK. The data bit shift out order on the SPI_IN and SPI_OUT is from MSB to LSB (MSB first, LSB last).

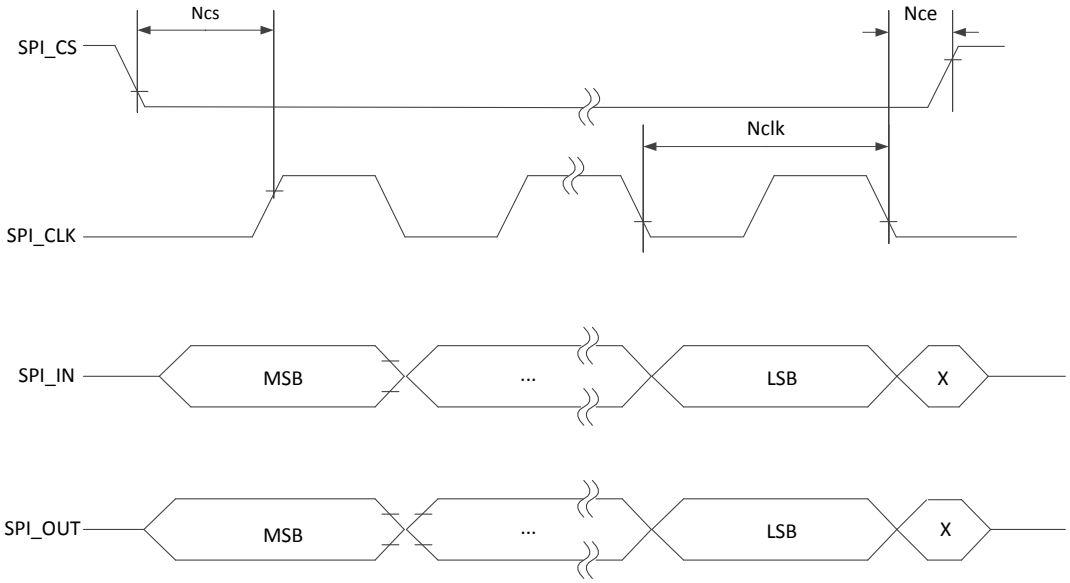


Figure 3. G-SPI Timing

Table 15. G-SPI Timing

Parameter	Min	Max	Unit
Nclk	-	25	MHz
Ncs	20	-	ns
Nce	20	-	ns

7.3. Power Management Handshake Interface Signal Level

■ SD_RESET Signal Level

The SD_RESET signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8822BS-CG via the VDD_IO_1 pin (Ball B7)

■ BT_DIS# Signal Level

The BT_DIS# signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8822BS-CG via the VDD_IO_1 pin (Ball B7)

■ CHIP_EN Signal Level

The CHIP_EN signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8822BS-CG via the VDD_IO_2 pin (Ball L8)

■ WL_DIS_N Signal Level

The WL_DIS_N signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8822BS-CG via the VDD_IO_2 pin (Ball L8)

7.4. System Power Sequence

7.4.1. System Power On Sequence

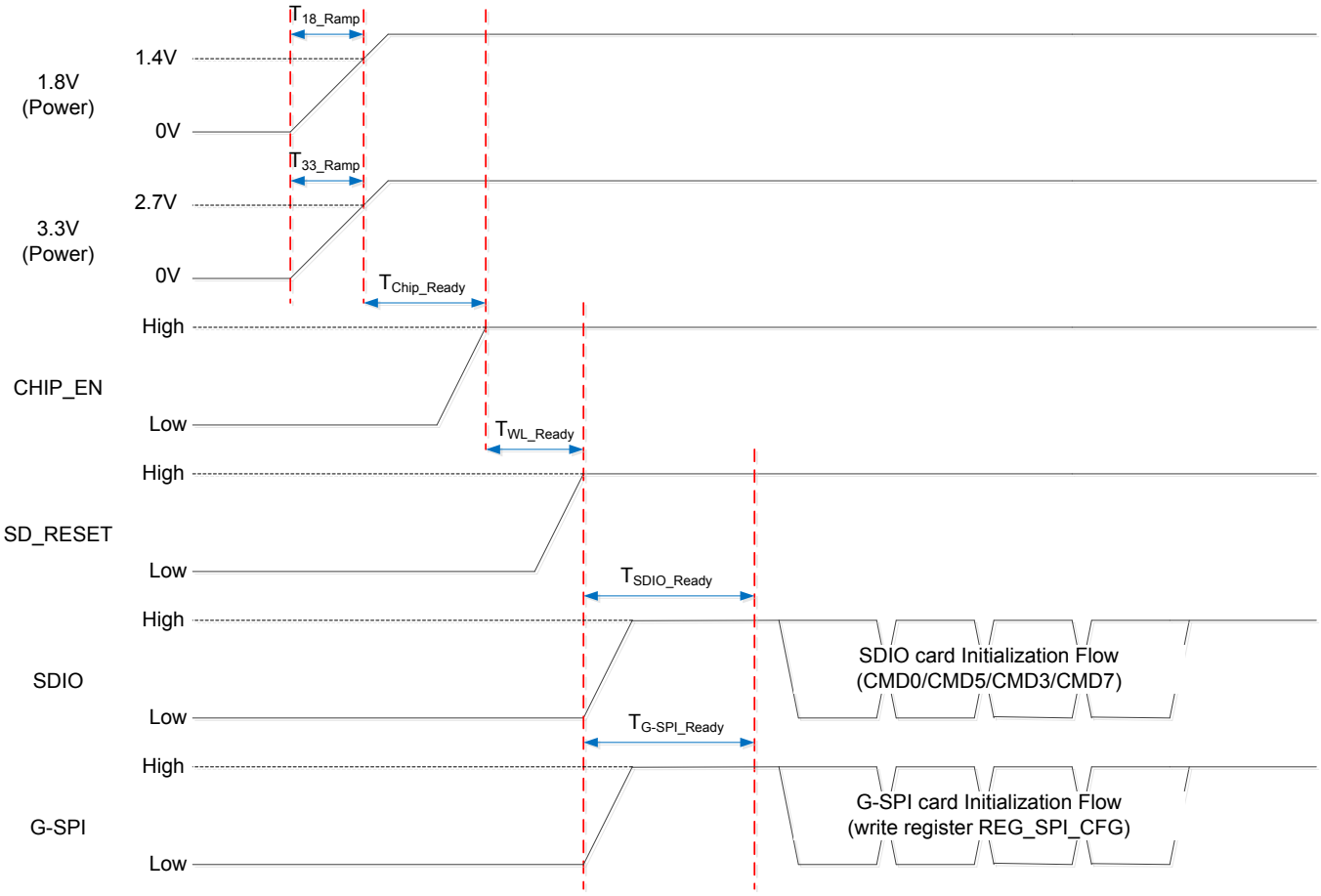


Figure 4. System Power-On Sequence

Table 16. System Power On Timing Parameters

	Min	Typical	Max	Unit	Description
T_{18_Ramp}	0.1	0.5	2.5	ms	The 1.8V main power ramp up duration.
T_{33_Ramp}	0.1	0.5	2.5	ms	The 3.3V main power ramp up duration.
T_{Chip_Ready}	0	10	X	ms	CHIP_EN pull high timing
T_{WL_Ready}	0	10	X	ms	SD_RESET pull high timing
T_{SDIO_Ready}	1	2	10	ms	SDIO Not Ready Duration. In this state, the RTL8822BS-CG may respond to commands without the ready bit being set. After the ready bit is set, the host will initiate complete card detection procedure.
$T_{G\text{-}SPI\_Ready}$	3	4	18	ms	The duration G-SPI device internal initialization. After

					$T_{G\text{-}SPI\_Ready}$, SPI host can then send command to write REG_SPI_CFG register. REG_SPI_CFG register is to control G-SPI endian and word length.

■ SDIO Interface Power On Sequence

After power-on, the SDIO interface is selected by the RTL8822BS-CG automatically when a valid SDIO command is received. To attain better SDIO host compatibility, the following power-on sequence is recommended.

We recommend that the card detection procedures are divided into two phases: A 3.3V/1.8V power pre-charge phase and a formal power-up phase.

After main 3.3V ramp up and 1.8V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enables the SDIO block. eFUSE is then autoloaded to SDIO circuits during the T_{SDIO_Ready} duration and then SDIO pins are pulled up. After CMD5/5/3/7 procedures, card detection is executed.

■ G-SPI Interface Power On Sequence

The G-SPI interface is enabled automatically when a valid G-SPI command is first received. The recommended power on sequence is as follows:

After main 3.3V/1.8V ramp up, the power management unit will be enabled by power ready detection circuit, and enables G-SPI block. Efuse is then autoloaded to G-SPI circuits, and the internal power circuits are configured during $T_{G\text{-}SPI\_Ready}$ duration.

■ SD_RESET Power On Sequence

To attain SD_RESET capability, the following power sequence is recommended.

After main 3.3V/1.8V ramp up, the power management unit is enabled by the power ready detection circuit.

The power management unit enables the SD_RESET function. After power management unit being enabled, SD_RESET needs to keep high for ensuring WLAN and SDIO/G-SPI function being alive.

■ CHIP_EN Power On Sequence

To attain CHIP_EN capability, the following power sequence is recommended.

After main 3.3V/1.8V ramp up, the power management unit is enabled by the power ready detection circuit.

The power management unit enables the CHIP_EN function. After power management unit being enabled, CHIP_EN needs to keep high for ensuring RTL8822BS-CG function being alive.

7.4.2. WLAN and SDIO/G-SPI Reset Sequence

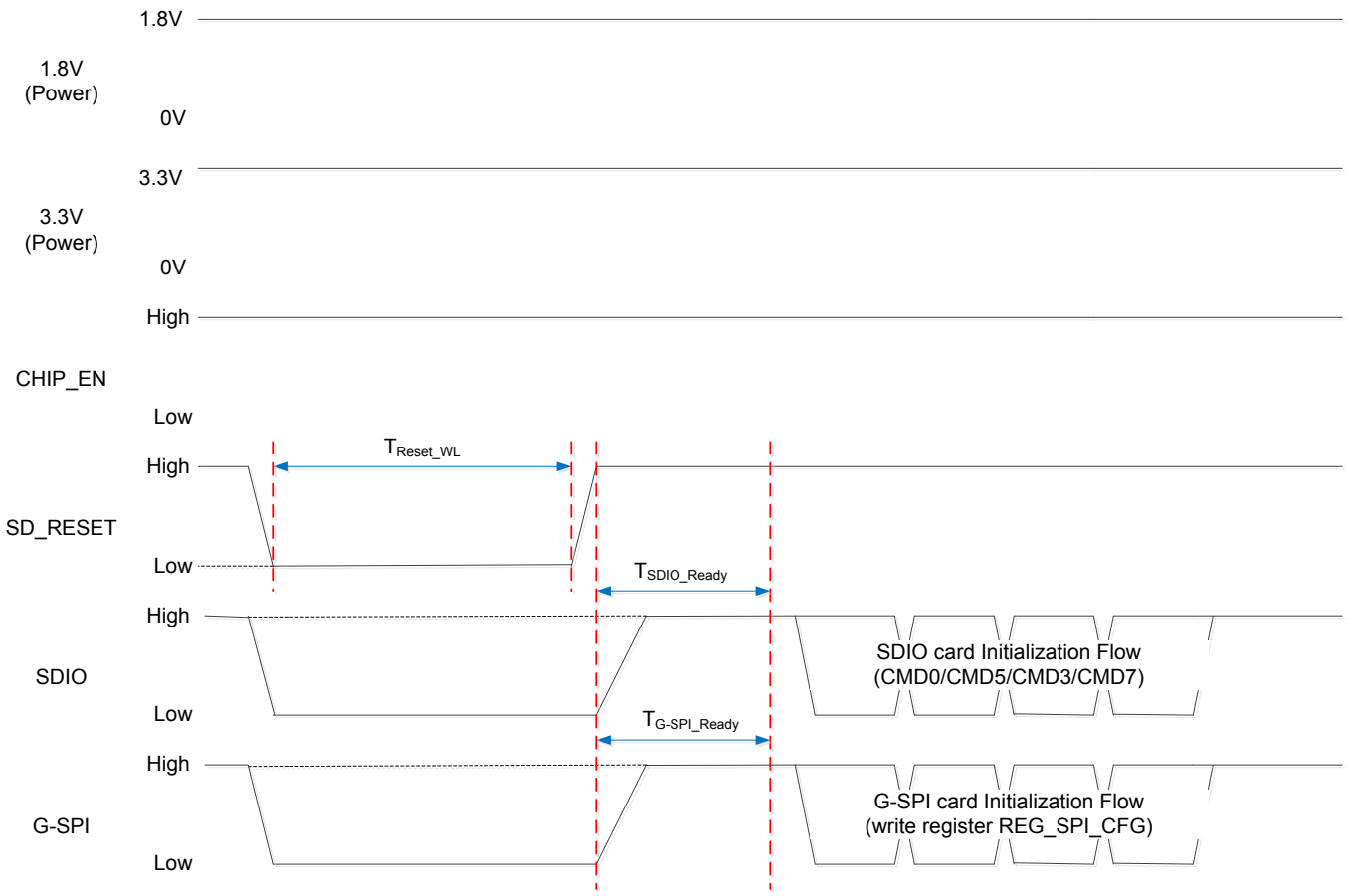


Figure 5. WLAN and SDIO/G-SPI Reset Sequence

Table 17. WLAN and SDIO/G-SPI Reset Timing Parameters

	Min	Typical	Max	Unit	Description
T_{Reset_WL}	10	10	X	ms	SD_RESET keep low duration
T_{SDIO_Ready}	1	2	10	ms	SDIO Not Ready Duration. In this state, the RTL8822BS-CG may respond to commands without the ready bit being set. After the ready bit is set, the host will initiate complete card detection procedure.
$T_{G\text{-}SPI\_Ready}$	3	4	18	ms	The duration G-SPI device internal initialization. After $T_{G\text{-}SPI\_Ready}$, SPI host can then send command to write REG_SPI_CFG register. REG_SPI_CFG register is to control G-SPI endian and word length.

■ WLAN Reset Sequence

SD_RESET can externally reset the RTL8822BS-CG WLAN function by pulled SD_RESET low and then pulled high. The keeping low duration must be more than T_{Reset_WL}.

When SD_RESET pulled low, SDIO/G-SPI interface will be disabled. After WLAN reset, SDIO/G-SPI card initialization is needed.

7.4.3. WLAN and SDIO/G-SPI Power Off Sequence

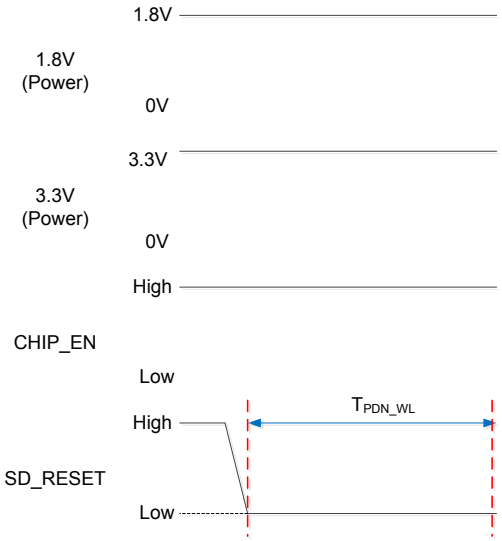


Figure 6. WLAN and SDIO/G-SPI Power Off Sequence

Table 18. WLAN and SDIO/G-SPI Power Off Timing Parameters

	Min	Typical	Max	Unit	Description
T_{PDN_WL}	100	100	X	ms	SD_RESET keep low duration

SD_RESET can externally shutdown the RTL8822BS-CG WLAN and SDIO/G-SPI function when SD_RESET is pulled low. The keeping low duration must be more than T_{PDN_WL}.

7.4.4. RTL8822BS-CG Power Off Sequence

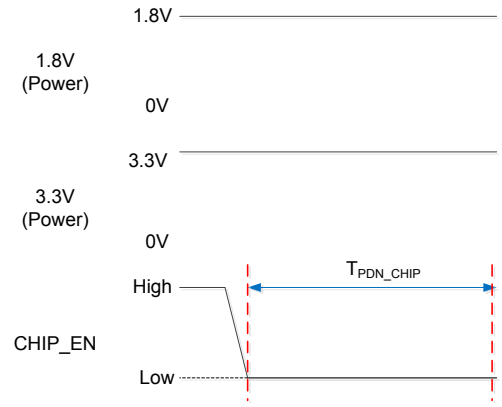


Figure 7. RTL8822BS-CG Power Off Sequence

Table 19. RTL8822BS-CG Power Off Timing Parameters

	Min	Typical	Max	Unit	Description
T_{PDN_CHIP}	100	100	X	ms	CHIP_EN keep low duration

CHIP_EN can externally shutdown the RTL8822BS-CG when CHIP_EN is pulled low. The keeping low duration must be more than T_{PDN_CHIP}

7.4.5. WLAN Radio On/Off Sequence

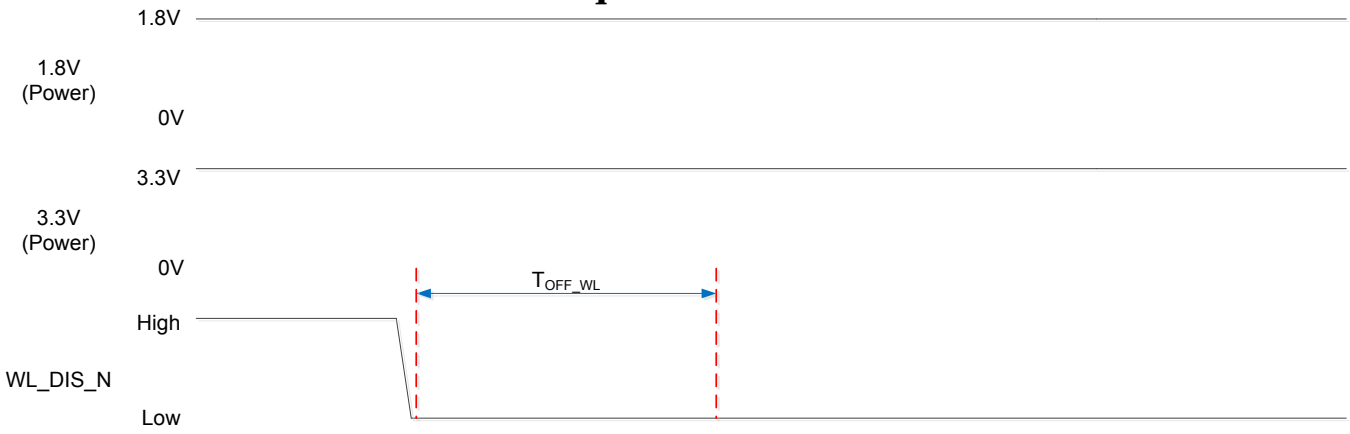


Figure 8. WLAN Radio Off Sequence

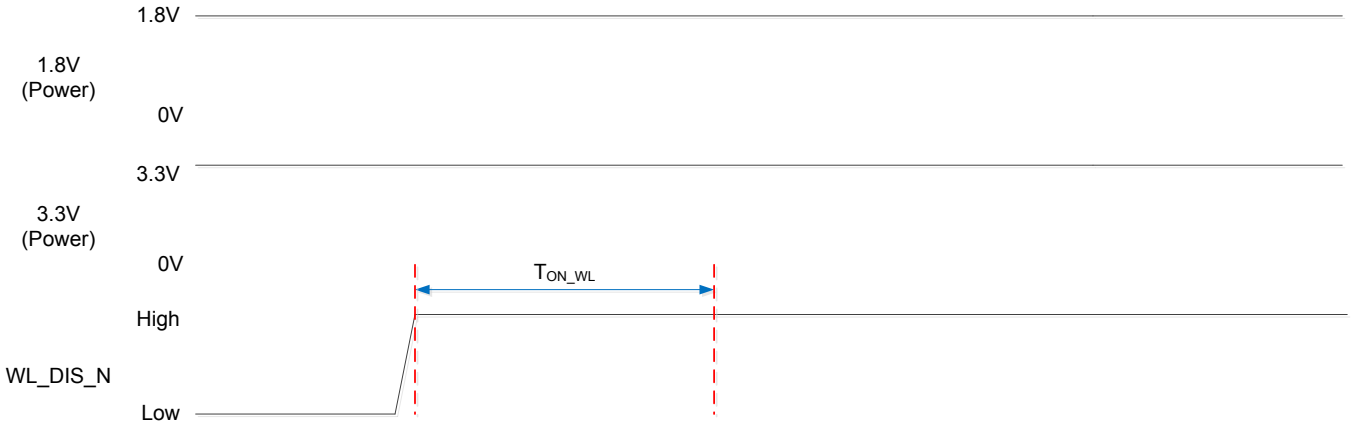


Figure 9. WLAN Radio On Sequence

WL_DIS_N can be defined as the WLAN Radio-off function with host interface remaining connected.
When WL_DIS_N is pulled low, WLAN Radio will be disabled. The keeping low duration must be more than T_{OFF_WL}.
When WL_DIS_N is pulled high, WLAN Radio will be enabled. The keeping high duration must be more than T_{ON_WL}.

Table 20. WLAN Radio On/Off Timing Parameters

	Min	Typical	Max	Unit	Description
T_{OFF_WL}	100	100	X	ms	WL_DIS_N keep low duration
T_{ON_WL}	100	100	X	ms	WL_DIS_N keep high duration

7.4.6. Power Reset Sequence

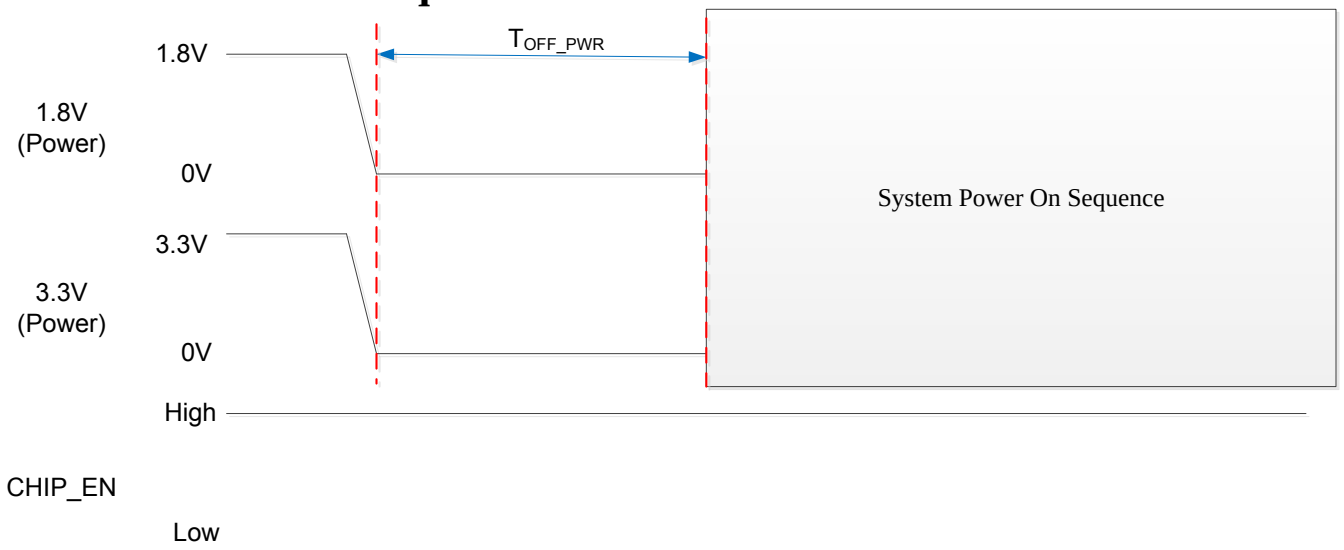


Figure 10. Power Reset Sequence

Main 3.3V/1.8V power should keep low at least T_{OFF_PWR} before calling system power on Sequence. CHIP_EN should be pulled high during power reset sequence.

Table 21. Power Reset Timing Parameters

	Min	Typical	Max	Unit	Description
T_{OFF_PWR}	100	100	X	ms	3.3V/1.8V power keep low duration

UART Interface Characteristics

The RTL8822BS-CG UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. The interface supports the Bluetooth 2.0 UART HCI H4 and H5 specifications. The default baud rate is 115.2 kbaud. In order to support high and low speed baud rate, the RTL8822BS-CG provides multiple UART clocks.

Table 22. UART Interface Power-On Timing Parameters

Desired Baud Rate	Error	Desired Baud Rate	Error
1200	0%	1382400	-0.22%
9600	0%	1444400	-0.20%
14400	0%	1500000	-0.31%
19200	0.01%	1843200	-0.22%
28800	0.01%	2000000	0%
38400	0.04%	2100000	0.25%
57600	0.01%	2500000	0%
76800	0.04%	2764800	-0.22%
115200	-0.08%	3000000	-0.31%
128000	0%	3250000	0.47%
153600	-0.08%	3692300	-0.38%
230400	-0.08%	3710000	0.29%
460800	-0.08%	3750000	0.39%
500000	0%	3800000	0.25%
921600	-0.22%	4000000	0%
1000000	0%		

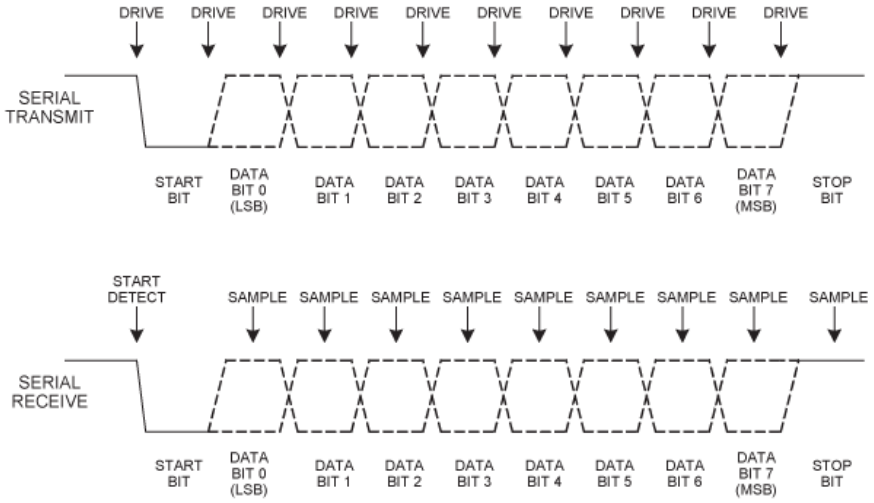


Figure 11. UART Interface Waveform

7.4.7. UART Interface Signal Levels

The UART signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8822BS-CG UART interface via the VIO_HOST pin .

7.4.8. UART Interface Power-On Sequence

The UART interface power-on sequence differs depending on whether or not host flow control is supported.

UART Hardware Flow Control Not Supported

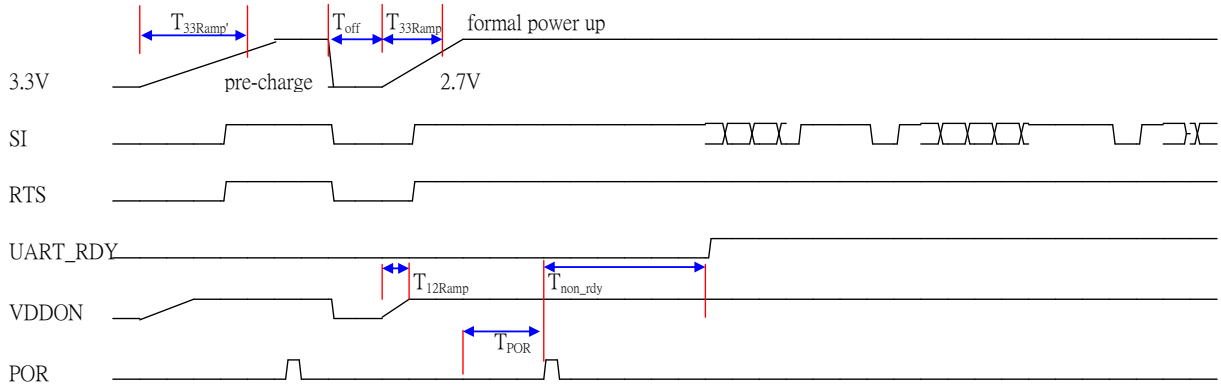


Figure 12. UART Power-On Sequence Without Hardware Flow Control

UART Hardware Flow Control Supported

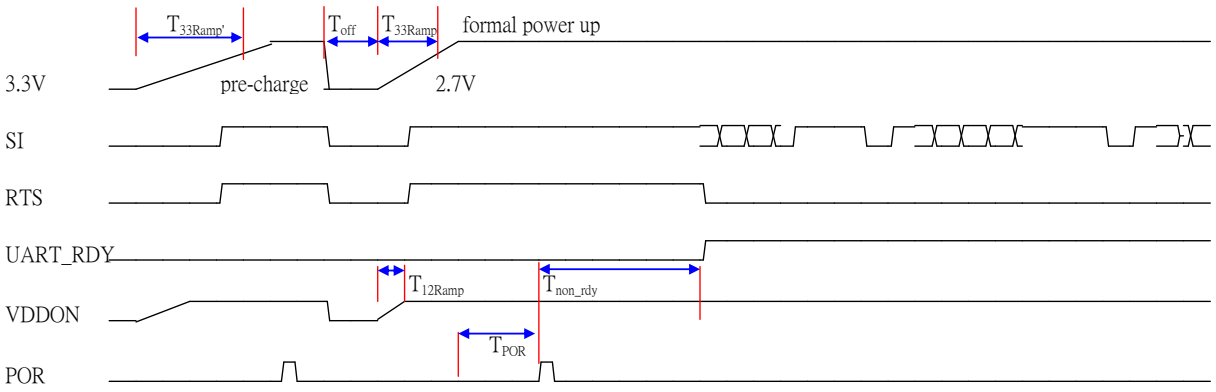


Figure 13. UART Power On Sequence With Hardware Flow Control

Table 23. UART Interface Power-On Sequence

Symbol	Description
T_{33ramp}	3.3V Power Pre-Charge Ramp Up Duration Before Formal Power Up. We recommend that a 3.3V power-on and then power-off sequence is executed by the host controller before the formal power on sequence. This procedure can eliminate host card detection issues when power ramp up duration is too long, or when a system warm reboot fails.
T_{off}	The duration 3.3V is cut off before formal power up.
T_{33ramp}	The 3.3V main power ramp up duration.
T_{12ramp}	The internal 1.2V ramp up duration.
T_{POR}	The duration from when the power-on reset releases and the power management unit executes power on tasks. A power on reset will detect both 3.3V and 1.2V power ramp up after a predetermined duration.
T_{non_rdy}	UART Not Ready Duration. In this state, the RTL8822BS-CG will not respond to any commands.

We recommend that the card detection procedures are divided into two phases: A 3.3V power pre-charge phase and a formal power-up phase.

During the 3.3V power pre-charge phase, the power ramp up duration is not limited. The 3.3V power is cut off and is turned on after the T_{off} period. The ramp up time is specified in the T_{33ramp} duration.

After main 3.3V ramp up and 1.2V ramp up, the power management unit is enabled by the power ready detection circuit. The power management unit enables the Bluetooth block. The Bluetooth firmware then initializes all circuits, included the UART. In addition to wait the T_{non_rdy} time, if the host supports UART hardware flow control it can detect RTS signals and follow the formal UART flow control handshake.

Table 24. UART Interface Power On Timing Parameters

	Min	Typical	Max	Unit
T_{33ramp}	-	-	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.1	0.5	2.5	ms

	Min	Typical	Max	Unit
T_{12ramp}	0.1	0.5	1.5	ms
T_{por}	2	2	8	ms
$T_{non-rdy}$	1	2	10	ms

7.5. PCM Interface Characteristics

The RTL8822B supports a PCM digital audio interface that is used for transmitting digital audio/voice data to/from the Audio Codec. Features are supported as below:

- Supports Master and Slave mode
- Programmable long/short Frame Sync
- Supports 8-bit A-law/μ-law, and 13/16-bit linear PCM formats
- Supports sign-extension and zero-padding for 8-bit and 13-bit samples
- Supports padding of Audio Gain to 13-bit samples
- PCM Master Clock Output: 64, 128, 256, or 512kHz
- Supports SCO/ESCO link

7.5.1. PCM Format

FrameSync is the synchronizing function used to control the transfer of DAC_Data and ADC_Data. A Long FrameSync indicates the start of ADC_Data at the rising edge of FrameSync (Figure 14), and a Short FrameSync indicates the start of ADC_Data at the falling edge of FrameSync (Figure 15).

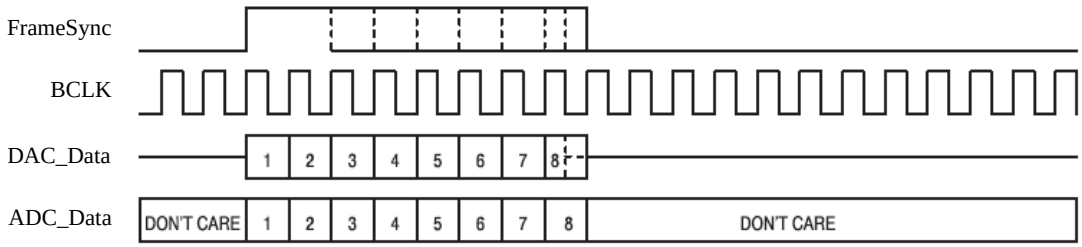


Figure 14. Long FrameSync

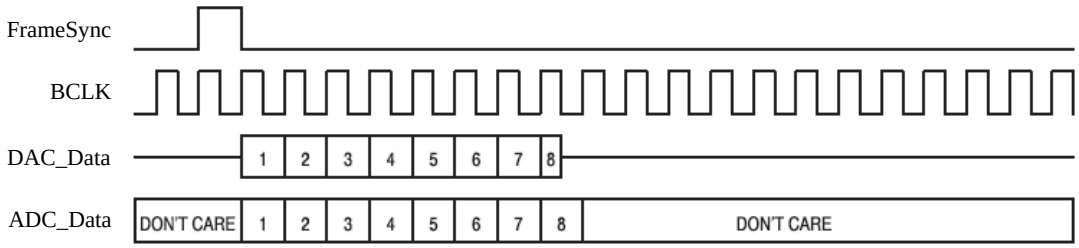


Figure 15. Short FrameSync

7.5.2. Sign Extension and Zero Padding for 8-Bit and 13-Bit Samples

For 16-bit linear PCM output, 3 or 8 unused bits may be sign extended/zero padded.

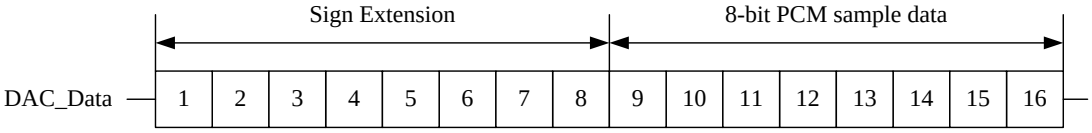


Figure 16. 16-Bit Output Data with 8-Bit PCM Sample Data and Sign Extension

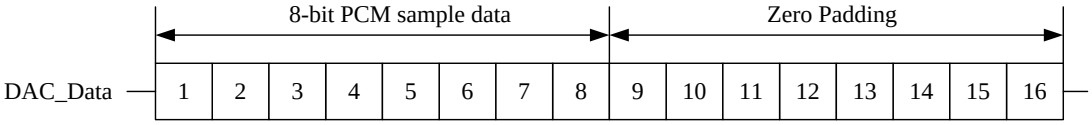


Figure 17. 16-Bit Output Data with 8-Bit PCM Sample Data and Zero Padding

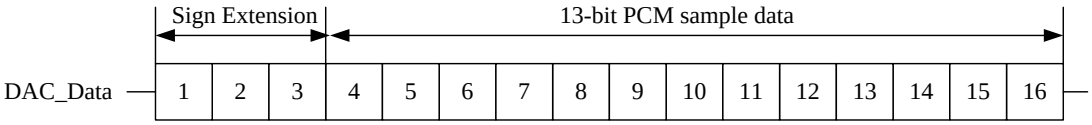


Figure 18. 16-Bit Output Data with 13-Bit PCM Sample Data and Sign Extension

For 16-bit linear PCM output, 3-bit programmable audio gain value can be padded to 13-bit sample data.

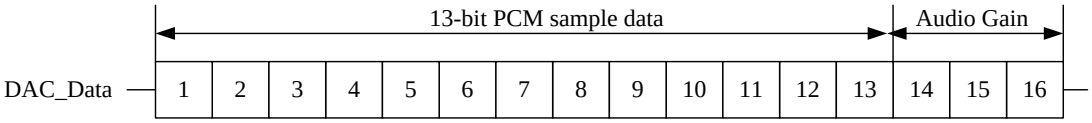


Figure 19. 16-Bit Output Data with 13-Bit PCM Sample Data and Audio Gain

7.5.3. PCM Interface Timing

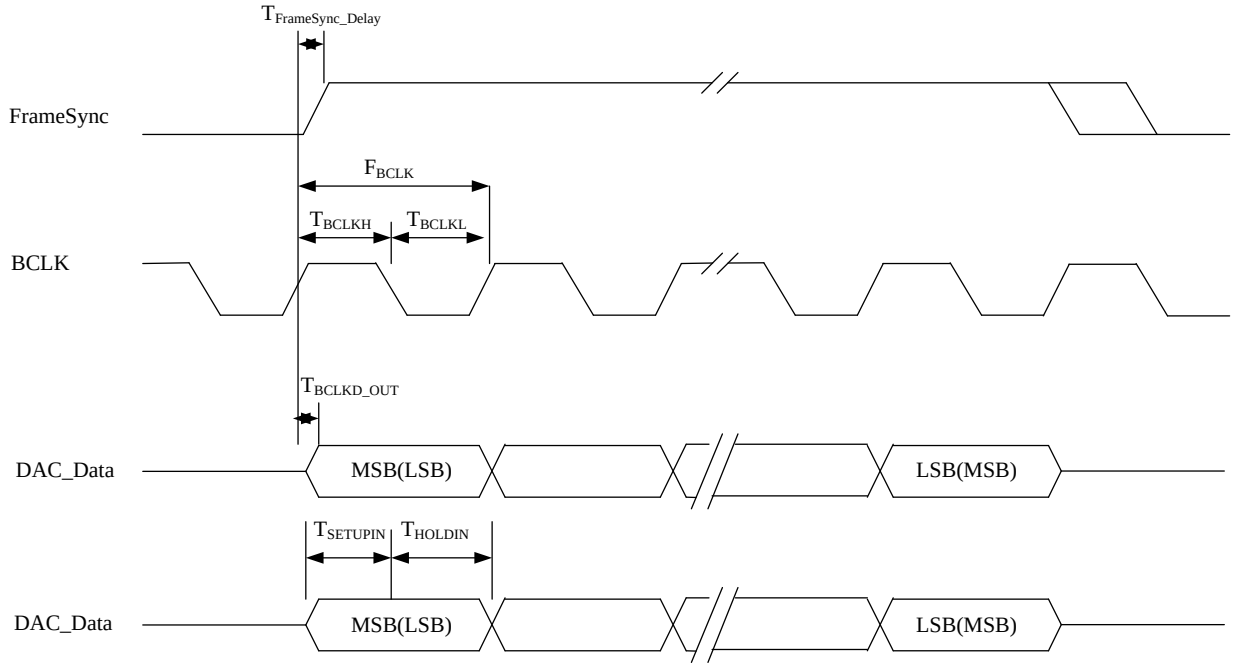


Figure 20. PCM Interface (Long FrameSync)

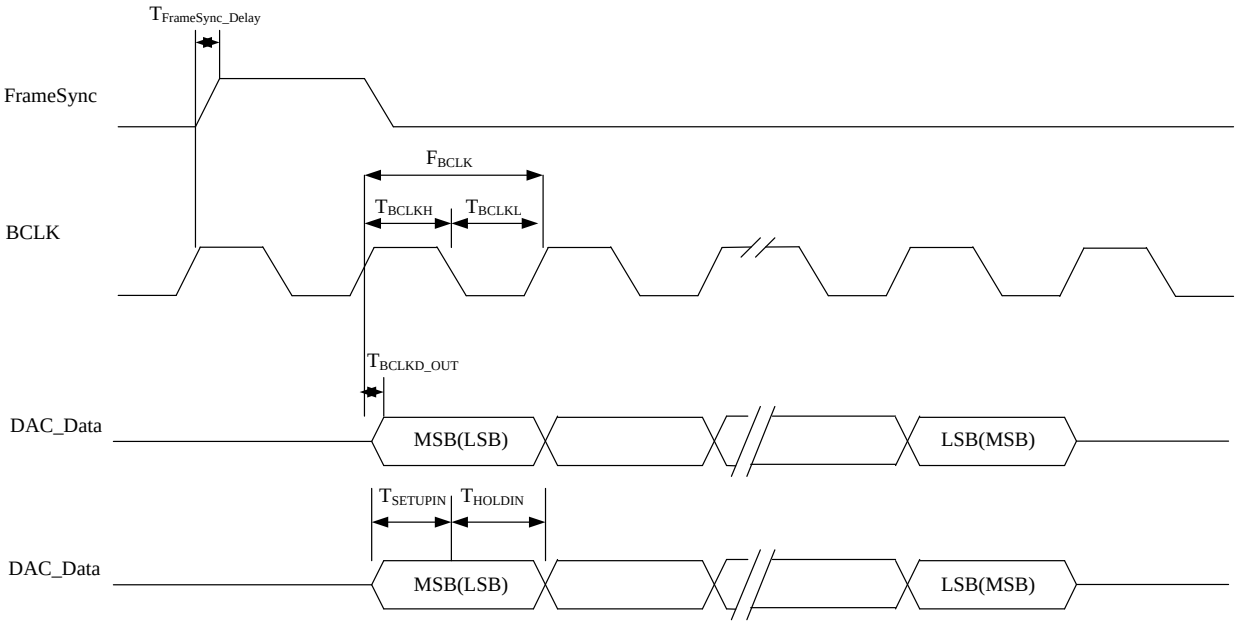


Figure 21. PCM Interface (Short FrameSync)

Table 25. PCM Interface Clock Specifications

Symbol	Description	Min.	Typ.	Max.	Unit
F_{BCLK}	Frequency of BCLK (Master)	64	-	512	kHz
$F_{FrameSync}$	Frequency of Frame Sync (Master)	-	8	-	kHz
F_{BCLK}	Frequency of BCLK (Slave)	64	-	512	kHz
$F_{FrameSync}$	Frequency of Frame Sync (Slave)	-	8	-	kHz
D	Data Size	8	8	16	bits
N	Number of Slots Per Frame	1	1	1	Slots

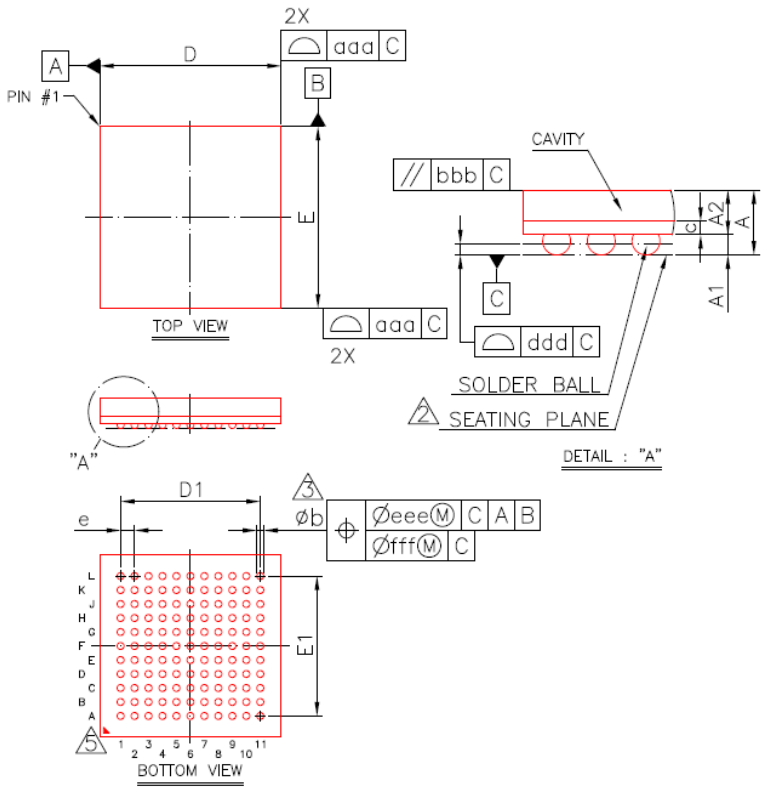
Table 26. PCM Interface Timing

Symbol	Description	Min.	Typ.	Max.	Unit
T_{BCLKH}	High Period of BCLK	980	-	-	ns
T_{BCLKL}	Low Period of BCLK	970	-	-	ns
$T_{FrameSync\_Delay}$	Delay Time from BCLK High to Frame Sync High	-	-	75	ns
T_{BCLKD_OUT}	Delay Time from BCLK High to Valid DAC_Data	-	-	125	ns
$T_{SETUPIN}$	Set-up Time for ADC_Data Valid to BCLK Low	10	-	-	ns
T_{HOLDIN}	Hold Time for BCLK Low to ADC_Data Invalid	125	-	-	ns

7.5.4. PCM Interface Signal Levels

The PCM signal level ranges from 1.8V to 3.3V. The host provides the power source with the targeted power level to the RTL8822BS-CG PCM interface via the VIO_HOST pin .

8. Mechanical Dimensions



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.11	0.16	0.21	0.004	0.006	0.008
A2	0.86	0.91	0.96	0.034	0.036	0.038
c	0.22	0.26	0.30	0.009	0.010	0.012
D	6.40	6.50	6.60	0.252	0.256	0.260
E	6.40	6.50	6.60	0.252	0.256	0.260
D1	---	5.00	---	---	0.197	---
E1	---	5.00	---	---	0.197	---
e	---	0.50	---	---	0.020	---
b	0.20	0.25	0.30	0.008	0.010	0.012
aaa		0.15			0.006	
bbb		0.10			0.004	
ddd		0.08			0.003	
eee		0.15			0.006	
fff		0.05			0.002	
MD/ME		11/11				

NOTE :

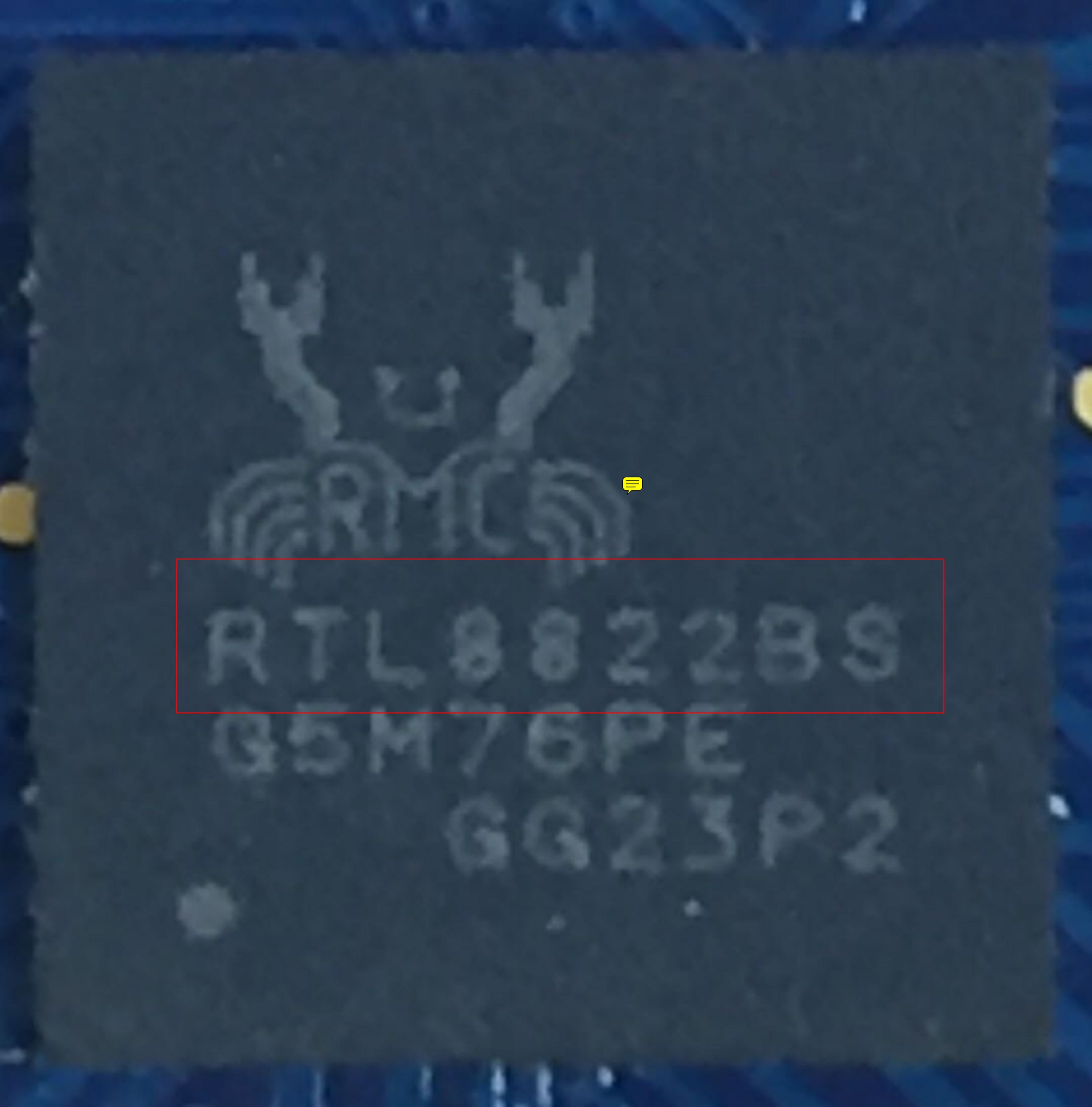
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: bbb,ddd
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.

9. Ordering Information

Table 27. Ordering Information

Part Number	Package	Status
RTL8822BS-CG	TFBGA121 , 'Green' Package	Mass Production

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II, Hsinchu Science Park,
Hsinchu 300, Taiwan, R.O.C.
Tel: 886-3-5780211 Fax: 886-3-5776047
www.realtek.com


RTL8822BS
GSM76PE
GG23P2