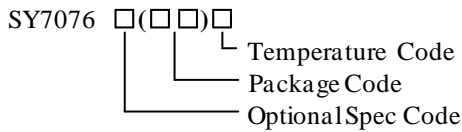


General Description

SY7076 is a high efficiency synchronous boost regulator that converts down to 2V input and up to 5.5V output voltage. It adopts NMOS for the main switch and PMOS for the synchronous switch. It can disconnect the output from input during the shutdown mode. It can program output current limit by ILIM pin.

Ordering Information



Ordering Number	Package type	Note
SY7076QMC	QFN2x2-10	----

Features

- 2V Minimum input voltage
- Adjustable output voltage from 2.5V to 5.5V
- 6A peak current limit
- Input under voltage lockout
- Load disconnect during shutdown
- Programmable output current limit protection
- ±10% output current limit accuracy
- Force PWM mode selectable
- Hic-cup mode for short protection
- Low $R_{DS(ON)}$ (main switch/synchronous switch) at 5.0V output: 20/40mΩ
- Output OVP protection
- Compact package QFN2x2-10 package

Applications

- All Single Cell Li or Dual Cell Battery Operated Products as MP-3 Player, PDAs, and Other Portable Equipment.

Typical Applications

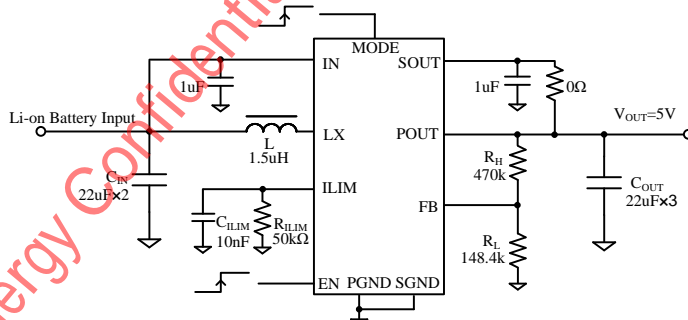


Figure 1. Schematic Diagram

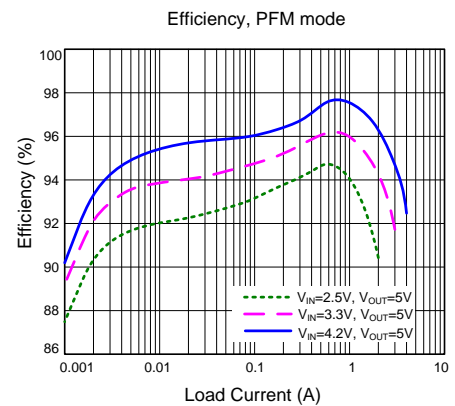
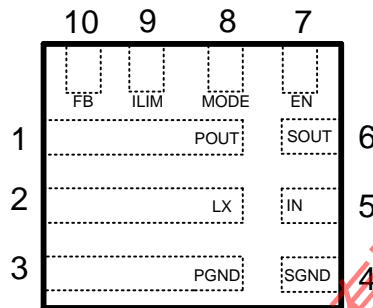


Figure 2. Efficiency vs. Load Current

Pinout (top view)



(QFN2x2-10)

Top mark: **Fnxyz** (Device code: Fn, x=year code, y=week code, z=lot number code)

Name		Description
POUT	1	Power output pin. Decouple this pin to GND pin with at least 2pcs 22uF ceramic cap.
LX	2	Inductor node. Connect an inductor between IN pin and LX pin.
PGND	3	Power ground pin.
SGND	4	Signal ground pin.
IN	5	Signal input pin. Decouple this pin to GND with at least 4.7uF ceramic cap.
SOUT	6	Signal output pin. Decouple this pin to GND pin with at least 1uF ceramic cap for noise immunity consideration.
EN	7	Enable pin. Internal integrated with 1MΩ pull down resistor.
MODE	8	PFM/PWM select pin. Low for auto PFM/PWM mode. High for force PWM mode. Internal integrated with 1MΩ pull down resistor.
ILIM	9	Current limit program pin, program output current limit by connecting resistor and capacitor parallel network to ground. $I_{LIM}(A)=100k/R_{ILIM}(\Omega)$. C_{ILIM} must be large than 10nF.
FB	10	Feedback pin. Connect a resistor R1 between OUT and FB, and a resistor R2 between FB and GND to program the output voltage. $V_{OUT}=1.2V \times (R_H/R_L+1)$.

Block Diagram

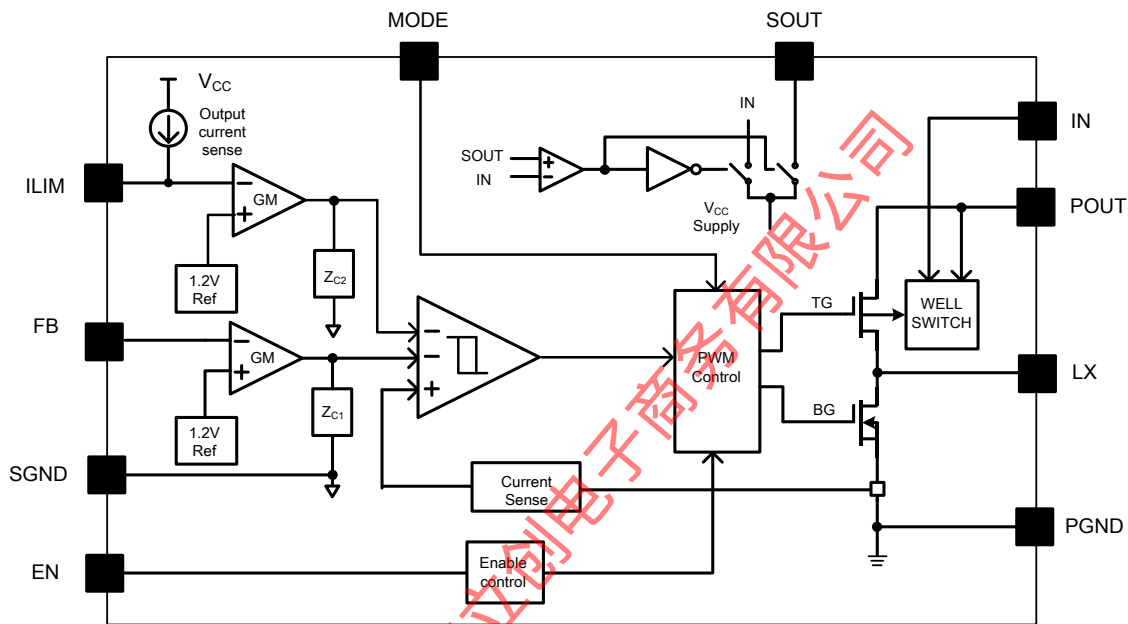


Figure 3. Block Diagram

Absolute Maximum Ratings (Note 1)

LX	-----	8.0V
All other Pins	-----	6.0V
Power Dissipation, P_D @ $T_A=25^\circ\text{C}$, QFN2x2-10	-----	2.5W
Package Thermal Resistance (Note 2)		
θ_{JA}	-----	50°C/W
θ_{JC}	-----	10°C/W
Junction Temperature Range	-----	150°C
Lead Temperature (Soldering, 10 sec.)	-----	260°C
Storage Temperature Range	-----	-65°C to 150°C

Recommended Operating Conditions (Note 3)

IN	-----	2.0V to 5.5V
OUT	-----	2.5V to 5.5V
All other pins	-----	0-5.5V
Junction Temperature Range	-----	-40°C to 125°C
Ambient Temperature Range	-----	-40°C to 85°C

Electrical Characteristics

($V_{IN}=3.0V$, $V_{OUT}=4.2V$, $I_{OUT}=500mA$, $T_A=25^{\circ}C$ unless otherwise specified)

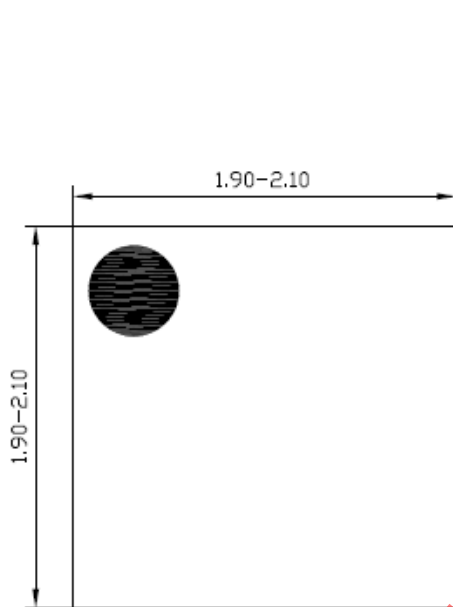
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage	V_{IN}		2		5.5	V
Output Voltage Range	V_{OUT}		2.5		5.5	V
Quiescent Current	V_{IN}	$I_O=0A, V_{EN}=V_{IN}=3.0V, V_{OUT}=5.0V$		10		μA
	V_{OUT}			27		μA
Shutdown Current	I_{SHDN}	$V_{EN}=0V, V_{IN}=3.0V$		0.1	1	μA
Linear Charge Current	I_{CHARGE}	$V_{OUT}<0.5V_{IN}$		2		A
Max Linear Charge Time	t_{CHG}			9		ms
Input Vin UVLO Threshold	V_{UVLO}				2.0	V
Vin UVLO Hysteresis	V_{HYS}			0.25		V
MODE & EN Rising Threshold	V_{ENH}		1.2			V
MODE & EN Falling Threshold	V_{ENL}				0.4	V
Low Side Main FET R_{ON}	$R_{DS(ON)N}$	$V_{OUT}=5.0V$		20		$m\Omega$
Synchronous FET R_{ON}	$R_{DS(ON)P}$	$V_{OUT}=5.0V$		40		$m\Omega$
Main FET Current Limit	I_{LIM1}		6.0			A
Output Current limit	I_{LIM2}	$R_{LIM}=100k\Omega$	0.9	1	1.1	A
Minimum Output Current Limit	$I_{LIM,MIN}$			0.8		A
Switching Frequency	F _{SW}			500		kHz
Feedback Reference Voltage	V_{REF}		1.182	1.2	1.218	V
Minimum On Time	$T_{ON,MIN}$			100		ns
Minimum Off Time	$T_{OFF,MIN}$			100		ns
Max On Time	$T_{ON,MAX}$			1.5		us
OUT pin OVP Protection	V_{OVP}			6.0		V
OUT pin OVP Hysteresis	$V_{OVP,HYS}$			0.2		V
Thermal Shutdown Temperature	T_{SD}			150		$^{\circ}C$
Thermal Shutdown Hysteresis	T_{HYS}			20		$^{\circ}C$

Note 1: Stresses beyond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

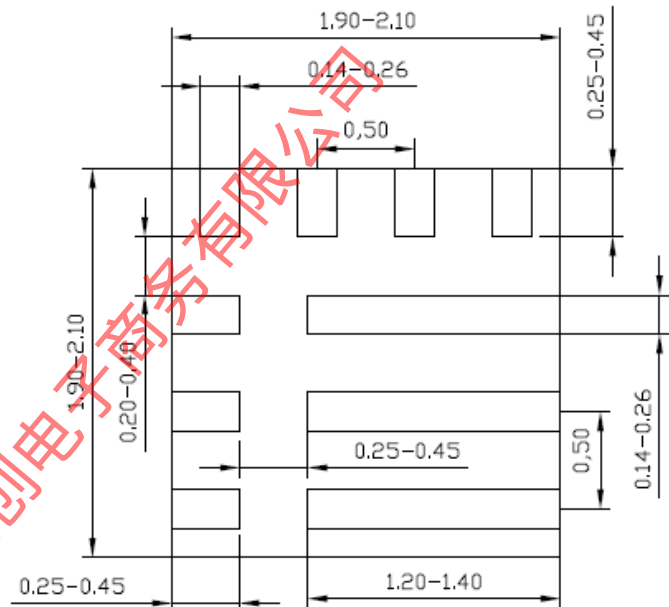
Note 2: θ_{JA} is measured in the natural convection at $T_A=25^{\circ}C$ on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions.

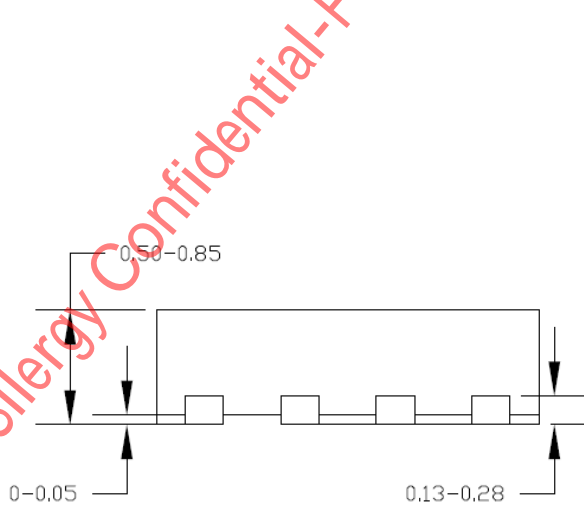
QFN2x2-10 Package Outline



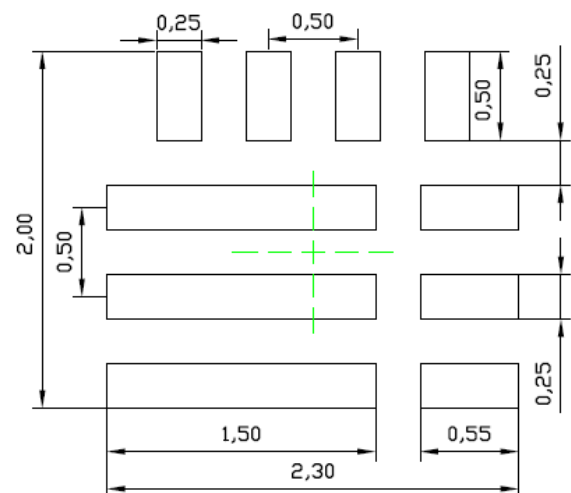
Top View



Bottom View



Side View



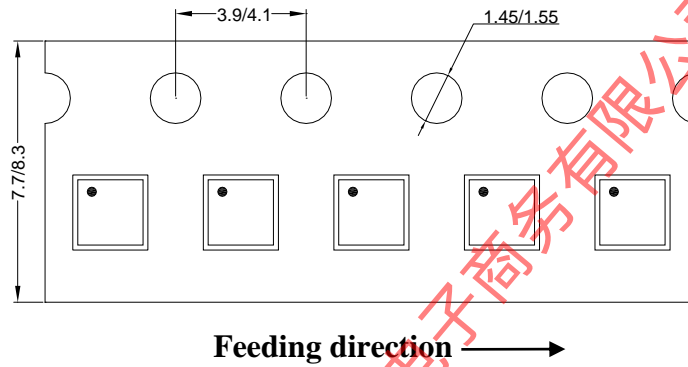
**Recommended PCB Layout
(Reference only)**

Notes: All dimension in millimeter and exclude mold flash & metal burr

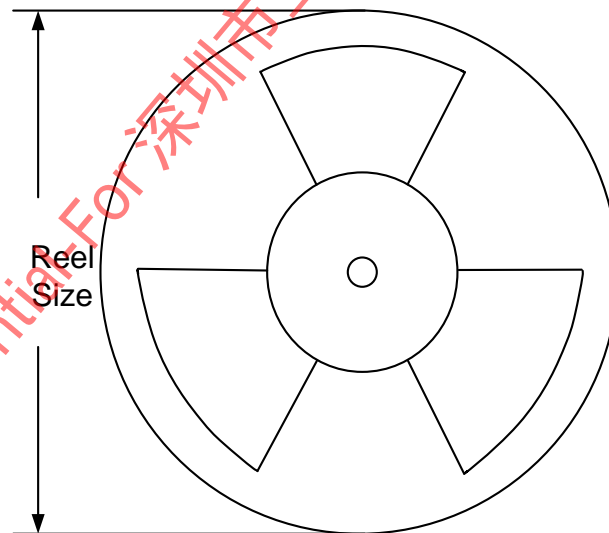
Taping & Reel Specification

1. Taping orientation

QFN2x2



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN2x2	8	4	7"	400	160	3000

3. Others: NA