

### Description

The IRS2113STR is a high voltage, high speed power MOSFET drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 700V.

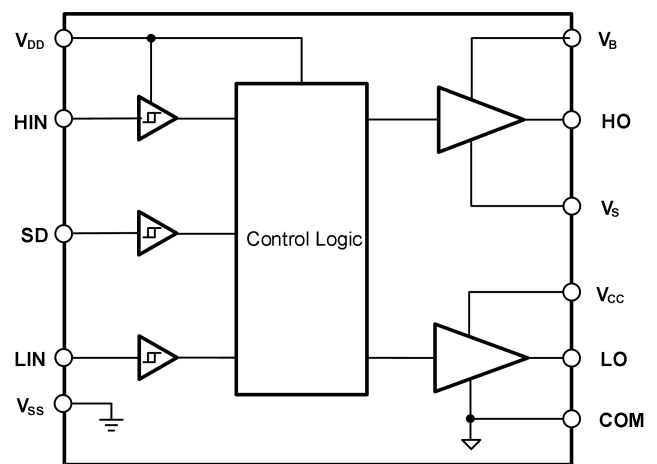
### Application

- UPS Universal inverter
- Half-bridge and full-bridge converters in AC and DC power supplies
- High-density switching power supplies for servers, telecommunications, IT and industrial infrastructure
- Solar inverter and motor driver

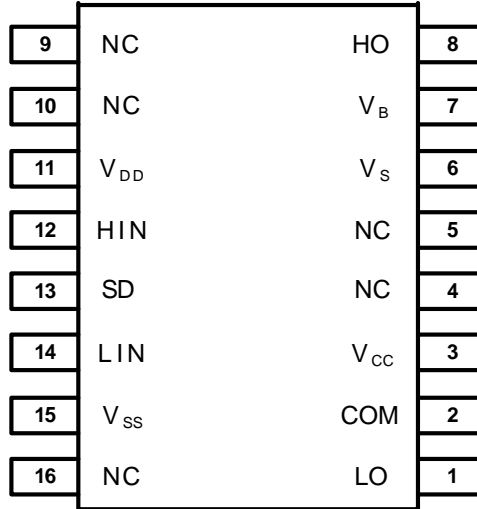
### Features and Benefits

- Floating channel designed for bootstrap operation
- Fully operational to +700 V
- 3.3V, 5V and 15V input logic compatible
- Tolerant to negative transient voltage dV/dt immune
- Allowable negative Vs capability: -9V
- Gate drive supply range from 10V to 20V
- Separate logic supply range from 3.3V to 20V Logic and power ground ±5V offset
- Undervoltage lockout for both channels
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Wide operating temperature range -40°C ~125°C
- Typically output Source/Sink current capability: 4A/4A

### Functional Block Diagram



**Function Pin Description**



**Figure6-1 SOP-16-300mil Top view**

**Table6-1 Lead Definitions**

Number	Symbol	Description
1	LO	Low side gate drive output
2	COM	Low side return
3	V <sub>CC</sub>	Low side supply
6	V <sub>S</sub>	High side floating supply return
7	V <sub>B</sub>	High side floating supply
8	HO	High side gate drive output
11	V <sub>DD</sub>	Logic supply
12	HIN	Logic input for high side gate driver output (HO), in phase
13	SD	Logic input for shutdown
14	LIN	Logic input for low side gate driver output (LO), in phase
15	V <sub>SS</sub>	Logic ground

### Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to VSS and an ambient temperature of 25°C.

Symbol	Definition	MIN.	MAX.	Units
V <sub>B</sub>	High side floating supply	-0.3	725	V
V <sub>S</sub>	High side floating supply return	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3	
V <sub>HO</sub>	High side gate drive output	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3	
V <sub>CC</sub>	Low side and main power supply	-0.3	25	
V <sub>LO</sub>	Low side gate drive output	-0.3	V <sub>CC</sub> + 0.3	
V <sub>DD</sub>	Logic supply	-0.3	V <sub>SS</sub> +25	
V <sub>SS</sub>	Logic ground	-5	+5	
V <sub>IN</sub>	Logic input of HIN & LIN	-0.3	V <sub>CC</sub> + 0.3	
dV <sub>S</sub> /dt	Allowable Offset Supply Voltage Transient		50	V/ns
ESD	HBM Model	1500		V
	Machine Model	500		V
P <sub>D</sub>	Package Power Dissipation @ TA ≤25°C		625	mW
R <sub>thJA</sub>	Thermal Resistance, Junction to Ambient		200	°C/W
T <sub>J</sub>	Junction Temperature		150	°C
T <sub>S</sub>	Storage Temperature	-55	150	
T <sub>L</sub>	Lead Temperature (Soldering, 10 seconds)		300	

### Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and VSS are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to VSS and the ambient temperature is 25°C.

Symbol	Definition	MIN.	MAX.	Units
V <sub>B</sub>	High side floating supply	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High side floating supply return	-9	700	
V <sub>HO</sub>	High side gate drive output	V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Low side and main power supply	10	20	
V <sub>LO</sub>	Low side gate drive output	0	V <sub>CC</sub>	
V <sub>DD</sub>	Logic supply	V <sub>SS</sub> + 3	V <sub>SS</sub> + 20	
V <sub>SS</sub>	Logic ground	-5	5	
V <sub>IN</sub>	Logic input of HIN & LIN	0	V <sub>CC</sub>	
T <sub>A</sub>	Ambient temperature	-40	125	°C

Note1: Transient negative VS can be used for VSS-50V with a pulse width of 50ns, guaranteed by design..

Note2: When the input pulse width is less than 1us, the input pulse cannot be transmitted normally .

**Electrical Characteristics**

 Valid for temperature range at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = V_{CC} = V_B = 15\text{V}$ ,  $C_L = 1\text{nF}$ , unless otherwise specified

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
$t_{ON}$	Turn-on propagation delay		130	200	ns	$V_S = 0\text{V}$
$t_{OFF}$	Turn-off propagation delay		130	200	ns	$V_S = 700\text{V}$
$t_{sd}$	Shutdown propagation delay		130	200	ns	$V_S = 700\text{V}$
$t_R$	Turn-on rise time		25	35	ns	
$t_F$	Turn-off fall time		17	25	ns	
MT	Matched propagation time delay			10	ns	
$V_{CCUV+}$	VCC supply UVLO threshold	8	8.9	9.8	V	
$V_{CCUV-}$		7.4	8.2	9.0	V	
$V_{CCUVHYS}$	hysteresis of $V_{CC}$ UVLO		0.7		V	
$V_{BSUV+}$	VBS supply UVLO threshold	8	8.9	9.8	V	
$V_{BSUV-}$		7.4	8.2	9.0	V	
$V_{BSUVHYS}$	hysteresis of $V_{BS}$ UVLO		0.7		V	
$I_{LK}$	High-side floating supply leakage current			50	$\mu\text{A}$	$V_B = V_S = 700\text{V}$
$I_{QBS}$	Quiescent VB supply current		70	120	$\mu\text{A}$	$V_{IN} = 0\text{V}$ or $V_{DD}$
$I_{QCC}$	Quiescent VCC supply current		120	240	$\mu\text{A}$	$V_{IN} = 0\text{V}$ or $V_{DD}$
$I_{QDD}$	Quiescent VDD supply current		15	30	$\mu\text{A}$	$V_{IN} = 0\text{V}$ or $V_{DD}$
$V_{IH}$	Logic "1" (HIN&LIN) input voltage	9.5			V	$V_{CC} = 10\text{V}$ to $20\text{V}$
$V_{IL}$	Logic "0" (HIN&LIN) input voltage			6	V	$V_{CC} = 10\text{V}$ to $20\text{V}$
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$			1.4	V	$I_O = 0\text{A}$
$V_{OL}$	Low level output voltage, $V_O$			0.1	V	$I_O = 0\text{A}$
$I_{IN+}$	Logic "1" Input bias current		20	40	$\mu\text{A}$	$V_{IN} = V_{DD}$
$I_{IN-}$	Logic "0" Input bias current			2	$\mu\text{A}$	$V_{IN} = 0\text{V}$
$I_{O+}$	Output high short circuit pulsed current	3	4		A	$V_O = 0\text{V}$ , $V_{IN} = V_{DD}$ $PW \leq 10\mu\text{s}$
$I_{O-}$	Output low short circuit pulsed current	3	4		A	$V_O = 15\text{V}$ , $V_{IN} = V_{DD}$ $PW \leq 10\mu\text{s}$

Function Description

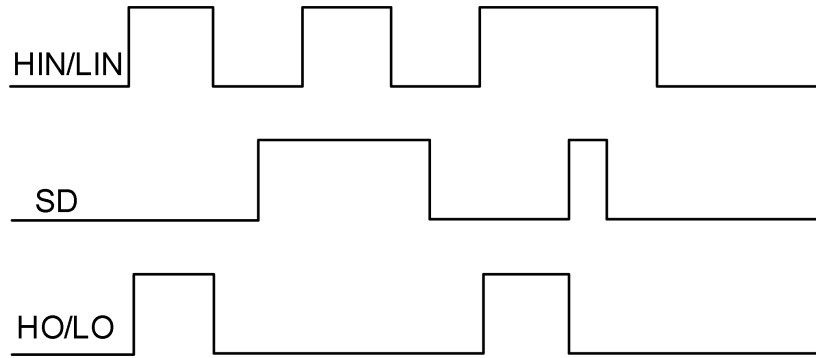


Figure 8-1 IRS2113STR Input and output timing waveform

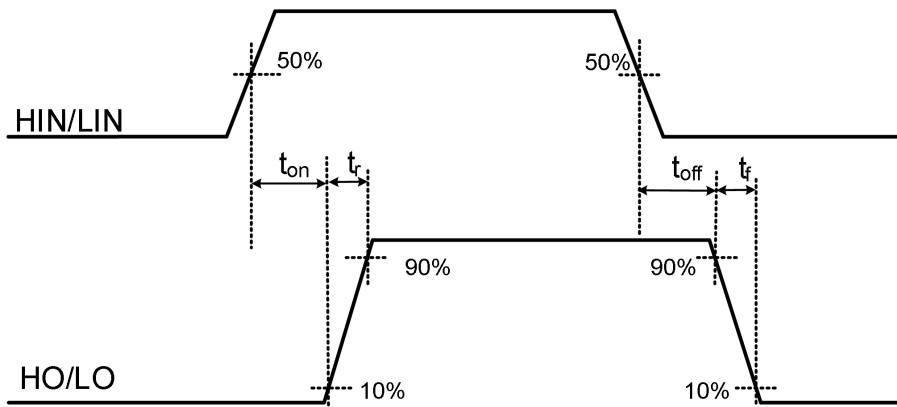


Figure 8-2 Propagation Time Waveform Definition

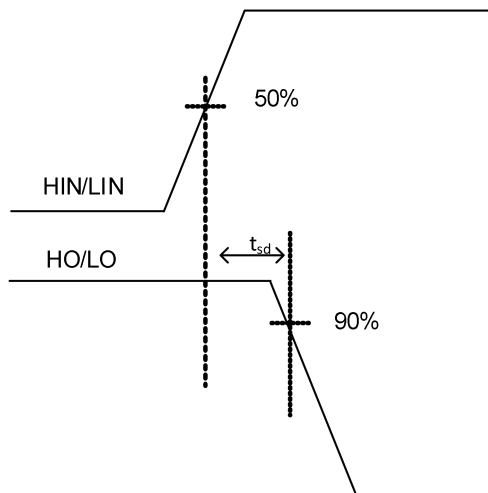


Figure 8-3 Shutdown Propagation Time Waveform Definition

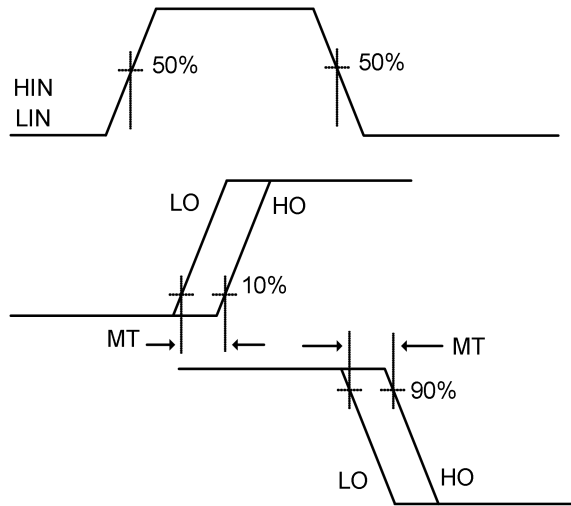


Figure 8-4 Matched propagation time delay Waveform Definition

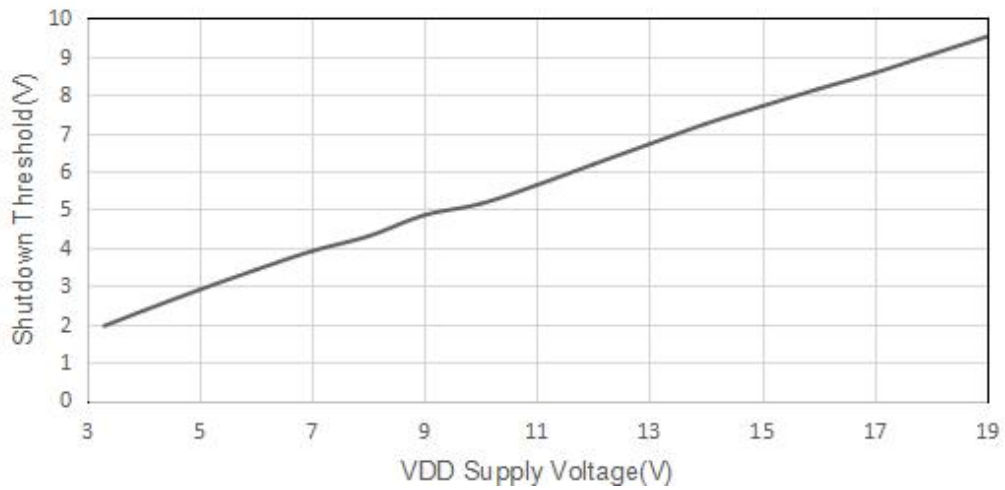


Figure 8-5 Mapping between input threshold voltage and VDD voltage (Typical)

Function Block Diagram

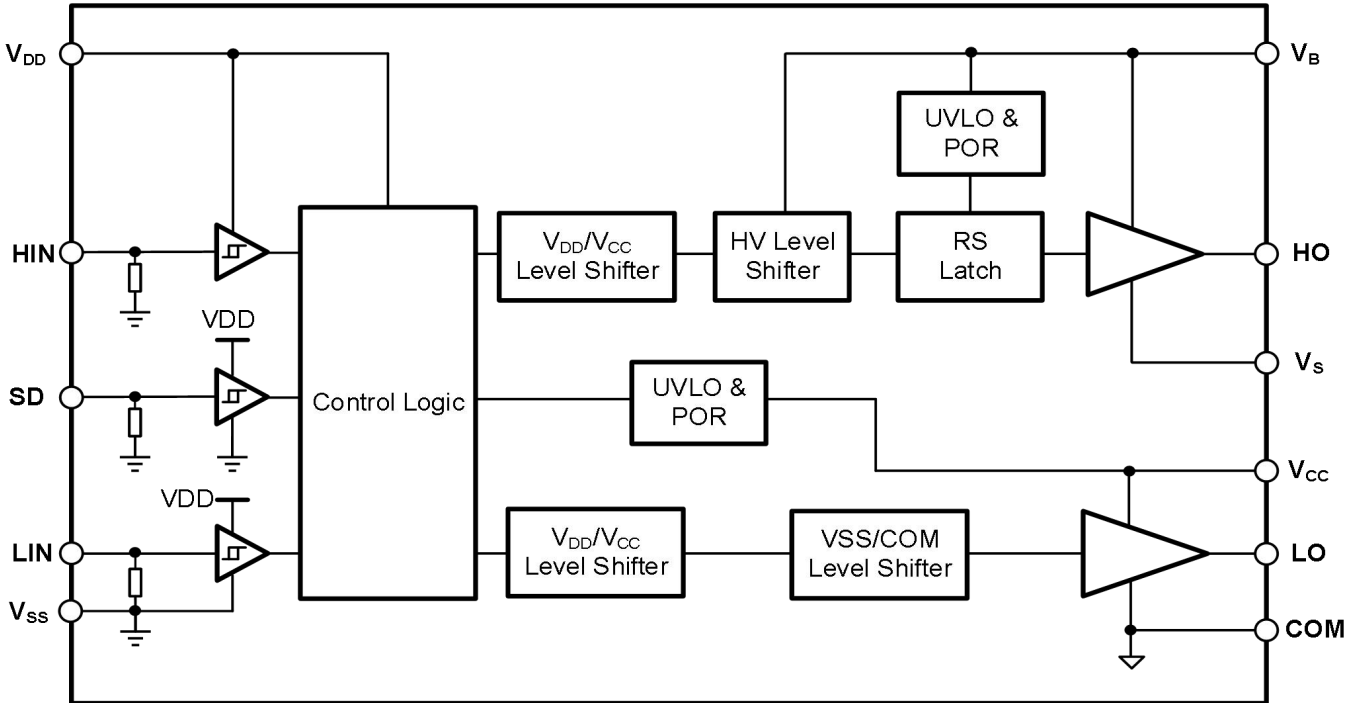


Figure9-1 Function Block Diagram of IRS2113STR

Application message

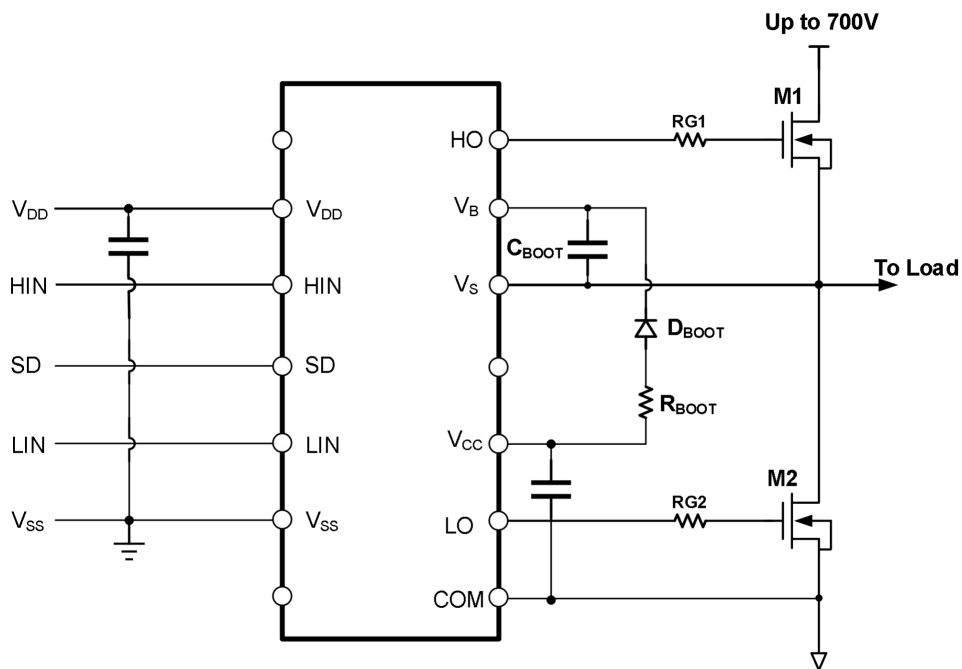
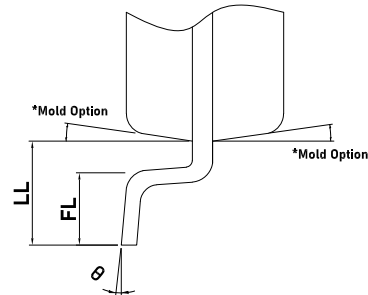
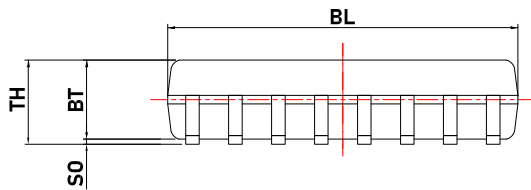
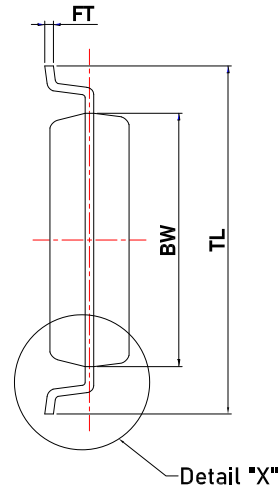
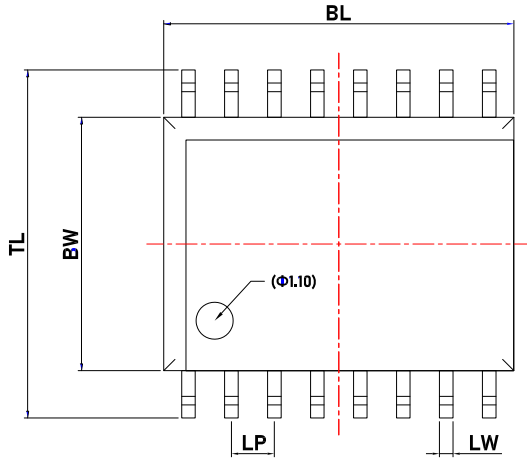


Figure9-2 Typical application circuit of IRS2113STR

SOP-16-300mil

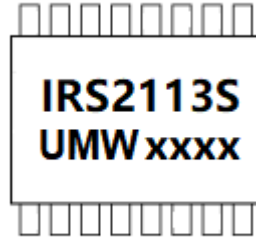


Dimensions

Item	BL	BW	TL	LW	LP	FT	BT	SO	TH	LL	FL	θ
Unit	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	°
Spec	10.45 (10.35) 10.20	7.70 (7.50) 7.30	10.50 (10.30) 10.10	0.400 TYP	1.270 TYP	0.300 (0.250) 0.170	2.44 (2.34) 2.24	0.250 (0.150) 0.100	2.590 Max.	1.50 (1.40) 1.30	1.00 (0.80) 0.60	8 (4) 0



**Marking**



**Ordering information**

Order code	Package	Baseqty	Deliverymode
UMW IRS2113STR	SOP-16-300mil	2000	Tape and reel