1. DESCRIPTION

The XL/XD74LS06 devices feature high-voltage, open- collector outputs to interface with high-level circuits (such as MOS), or for driving high-current loads, and also are characterized for use as inverter buffers for driving TTL inputs. The XL/XD74LS06 devices have a rated output voltage of 30 V.

2. FEATURE

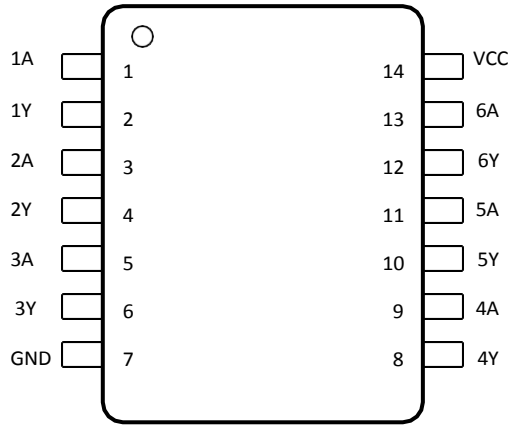
- Convert TTL Voltage Levels to MOS Levels
- High Sink-Current Capability
- Input Clamping Diodes Simplify System Design
- Open-Collector Driver for Indicator Lamps and Relays
- Inputs Fully Compatible With Most TTL Circuits

3. APPLICATIONS

- Factory Automation
- Building Automation
- Line Drivers
- Electronic Point of Sale
- Desktop or Notebook PCs

4. PIN CONFIGURATIONS AND FUNCTIONS

XL/XD74LS06

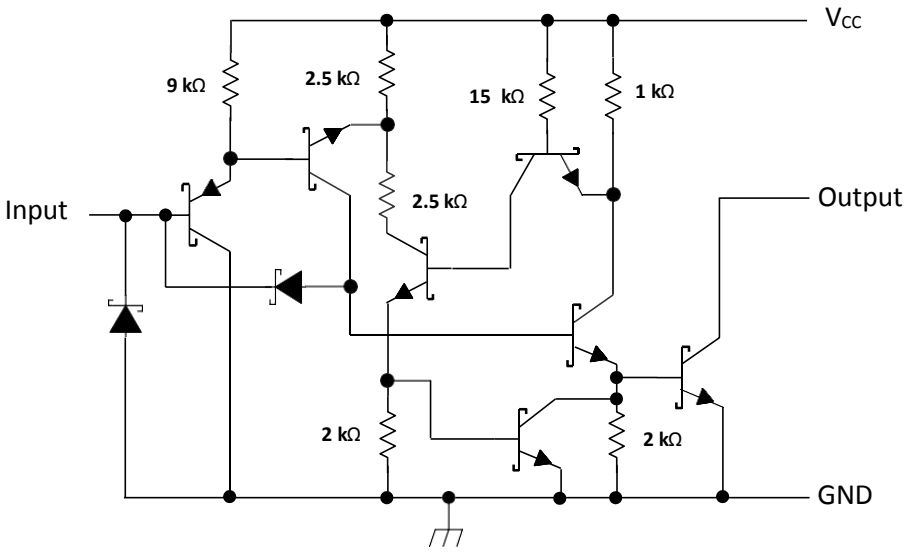


(Top View)

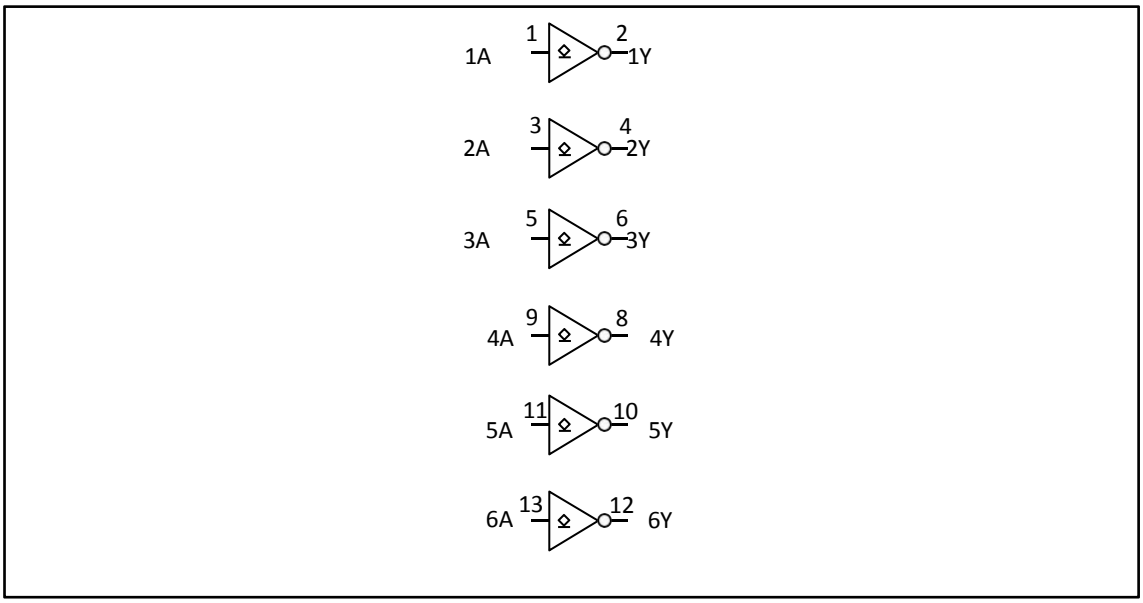
Pin Functions

PIN		I/O	DESCRIPTION
NAME	SOP, DIP		
1A	1	I	1A Input
1Y	2	O	1Y Output
2A	3	I	2A Input
2Y	4	O	2Y Output
3A	5	I	3A Input
3Y	6	O	3Y Output
4A	9	I	4A Input
4Y	8	O	4Y Output
5A	11	I	5A Input
5Y	10	O	5Y Output
6A	13	I	6A Input
6Y	12	O	6Y Output
GND	7	—	Ground
NC	—	—	No internal connection
V_{CC}	14	—	Power pin

5. FUNCTIONAL BLOCK DIAGRAM



Block Diagram



Logic Diagram (Positive Logic)

6. SPECIFICATIONS

6.1. Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

	MIN	MAX	UNIT
Supply voltage, V_{CC}		7	V
Input voltage, V_I[2]		7	V
Output voltage, V_O (XL/XD74LS06)[2][3]		30	V
Absolute maximum junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

[1] Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] All voltage values are with respect to GND.

[3] This is the maximum voltage that must be applied to any output when it is in the off state.

6.2. Thermal Resistance Characteristics

THERMAL METRIC[1]		XD/XL74LS06		UNIT
		DIP	SOP	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.2	82.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.5	40.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30	41.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.3	12.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.9	41.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

6.3. ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±2000	

[1] JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

[2] JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Tested on N package

6.4. Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage (XL/XD74LS06)				30	V
I_{OL}	Low-level output current	XD74LS06			30	mA
		XL74LS06			30	
T_A	Operating free-air temperature	XD74LS06	–40		85	°C
		XL74LS06	-40		85	

6.5. Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
V_{IK}	V_{CC} = MIN, I_I = –12 mA				–1.5	V
I_{OH}	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 30 V, XL/XD74LS06				0.25	mA
V_{OL}	V_{CC} = MIN, V_{IH} = 2 V	I_{OL} = 16 mA		0.25	0.4	V
		I_{OL} = 30 mA			0.7	
		I_{OL} = 40 mA, XL74LS06			0.7	
I_I	V_{CC} = MAX, V_I = 7 V				1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4 V				20	µA
I_{IL}	V_{CC} = MAX, V_I = 0.4 V				–0.2	mA
I_{CCH}	V_{CC}= MAX				18	mA
I_{CCL}	V_{CC}= MAX				60	mA

[1] For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.

[2] All typical values are at VCC = 5 V, and TA = 25°C.

6.6. Switching Characteristics

VCC = 5 V and TA = 25°C (see Figure 2)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	From A (input) to Y (output), R_L= 110 Ω, C_L = 15 pF	7	15		ns
t_{PHL}	From A (input) to Y (output), R_L= 110 Ω, C_L = 15 pF	10	20		

6.7. Typical Characteristics

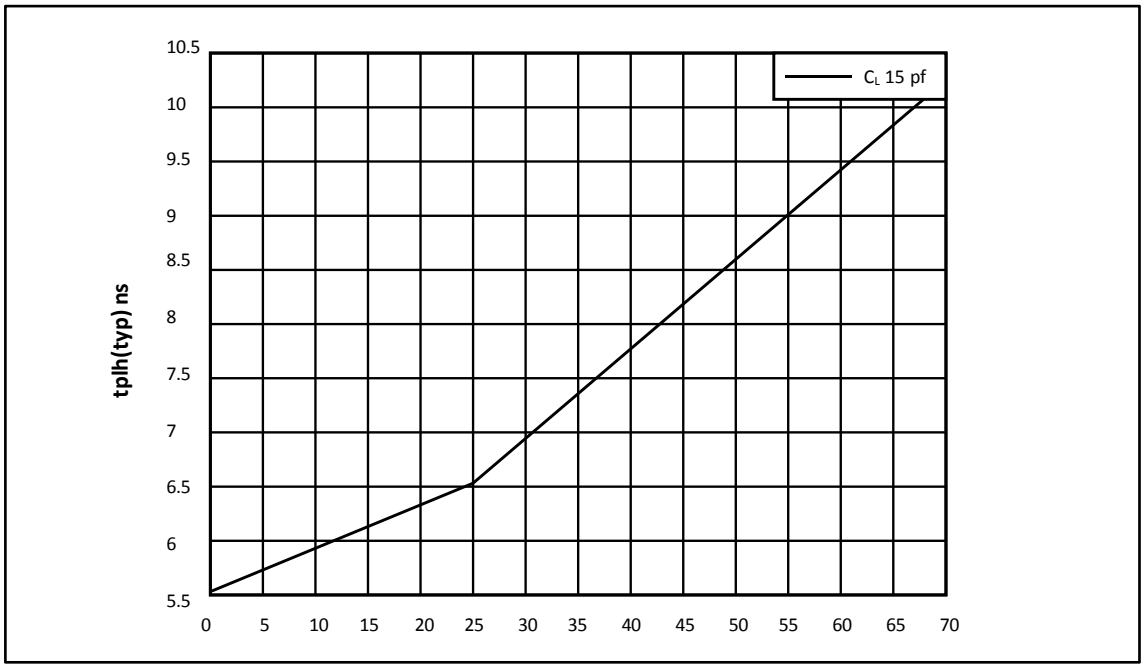
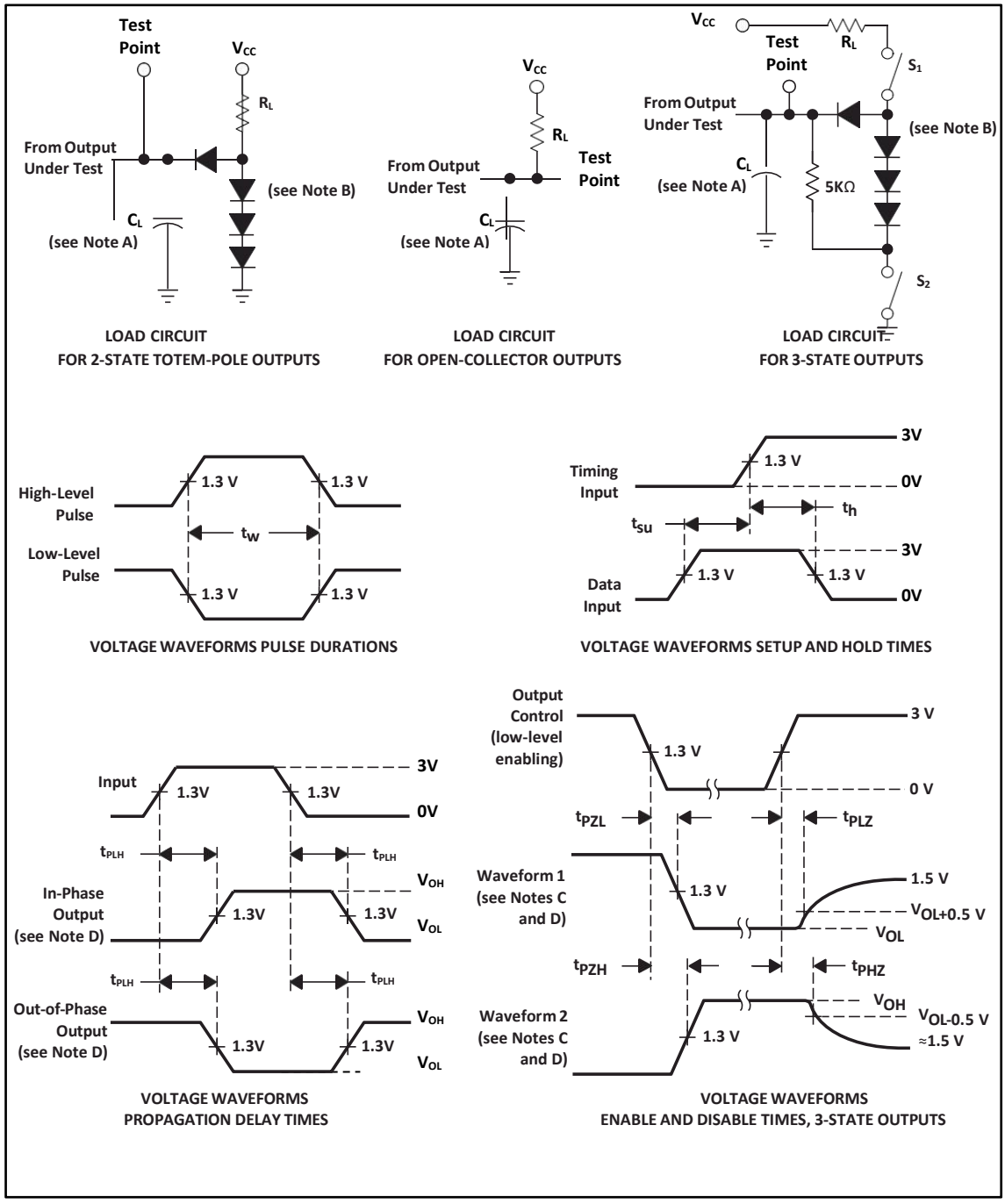


Figure 1. Propagation Delay vs Temperature

7. PARAMETER MEASUREMENT INFORMATION



[1] CL includes probe and jig capacitance.

[2] All diodes are 1N3064 or equivalent.

[3] Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

[4] S1 and S2 are closed for tPLH, tPHL, tPHZ, and tPLZ; S1 is open and S2 is closed for tPZH; S1 is closed and S2 is open for tPZL.

[5] Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.

[6] All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, ZO ≈ 50 Ω, tr≤ 1.5 ns, tf≤ 2.6 ns.

[7] The outputs are measured one at a time, with one input transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

8. DETAILED DESCRIPTION

8.1. Overview

The XL/XD74LS06 devices are open-collector output inverters. The maximum sink current for the XD74LS06 device is 30 mA, and for the XL74LS06 device it is 40 mA. These devices are compatible with most TTL families. Inputs are diode-clamped to minimize transmission effects, which simplifies design. Typical power dissipation is 175 mW, and average propagation delay time is 8 ns.

8.2. Feature Description

The XL/XD74LS06 devices can convert most TTL voltage circuit voltage level to MOS levels. The devices have high sink-current capability of up to 40 mA. The open-collector driver can be used for typical applications including Indicator lamps and relays.

8.3. Device Functional Modes

Table 1 lists the functional modes of the XL/XD74LS06 devices.

Table 1. Function Table

INPUT A	OUTPUT Y
H	L
L	Hi-Z

8.4. Application Information

The open-collector device is suitable for high-drive and high-voltage translation applications.

8.5. Typical Application

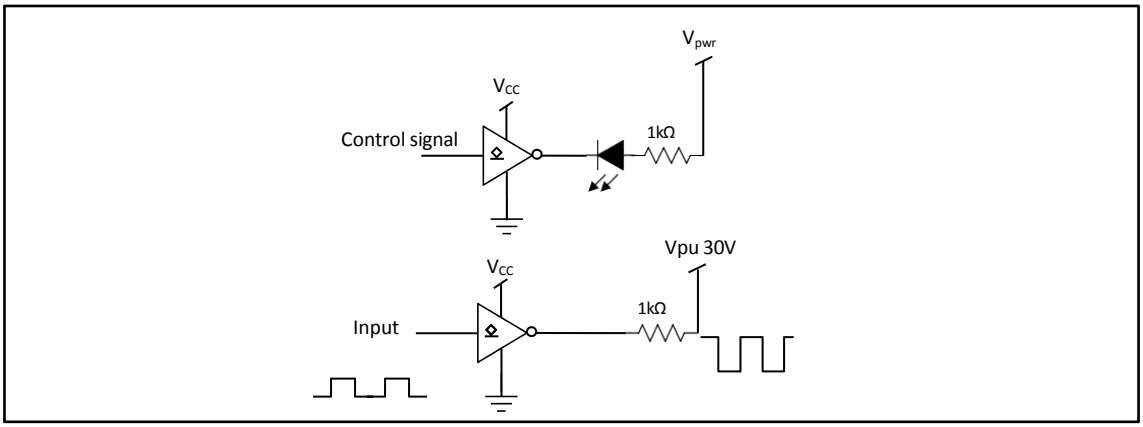


Figure 3. Application Schematic

8.5.1. Design Requirements

The XL/XD74LS06 are open-collector devices which can sink current (up to 40 mA on XL74LS06). The devices can be used in applications such as LED drivers and voltage translation using pullup resistors.

8.5.2. Detailed Design Procedure

1. Recommended input conditions:

   - Specified high and low levels. See (VIH and VIL) in the Recommended Operating Conditions.

   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid VCC.

2. Recommended output conditions:

   - Load currents must not exceed (IO max) per output.

   - Outputs can be pulled up to 30 V.

Typical Application (continued)

8.5.3. Application Curve

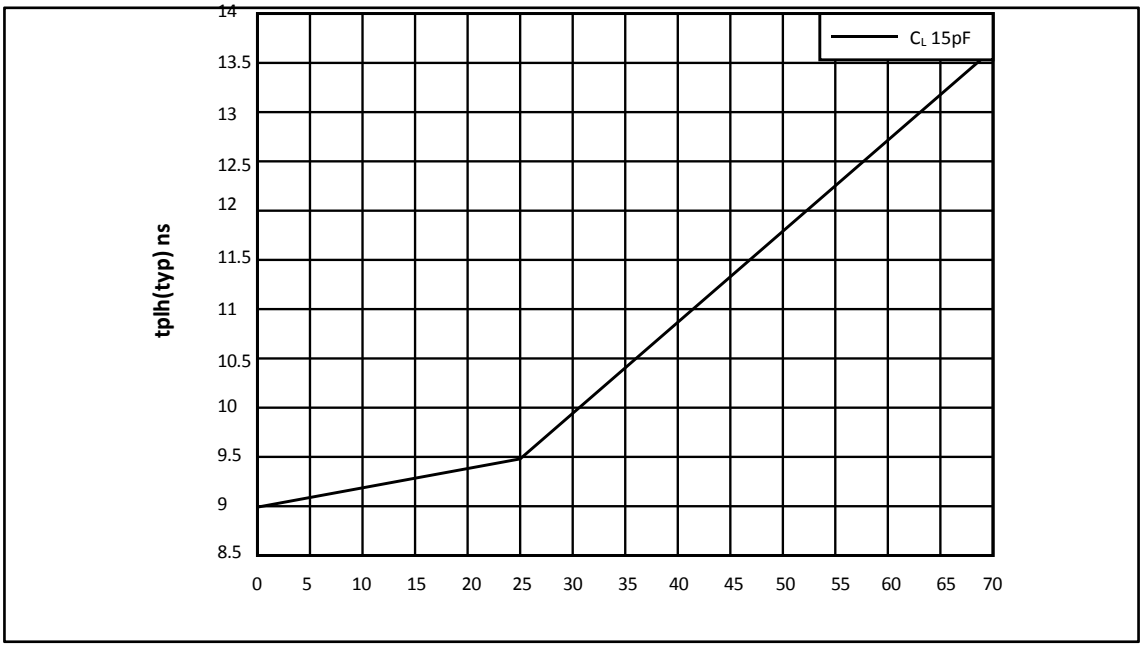


Figure 4. Propagation Delay vs Temperature

9. POWER SUPPLY RECOMMENDATIONS

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Recommended Operating Conditions.

Each VCC pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, XINLUDA recommends a 0.1-µF capacitor, and if there are multiple VCC pins, then XINLUDA recommends a 0.01-µF or 0.022- µF capacitor for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

10. LAYOUT

10.1. Layout Guidelines

When using multiple bit logic devices, inputs must not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input and gate are used or only 3 of the 4 buffer gates are used. Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. The following rules must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or VCC whichever make more sense or is more convenient. XINLUDA recommends keeping the signal lines as short and as straight as possible (see Figure 6). Incorporation of microstrip or stripline techniques are also recommended when signal lines are more than 1" long. These traces must be designed with a characteristic impedance of either 50 Ω or 75 Ω as required by the application.

10.2. Layout Examples

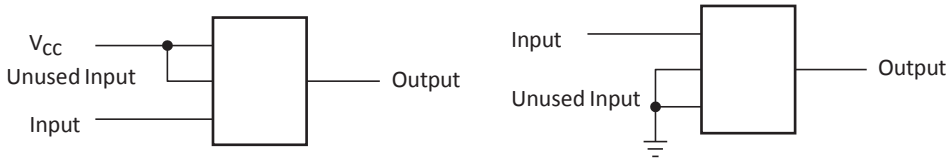


Figure 5. Layout Schematic

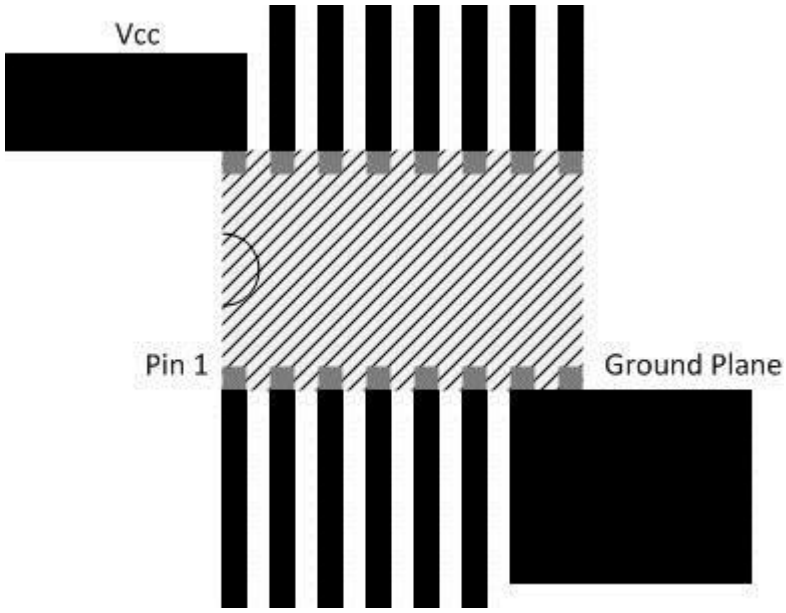


Figure 6. Signal Line Layout

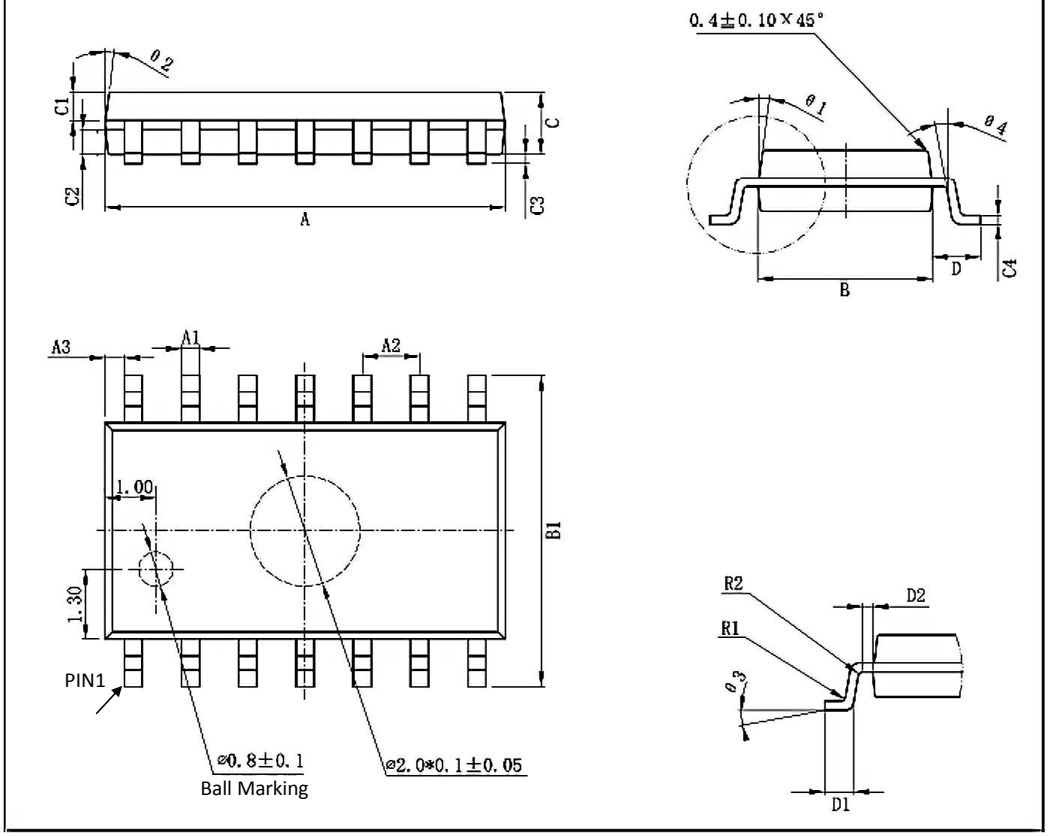
11. ORDERING INFORMATION

Ordering Information							
Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XL74LS06	XL74LS06	SOP14	8.75 * 4.00	- 40 to 85	MSL3	T&R	2500
XD74LS06	XD74LS06	DIP14	19.05 * 6.35	- 40 to 85	MSL3	Tube 25	1000

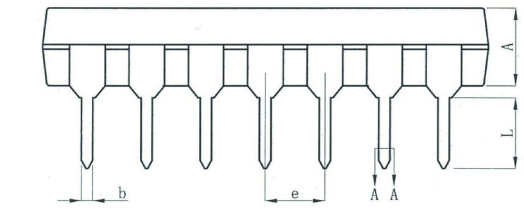
12. DIMENSIONAL DRAWINGS

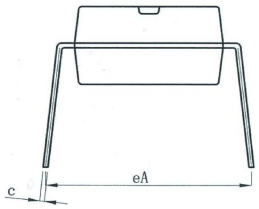
SOP14

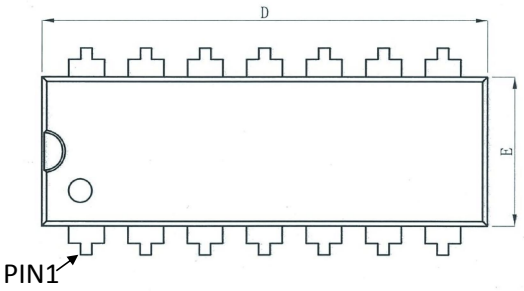
Size / Mark	Min (mm)	Max (mm)	Size / Mark	Min (mm)	Max (mm)
A	8.55	8.75	C4	0.193	0.213
A1	0.356	0.456	D	0.95	1.15
A2	1.27TYP		D1	0.40	0.70
A3	0.312TYP		D2	0.20TYP	
B	3.80	4.00	R1	0.20TYP	
B1	5.80	6.20	R2	0.20TYP	
C	1.40	1.60	θ1	8° ～ 12° TYP4	
C1	0.60	0.70	θ2	8° ～ 12° TYP4	
C2	0.55	0.65	θ3	0° ～ 8°	
C3	0.05	0.25	θ4	4° ～ 12°	

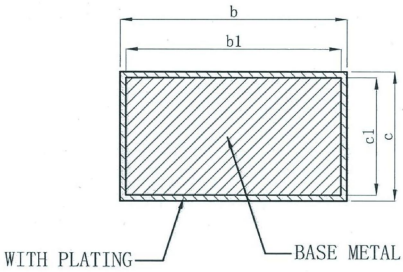


DIP14









SECTION A-A

symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	----	0.53
b1	0.43	0.46	0.49
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	----	----