2.7 V ~ 5.5 V Supply, Serial Input、Voltage Output Precision DAC

Features

- 18/16/14 bit resolution
- 2.7 V to 5.5 V single supply
- 1 μs settling time
- Power-on output:
  - ZJC2541-18/16/14: 0 V
  - ZJC2543-18/16/14: V_{REF} /2
- Low glitch: 1nV-s
- Low noise spectral density: 11 nV/$\sqrt{Hz}$
- Low gain temperature drift: 0.05 ppm/°C
- Low power dissipation: 120 μA supply current
- Package: SOIC-8 /MSOP-10/DFN-10
- Operating temperature range: - 40 °C to +125 °C

Application

- Precision Control Equipment
- Automated Testing
- Precision Instrument
- Medical Instrument

General Description

ZJC2541/3-18/16/14 (hereinafter referred to as ZJC2541/3) it is a single, serial data input, voltage output 18/16/14-bit resolution precision digital-to-analog converter (DAC). Its supply voltage is 2.7 V to 5.5 V, the output range is 0 V to V_{REF}, and monotonicity is guaranteed and can guarantee DNL/INL accuracy over temperature range of - 40 °C to +125 °C.

The output of ZJC2541/3 is un-buffered. The settling time is within 1 μs, and it has the characteristics of low power consumption and low offset error. Low noise performance and low glitches make it suitable for use in a variety of end systems.

ZJC2541/3 adopts multifunctional three-wire interface, and is compatible with SPI, QSPI, MCU and DSP interface standards.

ZJC2541-18/16/14 is 0 V; the default output voltage of ZJC2543-18/16/14 is V_{REF} /2. Other functions and performance indicators are exactly the same.

Application Example

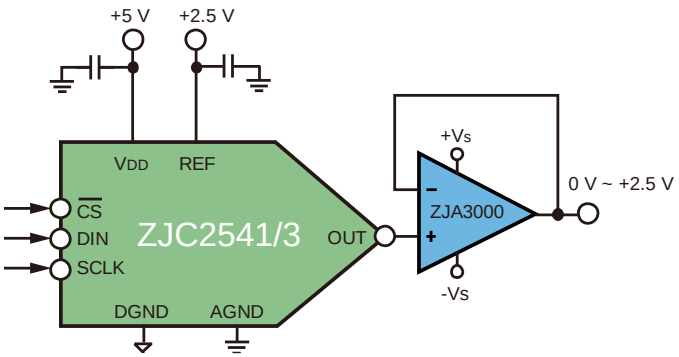

Figure 1. Applications

Typical Performance Characteristics

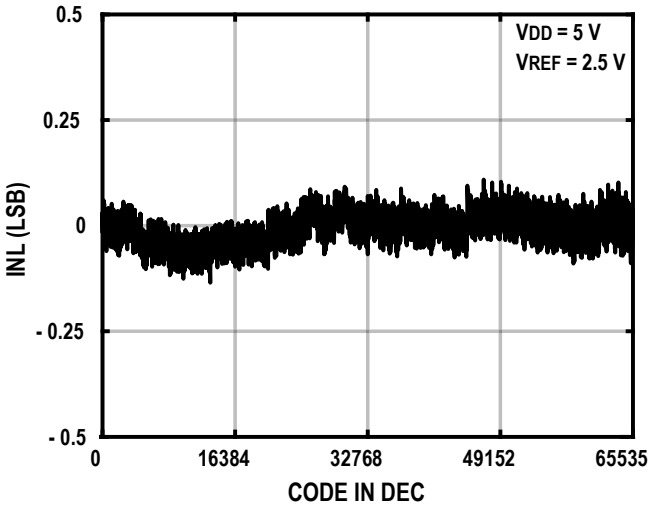

Figure 2. ZJC2541/3-16 INL

1 8 /16 /14 -bit unipolar DAC series models are as follows:

DAC Resolution (bit)	DAC Model	Power-on Output Voltage	Package
18	ZJC2541-18	0	SOIC-8/MSOP-10/DFN-10
18	ZJC2543-18	$V_{REF}/2$	
16	ZJC2541-16	0	
16	ZJC2543-16	$V_{REF}/2$	
14	ZJC2541-14	0	
14	ZJC2543-14	$V_{REF}/2$	

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Version (Release C)[1]

April 2024 - Release C

Add EPAD information at page 7

August 2023 - Release B

Full Text Formatting Update

Add MSOP -10, DFN -10 pin configuration and function at page 6/7

Timing diagram changes page 12

Add MSOP-10, DFN -10 package dimensions at page 24

June 2023 - Release A

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Pin Configuration And Function

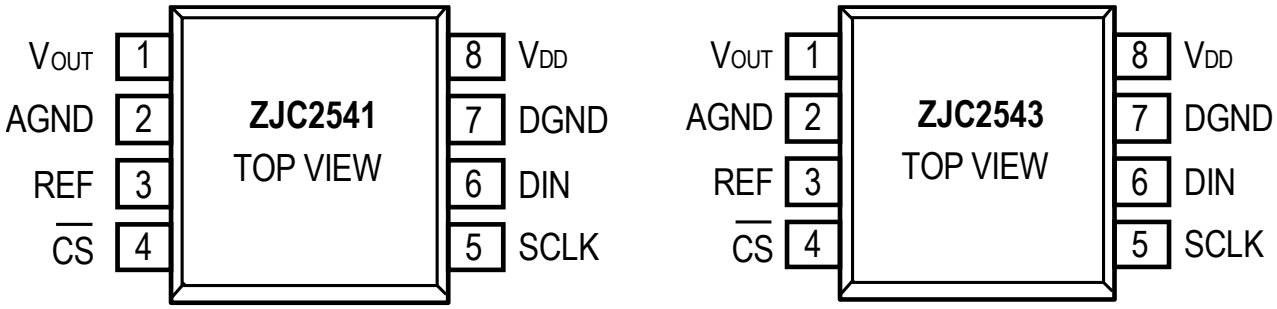


Figure 3. ZJC2541 and ZJC2543 with the Same 8-Pin SOIC Pinout Diagram

Mnemonic	Pin No.	Pin Type	Description
V_{OUT}	1	Analog Output	DAC voltage output.
AGND	2	Analog Ground	Analog ground.
REF	3	Analog Input	Voltage reference input.
$\overline{CS}$	4	Digital Input	Serial digital chip select input, active at low.
SCLK	5	Digital Input	Serial data clock input.
DIN	6	Digital Input	Serial digital signal input.
DGND	7	Digital Ground	Digital ground.
V_{DD}	8	Power Supply	Supply voltage input.

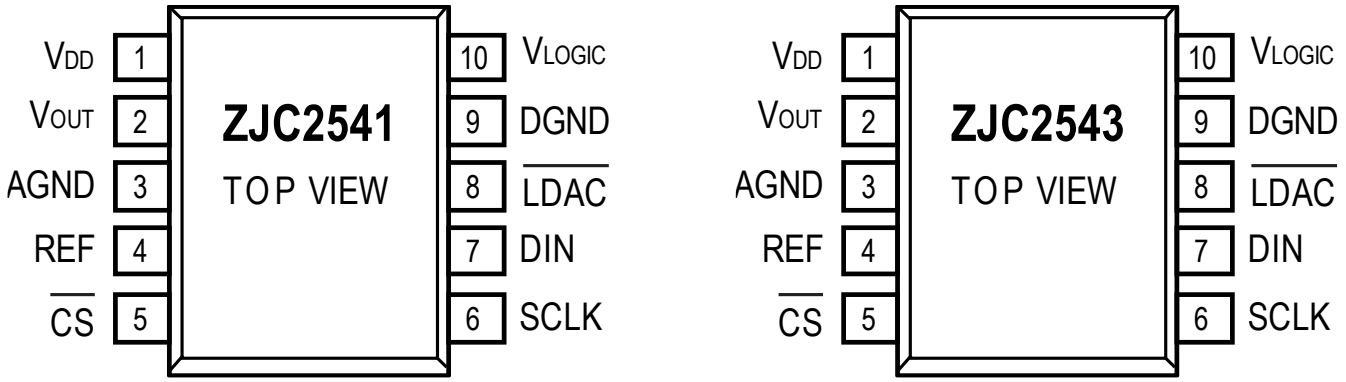


Figure 4. ZJC2541 and ZJC2543 with the Same 10 - Pin MSOP Pinouto diagram

Mnemonic	Pin No.	Pin Type	Description
V_{DD}	1	Power Supply	Supply voltage input.
V_{OUT}	2	Analog Output	DAC voltage output.
AGND	3	Analog Ground	Analog ground.
REF	4	Analog Input	Voltage reference Input.
$\overline{CS}$	5	Digital Input	Serial digital chip select input, active at low.
SCLK	6	Digital Input	Serial data clock input.
DIN	7	Digital Input	Serial digital signal input.
$\overline{LDAC}$	8	Digital Input	Digital input. Loads the data latch register code value to the output voltage.
DGND	9	Digital Ground	Digital ground.
V_{LOGIC}	10	Digital Power Supply	Digital interface supply voltage input.

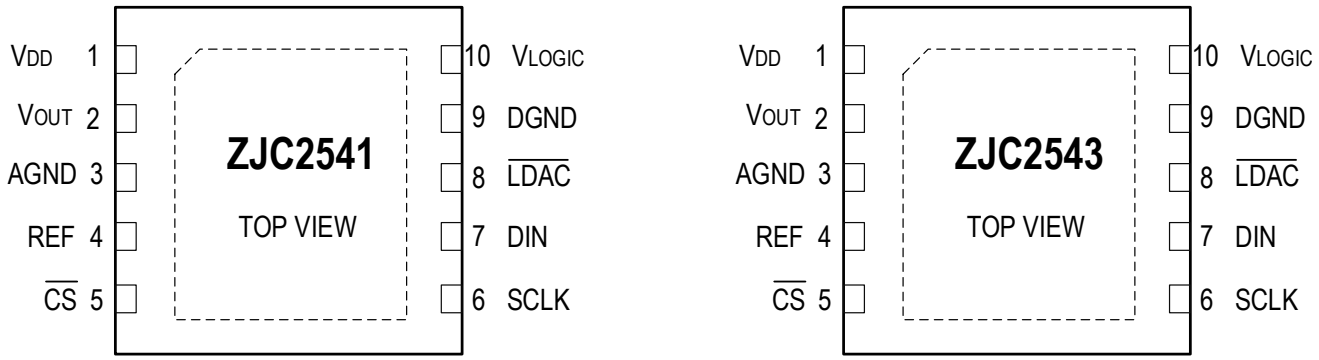


Figure 5. ZJC2541 and ZJC2543 with the same 10 - Pin DFN Pinout Diagram

Mnemonic	Pin No.	Pin Type	Description
V_{DD}	1	Power Supply	Supply voltage input.
V_{OUT}	2	Analog Output	DAC voltage output.
AGND	3	Analog Ground	Analog ground.
REF	4	Analog Input	Voltage reference Input.
$\overline{CS}$	5	Digital Input	Serial digital chip select input, active at low.
SC L K	6	Digital Input	Serial data clock input.
DIN	7	Digital Input	Serial digital signal input.
$\overline{LDAC}$	8	Digital Input	Digital input. Loads the data latch register code value to the output voltage.
DGND	9	Digital Ground	Digital ground.
V_{LOGIC}	10	Digital Power Supply	Digital interface supply voltage input.
EPAD	EP	EP	Exposed pad. Connect to ground.

Absolute Maximum Ratings[1]

Parameter	Rating
V_{DD} to AGND	- 0.3 V ~ + 6 V
REF to AGND	- 0.3 V ~ V_{DD} + 0.3 V
Digital Input to DGND	- 0.3 V ~ V_{DD} + 0.3 V
Input current to pins except V_{DD}	± 10 mA
Storage Temperature Range	- 65 °C ~ 150 °C
Junction Temperature Range	150 °C
Lead Temperature (Soldering, 10 seconds)	300 °C
Maximum Reflow Temperature[2]	260 °C
Electrostatic Discharge (ESD)[3]	
Human Body Model (HBM)[4]	3.5 kV
Charged Device Model (CDM)[5]	2 kV

Thermal Resistance[6]

Package Type	θ_{JA}	θ_{JC}	Unit
SOIC-8	122.3	60.4	°C/W
MSOP-10	150	50	°C/W
DFN-10	43	5.5	°C/W

[1] These ratings apply at 25 °C, unless otherwise noted. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

[2] IPC/JEDECJ–STD-020 Compliant.

[3] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[4] ANSI/ESDA/JEDEC JS-001 Compliant.

[5] ANSI/ESDA/JEDEC JS-002 Compliant.

[6] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

The ● denotes the full temperature range for specified performance. Unless otherwise noted. V_{DD} = 2.7 V ~ 5.5 V, T_A = 25°C, V_{REF} = 2.5 V ~ V_{DD}, AGND = DGND = 0 V.

Parameter	Symbol	Conditions			Min	Typ	Max	Unit
Resolution								
ZJC2541/3-18		18 bits			18			bits
ZJC2541/3-16		16 bits			16			
ZJC2541/3-14		14 bits			14			
Accuracy								
Integral Nonlinear Error	INL	18 bits	- 40 °C ≤ T_A ≤ 85 °C		- 2.5	± 1	+ 2.5	LSB
			- 40 °C ≤ T_A ≤ 125 °C	●	- 4	± 1	+ 4	
		16 bits		●	- 1	± 0.5	+ 1	
		14 bits		●	- 0.5	± 0.2	+ 0.5	
Differential Nonlinear Error	DNL	18 bits	- 40 °C ≤ T_A ≤ 85 °C		- 0.85	± 0.5	+ 0.85	LSB
			- 40 °C ≤ T_A ≤ 125 °C	●	- 1	± 0.5	+ 1	
		16 bits		●	- 0.75	± 0.25	+ 0.75	
		14 bits		●	- 0.25	± 0.1	+ 0.25	
Gain Error	GE	18 bits	T_A = 25 °C		- 1.5	± 0.5	+ 1.5	LSB
			- 40 °C ≤ T_A ≤ 85 °C		- 2.5	± 0.5	+ 2.5	
			- 40 °C ≤ T_A ≤ 125 °C	●	- 4	± 0.5	+ 4	
		16 bits	T_A = 25 °C		- 0.75	± 0.3	+ 0.75	
			- 40 °C ≤ T_A ≤ 85 °C		- 1	±0.5	+ 1	
			- 40 °C ≤ T_A ≤ 125 °C	●	- 1.5	± 0.5	+ 1.5	
		14 bits	T_A = 25 °C		- 0.3	± 0.1	+ 0.3	
			- 40 °C ≤ T_A ≤ 85 °C		- 0.5	± 0.15	+ 0.5	
			- 40 °C ≤ T_A ≤ 125 °C	●	- 0.75	± 0.25	+ 0.75	
Gain Error Temperature Drift						± 0.05		ppm/°C
Zero Code Error	ZCE	18 bits		●	- 2	± 0.5	+ 2	LSB
		16 bits		●	- 1	± 0.25	+ 1	
		14 bits		●	- 0.5	± 0.15	+ 0.5	
Zero Code Error Temperature Coefficient						± 0.1		ppm/°C
Output Characteristics								
Output Voltage Range				●	0		V_{REF} - 1 LSB	V
Output Voltage Settling Time		to 1/2 LSB of full scale, C_L = 10 pF						

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
		18 bits			1		µs
		16 bits			1		
		14 bits			1		
Slew rate		C_L = 10 pF measured from 0 % to 63 %			16		V/µs
Digital-to-Analog Conversion Glitch	Glitch	Major carry changes 1 LSB (16-bit resolution)			1		nV-s
Digital Feedthrough		All 1s sent to DAC, V_{REF} = 2.5 V			0.2		nV-s
DAC Output Impedance		General tolerance 20 %			6.25		kΩ
Output Noise Density		Frequency = 1 kHz			11		$nV/\sqrt{Hz}$
Output Noise		0.1 Hz to 10 Hz			0.18		μV_{P-P}
Spurious Free Dynamic Range	SFDR	f_{IN} = 1 kHz, V_{REF} = 5 V			87		dB
Total Harmonic Distortion	THD	DAC code = 0xFFFF, Frequency = 10 kHz, V_{REF} = 2.5 V ± 1 V_{P-P}			- 87		dB
Power Supply Rejection Ratio		Δ V_{DD} ± 10 %			± 0.5		LSB
DAC reference input							
Voltage Range			●	2		V_{DD}	V
Input Resistance[1]			●	8			kΩ
Reference -3dB bandwidth		All 1 code			2		MHz
Reference Feedthrough		All 0 codes, V_{REF} = 1 V_{P-P}, 100 kHz			1.5		mV_{P-P}
SINAD					92		dB
Reference Input Capacitance		DAC code= 0x0000			130		pF
		DAC code= 0xFFFF			190		pF
Digital Input							
Input High Voltage	V_{IH}		●	2.4/0.9*V_{LOGIC}			V
Input Low Voltage	VIL		●			0.8/0.1*V_{LOGIC}	V
Input Current			●	- 1		+ 1	µA
Input Capacitance						10	pF
Hysteresis Voltage					0.15		V
Power Supply							
Power Supply	V_{DD}		●	2.7		5.5	V
Electric Current	I_{VDD}	V_{DD} = 5 V			120		µA
Digital Interface Power	V_{LOGIC}			1.8		5.5	V
Temperature Range							
Rated Performance		T_{MIN} to T_{MAX}		- 40		+ 125	°C

[1] Reference input resistance varies with code, 16-bit minimum at 0x8555.

Timing Index

The ● denotes the full temperature range for specified performance. Unless otherwise specified, T_A = 25 °C, V_{DD} = 2.7 V to 5.5 V, V_{REF} = 2.5 V, V_{LOGIC} = 1.8 V to V_{DD}, V_{INH} = 3 V and 90 % of V_{DD}, V_{INL} = 0 V and 10 % of V_{DD}, AGND = DGND = 0 V.

Parameters [1,2]	Symbol		Limit 1.8 V ≤ V_{LOGIC} < 2.7 V	Limit 2.7 V ≤ V_{LOGIC} ≤ 5.5 V	Unit
SCLK Frequency	f_{SCLK}	●	14	50	MHz max
SCLK Period	t_1	●	70	20	ns min
SCLK High Level Time	t_2	●	35	9	ns min
SCLK Low Level Time	t_3	●	35	9	ns min
$\overline{CS}$ Low To SCLK High Setup Time	t_4	●	5	5	ns min
$\overline{CS}$ High To SCLK High Setup Time	t_5	●	50	50	ns min
SCLK High To $\overline{CS}$ Low Hold Time	t_6	●	5	5	ns min
SCLK High To $\overline{CS}$ High Hold Time	t_7	●	10	5	ns min
Data Creation Time	t_8	●	35	10	ns min
Data Hold Time (V_{INH} = 90 % of V_{DD} , V_{INL} = 10 % of V_{DD})	t_9	●	5	5	ns min
$\overline{CS}$ High Time Between Low Levels	t_{10}	●	15	15	ns min
$\overline{LDAC}$ Low Pulse Width	t_{11}	●	20	20	ns min
$\overline{CS}$ High To $\overline{LDAC}$ Low Settling Time	t_{12}	●	10	10	ns min
$\overline{LDAC}$ Low To SCLK High Setup Time	t_{13}	●	60	60	ns min

DB17 for 18-bit DAC code value, DB15 for 16 -bit DAC code value, and DB13 for 14 -bit DAC code value.

For a frame of SPI data operation, if the number of SCLK cycles during the chip select low level is greater than the number of bits of the DAC, the lower 18/16/14-bit data is valid, and the redundant high bits are ignored.

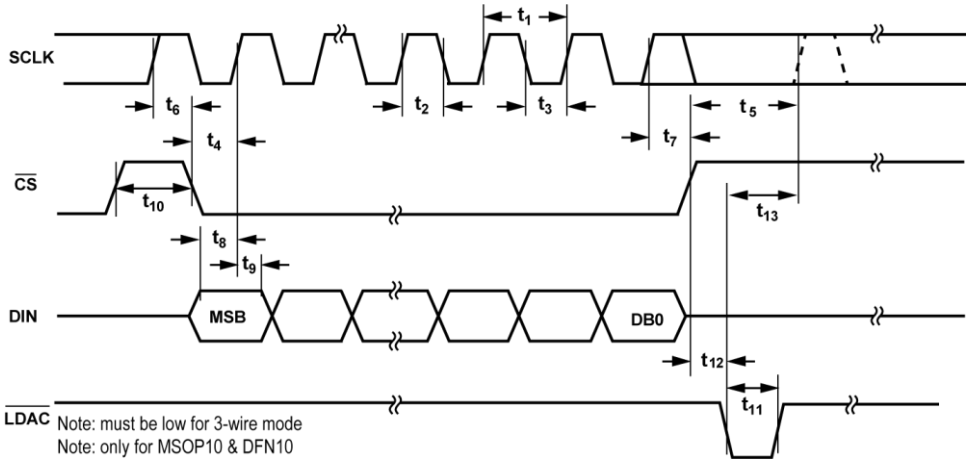


Figure 6. Digital Interface Timing

1 V_{DD} = 2.7 V to 5.5 V, the maximum SCLK frequency is 50 MHz.
2 All input signals are specified with t_R = t_F = 1 ns/V and from (V_{IL} + V_{IH})/2 level to start timing.

Typical Performance Characteristics

Unless otherwise noted, V_{DD} = 5.0 V, V_{REF} = 2.5 V, T_A = 25 °C.

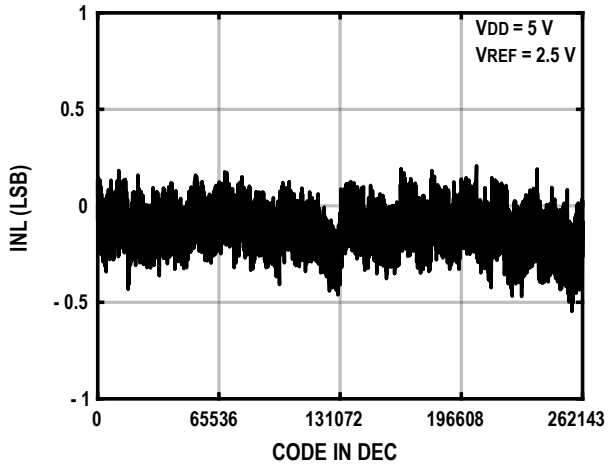


Figure 7. Integral Nonlinearity vs. Code-18 bits

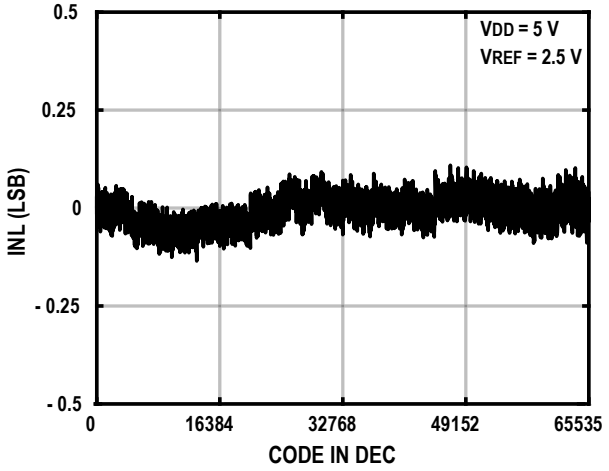


Figure 8. Integral Nonlinearity vs Code-16 bit

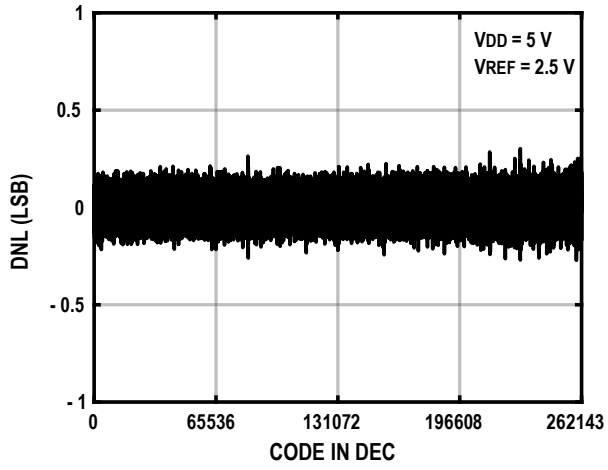


Figure 9. Differential Nonlinearity vs. Code-18 Bits

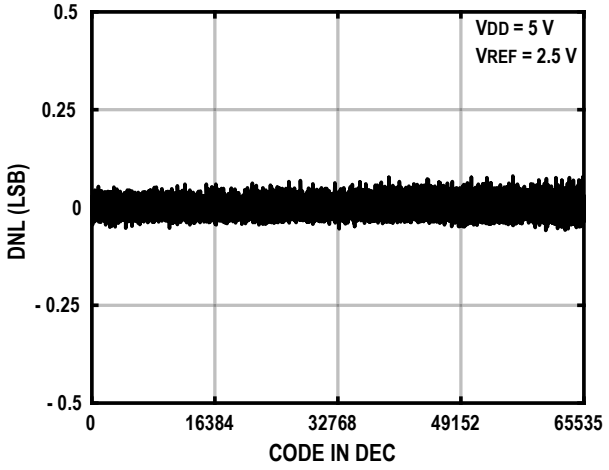


Figure 10. Differential Nonlinearity vs. Code-16 bits

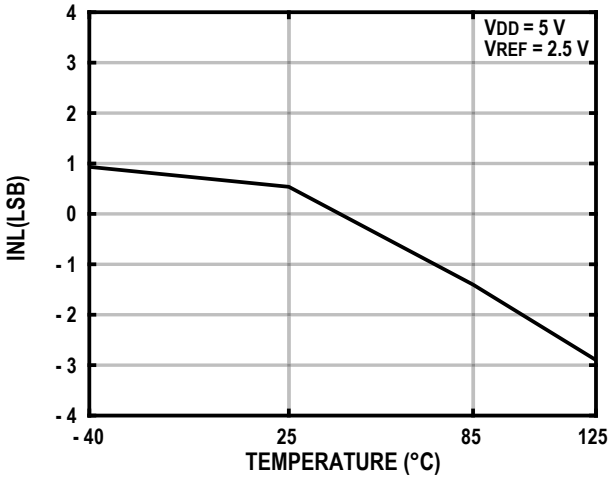


Figure 11. Integral Nonlinearity vs. Temperature-18 bits

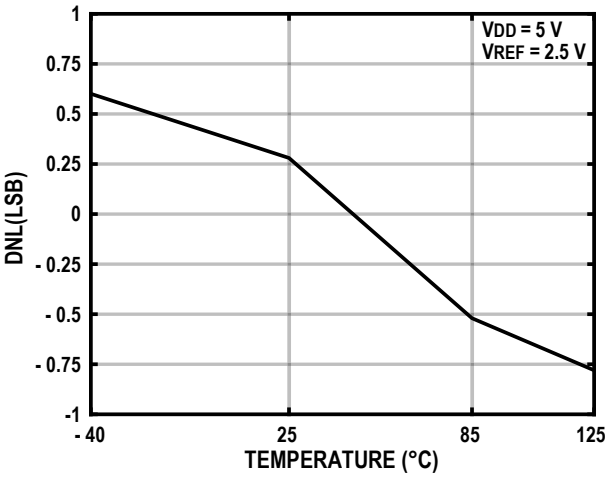


Figure 12. Differential Nonlinearity vs. Temperature-18 Bits

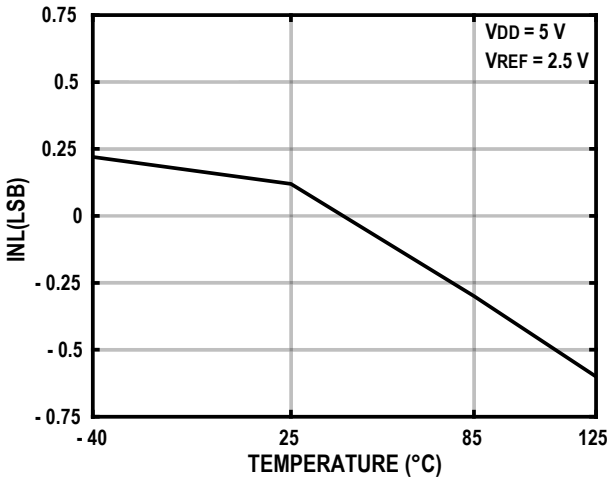


Figure 13. Integral Nonlinearity vs. Temperature-16 bits

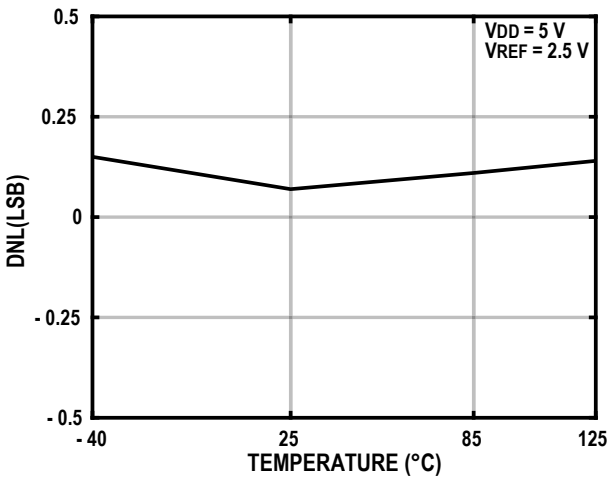


Figure 14. Differential Nonlinearity vs. Temperature-16 bits

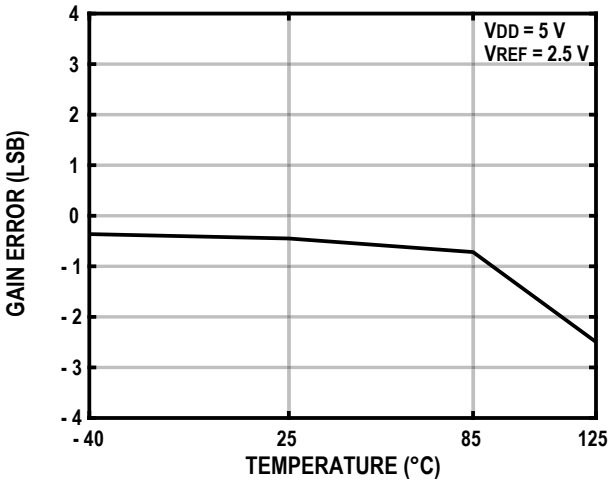


Figure 15. Gain Error vs Temperature-18 Bit

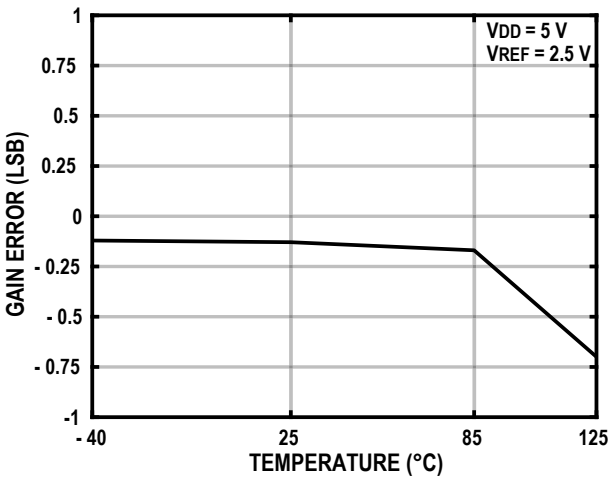


Figure 16. Gain Error vs Temperature-16 Bit

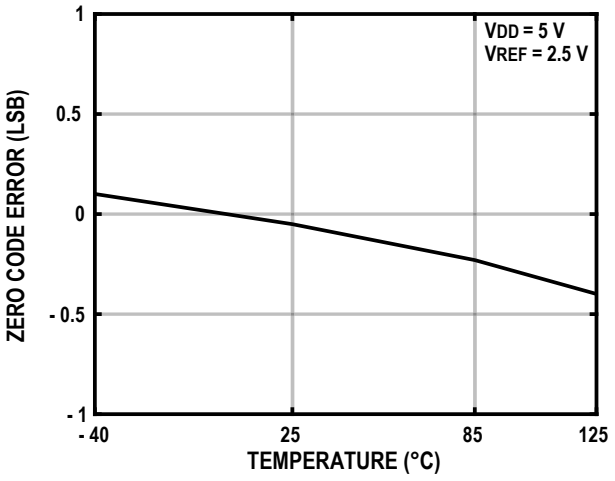


Figure 17. Zero Code Error vs Temperature-18 Bit

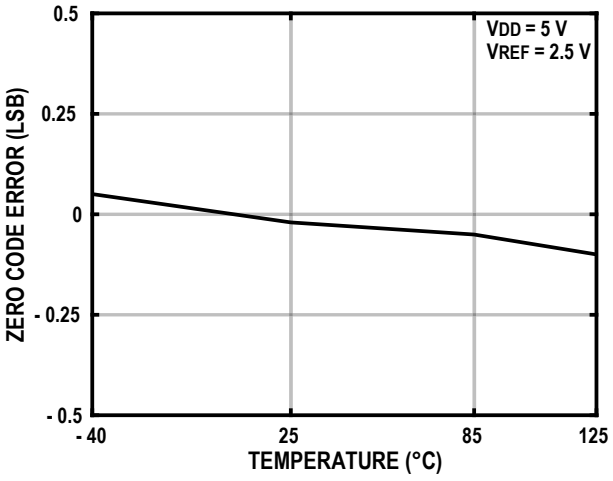


Figure 18. Zero Code Error vs Temperature-16 Bit

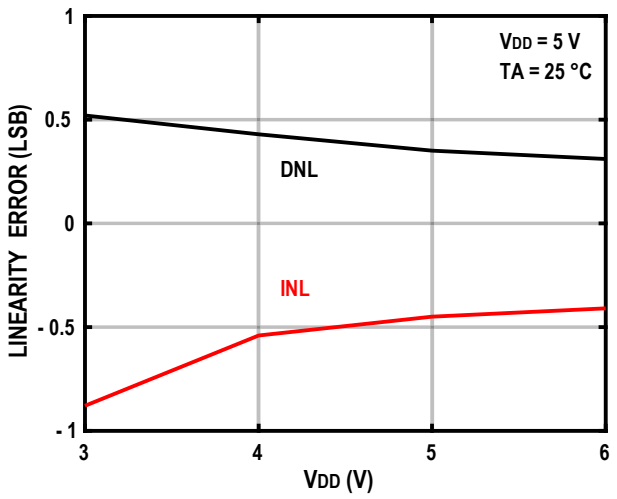


Figure 19. Linearity Error vs Supply Voltage-18 Bit

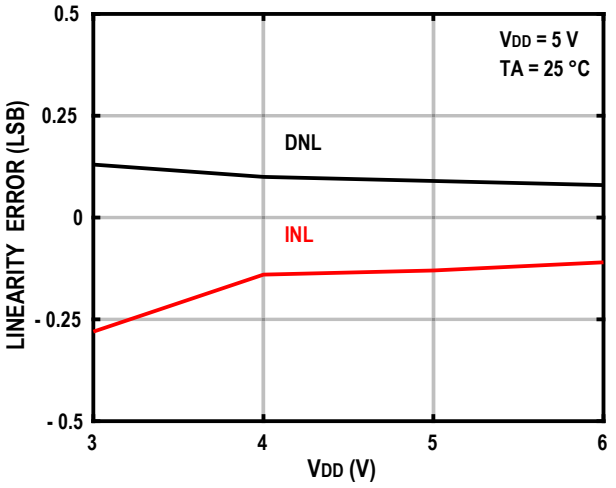


Figure 20. Linearity Error vs Supply Voltage-16 Bit

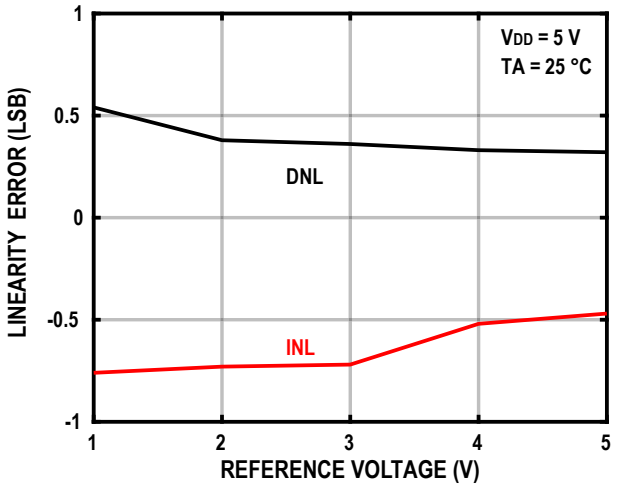


Figure 21. Linearity Error vs. Reference Voltage-18 Bit

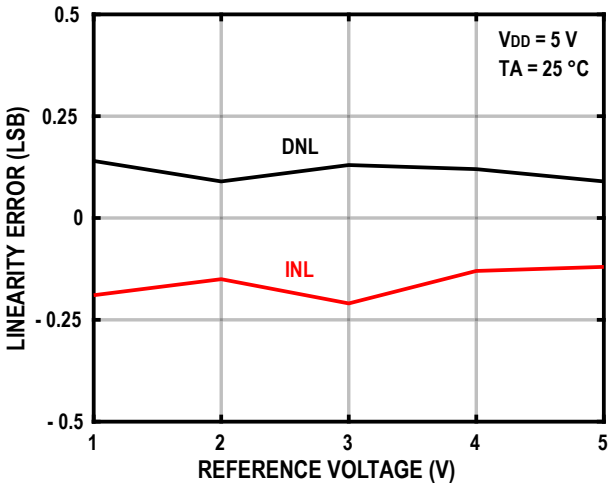


Figure 22. Linearity Error vs. Reference Voltage-16 Bit

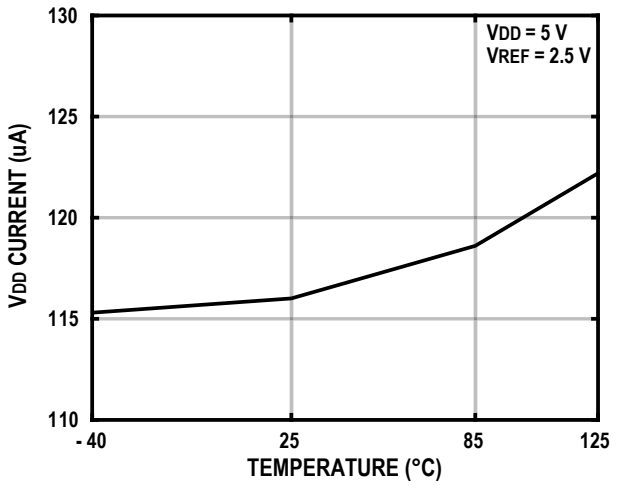


Figure 23. Supply Current vs. Temperature

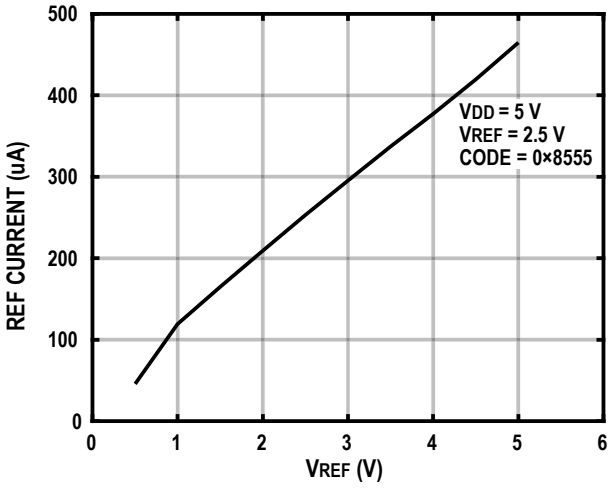


Figure 24. 16-bit DAC Reference Current vs. Voltage

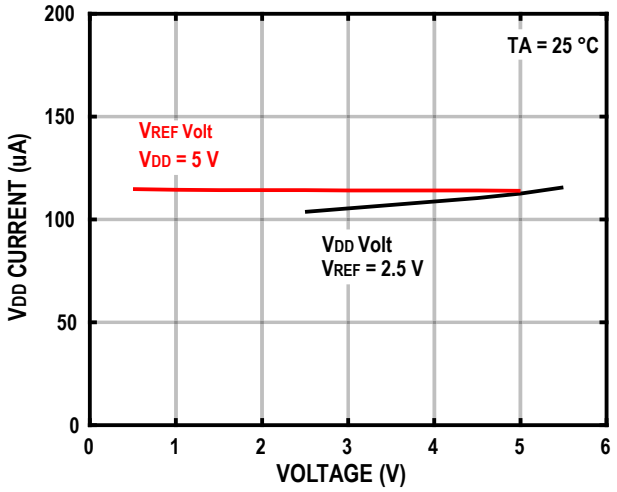


Figure 25. Current vs. Supply Voltage

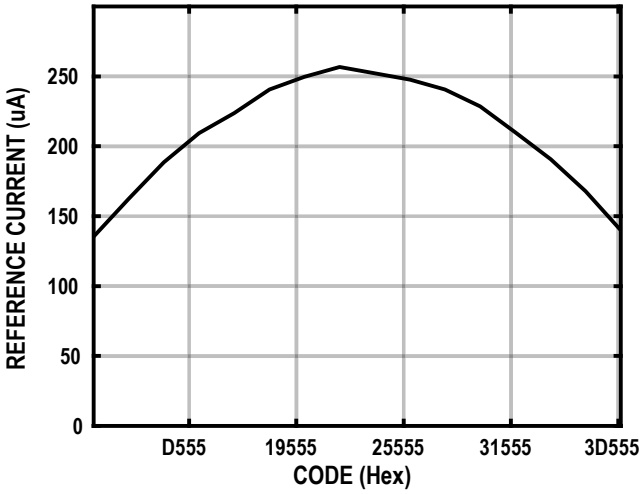


Figure 26. Reference Current vs. Code-18-bit

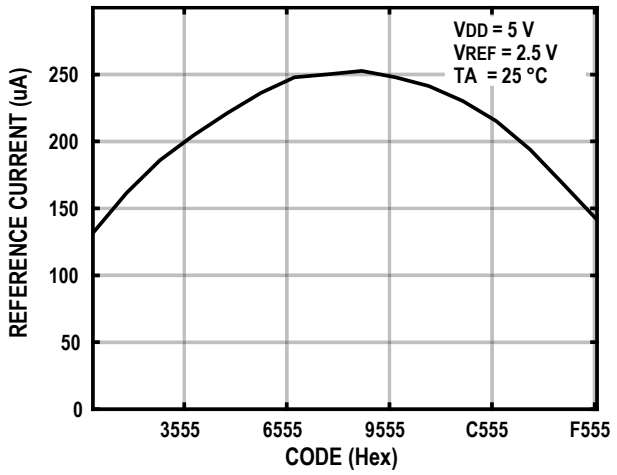


Figure 27. Reference Current vs. Code-16 bits

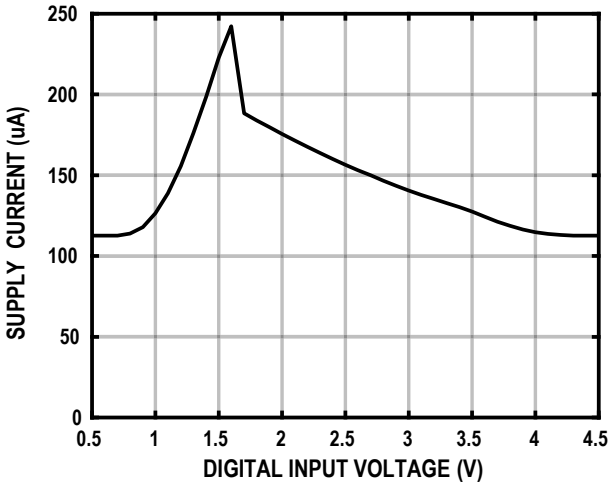


Figure 28. Supply Current vs. Digital Input Voltage

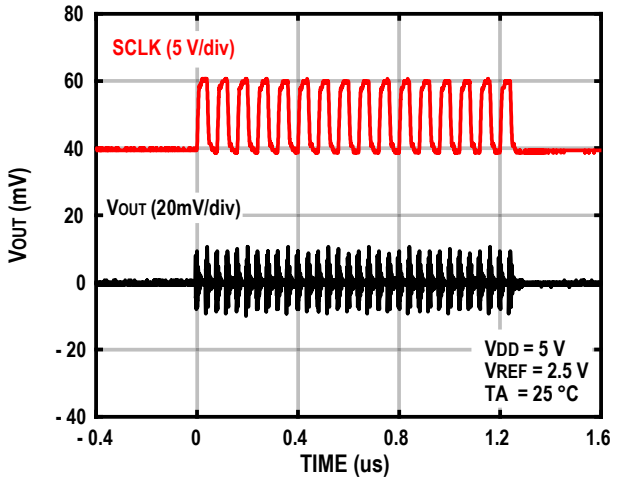


Figure 29. Digital Feedthrough

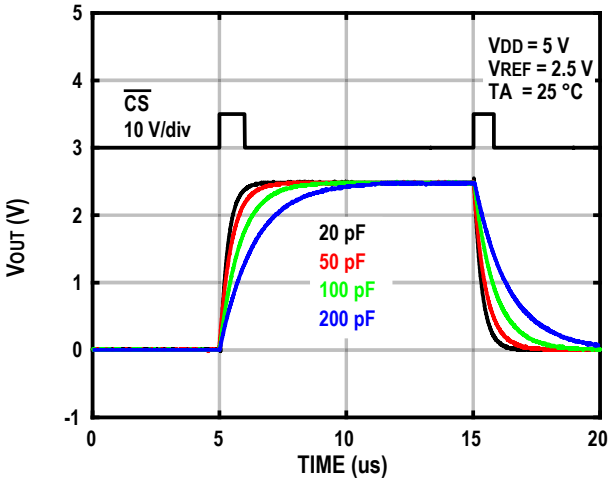


Figure 30. Large Signal Settling Time

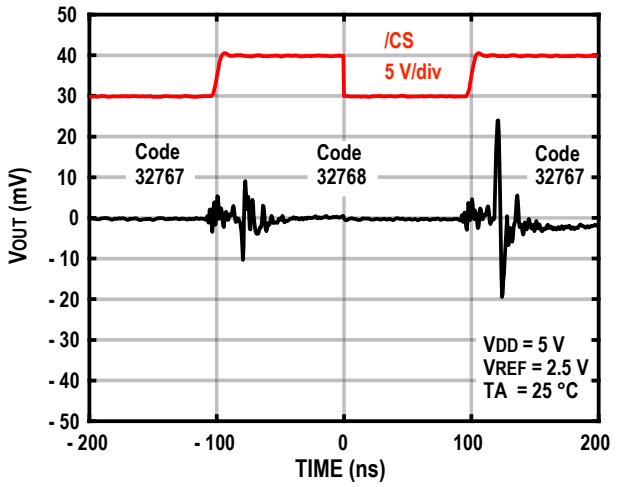


Figure 31. ZJC2541/3-16 DAC Glitch Pulse

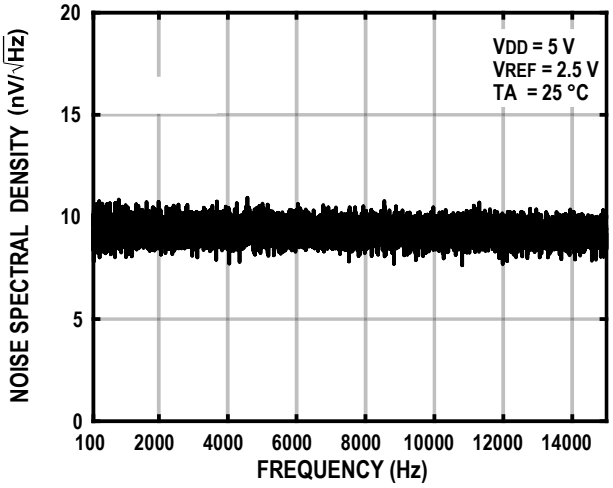


Figure 32. Noise Spectral Density vs. Frequency

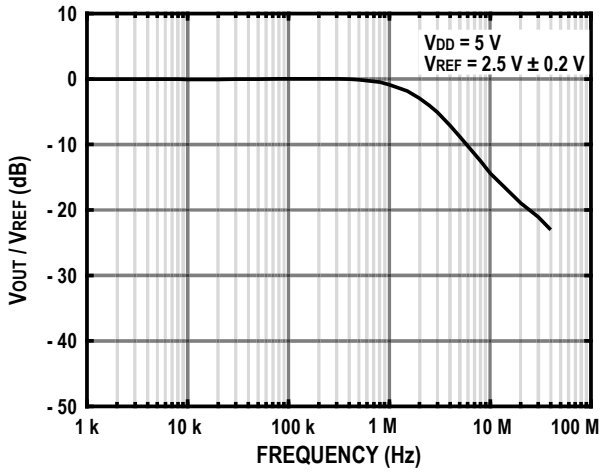


Figure 33. Multiplication Bandwidth

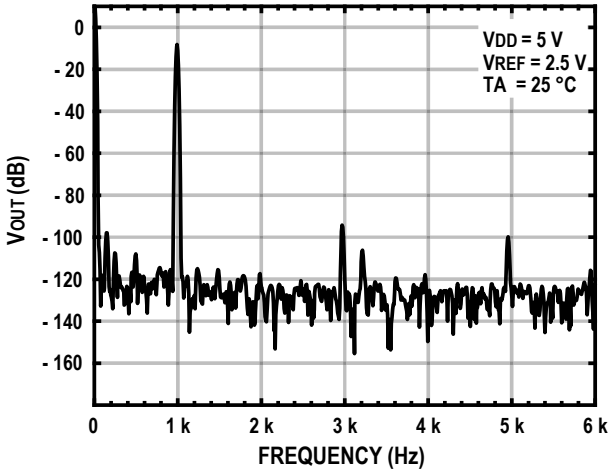


Figure 34. Harmonic Distortion

Theory Of Operation

ZJC2541/3 -18/16/14 is a single-channel 18/16/14 -bit, serial input, voltage output DAC. They operate from a single supply range of 2.7 V to 5.5 V and typically draw 120 μA from a 5 V supply. Data is written in 18/16/14 bit word format via a 3-wire serial interface. To ensure a known power-on state, these parts are designed with a power-on reset function. After ZJC2541 is powered on, the default output is 0 V; and after ZJC2543 is powered on, the default output is the middle level $V_{REF}/2$ of the reference.

Digital-to-Analog Conversion

The DAC architecture consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 35. The DAC structure of ZJC2541/3 is segmented. Taking ZJC2541-16 as an example, the four MSBs of the 16-bit data word are decoded to drive 15 switches, from E1 to E15. A switch connected to each termination resistor can gate AGND or V_{REF}. The lower 12 bits of the data word control the switching of switches S11 to S0 of the R-2R ladder network.

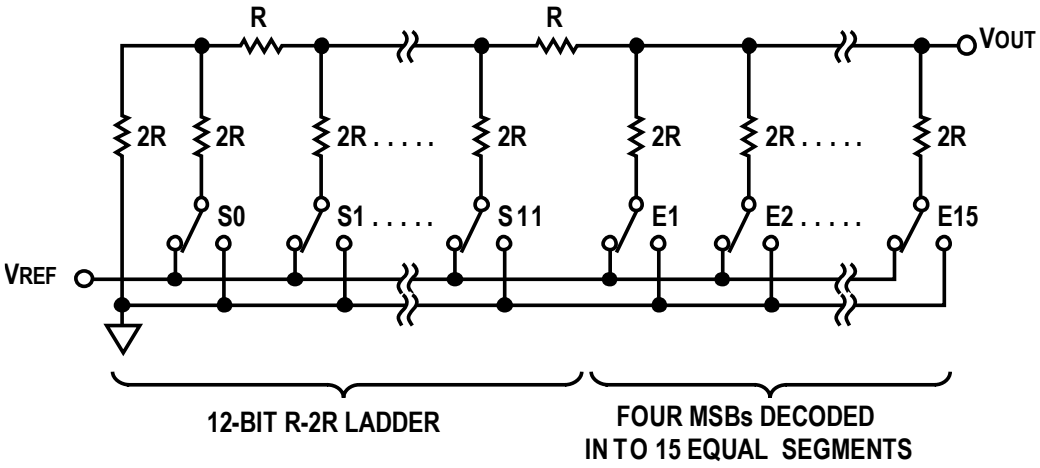


Figure 35. 16-bit DAC structure

With this type of DAC configuration, the output impedance is code independent, while the input impedance seen by the reference is code dependent. The output voltage is related to the reference level as shown in the following equation:

$$V_{OUT} = \frac{V_{REF} \times D}{2^N}$$

Where:

D is the decimal data word loaded into the DAC register.

N is the resolution of the DAC.

For a reference level of 2.5 V, the equation simplifies to:

$$V_{OUT} = \frac{2.5\ V \times D}{2^N}$$

This makes intermediate codes correspond to a V_{OUT} of 1.25 V and full codes correspond to a V_{OUT} of the DAC of 2.5 V-1 LSB.

The size of the LSB is $V_{REF}/2^N$.

Serial Interface

ZJC2541/3 is controlled by a general-purpose 3-wire serial interface with an operating clock frequency up to 50 MHz. The timing is shown in Figure 6. After $\overline{CS}$ a high-to-low transition, data is clocked by the serial (SCLK) Rising edge transfers synchronously into the input register. Data is loaded MSB first into 18/16/14-bit words. When all the data bits have been loaded into the serial input register, $\overline{CS}$ a rising edge on OUT transfers the contents of the shift register to the DAC.

The MSOP10 and DFN10 packages have $\overline{LDAC}$ features that allow the DAC latch to be updated asynchronously by pulling $\overline{LDAC}$ low after $\overline{CS}$ goes high. $\overline{LDAC}$ should be held high when data is being written to the input shift register. Alternatively, $\overline{LDAC}$ can be fixed low to update the DAC output by $\overline{CS}$ rising edge.

When initially loading data into the DAC, the specified number of bits of data should be loaded to prevent erroneous data in the output. If more than the specified number of digits are loaded, the data of the last few specified digits will be retained; if less than the specified number of digits is loaded, the previous valid data will be retained. For example, if ZJC2541-16 needs to interface with data less than 16 bits, it should be filled with 0 on the LSB bits.

Unipolar Output

ZJC2541/3 directly provides unipolar output swing from 0 V to $V_{REF.}$

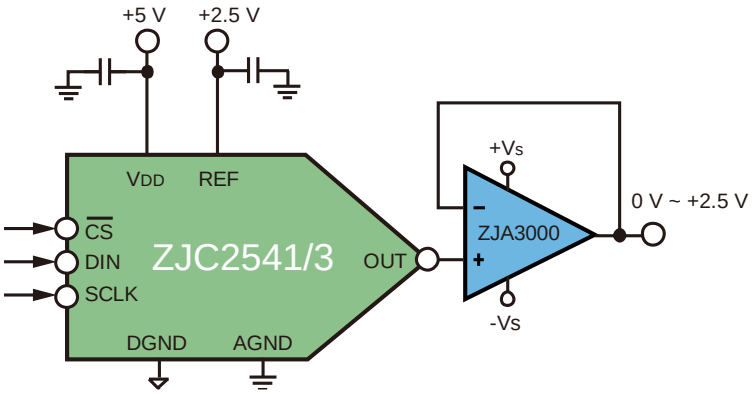


Figure 36. Typical Output Connections

ZJC2541/3-16 digital code value and ideal output voltage:

DAC Latch Data	Analog Output (Reference Input V_{REF})
1111 1111 1111 1111	V_{REF}×(65535/65536)
1000 0000 0000 0000	V_{REF}×(32768/65536) = ½ V_{REF}
0000 0000 0000 0001	V_{REF}×(1/65536)
0000 0000 0000 0000	0 V

The unipolar worst-case output voltage can be obtained by:

$$V_{OUT-UNI} = \frac{D}{2^{16}} \times (V_{REF-IDEAL} - V_{REF-ERROR} + V_{GE}) + V_{ZSE} + INL$$

Where:

$V_{OUT-UNI}$ is output in unipolar mode, and the unit is V.

D is the code value sent to the DAC.

$V_{REF-IDEAL}$ is the ideal voltage of the reference source, the unit is V.

$V_{REF-ERROR}$ is the voltage error of the reference source, the unit is V.

V_{GE} is gain error, the unit is V.

V_{ZCE} is the zero code error, the unit is V.

INL is the integral nonlinearity error in LSB .

ZJC2541/3-18- digit code value and ideal output voltage:

DAC Latch Data	Analog Output (Reference Input V_{REF})
11 1111 1111 1111 1111	V_{REF}×(262143/262144)
10 0000 0000 0000 0000	V_{REF}×(131072/262144) = ½ V_{REF}
00 0000 0000 0000 0001	V_{REF}×(1/262144)
00 0000 0000 0000 0000	0 V

ZJC2541/3-14 digital code value and ideal output voltage:

DAC Latch Data	Analog Output (Reference Input V_{REF})
11 1111 1111 1111	V_{REF}×(16383/16384)
10 0000 0000 0000	V_{REF}×(8192/16384) = ½ V_{REF}
00 0000 0000 0001	V_{REF}×(1/16384)
00 0000 0000 0000	0 V

Output Amplifier Selection

The selected op amp needs to have a very low offset voltage (For example, ZJC2541/3-16 when using 2.5 V reference voltage, 1 LSB is 38 μV) to eliminate the need for trimming the output bias. The input bias current should also be low because the bias current multiplied by the DAC output impedance (about 6.25 kΩ) will increase the zero code error. At the same time, the response of the operational amplifier should consider the settling time of the DAC. The output impedance of the DAC is constant and code independent, but to minimize gain error, the input impedance of the output amplifier should be as high as possible. The amplifier adds another time constant to the system, thus increasing the overall output settling time.

Precision operational amplifier ZJA3000 has low offset voltage (ambient temperature 35 μV), low noise (11 $nV/\sqrt{Hz}$), low input bias current (2 pA), is an excellent choice.

Reference Source And Ground

ZJC2541/3 input impedance is code dependent, so the reference pin should be driven from a low impedance source. The reference voltage range of ZJC2541/3 is 2 V ~ V_{DD}. The full-scale output voltage of the DAC is determined by the reference voltage.

Power On Reset

ZJC254 1/3 has a power-on reset function to ensure that the output is in a known state when powered on. At power-on, the ZJC2541-18/16/14 output voltage is 0 V; the ZJC2543-18/16/14 output voltage is $V_{REF}/2$ until the latch register data is loaded from the serial register. However, the serial input register is not cleared on power-up, so its contents are undefined.

Power Supply And Reference Decoupling

For accurate high-resolution performance, it is recommended that the reference voltage and supply pins be bypassed with a 10 μF capacitor in parallel with a 0.1 μF capacitor.

Controller Interface

Controllers, like MCU or FPGA, can communicate with ZJC2541/3 through a serial bus. The communication channel requires a 3-wire interface consisting of a clock signal, a data signal, and a chip select signal. ZJC2541/3 requires a 18/16/14-bit data word, and the data is valid on the rising edge of SCLK. ZJC2541/3 voltage output can be automatically completed after all data bits are locked (chip select $\overline{CS}$ rising edge); devices in MSOP10 and DFN10 packages can also use $\overline{LDAC}$ to update DAC output.

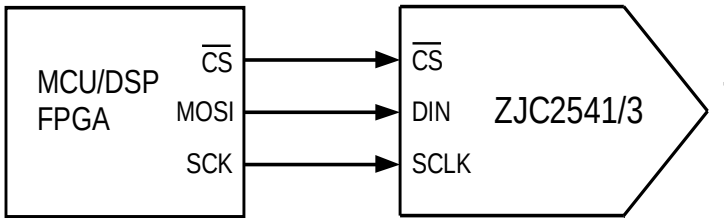


Figure 37. Connection between ZJC2541/3 and controller interface

Outline Dimensions

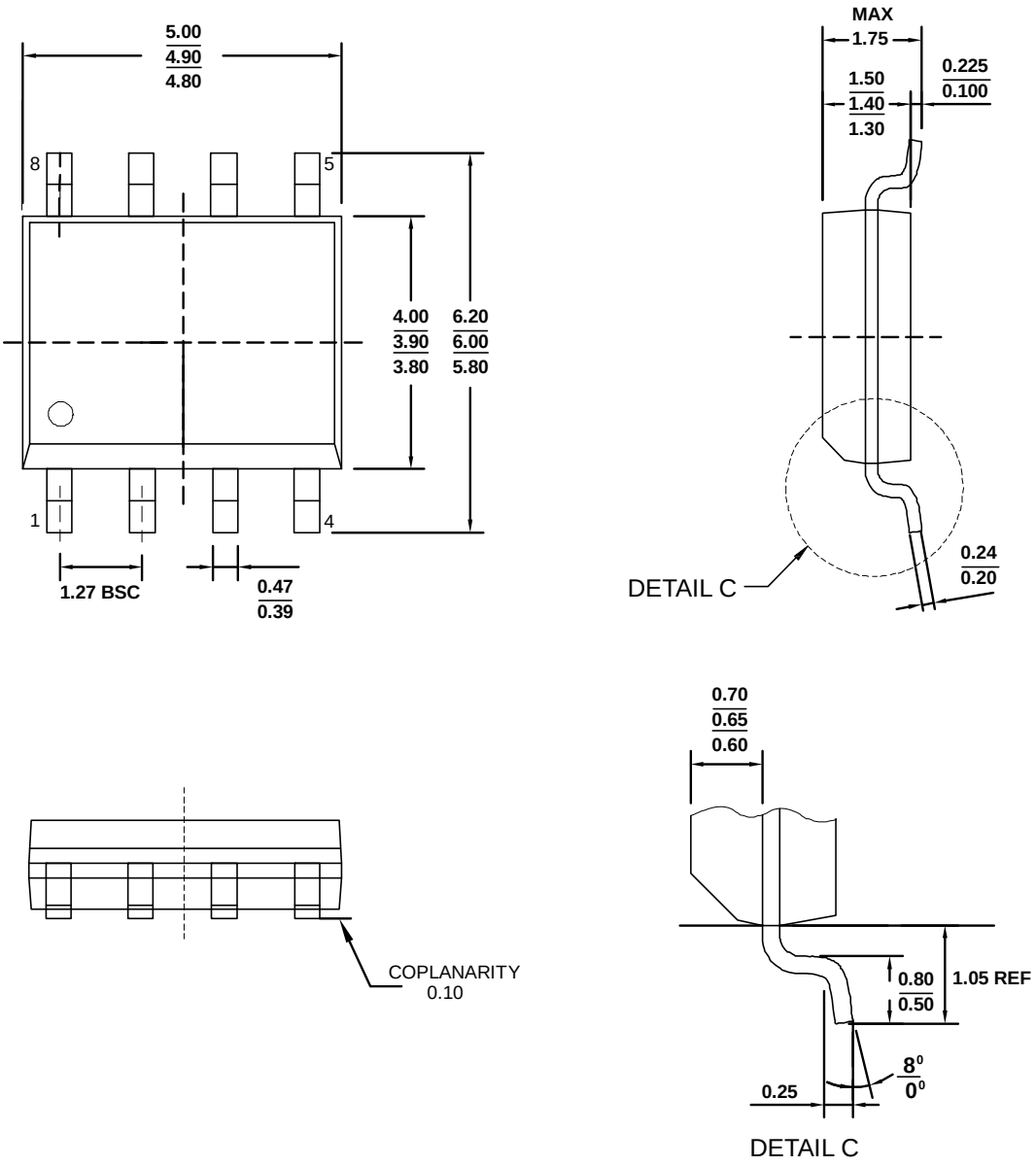


Figure 38. 8-Lead SOIC Package Dimensions shown in millimeter

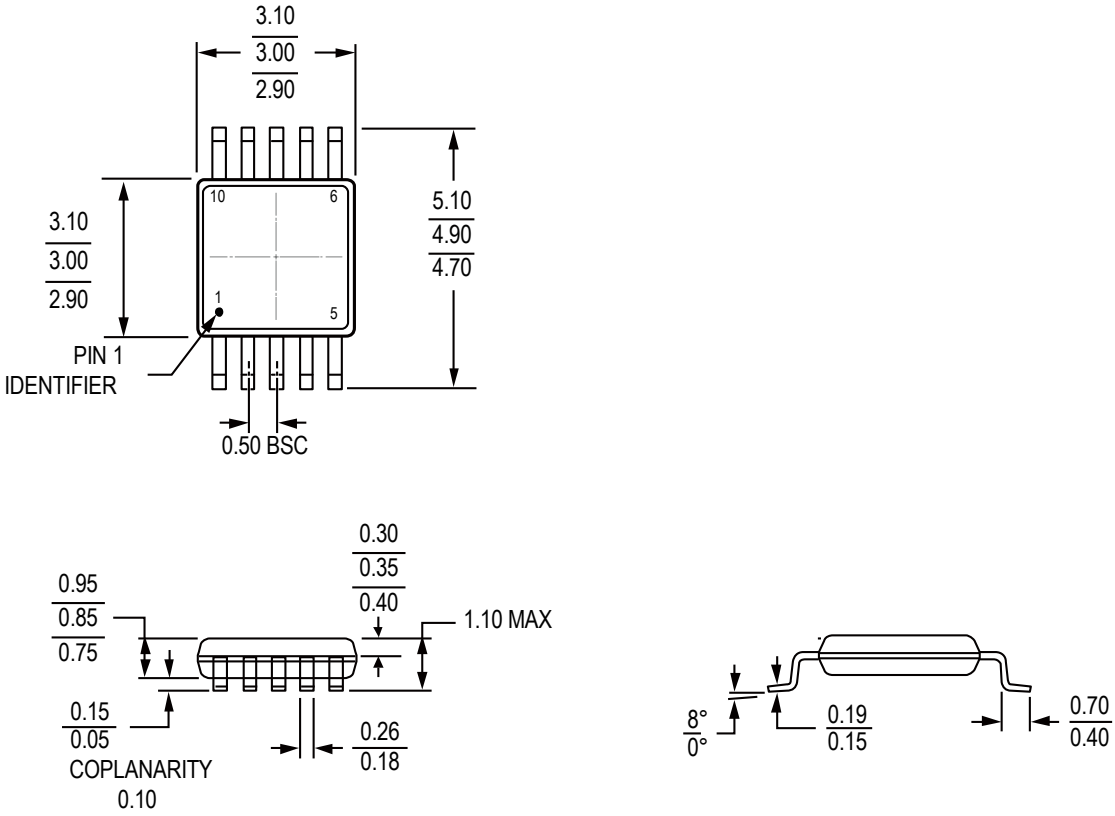


Figure 40. 10-Lead MSOP Package Dimensions shown in millimeter

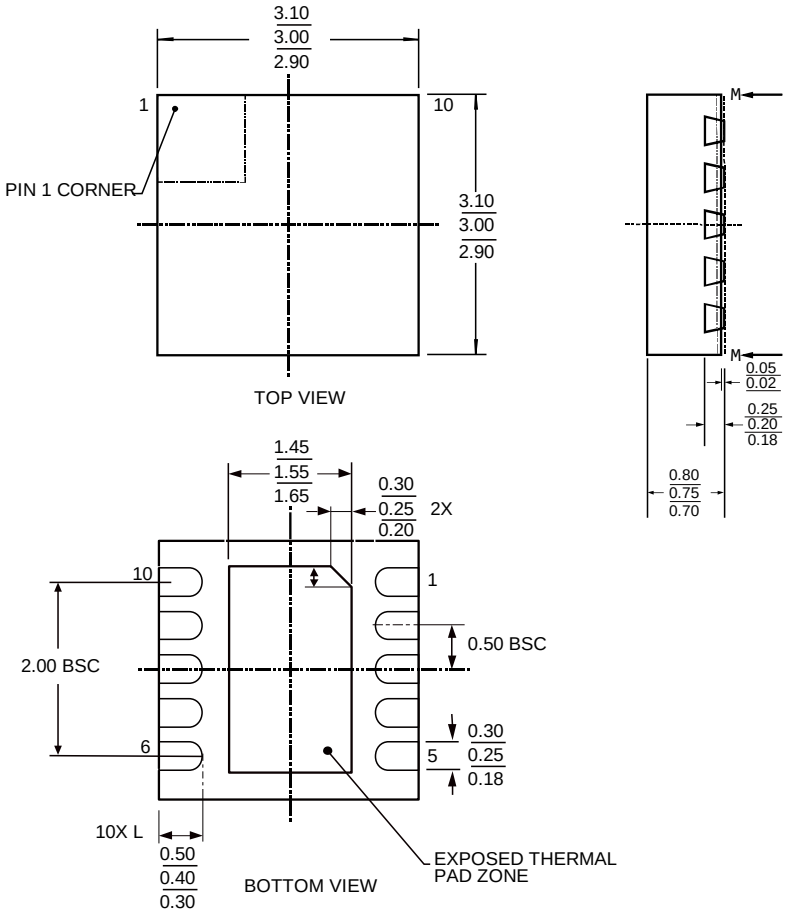
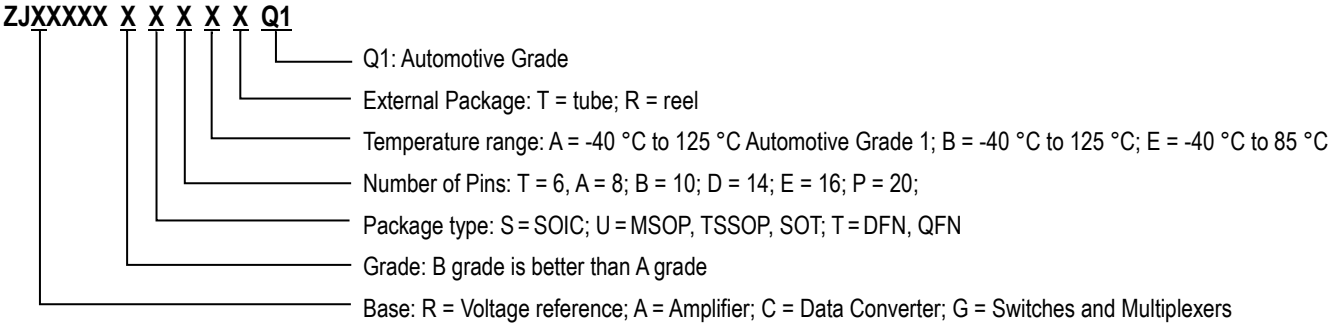


Figure 41. 10-Lead DFN Package Dimensions shown in millimeter

Ordering Guide

Model	Package	Orderable Device	Resolution (bit)	Silk Screen	Temperature Range (°C)	External Package
ZJC2541	SOIC-8	ZJC2541-18BSABT	18	2541-R	- 40 to +125	Tube
	SOIC-8	ZJC2541-18BSABR				13” Reel
	MSOP-10	ZJC2541-18BUBBT				Tube
	MSOP-10	ZJC2541-18BUBBR				13” Reel
	DFN-10	ZJC2541-18BTBBR				13” Reel
	SOIC-8	ZJC2541-16BSABT	16	2541-P	- 40 to +125	Tube
	SOIC-8	ZJC2541-16BSABR				13” Reel
	MSOP-10	ZJC2541-16BUBBT				Tube
	MSOP-10	ZJC2541-16BUBBR				13” Reel
	DFN-10	ZJC2541-16BTBBR				13” Reel
	SOIC-8	ZJC2541-14BSABT	14	2 541-N	- 40 to +125	Tube
	SOIC-8	ZJC2541-14BSABR				13” Reel
	MSOP-10	ZJC2541-14BUBBT				Tube
	MSOP-10	ZJC2541-14BUBBR				13” Reel
	DFN-10	ZJC2541-14BTBBR				13” Reel
ZJC2543	SOIC-8	ZJC2543-18BSABT	18	2543-R	- 40 to +125	Tube
	SOIC-8	ZJC2543-18BSABR				13” Reel
	MSOP-10	ZJC2543-18BUBBT				Tube
	MSOP-10	ZJC2543-18BUBBR				13” Reel
	DFN-10	ZJC2543-18BTBBR				13” Reel
	SOIC-8	ZJC2543-16BSABT	16	2543-P	- 40 to +125	Tube
	SOIC-8	ZJC2543-16BSABR				13” Reel
	MSOP-10	ZJC2543-16BUBBT				Tube
	MSOP-10	ZJC2543-16BUBBR				13” Reel
	DFN-10	ZJC2543-1 6 BTBBR				13” Reel
	SOIC-8	ZJC2543-14BSABT	14	2543-N	- 40 to +125	Tube
	SOIC-8	ZJC2543-14BSABR				13” Reel
	MSOP-10	ZJC2543-14BUBBT				Tube
	MSOP-10	ZJC2543-14BUBBR				13” Reel
	DFN-10	ZJC2543-14BTBBR				13” Reel

Orderable Device Explanation



Related Parts

Part Number	Description	Comments
ADC		
ZJC2000 / 2010	18-bit 400 / 200 kSPS SAR ADC	Fully differential, MSOP-10 and DFN-10 packages
ZJC2001 / 2011	16-bit 500 / 250 kSPS SAR ADC	Fully differential, MSOP-10 and DFN-10 packages
ZJC2002 / 2012	16-bit 500 / 250 kSPS SAR ADC	Pseudo-differential Unipolar, MSOP-10 and DFN-10 packages
ZJC2003 / 2013	16-bit 500 / 250 kSPS SAR ADC	Pseudo-differential Bipolar, MSOP-10 and DFN-10 packages
ZJC2004 / 2014	18-bit 400 / 200 kSPS SAR ADC	Pseudo-differential Unipolar, MSOP-10 and DFN-10 packages
ZJC2005 / 2015	18-bit 400 / 200 kSPS SAR ADC	Pseudo-differential Bipolar, MSOP-10 and DFN-10 packages
ZJC2007 / 2017	14-bit 600 / 300 kSPS SAR ADC	Pseudo-differential Unipolar, MSOP-10 and DFN-10 packages
ZJC2008 / 2018	14-bit 600 / 300 kSPS SAR ADC	Pseudo-differential Bipolar, MSOP-10 and DFN-10 packages
DAC		
ZJC2541-18 / 16 / 14 ZJC2543-18 / 16 / 14	18 / 16 / 14-bit 1 MSPS single-channel precision DAC	Unipolar output, power-on output 0 V (ZJC2541) & $V_{REF}/2$ (ZJC2543), SOIC-8 / MSOP-10 / DFN-10 packages
ZJC2542-18 / 16 / 14 ZJC2544-18 / 16 / 14	18 / 16 / 14-bit 1 MSPS single-channel precision DAC	Bipolar output, power-on output 0 V (ZJC2542) & $V_{REF}/2$ (ZJC2544), SOIC-14 / TSSOP-16 / QFN-16 packages
Amplifier		
ZJA3000-1/2/4	Single/Dual/Quad 36 V Precision Continuous Signal Processing Op Amps	3 MHz BW, 35 µV max Vos, 0.5 µV/°C m TCVos, SOIC-8 / MSOP-8 / SOIC-14 / TSSOP-14 packages
ZJA3600	36 V High Precision Instrumentation Amplifier	CMRR 110 dB min (G = 1), 100 pA max Ib, 25µV max Vosi, gain error 5 ppm max, classic pin-out in SOIC-8 package
ZJA3601	36 V High Precision Instrumentation Amplifier	CMRR 110 dB min (G = 1), 100 pA max Ib, 25 µV max Vosi, gain error 5ppm max, SOIC-8/MSOP-8 packages in optimized pin-out
ZJA3620	36 V Precision Instrumentation Amplifier	CMRR 93 dB min (G = 10), 2 nA max Ib, SOIC-8 package
Voltage Reference		
ZJR1000	15 V supply precision voltage reference	V_{OUT} = 1.25 / 2.048 / 2.5 / 3 / 4.096 / 5 V, 5 ppm/°C max TempCo, SOIC-8/MSOP-8 packages
ZJR1001 ZJR1002	5.5 V Low Power Precision Voltage Reference (ZJR1001 with off-chip filter function)	V_{OUT} = 2.5 / 3 / 4.096 / 5 V, 5 ppm/° C max TempCo, 130 µ A Isy, SOT23-6 package
ZJR1003	5.5 V Low Power Precision Voltage Reference	V_{OUT} = 2.5 / 3 / 4.096 / 5 V, 5 ppm/°C max TempCo, 130 µ A Isy, SOIC-8 / MSOP-8 packages
Switches and Multiplexers		
ZJG4438/4439	36 V Fault-Protected 8:1 / Dual 4:1 Multiplexer	Fault-protection - 50 V to + 50 V power-on or power-off, Ron 270 Ω, SOIC-16 / TSSOP-16 packages