36V Precision, Low Bias Current Op Amps

Features

- Low Offset Voltage:
  35 μV max (SOIC package)
  55 μV max (other packages)
- Low Offset Voltage Temperature Drift:
  0.5 μV/°C max (B Grade, SOIC package)
  1.0 μV/°C max (A Grade, SOIC package)
- Low Input Bias Current: 25 pA max
- Low Noise: 11 nV /$\sqrt{Hz}$ (f = 1 kHz)
- CMRR: 120 dB min
- PSRR: 120 dB min (full temperature range)
- A_{Vol}: 120 dB min (full temperature range)
- Supply Current: 1 mA/amplifier
- Gain Bandwidth Product: 3 MHz, unit gain stable
- Single/dual Power Supply: ±2.25 V to ±18 V, 4.5 V to 36 V
- Specified Temperature Range: -40 °C to +125 °C

Applications

- Precision data acquisition
- Instrumentation
- Sensor signal conditioning
- Industrial control
- Communication systems
- Smart grid

General Description

ZJA3001 series high-precision continuous operational amplifiers featuring lower than 35 μV offset voltage, better than 0.5 μV/°C offset voltage drift, 25 pA input bias current and 11 nA /$\sqrt{Hz}$ low noise. These features make them exceptionally suitable for precision signal conditioning, such as precision sensor interface, voltage amplification, current to voltage conversion and filtering. ZJA3001 has single, dual and quad channel versions.

The ZJA3001 has a wide power supply voltage range, operating from ±2.25 V to ±18 V for dual-supply operation or 4.5 V to 36V for single-supply. It further expands its input capabilities to negative rail, making it ideal for a variety of applications.

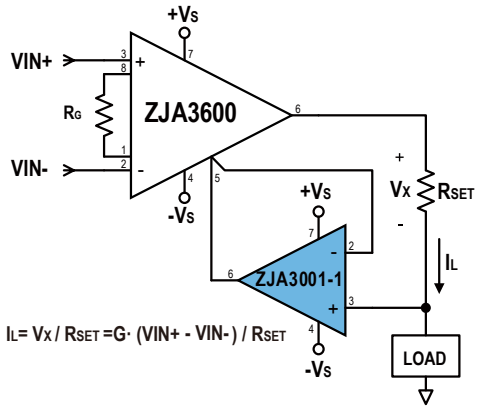
Ideal for demanding applications requiring precision and reliability, the ZJA3001 series boast the highest moisture sensitivity level (MSL-1), making them ideal for reflow soldering and high-volume production. They also operate reliably across a wide temperature range of -40 °C to +125 °C, making them perfect for precision sensor interfaces, medical instrumentation, and industrial control systems.

ZJA3001 series are available in single, dual, and quad configurations:

ZJA3001-1 (single): SOIC-8 and MSOP-8
ZJA3001-2 (dual): SOIC-8 and MSOP-8
ZJA3001-4 (quad): SOIC-14 and TSSOP-14

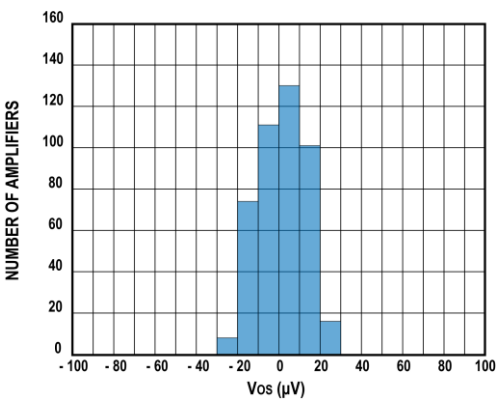
Application Examples

V-I conversion circuit



Typical Performance Characteristics

25 °C Offset Voltage Distribution, SOIC-8 Package



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Version (Release B) [1]

Revision History

April 2024 - Release B

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Orderable Device Explanation update at page 27

June 2023 - Release A

[1] Information furnished by ZJW Microelectronics is believed to be accurate and reliable. However, no responsibility is assumed by ZJW Microelectronics for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of ZJW Microelectronics. Trademarks and registered trademarks are the property of their respective owners.

Pin Configurations and Function Descriptions

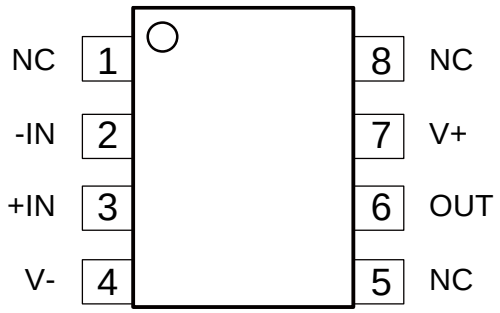

Figure 1. ZJA3001-1 Pin Configuration (8-lead SOIC and MSOP)

Mnemonic	Pin No.	I/O	Description
NC	1, 5, 8	--	No internal circuit connection
-IN	2	I	Inverting input
+IN	3	I	Non-inverting input
V-	4	--	Negative power supply
OUT	6	O	Output
V+	7	--	Positive power supply

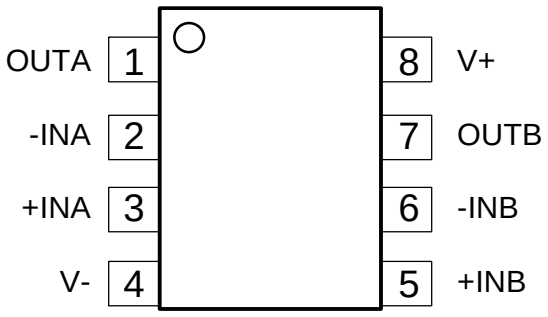

Figure 2. ZJA3001-2 Pin Configuration (8-lead SOIC and MSOP)

Mnemonic	Pin No.	I/O	Description
OUTA	1	O	Channel A output
-INA	2	I	Channel A inverting input
+INA	3	I	Channel A non-inverting input
V-	4	--	Negative power supply
+INB	5	I	Channel B non-inverting input
-INB	6	I	Channel B inverting input
OUTB	7	O	Channel B output
V+	8	--	Positive power supply

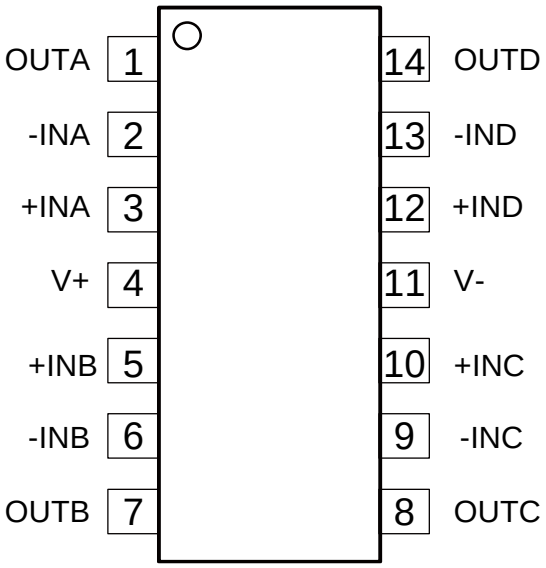

Figure 3. ZJA3001-4 Pin Configuration (14-lead SOIC and TSSOP)

Mnemonic	Pin No.	I/O	Description
OUTA	1	O	Channel A output
-INA	2	I	Channel A inverting input
+INA	3	I	Channel A non-inverting input
V+	4	--	Positive power supply
+INB	5	I	Channel B non-inverting input
-INB	6	I	Channel B inverting input
OUTB	7	O	Channel B output
OUTC	8	O	Channel C output
-INC	9	I	Channel C inverting input
+INC	10	I	Channel C non-inverting input
V-	11	--	Negative power supply
+IND	12	I	Channel D non-inverting input
-IND	13	I	Channel D inverting input
OUTD	14	O	Channel D output

Absolute Maximum Ratings [1]

Parameter	Rating
Supply Voltage	40 V
Input Voltage	$\pm V_{SY}$
Input Current [2]	±10 mA
Differential Input Voltage	$(+V_{SY})- (-V_{SY})$
Output Short-Circuit Duration to GND [3]	Continuous
Operating Temperature Range	-40 °C to +125 °C
Storage Temperature Range	-65 °C to +150 °C
Junction Temperature Range	-65 °C to +150 °C
Maximum Reflow Temperature [4]	260 °C
Lead Temperature, Soldering (10 sec)	300 °C
Electrostatic Discharge (ESD) [5]	
Human Body Model (HBM) [6]	1.5 kV
Charged Device Model (CDM) [7]	1 kV

Thermal Resistance [8]

Package Type	θ_{JA}	θ_{JC}	Unit
SOIC-8	158	43	°C/W
SOIC-14	120	36	°C/W
MSOP-8	190	44	°C/W
TSSOP-14	240	43	°C/W

[1] These ratings apply at 25 °C, unless otherwise noted. Note that stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] There are clamping diodes between the input pins and the power pins, and also between each other. When the input signal exceeds the supply rail by 0.3V, the input current is limited to 10 mA.

[3] Limited by Over Temperature Protection (OTP).

[4] IPC/JEDEC J-STD-020 Compliant

[5] Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[6] ANSI/ESDA/JEDEC JS-001 Compliant

[7] ANSI/ESDA/JEDEC JS-002 Complaint

[8] θ_{JA} addresses the conditions for soldering devices onto circuit boards to achieve surface mount packaging.

Specifications

The ● denotes the specification which apply over the specified temperature range, otherwise specifications are at V_S = ±15 V, V_{CM} = 0 V, T_A = 25 °C.

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
INPUT CHARACTERISTICS							
Offset Voltage	V_{OS}	B Grade, SOIC-8/SOIC-14			15	35	μV
			●		25	65	μV
		A Grade, SOIC-8/SOIC-14			15	35	μV
			●		40	100	μV
		B Grade, MSOP-8/TSSOP-14			25	55	μV
			●		40	85	μV
		A Grade, MSOP-8/TSSOP-14			25	55	μV
			●		70	160	μV
Offset Voltage Drift	TCV_{OS}	B Grade, SOIC-8/SOIC-14	●		0.25	0.5	μV/°C
		A Grade, SOIC-8/SOIC-14	●		0.5	1.0	μV/°C
		B Grade, MSOP-8/TSSOP-14	●		0.4	0.8	μV/°C
		A Grade, MSOP-8/TSSOP-14	●		0.7	1.5	μV/°C
Input Bias Current	I_B				5	25	pA
			●			5	nA
Input Offset Current	I_{OS}					10	pA
			●			2	nA
Input voltage range	IVR			-13		13	V
Common-ode Rejection Ratio	CMRR	V_{CM} = -13 V to 13 V		120	130		dB
			●	114			dB
Open-Loop Voltage Gain	A_{VOL}	R_L = 10 kΩ, Vo = ±10 V		126	140		dB
			●	120			dB
		R_L = 2 kΩ, Vo = ±10 V		126	140		dB
			●	120			dB
Input resistance/capacitance	R_{IN} /C_{IN}	Differential Mode			1.5/5.7		GΩ/pF
		Common Mode			2.5/1.7		TΩ/pF
OUTPUT CHARACTERISTICS							
Output Voltage (High)	V_{OH}	R_L = 10 kΩ			50	150	mV
			●		75	250	mV

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
		R_L = 2 kΩ			200	350	mV
			●		300	550	mV
Output Voltage (Low)	V_{OL}	R_L = 10 kΩ			40	150	mV
			●		60	250	mV
		R_L = 2 kΩ			160	350	mV
			●		240	550	mV
Short-Circuit Current	I_{SC}				67		mA
Open-Loop Output Impedance	Z_{OUT}	F = 1 kHz			15		Ω
POWER SUPPLY							
Supply Current (per Amplifier)	I_{SY}	V_O = 0 V			1.0	1.1	mA
			●			1.2	mA
Power Supply Rejection Ratio	PSRR	V_{SY} = ±3 V to ±18 V		126	140		dB
			●	120			dB
DYNAMIC PERFORMANCE							
Slew Rate	SR	R_L = 2 kΩ			2.3		V/μs
Gain Bandwidth Product	GBP	R_L = 2 kΩ, G = 100, VIN = 100 mV_{P-P}			3		MHz
Settling Time	t_S	to 0.1 %, G = -1, 0 to 10 V step			4.6		μs
		to 0.01 %, G = -1, 0 to 10 V step			8.8		μs
Overload Recovery Time	t_{OR}	R_L = 10 kΩ, G = -10, VIN = ±2 V step			330		ns
Total Harmonic Distortion + Noise	THD+N	R_L = 2 kΩ, G = 1, f = 1 kHz, V_O = 3.5 Vrms			-124		dB
Phase Margin	PM	R_L = 2 kΩ, G = 1, VIN = 100 mV_{P-P}			55		°
Multiple Amplifier Channel Separation	C_S	R_L = 10 kΩ, f = 1 kHz			150		dB
NOISE PERFORMANCE							
Voltage Noise	$e_{n,\ P-P}$	0.1 Hz to 10 Hz			2		$μV_{P-P}$
Voltage Noise Density	e_n	f = 1 kHz			11		$nV/\sqrt{Hz}$
Current Noise Density	i_n	f = 1 kHz			2		$fA/\sqrt{Hz}$
OVER TEMPERATURE PROTECTION							
Trigger Temperature	T_{IN}				150		°C
Exit Temperature	T_{EXIT}				130		°C
TEMPERATURE RANGE		Specified Temperature Range		-40		125	°C

Typical Performance Characteristics

Unless otherwise stated, V_{SY} = ±15.0 V, V_{CM} = 0 V, T_A = 25 °C.

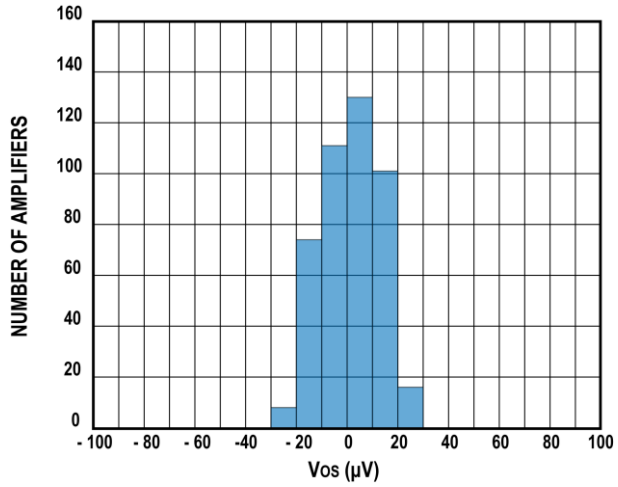

Figure 4. Input Offset Voltage Distribution, SOIC-8 Package

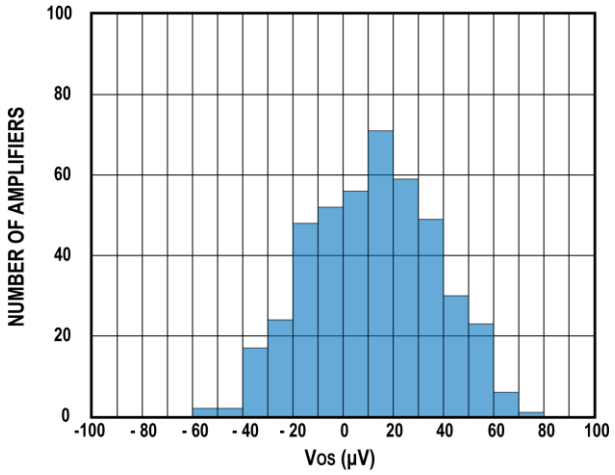

Figure 5. Input Offset Voltage Distribution at -40 °C, SOIC-8 Package

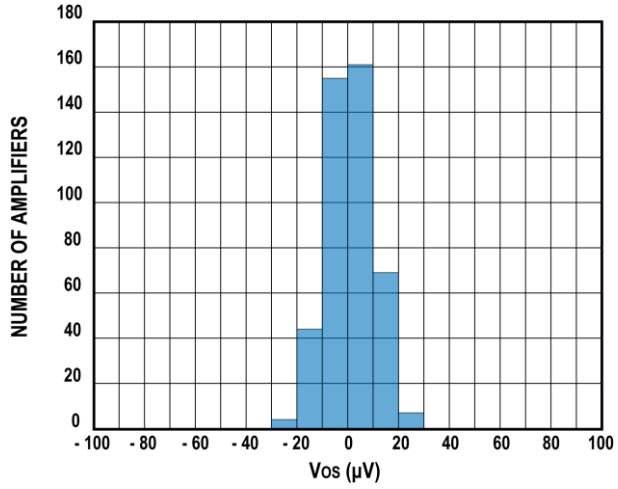

Figure 6. Input Offset Voltage Distribution at 85 °C, SOIC-8 Package

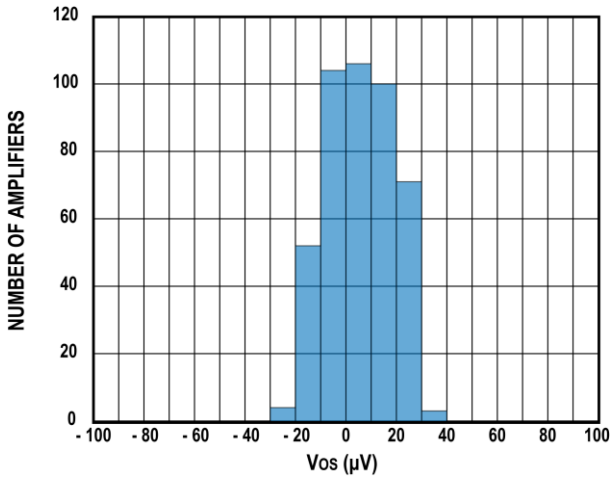

Figure 7. Input Offset Voltage Distribution at 125 °C, SOIC-8 Package

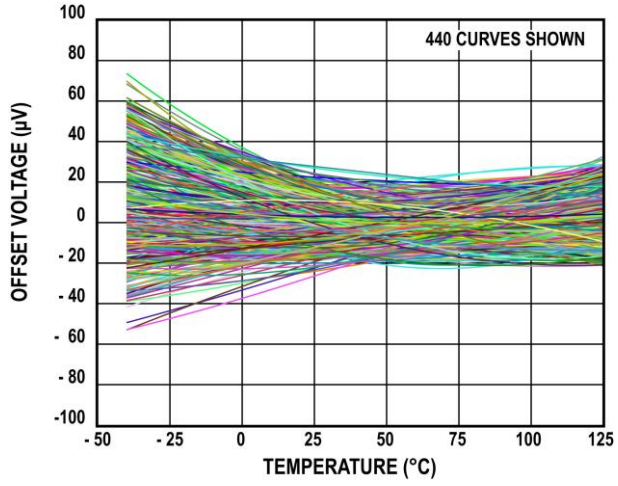

Figure 8. Input Offset Voltage vs. Temperature, SOIC-8 Package

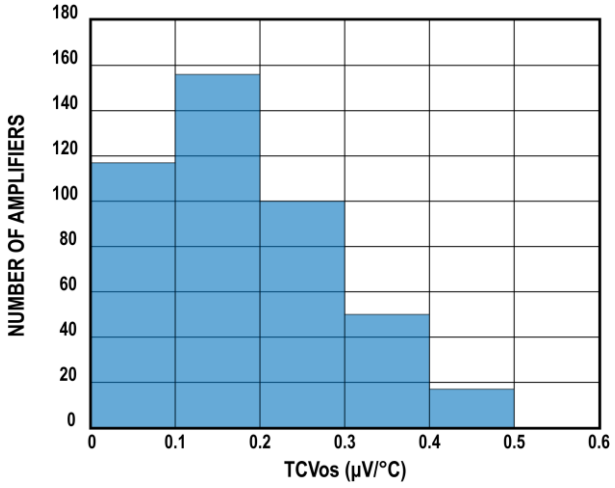

Figure 9. Input Offset Voltage Drift Distribution, SOIC-8 Package

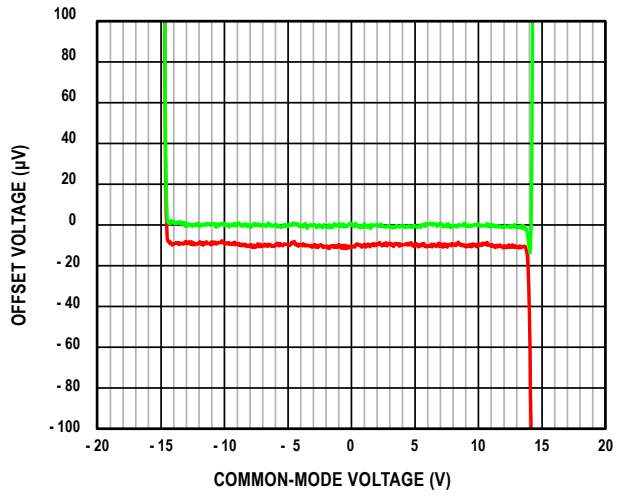

Figure 10. Offset Voltage vs. Input Common-Mode Voltage

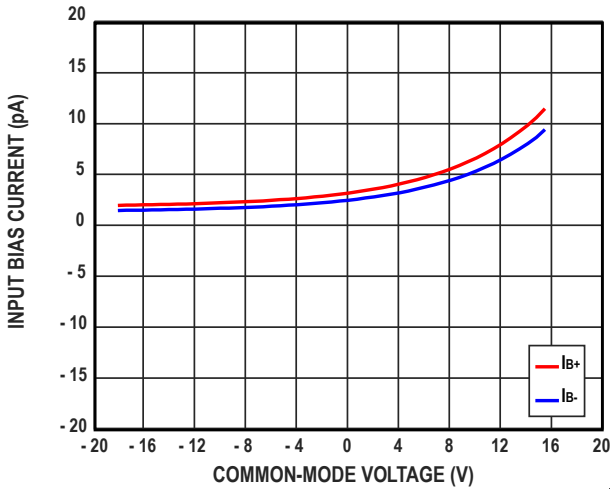

Figure 11. Input Current vs. Input Common-Mode Voltage (V_{SY} =±18 V)

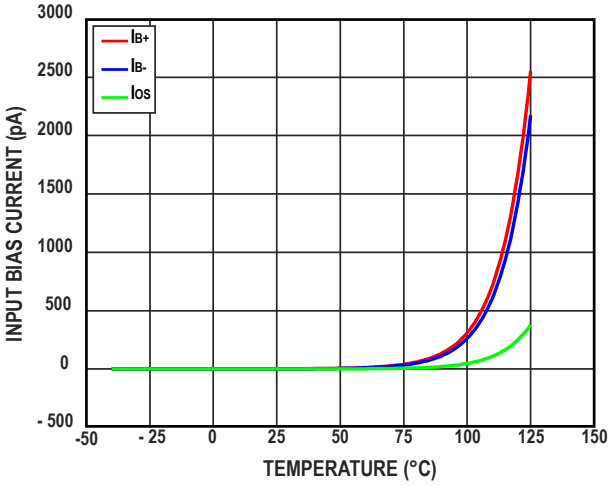

Figure 12. Input Bias Current vs. Temperature

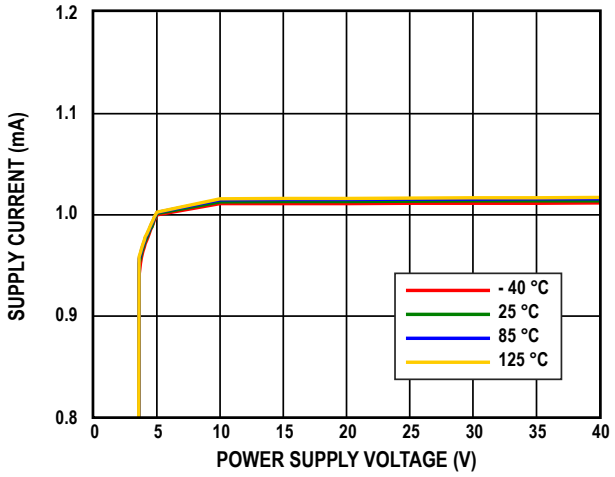

Figure 13. Supply Current per Amplifier vs. Power Supply Voltage

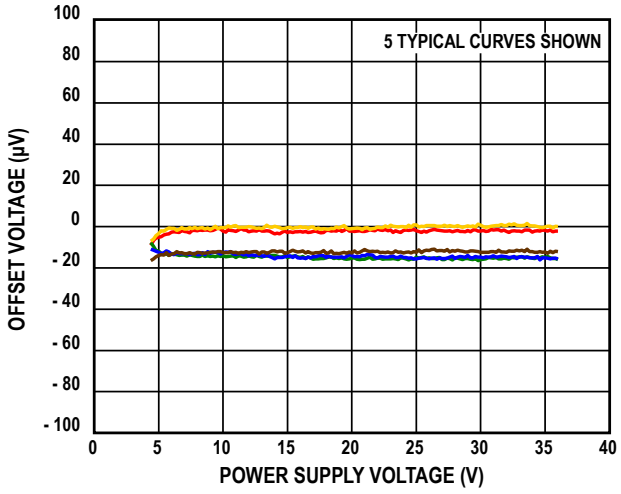

Figure 14. Input Offset Voltage vs. Power Supply Voltage

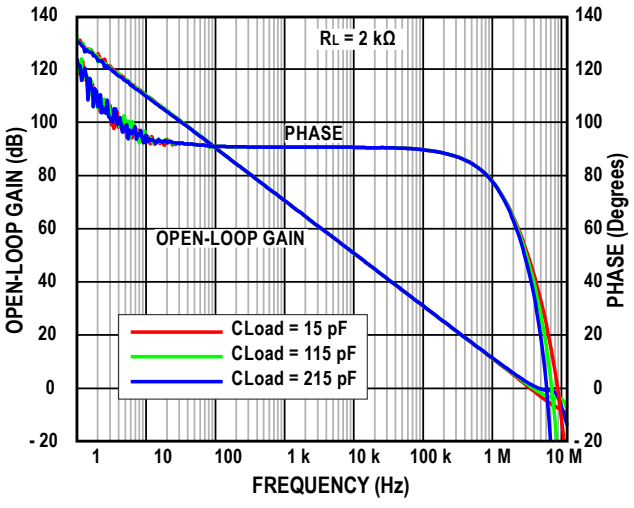

Figure 15. Open-Loop Gain and Phase vs. Frequency

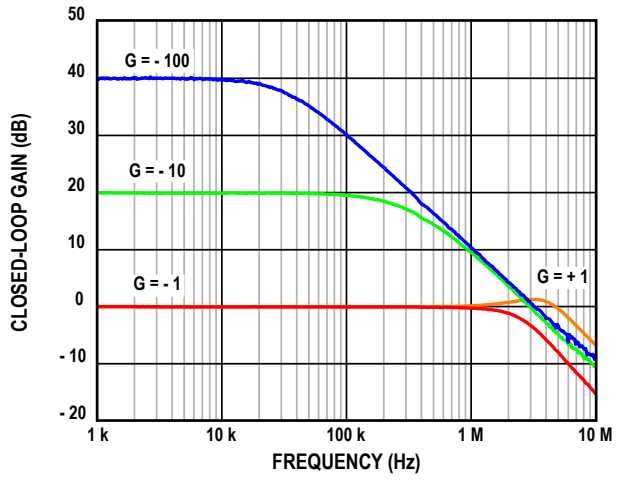

Figure 16. Closed-Loop Gain vs. Frequency

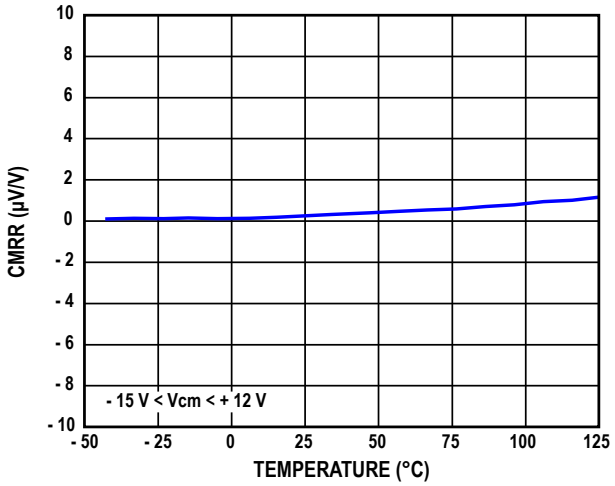

Figure 17. Common Mode Rejection Ratio (CMRR) vs. Temperature

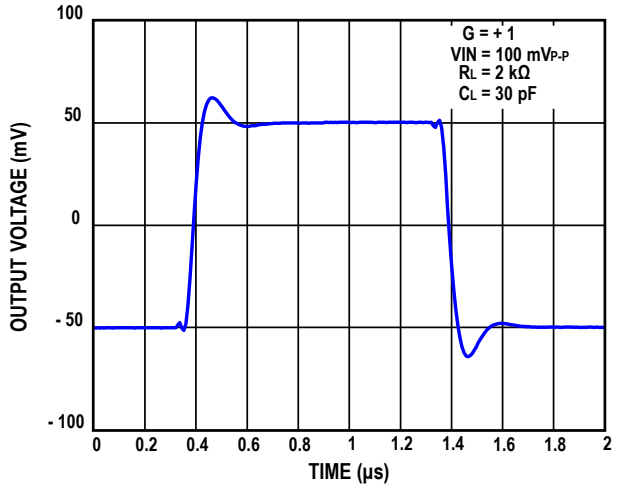

Figure 18. Small Signal Transient Response

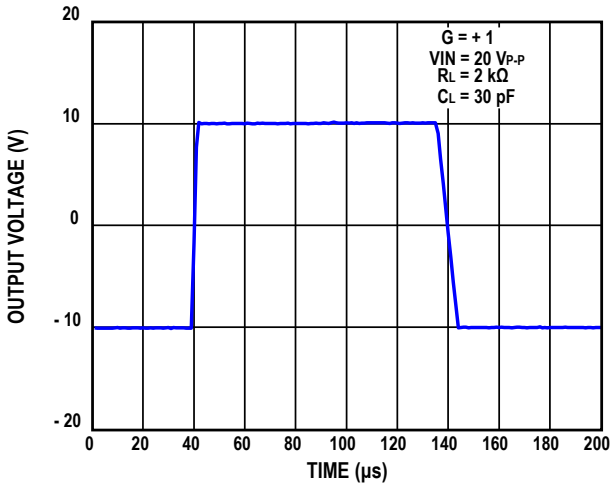

Figure 19. Large Signal Transient Response

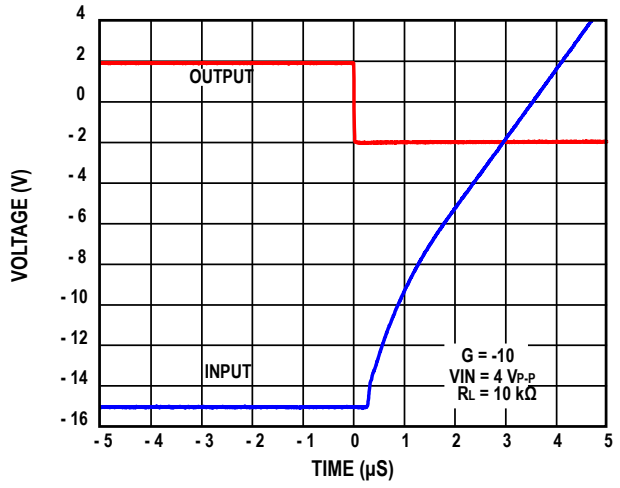

Figure 20. Positive Overload Recovery

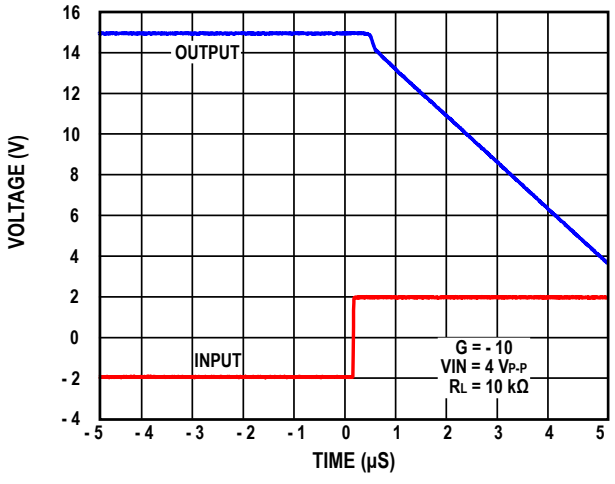

Figure 21. Negative Overload Recovery

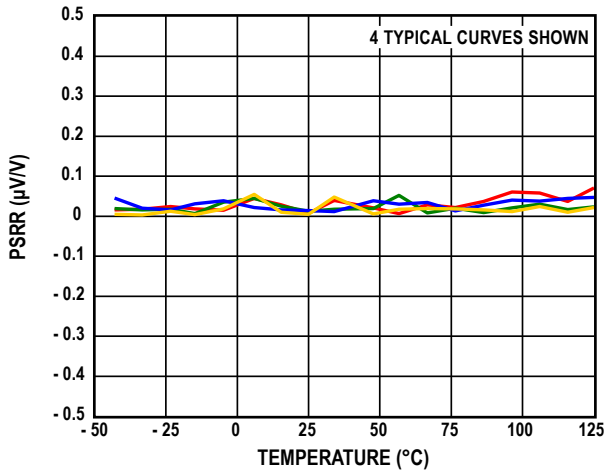

Figure 22. Power Supply Rejection Ratio (PSRR) vs. Temperature

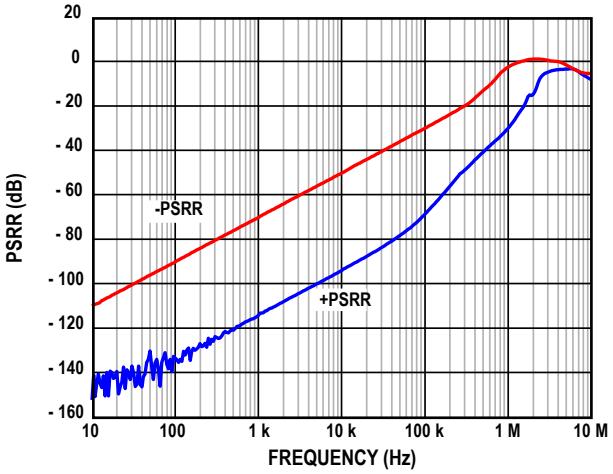

Figure 23. Power Supply Rejection Ratio (PSRR) vs. Frequency

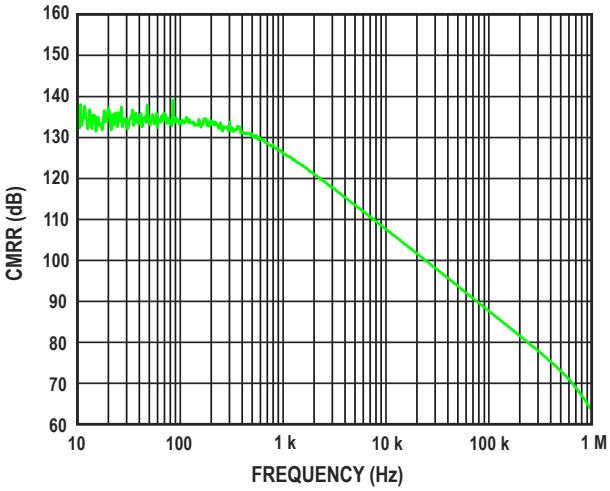

Figure 24. Common Mode Rejection Ratio (CMRR) vs. Frequency

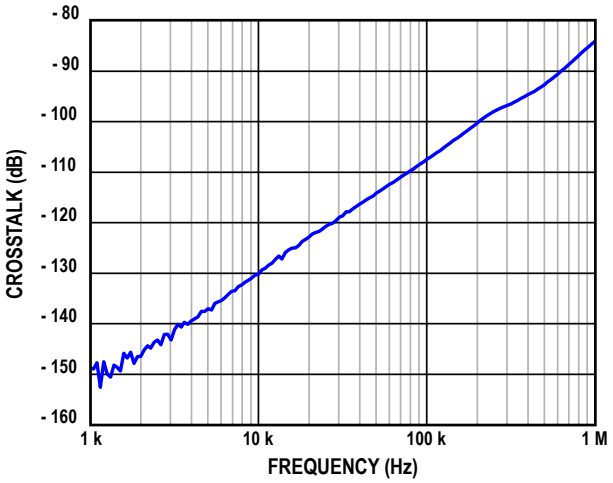

Figure 25. Channel Separation vs. Frequency

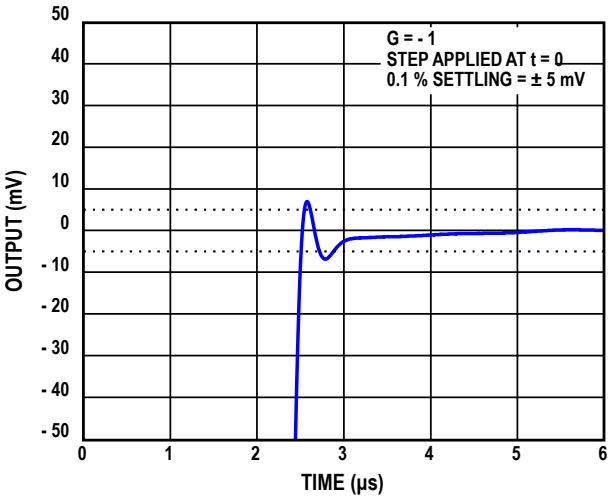

Figure 26. Positive Settling Time to 0.1%

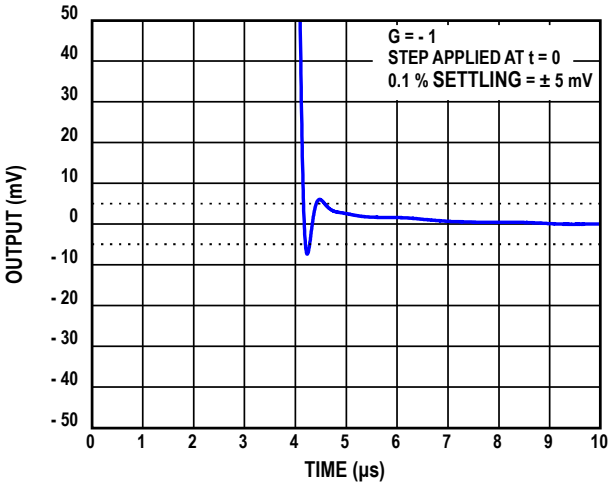

Figure 27. Negative Settling Time to 0.1%

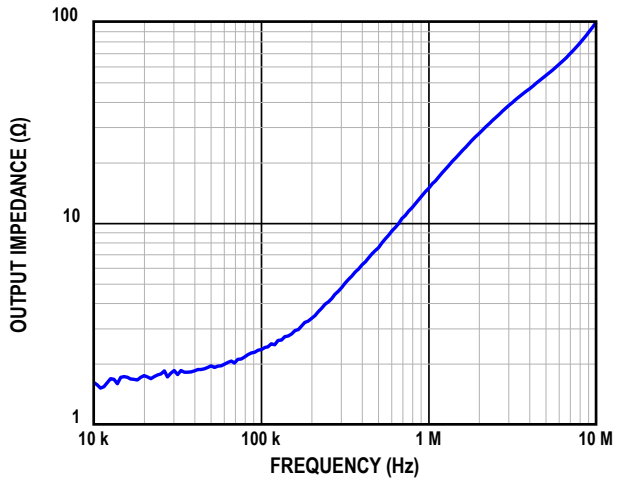

Figure 28. Output Impedance vs. Frequency

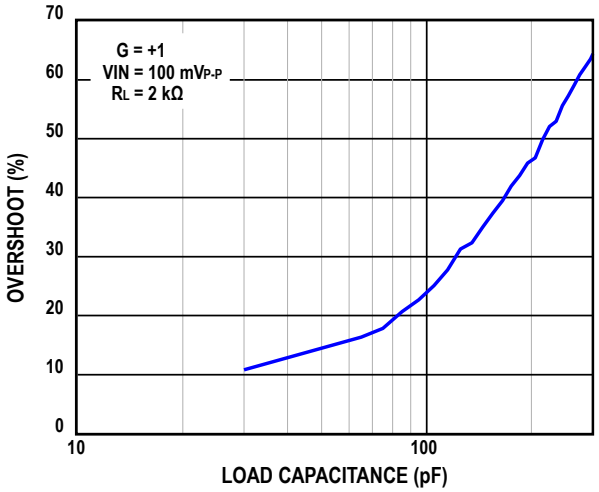

Figure 29. Small Signal Overshoot vs. Load Capacitance

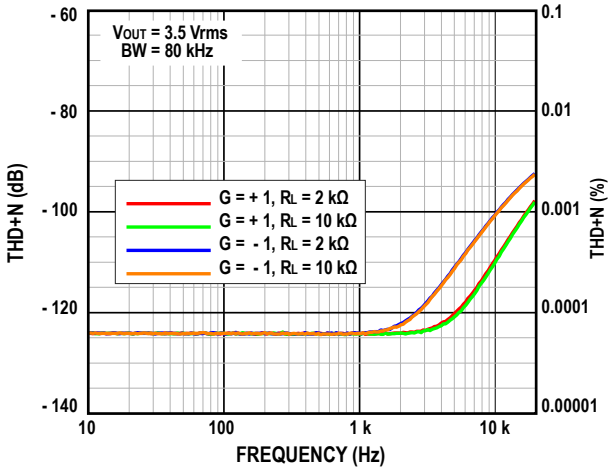

Figure 30. THD+N vs. Frequency

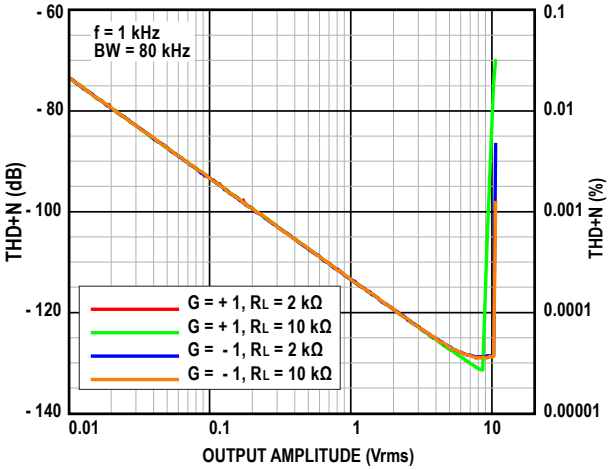

Figure 31. THD+N vs Amplitude

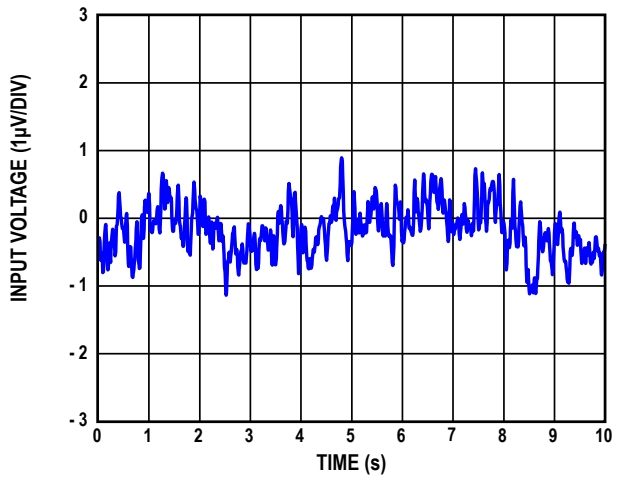

Figure 32. 0.1 Hz to 10 Hz Noise

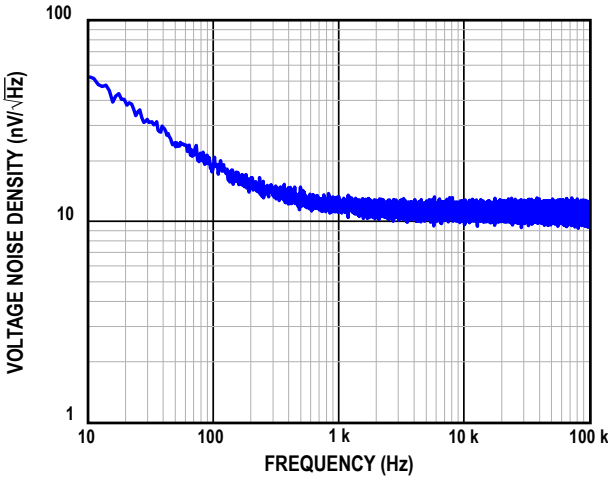

Figure 33. Voltage Noise Density vs. Frequency

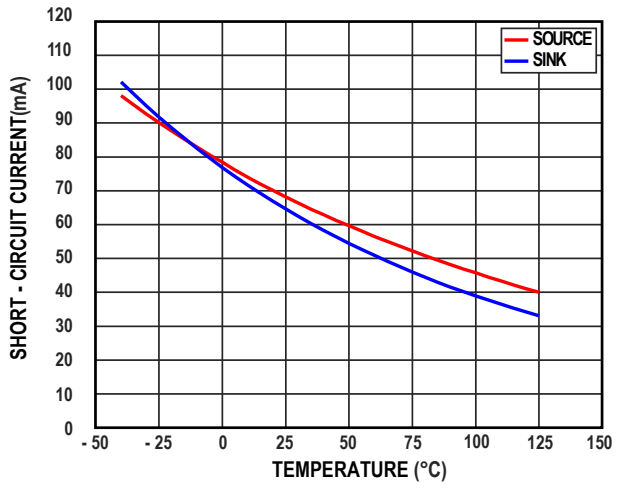

Figure 34. Output Short-Circuit Current vs. Temperature

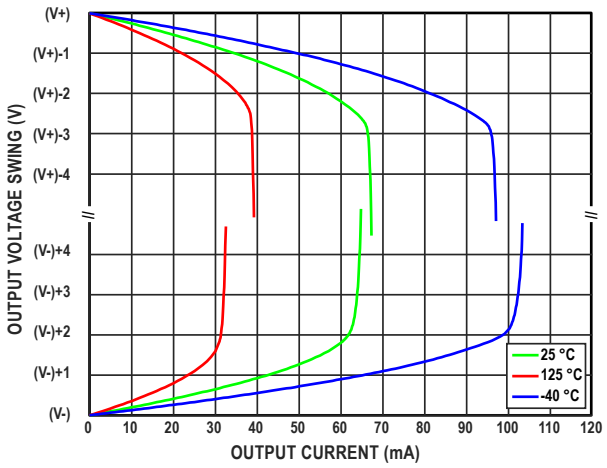

Figure 35. Output Voltage Swing vs. Output Current

Theory of Operation

Post-package Trimming

The ZJA3001 precision operational amplifier boasts a carefully designed MOS input stage, enabling it to maintain an exceptionally low input current of 25 pA maximum at 25 °C. Taking precision to the next level, the ZJA3001 employs ZJW's proprietary post-package trimming technology ZHIJINGTRIM®. This innovative approach involves fine-tuning adjustments (as shown in Figure 36), offering distinct advantages over traditional laser trimming techniques used at the wafer test stage. This post-package trimming method not only minimizes inherent process variations introduced during wafer manufacturing, but also significantly reduces additional defects potentially generated during the plastic molding process. Ultimately, the trimming results in the ZJA3001's exceptional performance: ultra-low offset voltage (35 µV maximum at 25 °C) and ultra-low offset voltage drift (0.5 µV/°C maximum across the specified temperature range in SOIC-8 package). Furthermore, ZJA3001 delivers consistent high accuracy cross wide supply voltage range from 4.5 V to 36 V. These remarkable characteristics make the ZJA3001 the ideal choice for demanding applications, such as high-impedance sensors interface, precision filtering and high-voltage high-precision data acquisition.

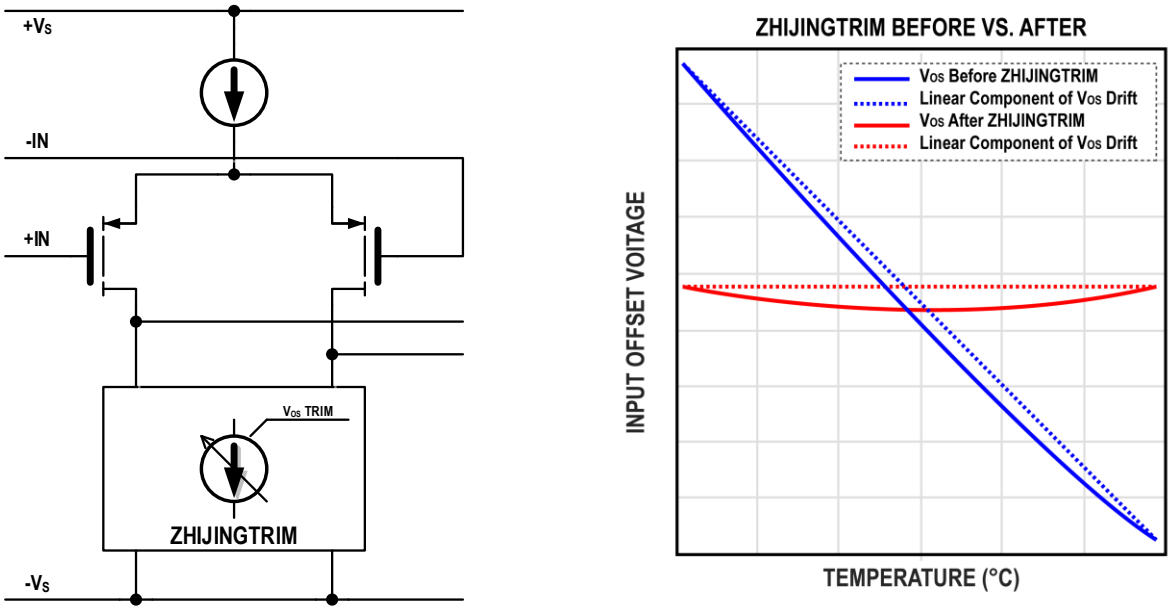

Figure 36. Diagram of Post-package Trimming Scheme (Left) and Effect (Right)

Applications Information

Source Impedance, Input Bias Current Affect both Output Noise and System Offset Voltage

As shown in Figure 37, the output noise density of classic bipolar input stage amplifiers #1, #2, and ZJA3001 is depicted at the 1 kHz frequency point under various source impedances. Bipolar amplifiers typically have large input bias current, leading to significant input current noise. When the source impedance exceeds 100 kΩ, the system noise rapidly increases. In contrast, the ZJA3001 has exceptionally low input bias current, resulting in minimal input noise current, thus its noise contribution to the system is negligible. When the source impedance surpasses 10 kΩ, the system noise is mainly contributed by the source impedance, which appears in the graph as a straight line overlapping the black line representing the noise contributed by source impedance. Similarly, high source impedance can cause considerable system offset voltage and its temperature drift due to the amplifier's input bias current, input offset current, and their temperature drifts. These effects are common in bipolar input amplifiers and zero-drift amplifiers. The ZJA3001, however, leverages its exceptional low input current to fully guarantee low system offset voltage and its temperature drift.

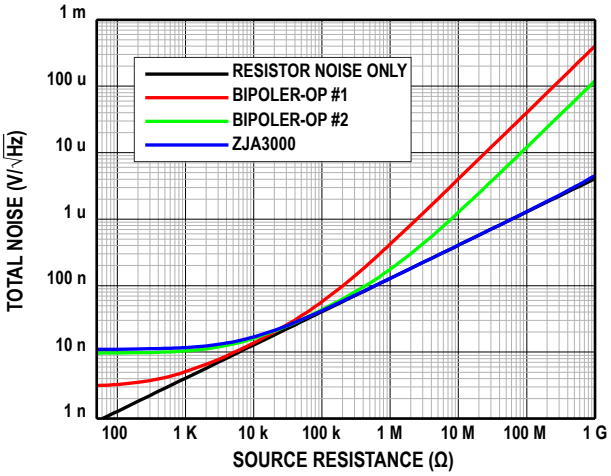

Figure 37. System Total Noise vs. Source Impedance

Input Common Mode Voltage Range

While traditional bipolar amplifiers demand 1 V to 2 V of headroom from both supply rails for proper input common-mode voltage operation, often necessitating dual-supply configurations for applications with 0 V input common-mode signals. ZJA3001, in order to be compatible with it, also has the same input range. However, ZJA3001 has the ability to output to the rails, which can meet the needs of applications with a wider output range.

Exceptional Linearity

Harnessing a proprietary linearity optimization design, the ZJA3001 achieves exceptional THD+N performance—reaching a remarkable minimum of -130 dB across the entire audio range and output amplitude, as shown in Figure 30 and Figure 31. This remarkable feat is made possible by its ultra-high open-loop gain, excellent frequency response, and extremely low noise characteristics.

Output Phase Reversal

Phase reversal is defined as a change of polarity in the amplifier transfer function. Many operational amplifiers exhibit phase reversal

when the voltage applied to the input is greater than the maximum common-mode voltage. In some instances, this can cause permanent damage to the amplifier. In feedback loops, it can result in system lockups or equipment damage. The ZJA3001 is immune to phase reversal problems even at input voltages beyond the supplies.

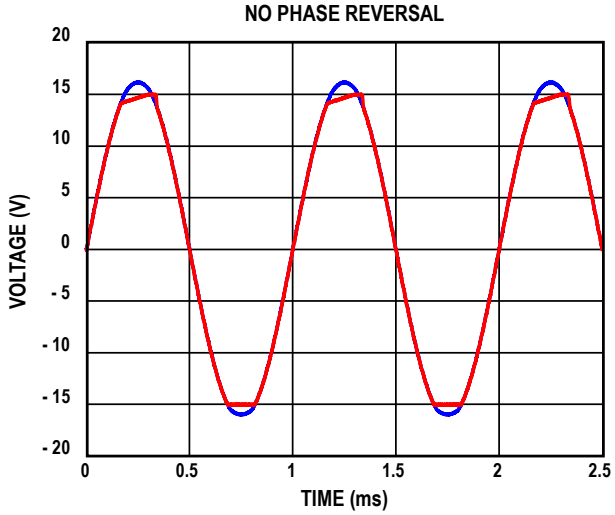

Figure 38. ZJA3001 Has No Output Phase Reversal

Overload Recovery Time

Many zero-drift amplifiers, whether auto-zero or chopping, are plagued by a long overload recovery time, often in ms, due to the complicated settling behavior of the internal nulling loops after saturation of the outputs. Recovery time is important in many applications, particularly where the operational amplifier must amplify small signals in the presence of large transient voltages. The ZJA3001, as a continuous signal processing amplifier, stands out in this regard. Compared to zero-drift amplifiers, its overload recovery time is significantly shorter, falling within a remarkable 7 μs, as demonstrably shown in the table below.

Model	Positive Overload Recovery (μs)	Negative Overload Recovery (μs)
ZJA3001	3.5	6.5
Competitor A	12.3	18

Over Temperature Protection

Due to its high operating voltage (up to 36 V) and short-circuit current (up to 67 mA), the ZJA3001 can dissipate up to 2 W to 3 W of power during use. As thermal resistance for various package formats typically exceeds 100 °C/W, self-heating and the risk of permanent damage from high temperatures are concerns in real-world applications. To address this, the ZJA3001 incorporates an automatic over-temperature protection (OTP) function. When the chip temperature reaches 150 °C, OTP triggers, putting the chip into shutdown mode. Both input and output terminals enter a high-impedance state, significantly reducing power consumption and facilitating temperature drop. Once the chip cools down to 130 °C, OTP disengages, and the chip resumes normal operation.

Input Bias Current Return Path

As shown in Figure 39, a simple AC coupling can be achieved by connecting a capacitor (C_{IN}) in series between the non-inverting input (+) of the operational amplifier and the actual input (VIN) to isolate the DC voltage component of the input voltage. This coupling method is especially common in high-gain applications: when the gain is high, even a small DC voltage component at the amplifier input can affect the available output dynamic range of the op amp, and may even cause output saturation. However, for this AC coupling method located at the high-impedance input, if the input current of the positive input is not provided with a proper bias current return path, it will cause serious bias problems: in fact, the input bias current will slowly charge /discharge the capacitor C_{IN}, depending on the polarity of the input bias current, the capacitor will charge to the positive supply voltage or discharge to the negative supply voltage. This bias current caused offset voltage will be amplified by the op amp's closed-loop DC gain until the op amp's input voltage exceeds its input voltage range or the amplified output voltage exceeds its output voltage range, and this process may take a long time. For example, for an operational amplifier with an FET input stage, if its input current is 1 pA, through a 0.1 μF capacitor, the offset voltage will be ramped at the speed of:

$$10\ pA/0.1\ \mu F = 10\ \mu V/s = 0.6\ mV/min = 36\ mV/h$$

When the closed-loop DC gain is 100, the output voltage ramp rate is 3.6 V/h. Therefore, the actual circuit will not show obvious failure until after several hours. Using an AC coupled oscilloscope for a short-term test may not be able to find this problem.

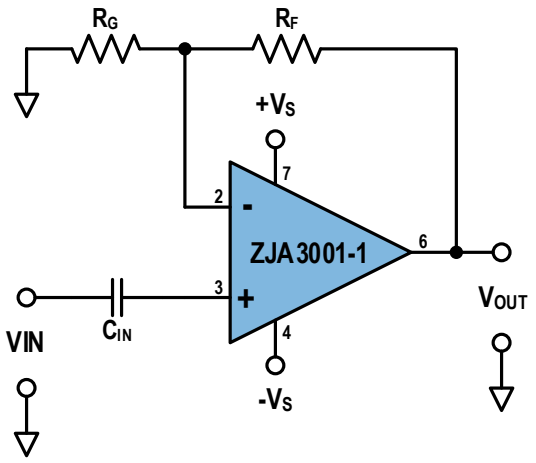

Figure 39. Incorrect AC-Coupled Op Amp Circuit

One simple solution is shown in Figure 40. A resistor (R_{IN}) is connected between the input of the operational amplifier and ground, providing an input bias current return path. Unlike operational amplifiers with FET inputs, traditional bipolar operational amplifiers need to set R_{IN} to the parallel value of R_G and R_F to minimize the input offset voltage caused by input bias current, considering the mis-matching between the two inputs of the op amp. Since this resistor will introduce additional noise to the overall circuit, the value of the input coupling capacitor and the resistor should be balanced between non-ideal factors such as input impedance, input high-pass cutoff frequency, and input offset voltage according to actual needs. Typical resistor value is generally between 100 kΩ and 1 MΩ.

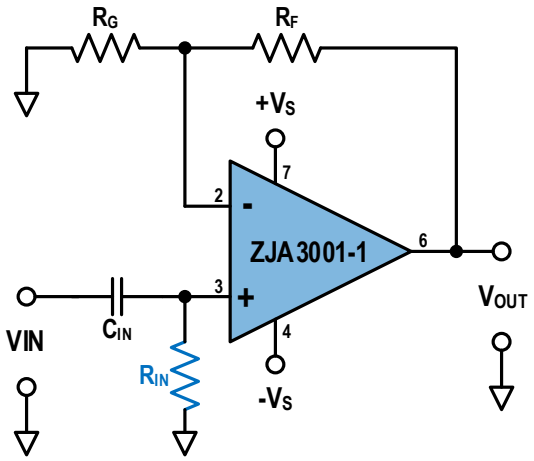

Figure 40. Creating an Input Bias Current Return Path

Applications and Implementation

Bandpass KRC Filter

The ZJA3001 series of amplifiers are particularly suitable for use in the design of precision filters, such as the typical KRC filter, as shown in Figure 41. With their excellent low offset and high CMRR performance, precision filters using ZJA3001 can guarantee stable performance over a wide input range while also having sufficient output dynamic range even at high gain. On the other hand, due to the ZJA3001-2/ZJA3001-4's ultra-high channel separation, even using the dual amplifiers in the same ZJA3001-2 can achieve excellent filter design without worrying about performance degradation caused by channel crosstalk.

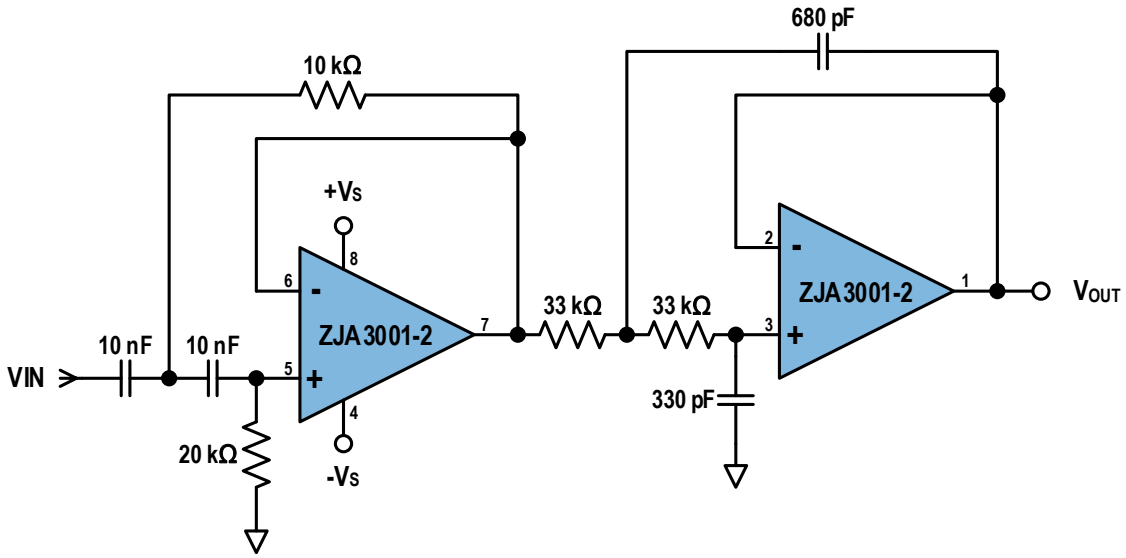

Figure 41. Using ZJA3001-2 to Build a 2-stage Band-pass KRC Filter

Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 46,Figure 47,Figure 48 and Figure 49, keeping R_F, R_G and C_F close to the inverting input minimizes parasitic capacitance.
  - Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85 °C for 30 minutes is sufficient for most circumstances.

Layout Example

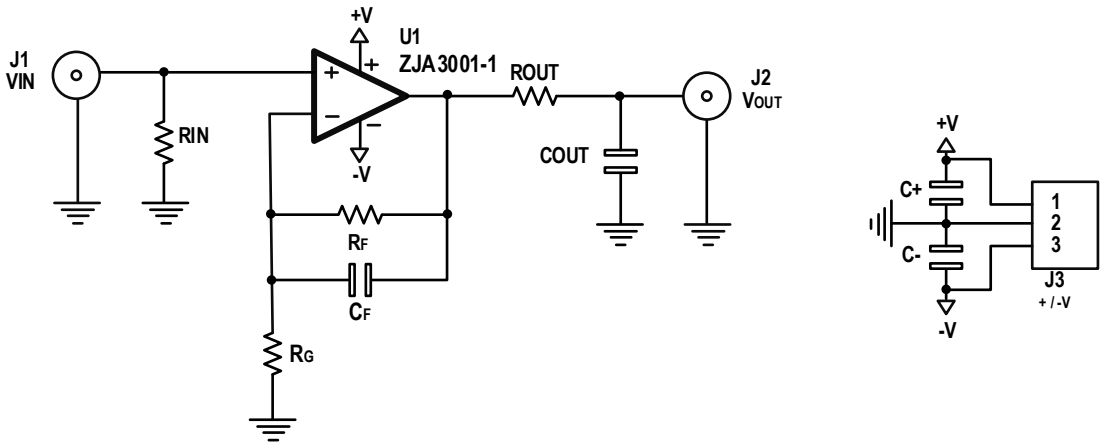

Figure 42. Op Amp Schematic for Non-inverting Configuration

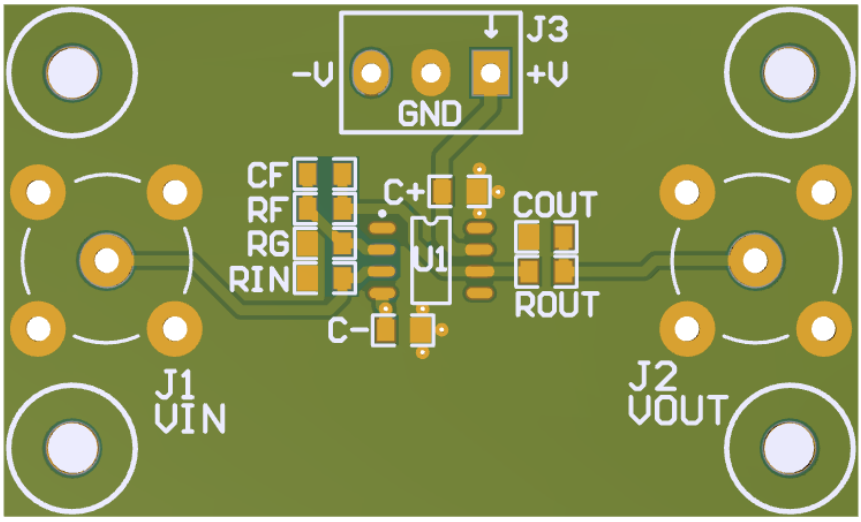

Figure 43. Layout of Op Amplifier in Non-Inverting Configuration (Silkscreen Layer)

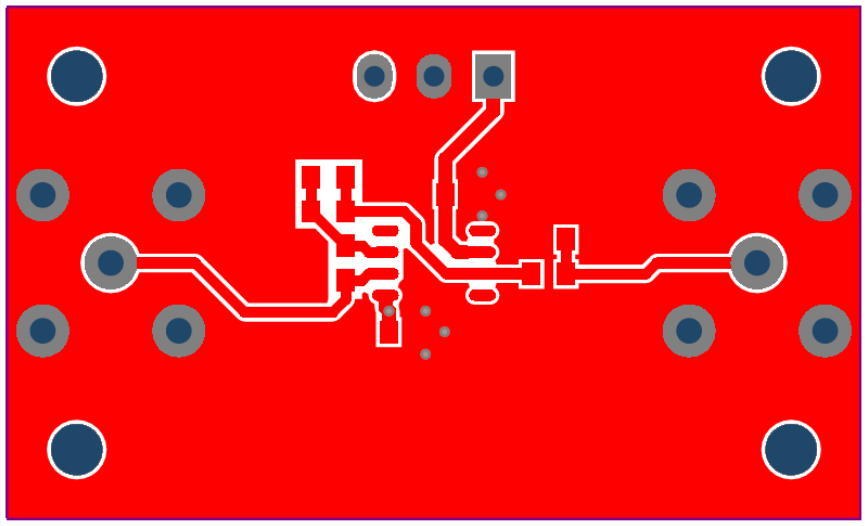

Figure 44. Layout of Op Amplifier in Non-inverting Configuration (Top Layer)

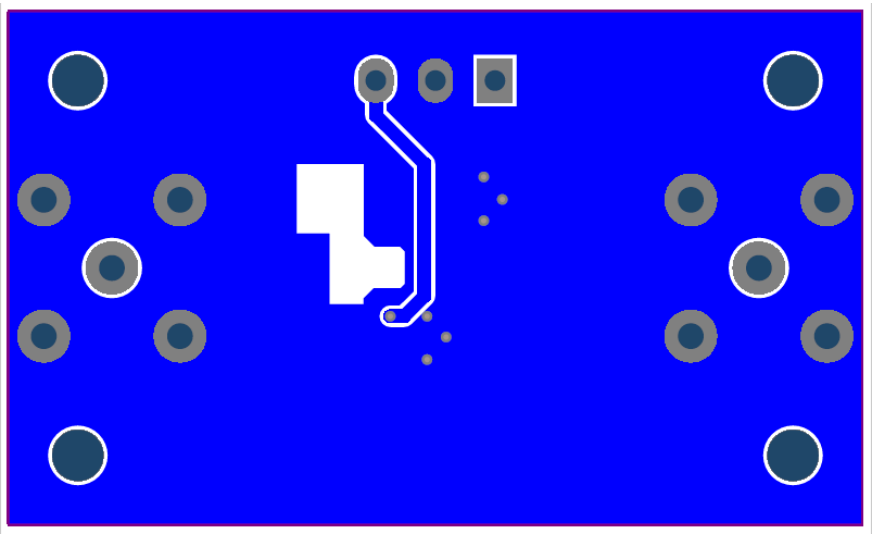

Figure 45. Layout of Op Amplifier in Non-inverting Configuration (Bottom Layer)

Outline Dimensions

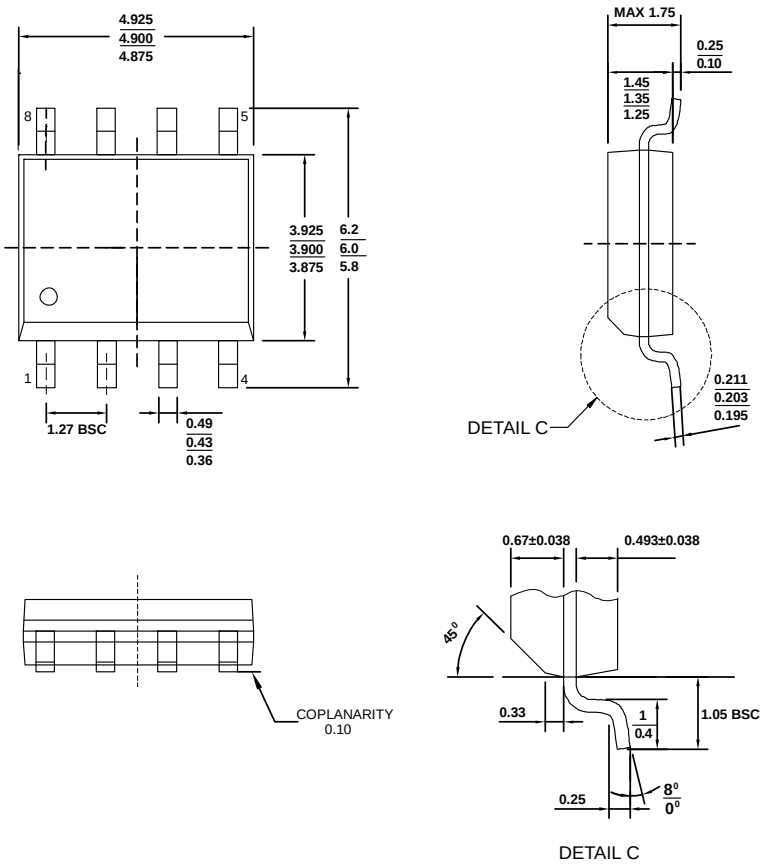

Figure 46. 8-Lead SOIC Package Dimensions shown in millimeters

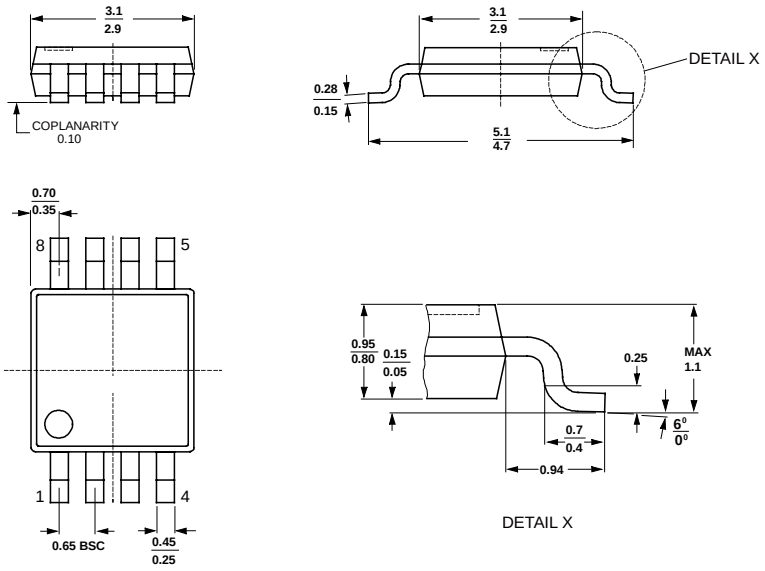

Figure 47. 8-Lead MSOP Package Dimensions shown in millimeters

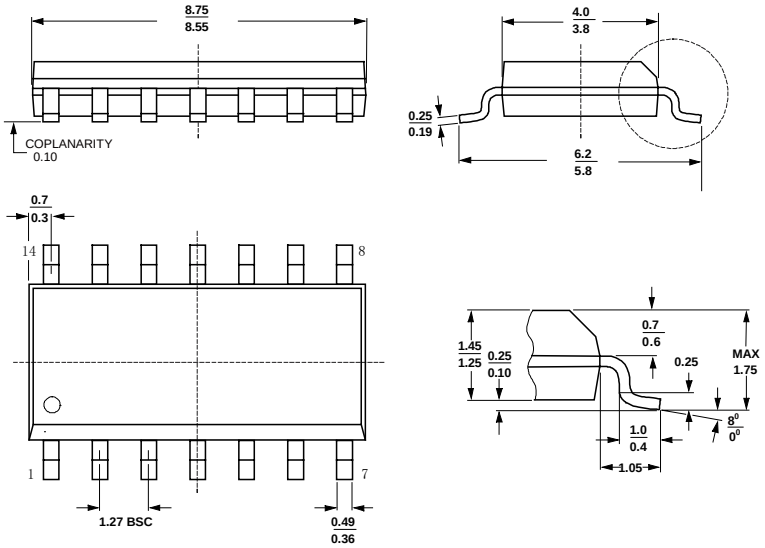

Figure 48. 14-Lead SOIC Package Dimensions shown in millimeters

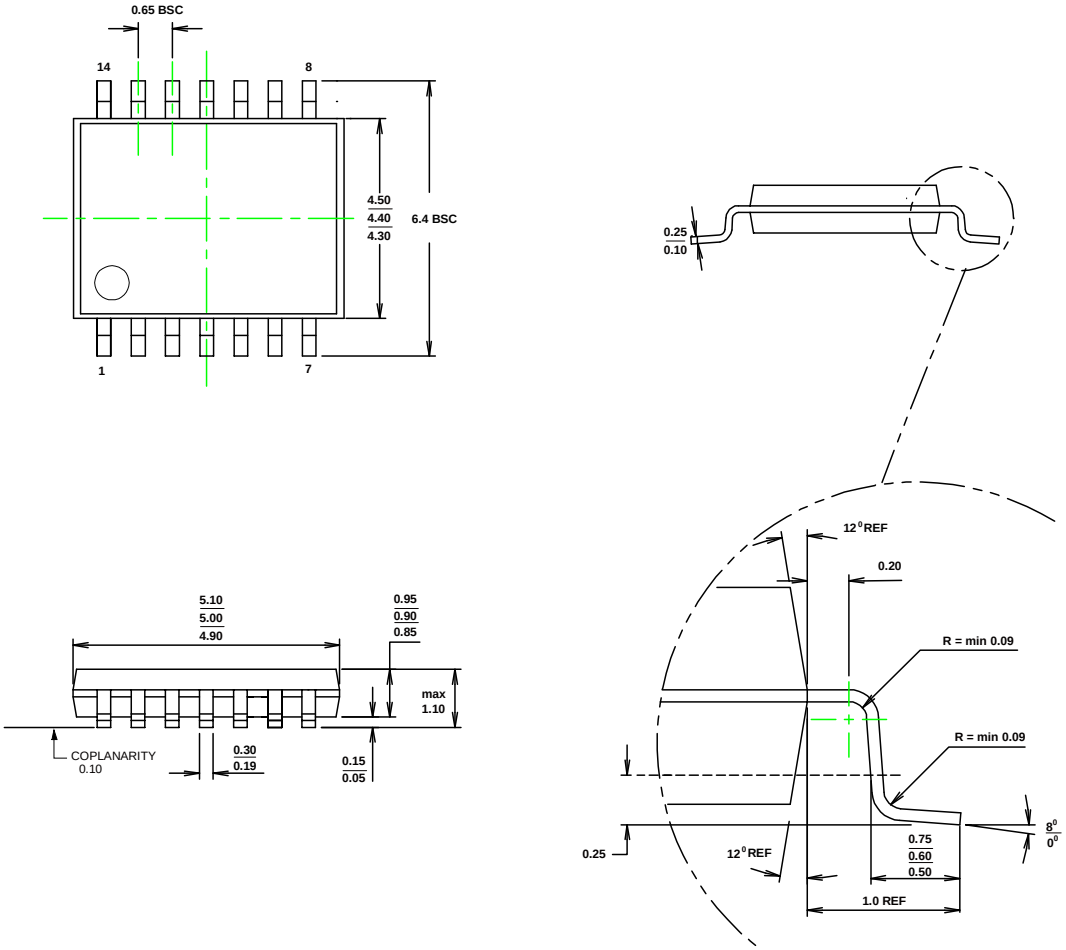

Figure 49. 14-Lead TSSOP Package Dimensions shown in millimeters

Ordering Guide

Model	Package	Orderable Device	Maximum V_{OS} & TCV_{OS}	Temperature Range (°C)	External Package
ZJA3001-1	SOIC-8	ZJA3001-1BSABT	35 μV & 0.5 μV/°C	- 40 to 125	Tube
	SOIC-8	ZJA3001-1BSABR	35 μV & 0.5 μV/°C	- 40 to 125	13” reel
	SOIC-8	ZJA3001-1ASABT	35 μV& 1.0 μV/°C	- 40 to 125	Tube
	SOIC-8	ZJA3001-1ASABR	35 μV& 1.0 μV/°C	- 40 to 125	13” reel
	MSOP-8	ZJA3001-1BUABT	55 μV & 0.8 μV/°C	- 40 to 125	Tube
	MSOP-8	ZJA3001-1BUABR	55 μV & 0.8 μV/°C	- 40 to 125	13” reel
	MSOP-8	ZJA3001-1AUABT	55 μV & 1.5 μV/°C	- 40 to 125	Tube
	MSOP-8	ZJA3001-1AUABR	55 μV & 1.5 μV/°C	- 40 to 125	13” reel
ZJA3001-2	SOIC-8	ZJA3001-2BSABT	35 μV & 0.5 μV/°C	- 40 to 125	Tube
	SOIC-8	ZJA3001-2BSABR	35 μV & 0.5 μV/°C	- 40 to 125	13” reel
	SOIC-8	ZJA3001-2ASABT	35 μV & 1.0 μV/°C	- 40 to 125	Tube
	SOIC-8	ZJA3001-2ASABR	35 μV & 1.0 μV/°C	- 40 to 125	13” reel
	MSOP-8	ZJA3001-2BUABT	55 μV & 0.8 μV/°C	- 40 to 125	Tube
	MSOP-8	ZJA3001-2BUABR	55 μV & 0.8 μV/°C	- 40 to 125	13” reel
	MSOP-8	ZJA3001-2AUABT	55 μV & 1.5 μV/°C	- 40 to 125	Tube
	MSOP-8	ZJA3001-2AUABR	55 μV & 1.5 μV/°C	- 40 to 125	13” reel
ZJA3001-4	SOIC-14	ZJA3001-4BSDBT	35 μV & 0.5 μV/°C	- 40 to 125	Tube
	SOIC-14	ZJA3001-4BSDBR	35 μV & 0.5 μV/°C	- 40 to 125	13” reel
	SOIC-14	ZJA3001-4ASDBT	35 μV & 1.0 μV/°C	- 40 to 125	Tube
	SOIC-14	ZJA3001-4ASDBR	35 μV & 1.0 μV/°C	- 40 to 125	13” reel
	TSSOP-14	ZJA3001-4BUDBT	55 μV & 0.8 μV/°C	- 40 to 125	Tube
	TSSOP-14	ZJA3001-4BUDBR	55 μV & 0.8 μV/°C	- 40 to 125	13” reel
	TSSOP-14	ZJA3001-4AUDBT	55 μV & 1.5 μV/°C	- 40 to 125	Tube
	TSSOP-14	ZJA3001-4AUDBR	55 μV & 1.5 μV/°C	- 40 to 125	13” reel

Orderable Device Explanation

ZJXXXXX X X X X X Q1

- Q1: Automotive Grade
- External Package: T = tube; R = reel
- Temperature range: A = -40 °C to 125 °C Automotive Grade 1; B = -40 °C to 125 °C; E = -40 °C to 85 °C
- Number of Pins: T = 6, A = 8; B = 10; D = 14; E = 16; P = 20;
- Package type: S = SOIC; U = MSOP, TSSOP, SOT; T = DFN, QFN
- Grade: B grade is better than A grade
- Base: R = Voltage reference; A = Amplifier; C = Data Converter; G = Switches and Multiplexers

Related Parts

Part Number	Description	Comments
ADC		
ZJC2000/2010	18-bit 400 kSPS/200 kSPS SAR ADC	Fully differential input, SINAD 99.3 dB, THD -113 dB
ZJC2001/2011	16-bit 500 kSPS/250 kSPS SAR ADC	Fully differential input, SINAD 95.3 dB, THD -113 dB
ZJC2002/2012 ZJC2003/2013	16-bit 500 kSPS/250 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 91.7 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 91.7 dB, THD -105 dB
ZJC2004/2014 ZJC2005/2015	18-bit 400 kSPS/200 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 94.2 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 94.2 dB, THD -105 dB
ZJC2007/2017 ZJC2008/2018	14-bit 600 kSPS/300 kSPS SAR ADC	Pseudo-differential unipolar input, SINAD 85 dB, THD -105 dB Pseudo-differential bipolar input, SINAD 85 dB, THD -105 dB
ZJC2100/1-18 ZJC2100/1-16	18-bit 400 kSPS/200 kSPS 4-ch differential SAR ADC, SINAD 99.3 dB, THD -113 dB 16-bit 500 kSPS/250 kSPS 4-ch differential SAR ADC, SINAD 95.3 dB, THD -113 dB	
ZJC2102/3-18 ZJC2102/3-16 ZJC2102/3-14	18-bit 400 kSPS/200 kSPS 8-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 8-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB 14-bit 600 kSPS/300 kSPS 8-ch pseudo-differential SAR ADC, SINAD 85 dB, THD -105 dB	
ZJC2104/5-18 ZJC2104/5-16	18-bit 400 kSPS/200 kSPS 4-ch pseudo-differential SAR ADC, SINAD 94.2 dB, THD -105 dB 16-bit 500 kSPS/250 kSPS 4-ch pseudo-differential SAR ADC, SINAD 91.7 dB, THD -105 dB	
DAC		
ZJC2541-18/16/14 ZJC2543-18/16/14	18/16/14-bit 1 MSPS single channel DAC with unipolar output	Power on reset to 0 V (ZJC2541) or V_{REF}/2 (ZJC2543), 1 nV-S glitch, SOIC-8/MSOP-10/DFN-10 packages
ZJC2542-18/16/14 ZJC2544-18/16/14	18/16/14-bit 1 MSPS single channel DAC with bipolar output	Power on reset to 0 V (ZJC2542) or V_{REF}/2 (ZJC2544), 1 nV-S glitch, SOIC-14/TSSOP-16/QFN-16 packages
Amplifier		
ZJA3000-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz GBW, 35 µV max Vos, 0.5 µV/°C max Vos drift, 25 pA max Ibias, 1 mA/Amplifier, input to V-, RRO, 4.5 V to 36 V
ZJA3001-1/2/4	Single/Dual/Quad 36 V low bias current precision Op Amps	3 MHz GBW, 35 µV max Vos, 0.5 µV/°C max Vos drift, 25 pA max Ibias, 1 mA/Amplifier, RRO, 4.5 V to 36 V
ZJA3512-2/4	Dual/Quad 36 V 7 MHz precision JFET Op Amps	7 MHz GBW, 35 V/µS SR, 50 µV max Vos, 1 µV/°C max Vos drift, 2 mA/Amplifier, RRO, 4.5 V to 35 V
ZJA3600/1	36 V ultra-high precision in-amp	CMRR 105 dB min (G = 1), 25 pA max Ibias, 25 µV max Vosi, gain error 0.001% max (G = 1), 625 kHz BW (G = 10), 3.3 mA/Amplifier, ±2.4 V to ±18 V, - 40 °C to 125 °C specified
ZJA3622/8	36 V low cost precision in-amp	CMRR 93 dB min (G = 10), 0.5 nA max Ibias, 125 µV max Vosi, 625 kHz BW (G = 10), 3.3 mA/Amplifier, ±2.4 V to ±18 V
ZJA3611, ZJA3609	36 V ultra-high precision wider bandwidth precision in-amp (min gain of 10)	CMRR 120 dB min (G = 10), 25 pA max Ibias, 25 µV max Vosi, 1.2 MHz BW (G = 10), 3.3 mA/Amplifier, ±2.4 V to ±18 V, - 40 °C to 125 °C specified
ZJA3676/7	Low power, G = 1 Single/Dual 36 V difference amplifier	Input protection to ±65 V, CMRR 104 dB min, Vos 100 µV max, gain error 15 ppm max, 500 kHz BW, 330 µA, 2.7 V to 36 V
Voltage Reference		
ZJR1000	15 V supply precision voltage reference	V_{OUT} = 1.25/2.048/2.5/3/4.096/5 V, 5 ppm/°C max drift - 40 °C to 125 °C, ±0.05% initial error
ZJR1001 ZJR1002 ZJR1003	5.5 V low power voltage reference (ZJR1001 with noise filter option)	V_{OUT} = 2.5/3/4.096/5 V, 5 ppm/°C max drift - 40 °C to 125 °C, ±0.05% initial error, 130 µA, ZJR1001/2 in SOT23-6, ZJR1003 in SOIC/MS-8
Switches and Multiplexers		
ZJG4438/4439	36 V fault protection 8:1/dual 4:1 multiplexer	Protection to ±50 V power on & off, latch-up immune, Ron 270 Ω,14.8 pC charge injection, t_{ON} 166 nS, 10 V to 36 V