

# C2M0045170P

Silicon Carbide Power MOSFET  
C2M™ MOSFET Technology  
N-Channel Enhancement Mode

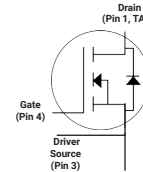


TO-247-4L Plus



## Features

- 2<sup>nd</sup> generation SiC MOSFET technology
- Optimized package with separate driver source pin
- 8mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High speed switching with low capacitances
- Resistant to latch-up
- Halogen free, RoHS compliant



Package Types: TO-247-4L Plus  
PN's: C2M0045170P

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## Applications

- Solar inverters
- Switch mode power supplies
- High voltage DC/DC converters
- Motor drive
- Pulsed power applications

## Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency

## Maximum Ratings ( $T_c = 25\text{ }^\circ\text{C}$ Unless Otherwise Specified)

Parameter	Symbol	Value	Unit	Test Conditions	Note
Drain - Source Voltage	$V_{DSmax}$	1700	V	$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	
Gate - Source Voltage	$V_{GSmax}$	-10/+25		Absolute Maximum Values, AC ( $f > 1\text{ Hz}$ )	Note: 1
Gate - Source Voltage	$V_{GSop}$	-5/+20		Recommended Operational Values	Note: 2
Continuous Drain Current	$I_D$	75	A	$V_{GS} = 20\text{ V}, T_c = 25\text{ }^\circ\text{C}$	Fig. 19
		48		$V_{GS} = 20\text{ V}, T_c = 100\text{ }^\circ\text{C}$	
Pulsed Drain Current	$I_{D(pulse)}$	160		Pulse Width $t_p$ Limited by $T_{jmax}$	Fig. 22
Power Dissipation	$P_D$	338	W	$T_c = 25\text{ }^\circ\text{C}, T_J = 150\text{ }^\circ\text{C}$	Fig. 20
Operating Junction and Storage Temperature	$T_J, T_{stg}$	-40 to +150	$^\circ\text{C}$		
Solder Temperature	$T_L$	260	$^\circ\text{C}$	According to JEDEC J-STD-020	

Note (1): When using MOSFET body diode  $V_{GSmax} = -5\text{ V}/+25\text{ V}$ .

Note (2): MOSFET can also safely operate at  $0/+20\text{ V}$ .


**Electrical Characteristics** ( $T_C = 25\text{ }^\circ\text{C}$  Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1700				$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	
Gate Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4	V	$V_{DS} = V_{GS}, I_D = 18\text{ mA}$	Fig. 11
			2.5			$V_{DS} = V_{GS}, I_D = 18\text{ mA}, T_J = 150\text{ }^\circ\text{C}$	
Zero Gate Voltage Drain Current	$I_{DSS}$		2	100	$\mu\text{A}$	$V_{DS} = 1700\text{ V}, V_{GS} = 0\text{ V}$	
Gate-Source Leakage Current	$I_{GSS}$			600	nA	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	
Drain-Source On-State Resistance	$R_{DS(on)}$		40	70	m $\Omega$	$V_{GS} = 20\text{ V}, I_D = 50\text{ A}$	Fig. 4,5,6
			80			$V_{GS} = 20\text{ V}, I_D = 50\text{ A}, T_J = 150\text{ }^\circ\text{C}$	
Transconductance	$g_{fs}$		24.7		S	$V_{DS} = 20\text{ V}, I_{DS} = 50\text{ A}$	Fig. 7
			23.4			$V_{DS} = 20\text{ V}, I_{DS} = 50\text{ A}, T_J = 150\text{ }^\circ\text{C}$	
Input Capacitance	$C_{iss}$		3455		pF	$V_{GS} = 0\text{ V}$ $V_{DS} = 1200\text{ V}$ $f = 1\text{ MHz}$ $V_{AC} = 25\text{ mV}$	Fig. 17,18
Output Capacitance	$C_{oss}$		171				
Reverse Transfer Capacitance	$C_{riss}$		6.7				
$C_{oss}$ Stored Energy	$E_{oss}$		139		$\mu\text{J}$		Fig. 16
Effective Output Capacitance (Energy Related)	$C_{o(er)}$		188		pF	$V_{GS} = 0\text{ V}, V_{DS} = 0 \dots 1200\text{ V}$	Note: 3
Effective Output Capacitance (Time Related)	$C_{o(tr)}$		255		pF		
Turn-On Switching Energy (SiC Diode FWD)	$E_{ON}$		0.52		mJ	$V_{DS} = 1200\text{ V}, V_{GS} = -5/20\text{ V},$ $I_D = 50\text{ A}, R_{G(ext)} = 2.5\text{ }\Omega, L = 99\text{ }\mu\text{H},$ $T_J = 150\text{ }^\circ\text{C},$ Using SiC Diode as FWD	Fig. 26, 29b Note 2
Turn Off Switching Energy (SiC Diode FWD)	$E_{OFF}$		0.43				
Turn-On Switching Energy (Body Diode FWD)	$E_{ON}$		2.0		mJ	$V_{DS} = 1200\text{ V}, V_{GS} = -5/20\text{ V},$ $I_D = 50\text{ A}, R_{G(ext)} = 2.5\text{ }\Omega, L = 99\text{ }\mu\text{H},$ $T_J = 150\text{ }^\circ\text{C},$ Using MOSFET as FWD	Fig. 26, 29a Note 2
Turn Off Switching Energy (Body Diode FWD)	$E_{OFF}$		0.31				
Turn-On Delay Time	$t_{d(on)}$		15		ns	$V_{DD} = 1200\text{ V}, V_{GS} = -5/20\text{ V}$ $I_D = 50\text{ A},$ $R_{G(ext)} = 2.5\text{ }\Omega,$ Timing Relative to $V_{DS}$ Inductive Load	Fig. 27, 29 Note 2
Rise Time	$t_r$		18				
Turn-Off Delay Time	$t_{d(off)}$		34				
Fall Time	$t_f$		12				
Internal Gate Resistance	$R_{G(int)}$		1.3		$\Omega$	$f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$	
Gate to Source Charge	$Q_{gs}$		46		nC	$V_{DS} = 1200\text{ V}, V_{GS} = -5/20\text{ V}$ $I_D = 50\text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	$Q_{gd}$		71				
Total Gate Charge	$Q_g$		204				

Note (3):  $C_{o(er)}$ , a lumped capacitance that gives same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 1200 V.

$C_{o(tr)}$ , a lumped capacitance that gives same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 1200 V.



## Reverse Diode Characteristics

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Note
Diode Forward Voltage	$V_{SD}$	3.8		V	$V_{GS} = -5\text{ V}, I_{SD} = 25\text{ A}$	Fig. 8, 9, 10 Note 1
		3.4			$V_{GS} = -5\text{ V}, I_{SD} = 25\text{ A}, T_J = 150\text{ }^\circ\text{C}$	
Continuous Diode Forward Current	$I_S$		76	A	$V_{GS} = -5\text{ V}, T_C = 25\text{ }^\circ\text{C}$	Note 1
Diode Pulse Current	$I_{S, pulse}$		160		$V_{GS} = -5\text{ V}, \text{Pulse Width } t_p \text{ Limited by } T_{Jmax}$	Note 1
Reverse Recovery Time	$t_{rr}$	44		ns	$V_{GS} = -5\text{ V}, I_{SD} = 50\text{ A}, V_R = 1200\text{ V}$ $dif/dt = 4030\text{ A}/\mu\text{s}, T_J = 150\text{ }^\circ\text{C}$	
Reverse Recovery Charge	$Q_{rr}$	1.9		nC		
Peak Reverse Recovery Current	$I_{rrm}$	64		A		
Reverse Recovery Time	$t_{rr}$	25		ns	$V_{GS} = -5\text{ V}, I_{SD} = 50\text{ A}, V_R = 1200\text{ V}$ $dif/dt = 13450\text{ A}/\mu\text{s}, T_J = 150\text{ }^\circ\text{C}$	
Reverse Recovery Charge	$Q_{rr}$	2.4		nC		
Peak Reverse Recovery Current	$I_{rrm}$	166		A		

## Thermal Characteristics

Parameter	Symbol	Typ.	Max	Unit	Test Conditions	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.22	0.37	$^\circ\text{C}/\text{W}$		Fig. 21
Thermal Resistance from Junction to Ambient	$R_{\theta JA}$		40			



Typical Performance

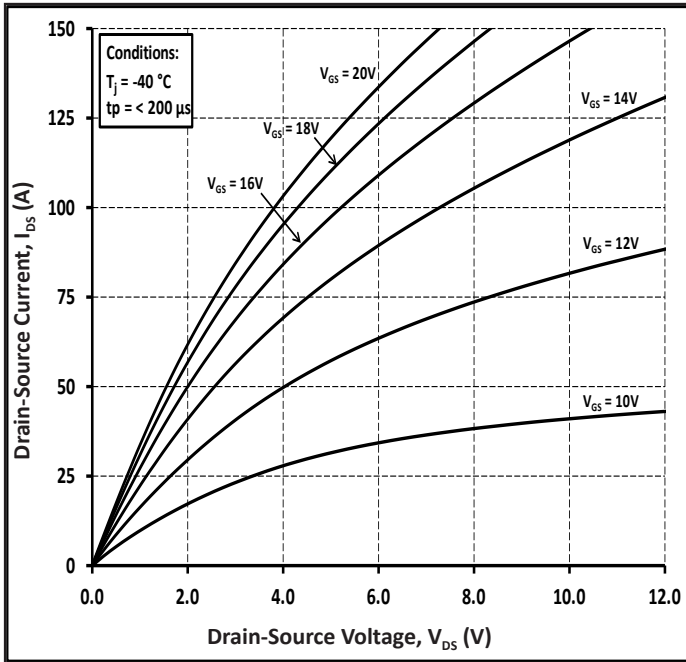


Figure 1. Output Characteristics  $T_j = -40\text{ }^\circ\text{C}$

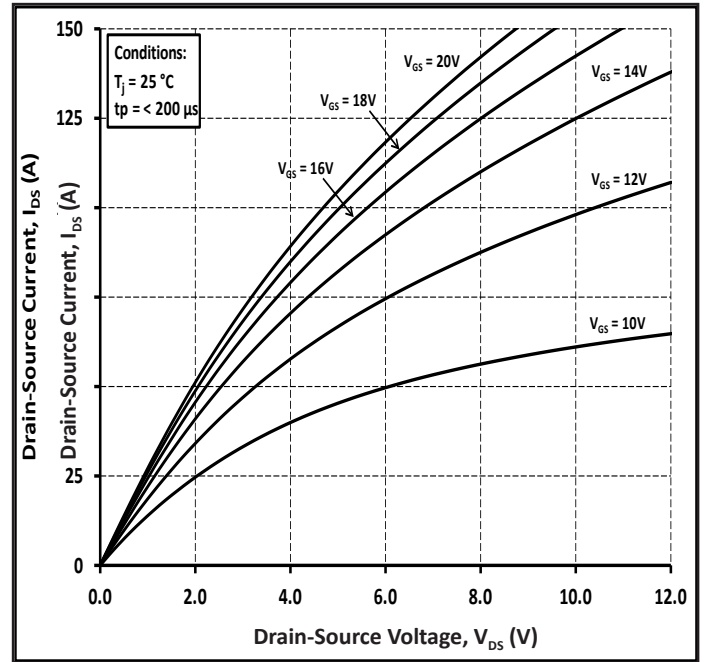


Figure 2. Output Characteristics  $T_j = 25\text{ }^\circ\text{C}$

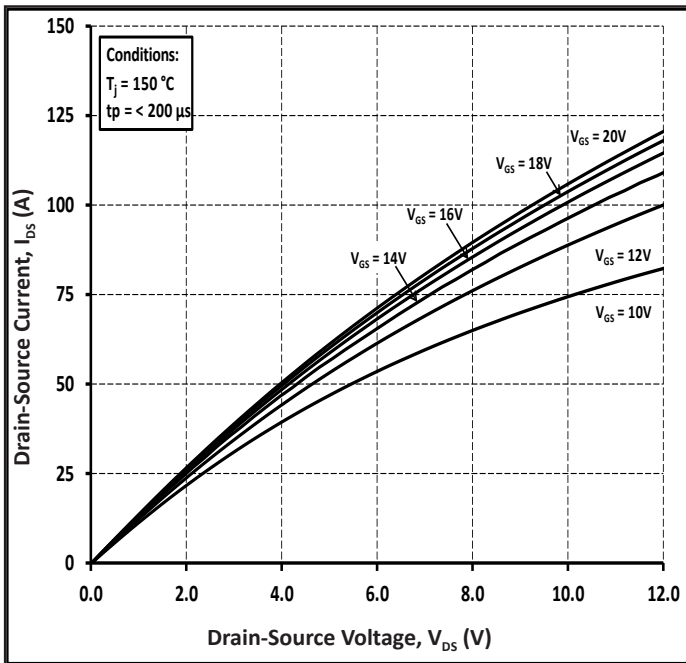


Figure 3. Output Characteristics  $T_j = 150\text{ }^\circ\text{C}$

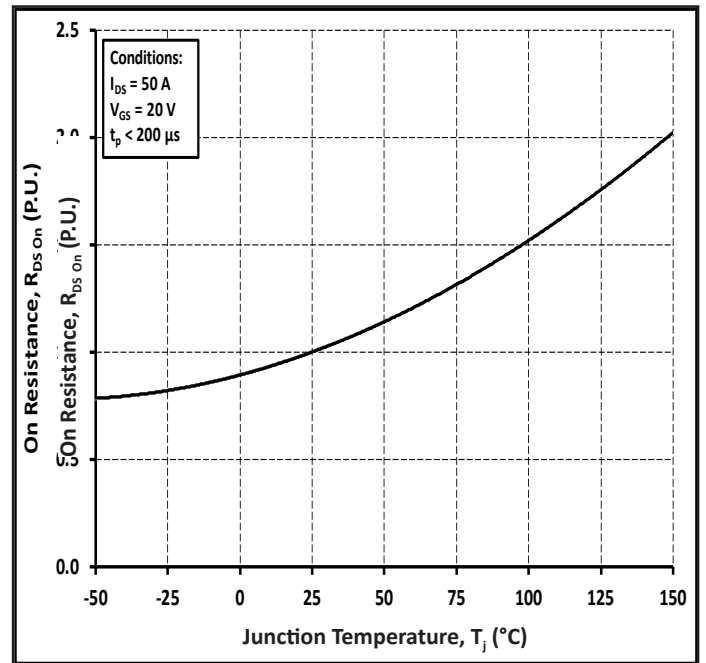


Figure 4. Normalized On-Resistance vs Temperature



Typical Performance

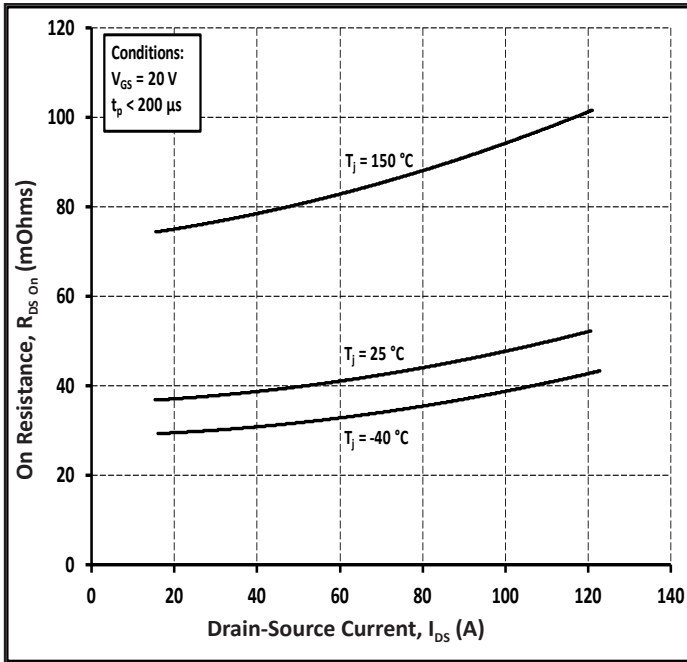


Figure 5. On-Resistance vs Drain Current for Various Temperatures

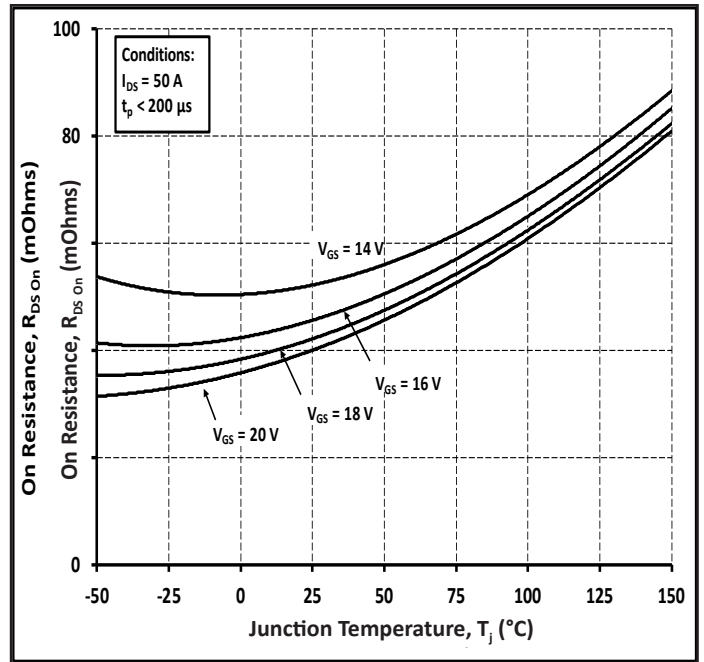


Figure 6. On-Resistance vs Temperature for Various Gate Voltage

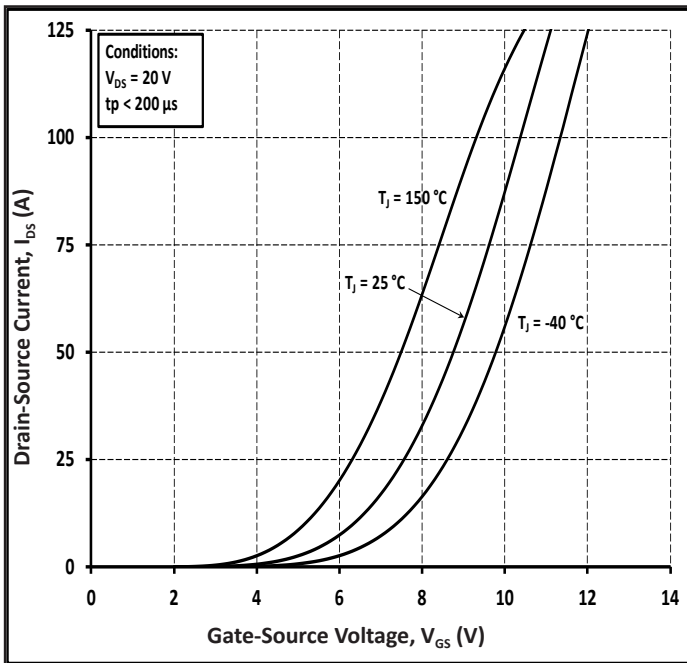


Figure 7. Transfer Characteristic for Various Junction Temperatures

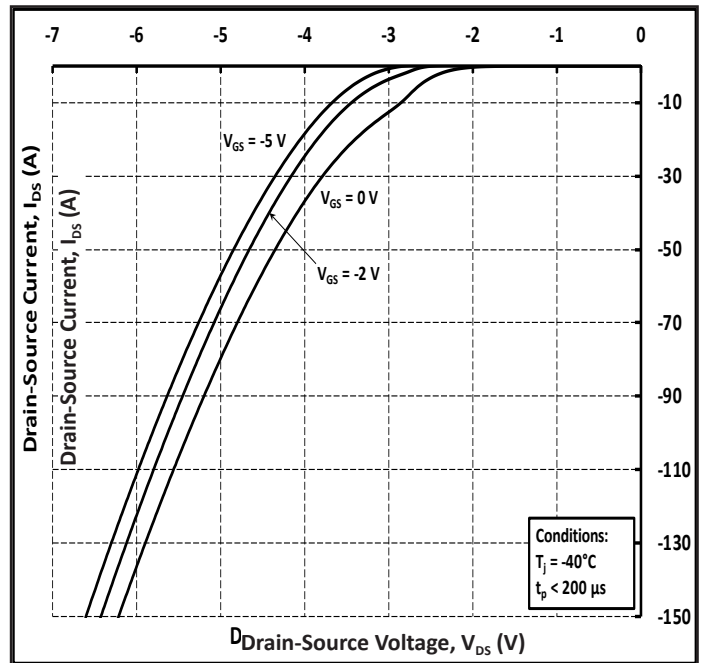


Figure 8. Body Diode Characteristic at -40 °C



Typical Performance

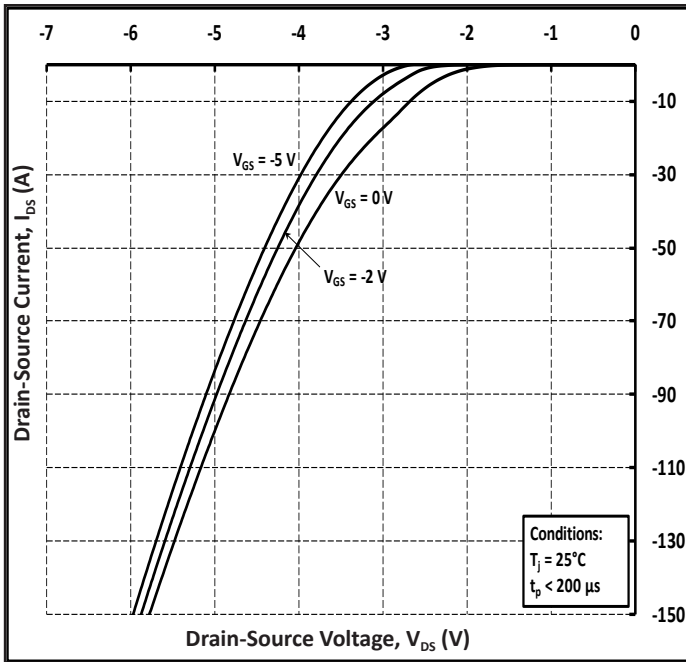


Figure 9. Body Diode Characteristic at 25 °C

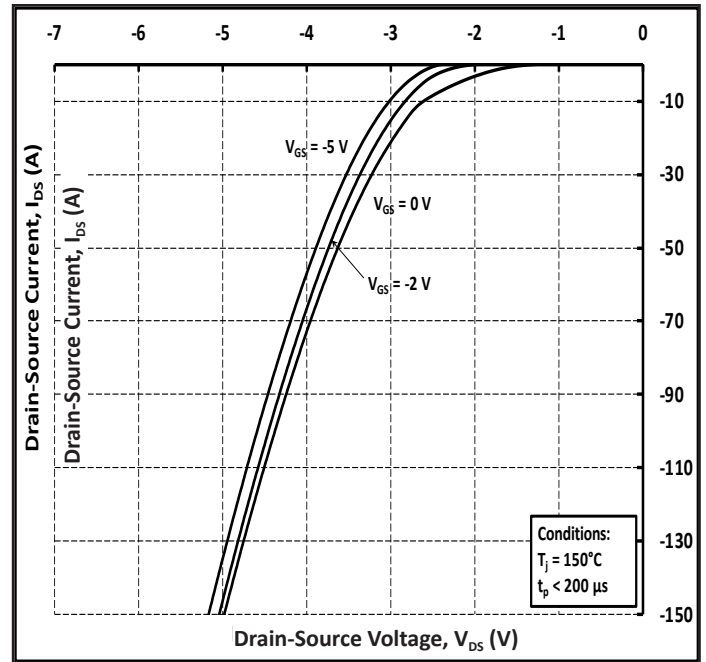


Figure 10. Body Diode Characteristic at 150 °C

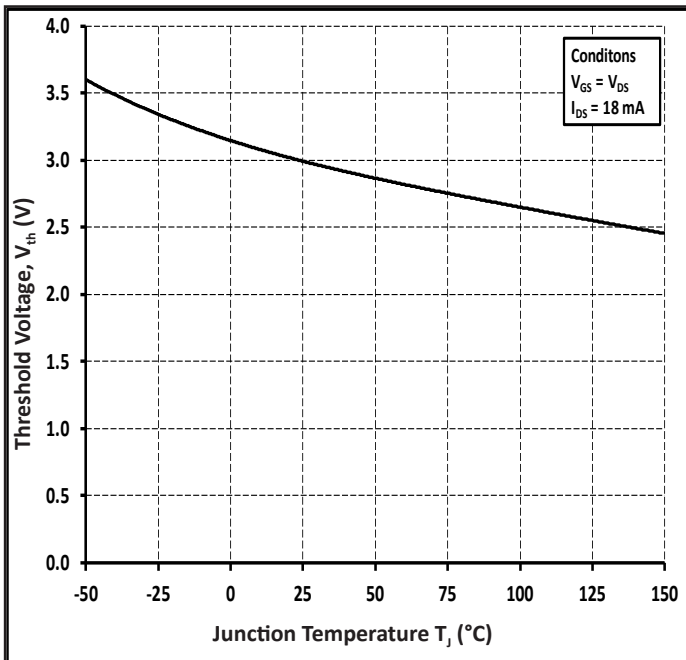


Figure 11. Threshold Voltage vs Temperature

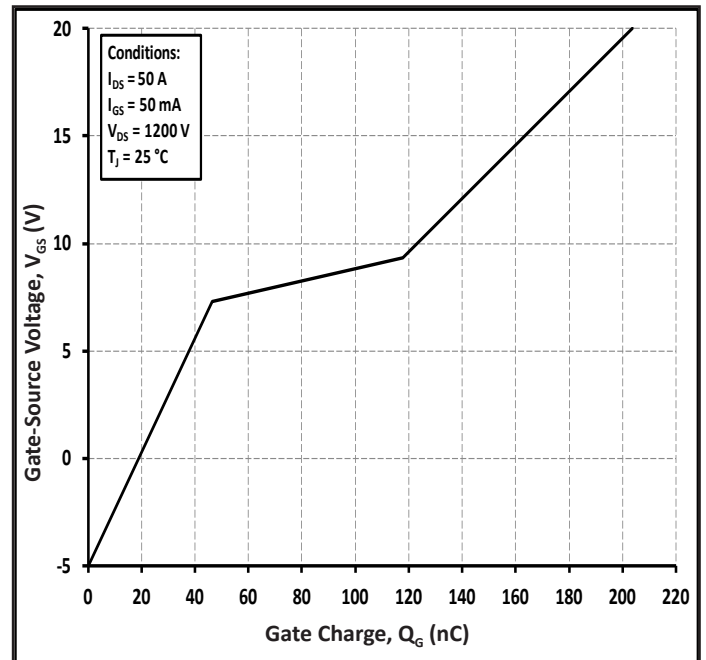


Figure 12. Gate Charge Characteristic

Typical Performance

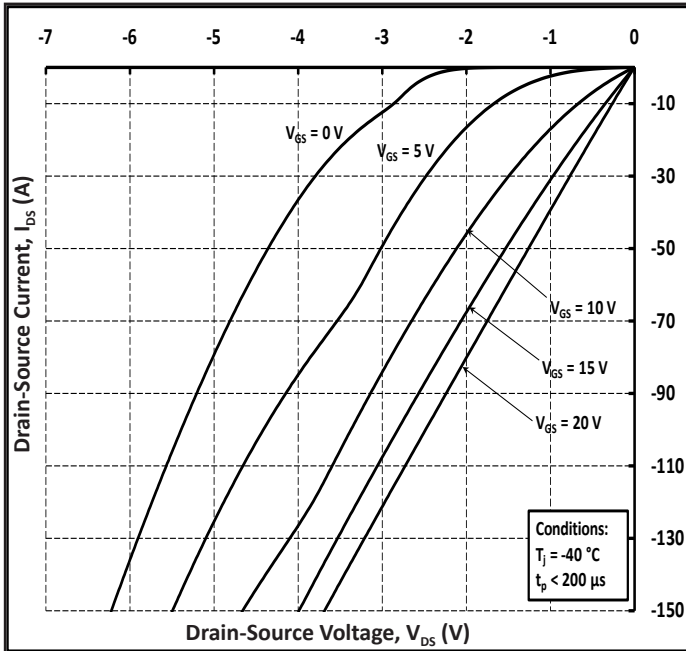


Figure 13. 3<sup>rd</sup> Quadrant Characteristic at  $-40\text{ }^{\circ}\text{C}$

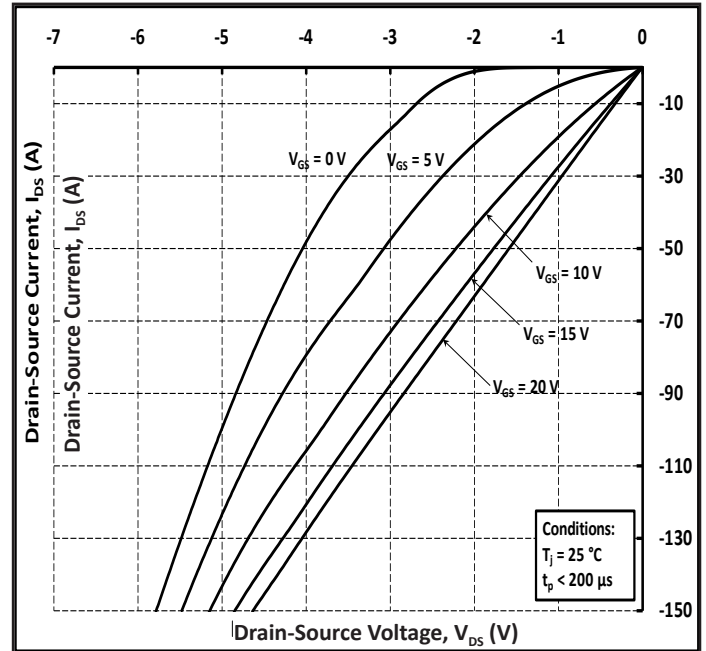


Figure 14. 3<sup>rd</sup> Quadrant Characteristic at  $25\text{ }^{\circ}\text{C}$

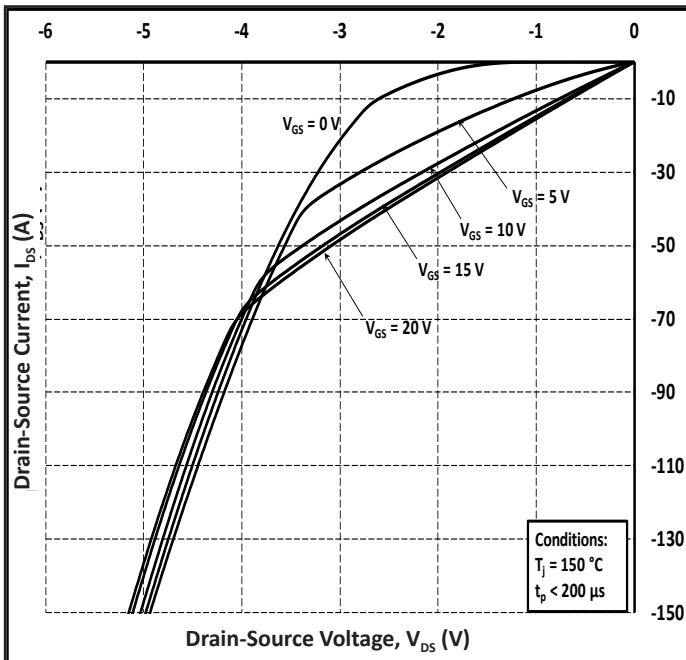


Figure 15. 3<sup>rd</sup> Quadrant Characteristic at  $150\text{ }^{\circ}\text{C}$

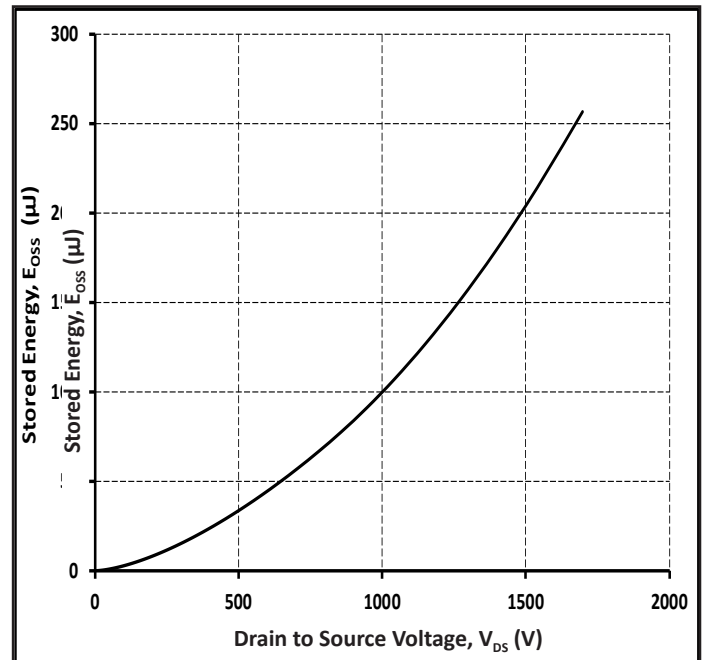


Figure 16. Output Capacitor Stored Energy



Typical Performance

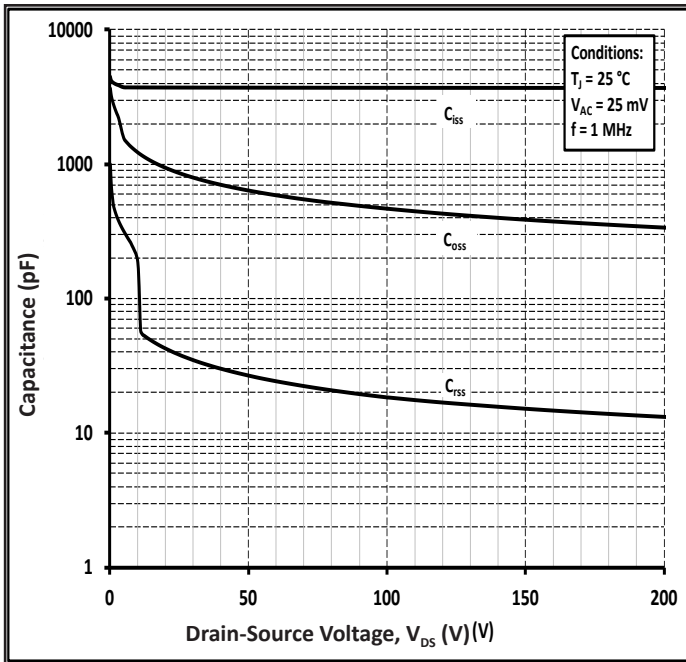


Figure 17. Capacitances vs Drain-Source Voltage (0-200 V)

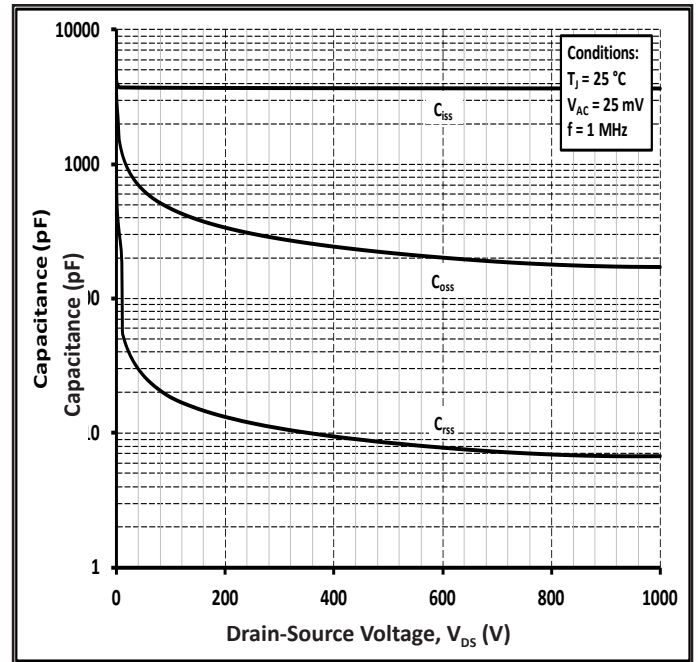


Figure 18. Capacitances vs Drain-Source Voltage (0-1000 V)

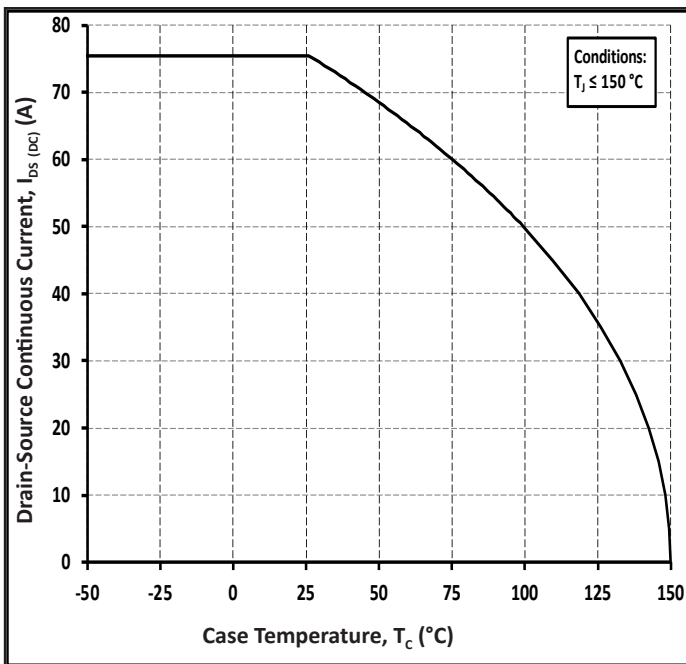


Figure 19. Continuous Drain Current Derating vs Case Temperature

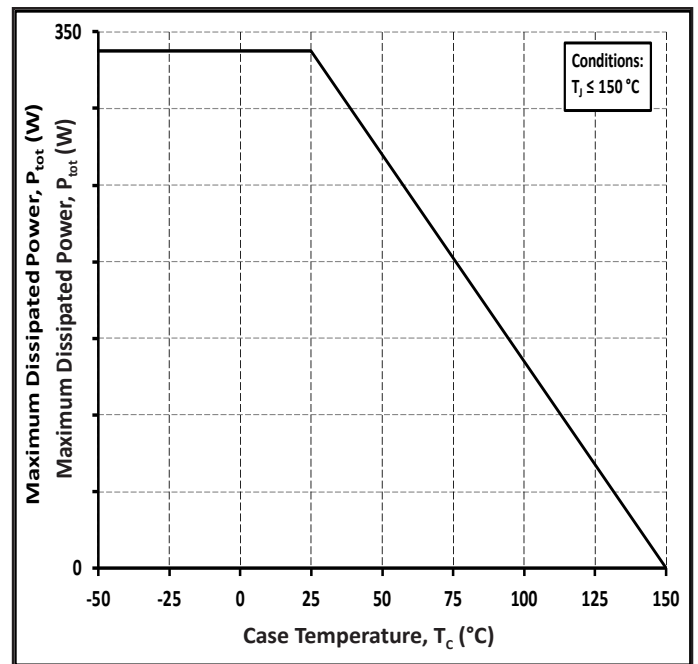


Figure 20. Maximum Power Dissipation Derating vs Case Temperature





Typical Performance

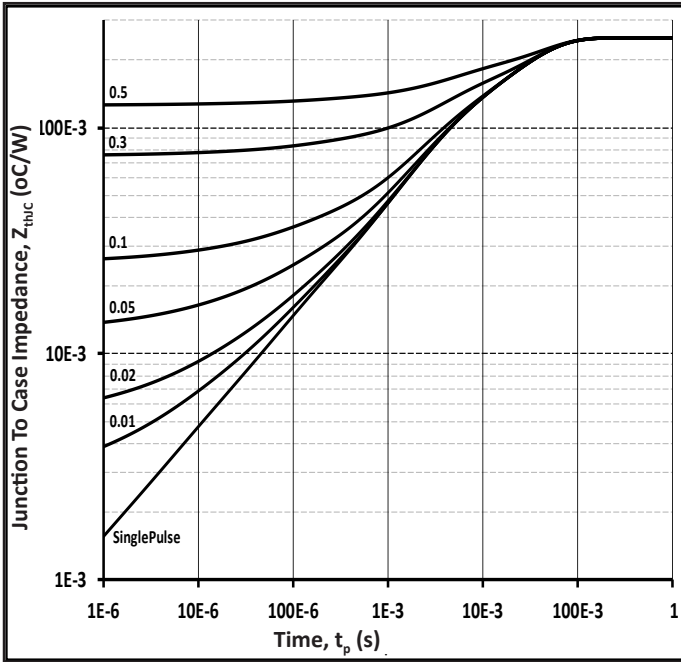


Figure 21. Transient Thermal Impedance (Junction - Case)

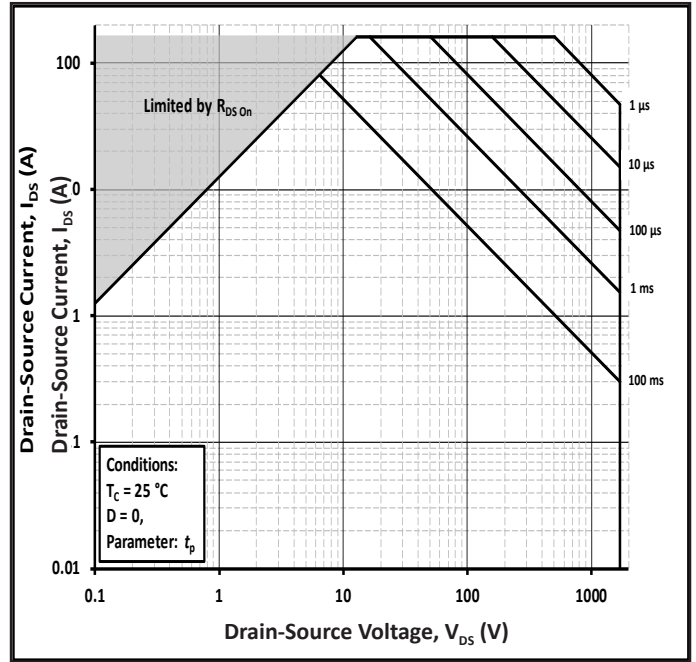


Figure 22. Safe Operating Area

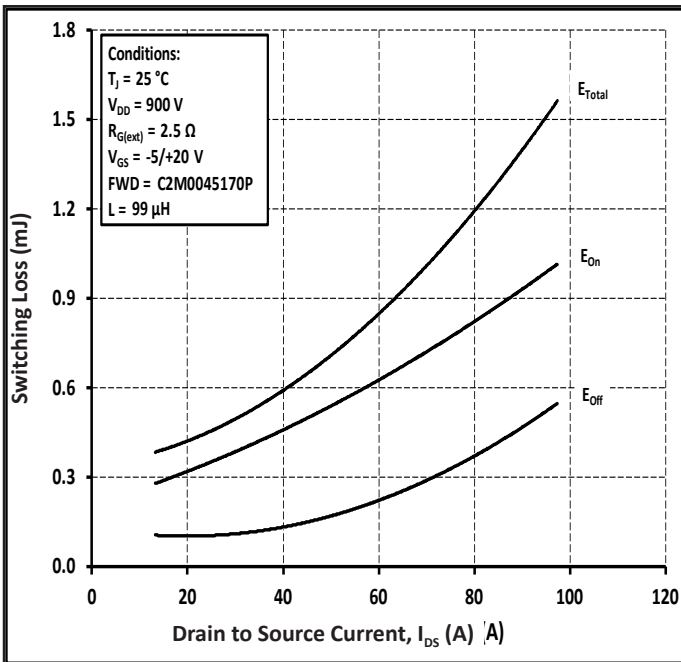


Figure 23. Clamped Inductive Switching Energy vs Drain Current ( $V_{DD} = 900\text{ V}$ )

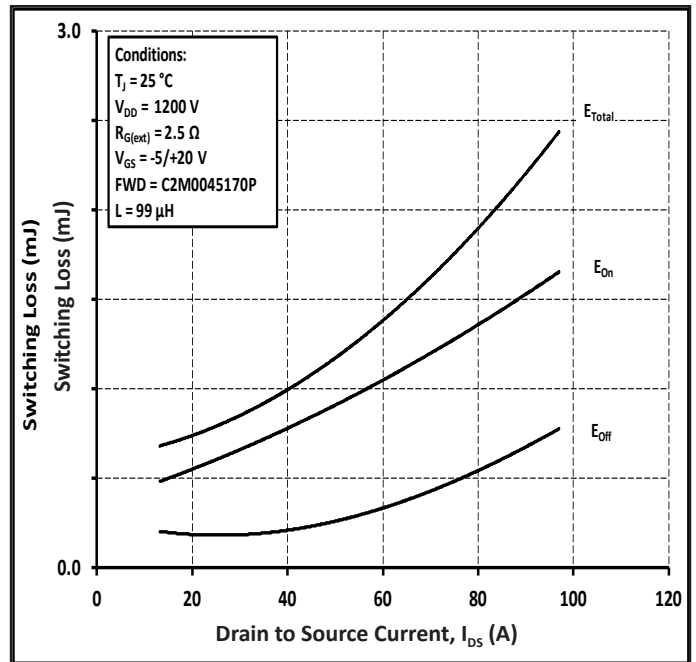


Figure 24. Clamped Inductive Switching Energy vs Drain Current ( $V_{DD} = 1200\text{ V}$ )



Typical Performance

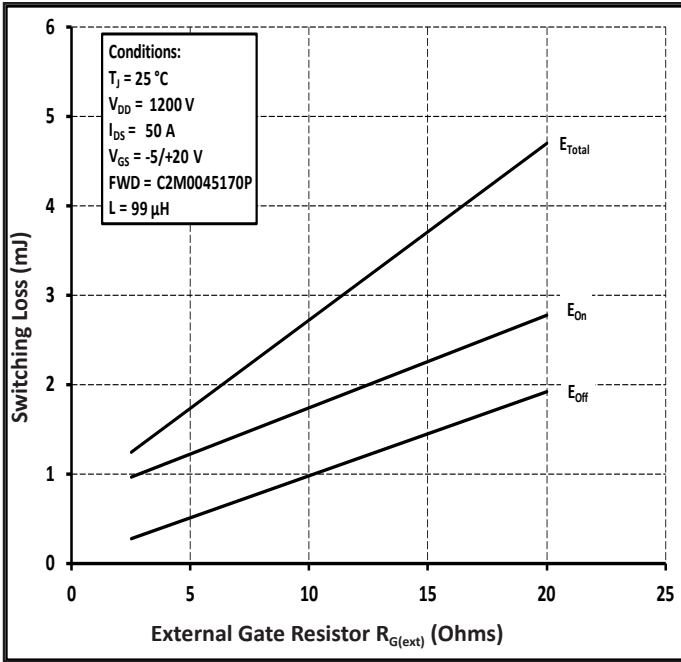


Figure 25. Clamped Inductive Switching Energy vs  $R_{G(ext)}$

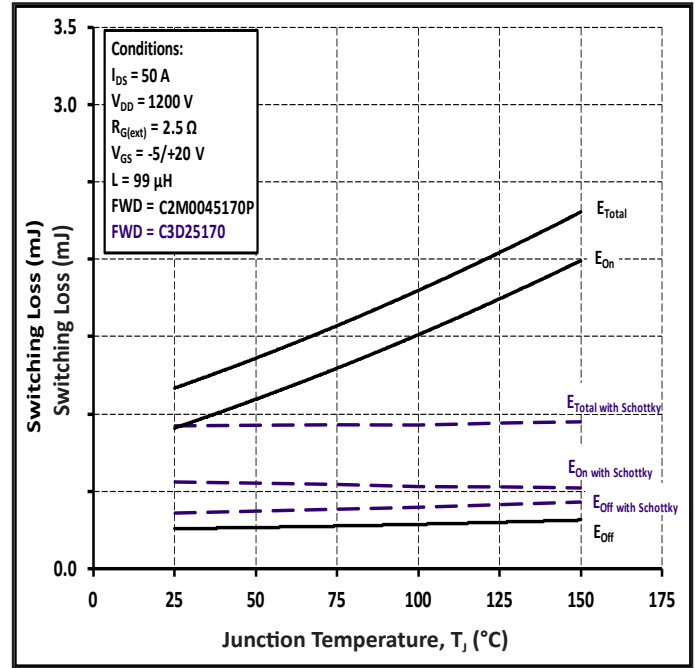


Figure 26. Clamped Inductive Switching Energy vs Temperature

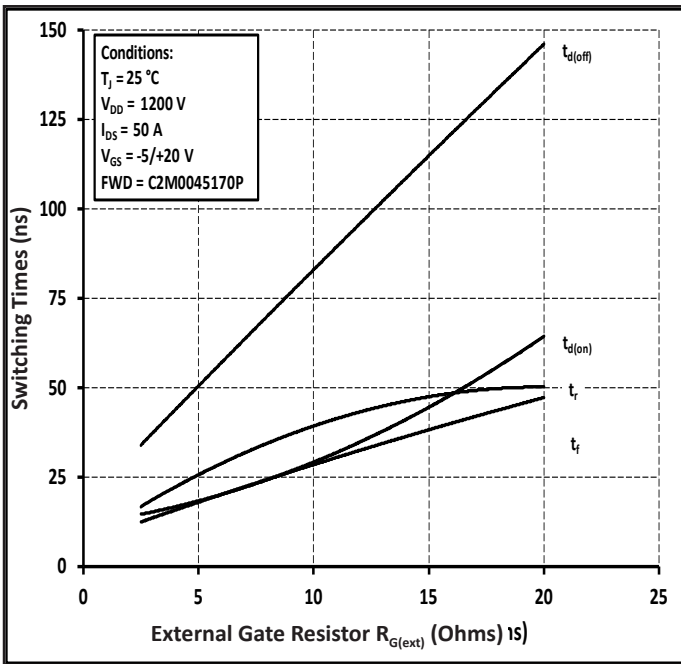


Figure 27. Switching Times vs  $R_{G(ext)}$

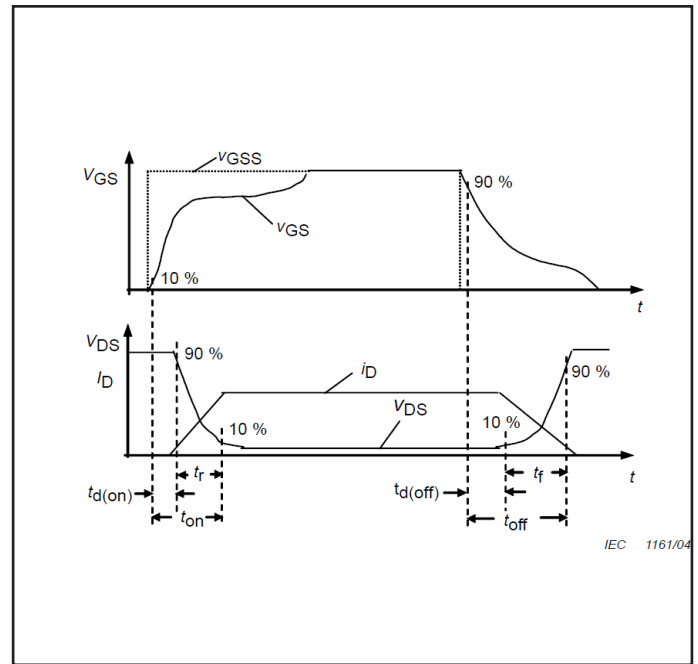


Figure 28. Switching Times Definition



**Test Circuit Schematic**

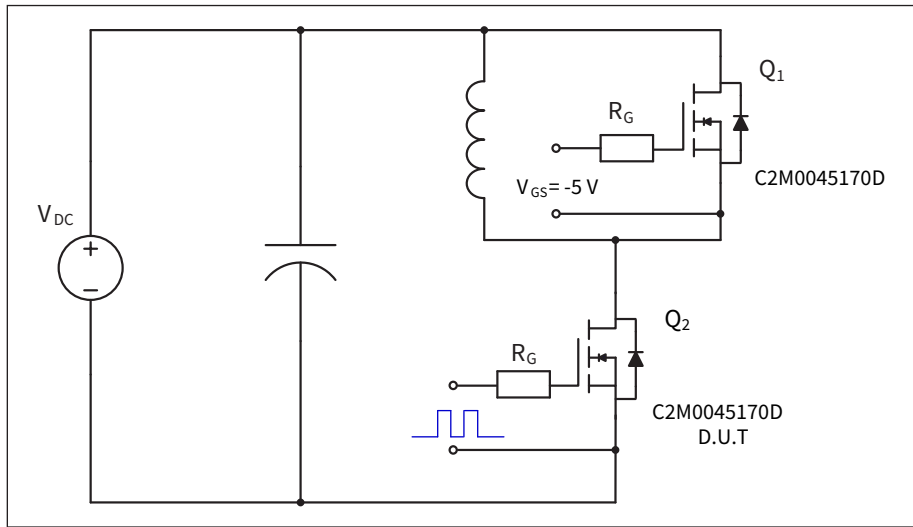


Figure 29a. Clamped Inductive Switching Test Circuit Using MOSFET Intrinsic Body Diode

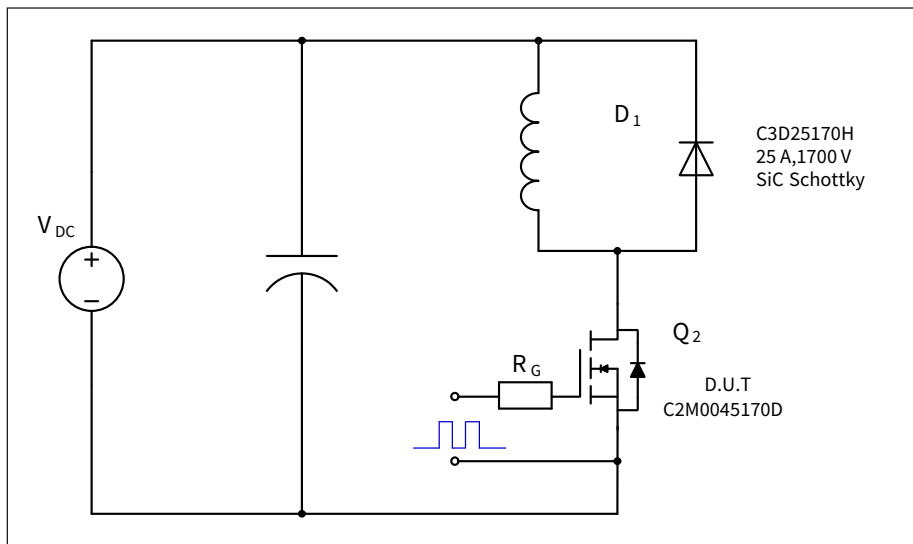
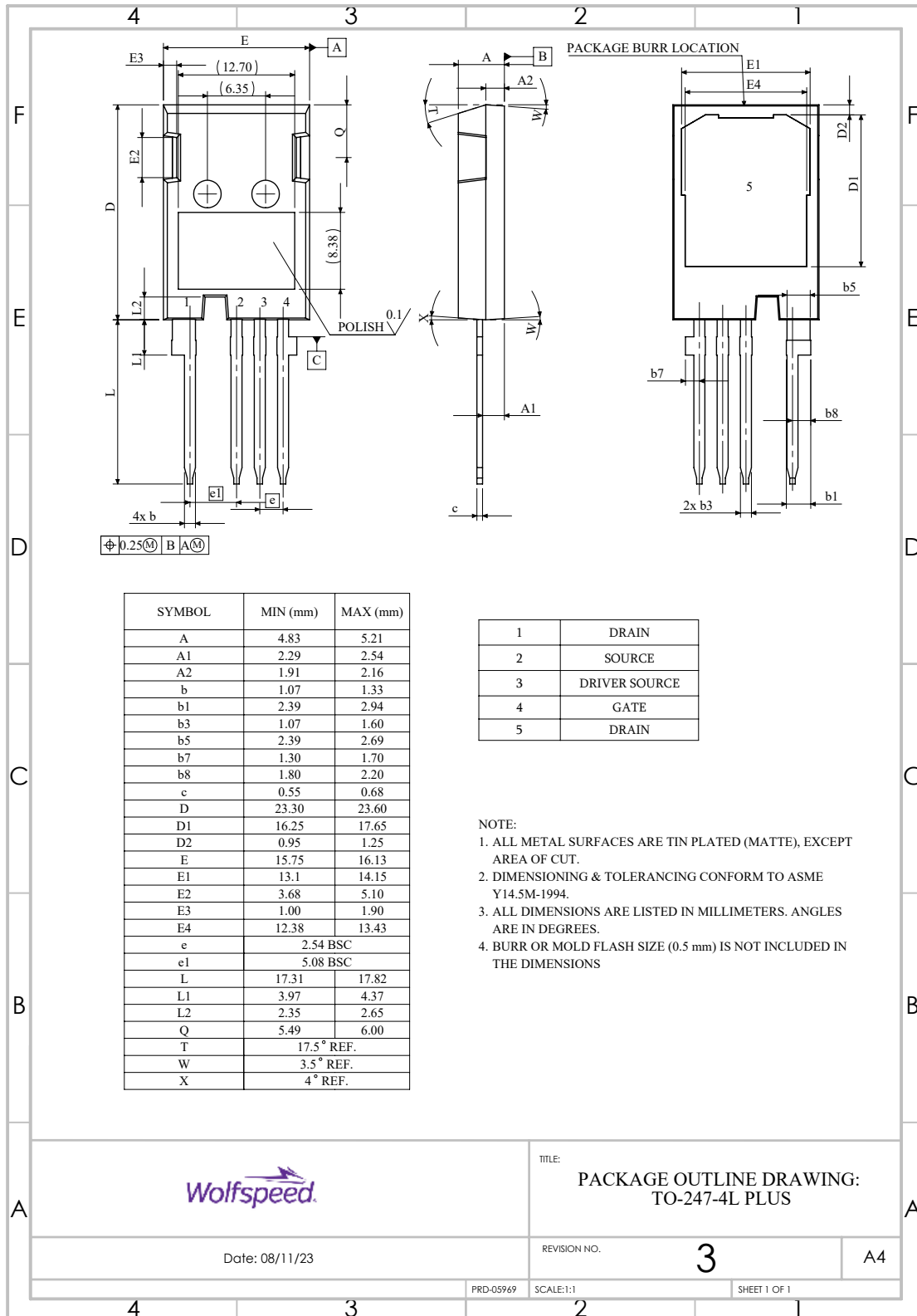


Figure 29b. Clamped Inductive Switching Test Circuit Using SiC Schottky Diode



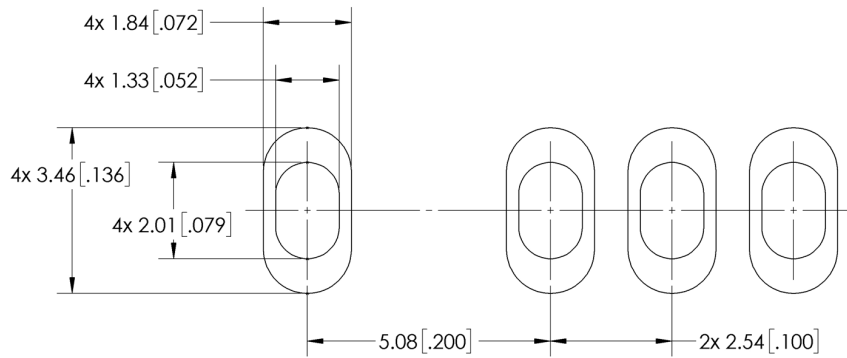
### Package Dimensions

Package: TO-247-4L





**Recommended Solder Pad Layout**



Part Number	Package	Marking
C2M0045170P	TO-247-4L	C2M0045170P



## Revision History

Current Revision	Date of Release	Description of Changes
2	May-2022	Initial Release
3	October-2023	Wolfspeed branding, POD, Package image, Solder Temp conditions note changed to JEDEC standard
4	November-2023	Corrected POD A1, D2, and L



## Notes & Disclaimer

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