

## Low Quiescent Programmable-Delay Supervisory

### Description

The DIODES PT7M3808G family of microprocessor supervisory circuits monitor system voltage from 0.4V to 5.0V, asserting an open-drain  $\overline{\text{RESET}}$  signal when the SENSE voltage drops below a preset threshold or when the manual reset (  $\overline{\text{MR}}$  ) pin drops to a logic low. The  $\overline{\text{RESET}}$  output remains low for the user-adjustable delay time after the SENSE voltage and manual reset (  $\overline{\text{MR}}$  ) return above the respective thresholds.

The PT7M3808G series uses a precision reference to achieve 0.5% threshold accuracy for  $V_{IT} \leq 3.3$  V. The reset delay time can be set to 20ms by disconnecting the  $C_T$  pin, 300ms by connecting the  $C_T$  pin to  $V_{DD}$  using a resistor, or can be user-adjusted between 1.25ms and 10s by connecting the  $C_T$  pin to an external capacitor. The PT7M3808 has a very low typical quiescent current of 2.8 $\mu$ A so it is well-suited to battery-powered applications. It is available in a small SOT23 and an ultra-small 2.0x2.0 TDFN package, and is fully specified over a temperature range of -40°C to +125°C.

### Application(s)

- DSP or Microcontroller Applications Capacitor
- Notebook/Desktop Computers
- PDAs/Hand-Held Products Battery-powered Applications
- Portable/Battery-Powered Products
- FPGA/ASIC Applications

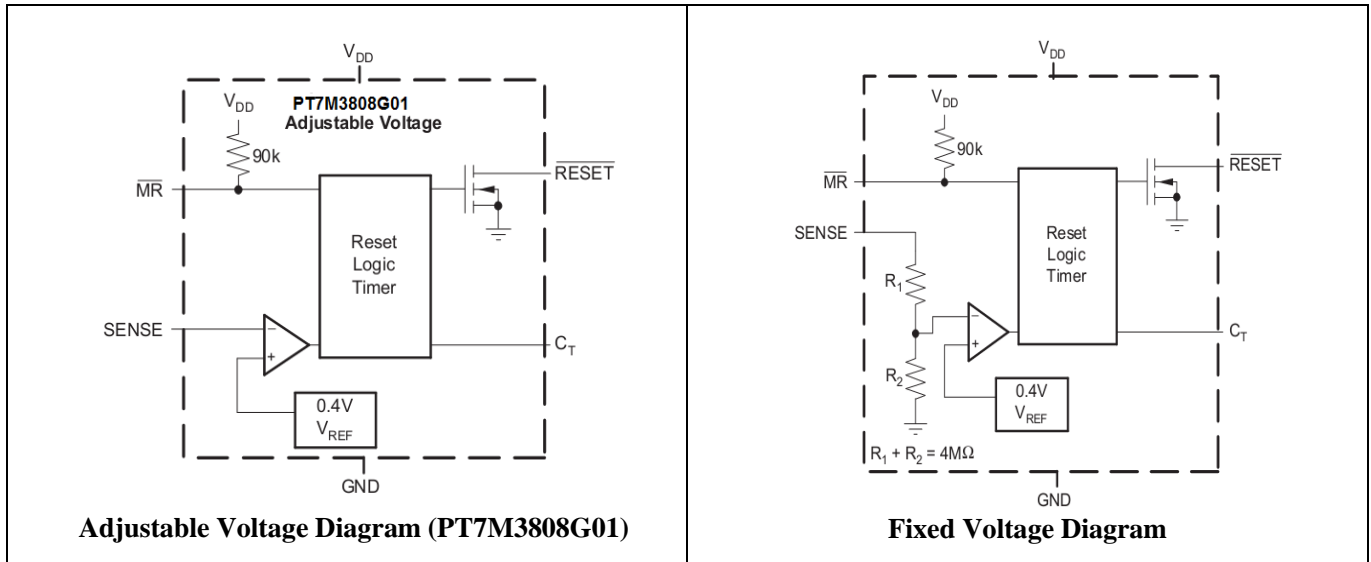
### Features

- Power-On Reset Generator with Adjustable Delay Time: 1.25ms to 10s.
- Very Low Quiescent Current: 2.8 $\mu$ A Typical
- High Threshold Accuracy: 0.5% Typ.
- Fixed Threshold Voltages for Standard Voltage Rails from 0.9V to 5V and Adjustable Voltage Down to 0.4V are available.
- Manual Reset (  $\overline{\text{MR}}$  ) Input.
- Open-Drain  $\overline{\text{RESET}}$  Output.
- Temperature Range: -40°C to +125°C
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/104/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](#) or your local Diodes representative.  
<https://www.diodes.com/quality/product-definitions/>
- Packaging (Pb-free & Green):
  - 6-pins, TDFN 2.0x2.0 (ZC)
  - 6-pins, SOT23 (TA)

#### Notes:

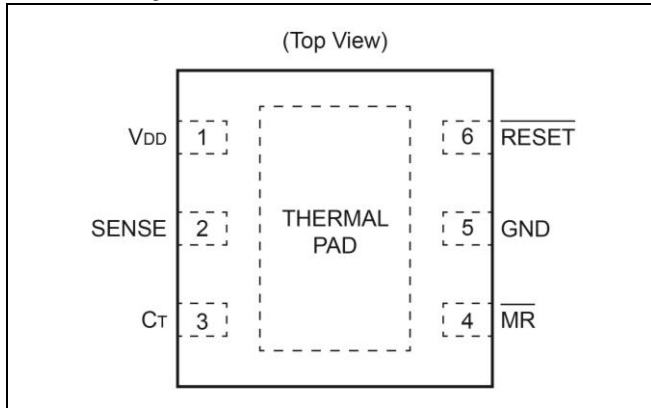
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

**Block Diagram**

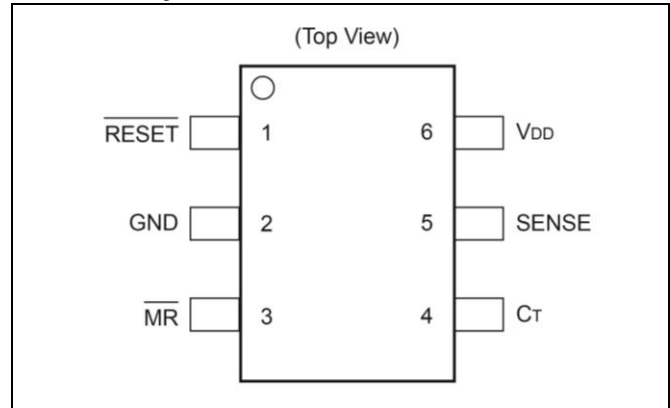


## Pin Configuration

TDFN Package



SOT23 Package



## Pin Description

Pin#		Pin Name	Description
SOT23	TDFN		
1	6	$\overline{\text{RESET}}$	An open-drain output that is driven to a low impedance state when $\overline{\text{RESET}}$ is asserted. $\overline{\text{RESET}}$ will remain low (asserted) for the reset period after both SENSE is above $V_{IT}$ and $\overline{\text{MR}}$ is set to a logic high. A pull-up resistor from 10k $\Omega$ to 1Mohm should be used on this pin, and allows the reset pin to attain voltages higher than $V_{DD}$ .
2	5	GND	Ground.
3	4	$\overline{\text{MR}}$	Driving the manual reset pin ( $\overline{\text{MR}}$ ) low asserts $\overline{\text{RESET}}$ . MR is internally tied to $V_{DD}$ by a 90kohm pull-up resistor.
4	3	$C_T$	Reset period programming pin. Connection this pin to $V_{DD}$ through a 40k $\Omega$ to 200k $\Omega$ resistor for 300ms or leaving it open results in fixed delay times 20ms. And connecting this pin with a cap $\geq 100\text{pF}$ to ground a user-programmable delay time.
5	2	SENSE	This pin is connected to the voltage to be monitored. If the voltage at this terminal drops below the threshold voltage $V_{IT}$ , then $\overline{\text{RESET}}$ is asserted.
6	1	$V_{DD}$	Supply Voltage. Place a 0.1 $\mu\text{F}$ ceramic capacitor close to this pin.
-	PAD	Thermal Pad	Thermal Pad. Connect to ground plane to enhance thermal performance of package.

## Maximum Ratings

Storage Temperature.....	-65°C to +150°C
Operating Junction Temperature, T <sub>J</sub> .....	-40°C to +125°C
Input Voltage Range, V <sub>DD</sub> .....	-0.3V to +7.0V
C <sub>T</sub> Voltage Range, V <sub>CT</sub> .....	-0.3V to V <sub>DD</sub> +0.5V
Other Voltage Range, V <sub>RESET</sub> , V <sub>MR</sub> , V <sub>SENSE</sub> .....	-0.3V to +7.0V
RESET pin Current.....	5mA
ESD rating, HBM.....	2kV
ESD rating, CDM.....	500V

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended Operation Conditions

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply Voltage		1.7		6.5	V
V <sub>IH</sub>	Input High Voltage $\overline{MR}$				V <sub>DD</sub>	V
	Input High Voltage for Open-drain RESET, SENSE		0		6.5	V
V <sub>IL</sub>	Input Low Voltage $\overline{MR}$ .				0.3V <sub>DD</sub>	V
T <sub>A</sub>	Operating Temperature		-40		125	°C

## Electrical Characteristics

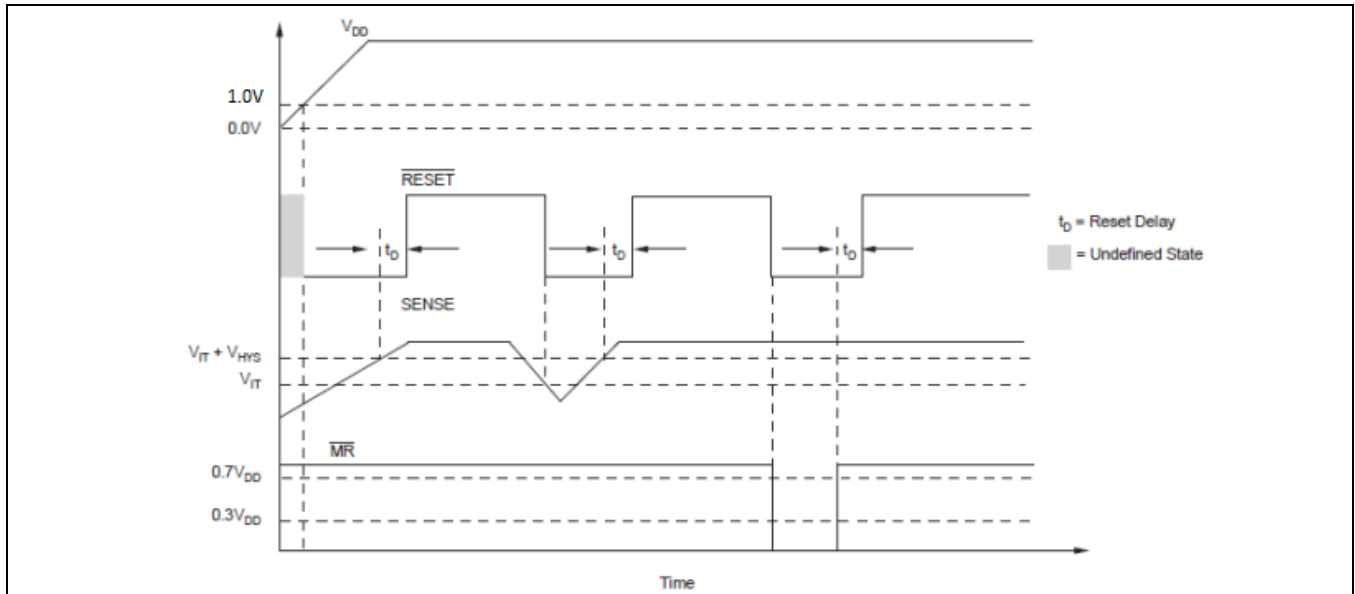
Unless otherwise specified, -40°C ≤ T<sub>A</sub> ≤ 125°C, 1.7V ≤ V<sub>DD</sub> ≤ 6.5V, R<sub>RESET</sub> = 100kΩ, C<sub>RESET</sub> = 50Pf, Typical values are at T<sub>A</sub> = +25°C.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply voltage		1.7		6.5	V
I <sub>DD</sub>	Supply current	V <sub>DD</sub> = 3.3V, $\overline{RESET}$ not asserted, $\overline{MR}$ , $\overline{RESET}$ , C <sub>T</sub> open.		2.8	5.0	μA
		V <sub>DD</sub> = 6.5V, $\overline{RESET}$ not asserted, $\overline{MR}$ , $\overline{RESET}$ , C <sub>T</sub> open.		3.0	6.0	uA
V <sub>OL</sub>	Low level output voltage	1.3V ≤ V <sub>DD</sub> < 1.8V, I <sub>OL</sub> = 0.4mA			0.3	V
		1.8V ≤ V <sub>DD</sub> ≤ 6.5V, I <sub>OL</sub> = 1.0mA			0.4	
V <sub>POR</sub>	Power-up reset voltage *	V <sub>OL</sub> = 0.2V, I <sub>RESET</sub> = 15μA			1.0	V
V <sub>IT</sub>	Negative-going input threshold	PT7M3808G01	0.375	0.405	0.409	V
		PT7M3808G09	0.81	0.84	0.844	
		PT7M3808G12	1.092	1.12	1.126	
		PT7M3808G125	1.132	1.16	1.166	
		PT7M3808G15	1.373	1.4	1.407	
		PT7M3808G18	1.644	1.67	1.678	
		PT7M3808G19	1.745	1.77	1.779	
		PT7M3808G25	2.308	2.33	2.342	
		PT7M3808G30	2.770	2.79	2.804	
		PT7M3808G33	3.055	3.07	3.085	

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	
		PT7M3808G50	4.604	4.65	4.697		
$V_{HYS}$	Hysteresis on $V_{IT}$ pin	PT7M3808G01		1.5	3.0	% $V_{IT}$	
		Fixed versions		1	2.5		
$\overline{R_{MR}}$	$\overline{MR}$ Internal pull-up resistance		70	90		k $\Omega$	
$I_{SENSE}$	Input current at SENSE pin	PT7M3808G01	$V_{SENSE}=V_{IT}$	-25	25	nA	
		Fixed versions	$V_{SENSE}=6.5V$	1.8		$\mu A$	
$I_{OH}$	$\overline{RESET}$ Leakage Current	$V_{RESET}=6.5V$ , $\overline{RESET}$ not asserted			300	nA	
$C_{IN}$	Input capacitance, any pin	$C_T$ pin	$V_{IN}=0V$ to $V_{DD}$	5		pF	
		Other pins	$V_{IN}=0V$ to $6.5V$	5			
$V_{IL}$	$\overline{MR}$ logic low input		0		$0.3V_{DD}$	V	
$V_{IH}$	$\overline{MR}$ logic High input		$0.7V_{DD}$		$V_{DD}$	V	
$t_w$	Input pulse width to $\overline{RESET}$	SENSE	$V_{IH}=1.05V_{IT}$ , $V_{IL}=0.95V_{IT}$	20		$\mu s$	
		$\overline{MR}$	$V_{IH}=0.7V_{DD}$ , $V_{IL}=0.3V_{DD}$	0.001		$\mu s$	
$t_D$	$\overline{RESET}$ delay time	$C_T=open$		12	20	28	ms
		$C_T=V_{DD}$		180	300	420	ms
		$C_T=100pF$		0.75	1.25	1.75	ms
		$C_T=180nF$		0.7	1.2	1.7	s
$t_{pHL}$	Propagation delay	$\overline{MR}$ to $\overline{RESET}$	$V_{IH}=0.7V_{DD}$ , $V_{IL}=0.3V_{DD}$	150		ns	
	High to low level $\overline{RESET}$ delay	SENSE to $\overline{RESET}$	$V_{IH}=1.05V_{IT}$ , $V_{IL}=0.95V_{IT}$	20		us	

**Note:** The lowest supply voltage ( $V_{DD}$ ) at which  $\overline{RESET}$  becomes active.  $Trise(V_{DD}) \geq 15\mu s/V$ .

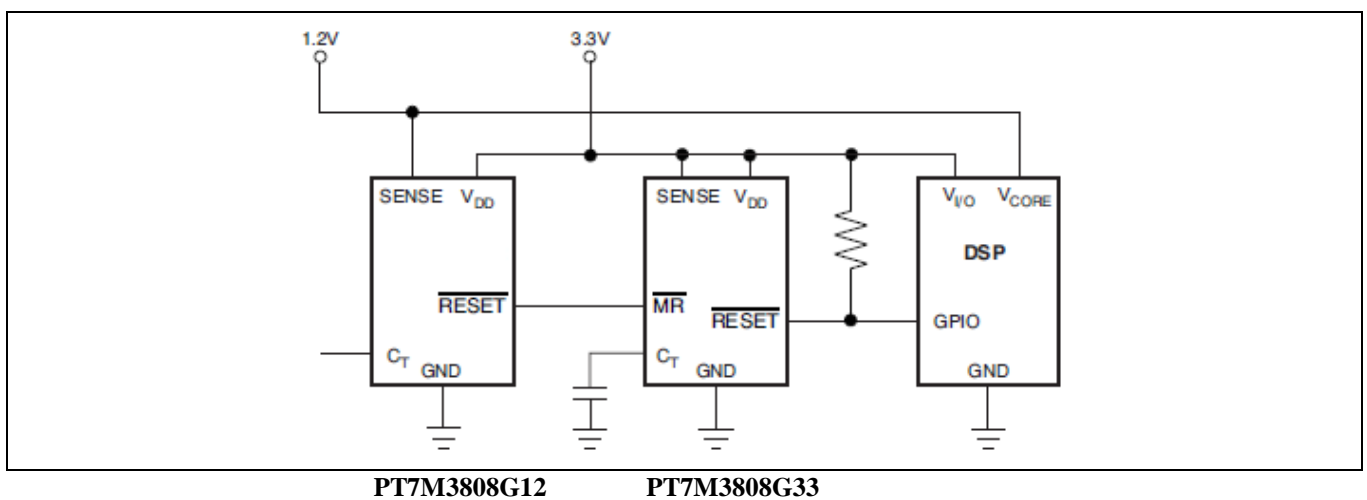
**Timing Diagram**



**Truth Table**

$\overline{MR}$	$SENSE > V_{IT}$	$\overline{RESET}$
L	0	L
L	1	L
H	0	L
H	1	H

**Typical Application Circuit**



## Functional Description

The PT7M3808 microprocessor supervisory product family is designed to assert a  $\overline{\text{RESET}}$  signal when either the SENSE pin voltage drops below  $V_{IT}$  or the manual reset ( $\overline{\text{MR}}$ ) is driven low. The  $\overline{\text{RESET}}$  output remains asserted for a user-adjustable time after both the manual reset ( $\overline{\text{MR}}$ ) and SENSE voltages return above the respective thresholds. A broad range of the voltage threshold and reset delay time adjustments are available, allowing these devices to be used in a wide array of applications. Reset threshold voltages can be factory-set from 0.82V to 3.3V or from 4.4V to 5.0V, while the PT7M3808G01 can be set to any voltage above 0.405V using an external resistor divider. Two preset delay times are also user-selectable: connecting the  $C_T$  pin to  $V_{DD}$  results in a 300ms reset delay, while leaving the  $C_T$  pin open yields a 20ms reset delay. In addition, connecting a capacitor between  $C_T$  and GND allows the designer to select any reset delay period from 1.25ms to 10s.

### RESET Output

The open-drain  $\overline{\text{RESET}}$  output is typically connected to the  $\overline{\text{RESET}}$  input of a microprocessor. A pull-up resistor must be used to hold this line high when  $\overline{\text{RESET}}$  is not asserted. The  $\overline{\text{RESET}}$  output is undefined for voltage below 1.0V, but this is normally not a problem since most microprocessors do not function below this voltage.  $\overline{\text{RESET}}$  remains high (unasserted) as long as SENSE is above its threshold ( $V_{IT}$ ) and the manual reset ( $\overline{\text{MR}}$ ) is logic high. If either SENSE falls below  $V_{IT}$  or  $\overline{\text{MR}}$  is driven low,  $\overline{\text{RESET}}$  is asserted, driving the  $\overline{\text{RESET}}$  pin to low impedance.

Once  $\overline{\text{MR}}$  is again logic high and SENSE is above  $V_{IT} + V_{HYS}$  (the threshold hysteresis), a delay circuit is enabled which holds  $\overline{\text{RESET}}$  low for a specified reset delay period. Once the reset delay has expired, the  $\overline{\text{RESET}}$  pin goes to a high impedance state. The pull-up resistor from the open-drain  $\overline{\text{RESET}}$  to the supply line can be used to allow the reset signal for the microprocessor to have a voltage higher than  $V_{DD}$  (up to 6.5V). The pull-up resistor should be no smaller than 10k $\Omega$  as a result of the finite impedance of the  $\overline{\text{RESET}}$  line.

### SENSE Input

The SENSE input provides a pin at which any system voltage can be monitored. If the voltage on this pin drops below  $V_{IT}$ , then  $\overline{\text{RESET}}$  is asserted. The comparator has a built-in hysteresis to ensure smooth  $\overline{\text{RESET}}$  assertions and de-assertions. It is good analog design practice to put a 1nF to 10nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitic.

The PT7M3808G01 can be used to monitor any voltage rail down to 0.405V by resistor divider.

### Manual Reset ( $\overline{\text{MR}}$ ) Input

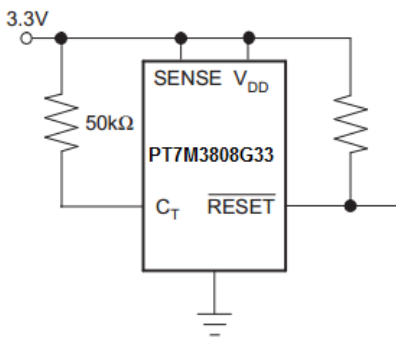
The manual reset ( $\overline{\text{MR}}$ ) input allows a processor or other logic circuits to initiate a reset. A logic low ( $0.3V_{DD}$ ) on  $\overline{\text{MR}}$  will cause  $\overline{\text{RESET}}$  to assert. After  $\overline{\text{MR}}$  returns to a logic high and SENSE is above its reset threshold,  $\overline{\text{RESET}}$  is de-asserted after the user defined reset delay expires. Note that  $\overline{\text{MR}}$  is internally tied to  $V_{DD}$  using a 90k $\Omega$  resistor so this pin can be left unconnected if  $\overline{\text{MR}}$  will not be used. Do not apply voltage level over  $V_{DD}$ .

**Selecting the RESET Delay Time**

The PT7M3808 has three options for setting the  $\overline{\text{RESET}}$  delay time.

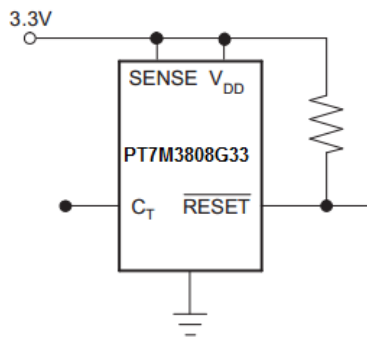
1. A fixed 300ms typical delay time by tying  $C_T$  to  $V_{DD}$  through a resistor from 40kΩ to 200kΩ. As below Figure (a) shown.
2. A fixed 20ms delay time by leaving the  $C_T$  pin open. As below Figure (b) shown.
3. A ground referenced capacitor connected to  $C_T$  for a user-defined program time between 1.25ms and 10s. The capacitor  $C_T$  should be  $\geq 100\text{pF}$  nominal value in order for the PT7M3808xxx to recognize that the capacitor is present. The capacitor value for a given delay time can be calculated using the following equation:  $C_T(\text{nF}) = [t_D(\text{s}) - 0.5 \times 10^{-3}(\text{s})] \times 175$ . As below Figure (c) shown.

The reset delay time is determined by the time it takes an on-chip precision 220nA current source to charge the external capacitor to 1.23V. When a  $\overline{\text{RESET}}$  is asserted the capacitor is discharged. When the  $\overline{\text{RESET}}$  conditions are cleared, the internal current source is enabled and begins to charge the external capacitor. When the voltage on this capacitor reaches 1.23V,  $\overline{\text{RESET}}$  is de-asserted. Note that a low leakage type capacitor such as a ceramic should be used and the stray capacitance around this pin may cause errors in the reset delay time.



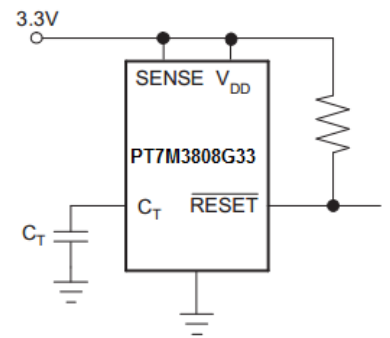
300ms Delay

**(a)**



20ms Delay

**(b)**



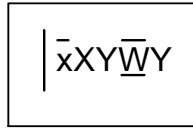
$$\text{Delay (s)} = \frac{C_T \text{ (nF)}}{175} + 0.5 \times 10^{-3} \text{ (s)}$$

**(c)**



## Part Marking

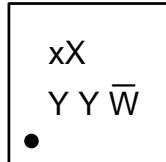
### (1) SOT23-6 (TA)



$\bar{x}X$  : Identification code  
 1<sup>st</sup> Y : Year  
 W : Date Code (Workweek)  
 2<sup>nd</sup> Y : Die Rev  
 Vertical line in front of top mark means Pin1  
 Bar about W means Cu wire

Part Number	Package Code	Package	Identification Code	Quantity
PT7M3808G01TAE	TA	SOT23-6	tG	3000
PT7M3808G09TAE	TA	SOT23-6	uU	3000
PT7M3808G12TAE	TA	SOT23-6	uV	3000
PT7M3808G125TAE	TA	SOT23-6	uW	3000
PT7M3808G15TAE	TA	SOT23-6	uX	3000
PT7M3808G18TAE	TA	SOT23-6	uY	3000
PT7M3808G19TAE	TA	SOT23-6	uZ	3000
PT7M3808G25TAE	TA	SOT23-6	wA	3000
PT7M3808G30TAE	TA	SOT23-6	wB	3000
PT7M3808G33TAE	TA	SOT23-6	tH	3000
PT7M3808G50TAE	TA	SOT23-6	wC	3000

### (2) TDFN-6 (ZC)

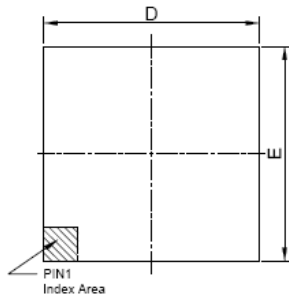


xX : Identification code  
 1<sup>st</sup> Y : Die Rev  
 2<sup>nd</sup> Y : Year  
 W : Date Code (Workweek)  
 Bar about W means Cu wire

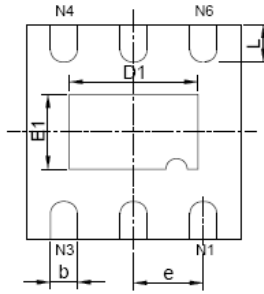
Part Number	Package Code	Package	Identification Code	Quantity
PT7M3808G01ZCE	ZC	TDFN-6	tG	3000
PT7M3808G09ZCE	ZC	TDFN-6	uU	3000
PT7M3808G12ZCE	ZC	TDFN-6	uV	3000
PT7M3808G125ZCE	ZC	TDFN-6	uW	3000
PT7M3808G15ZCE	ZC	TDFN-6	uX	3000
PT7M3808G18ZCE	ZC	TDFN-6	uY	3000
PT7M3808G19ZCE	ZC	TDFN-6	uZ	3000
PT7M3808G25ZCE	ZC	TDFN-6	wA	3000
PT7M3808G30ZCE	ZC	TDFN-6	wB	3000
PT7M3808G33ZCE	ZC	TDFN-6	tH	3000
PT7M3808G50ZCE	ZC	TDFN-6	wC	3000

**Packaging Mechanical**

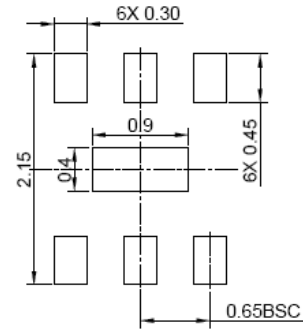
**6-TDFN (ZC)**



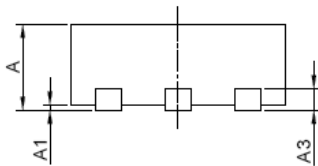
TOP VIEW



BOTTOM VIEW



RECOMMENDED LAND PATTERN(unit:mm)



SIDE VIEW

PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
D	2.00 BSC	
E	2.00 BSC	
D1	1.10	1.30
E1	0.60	0.80
b	0.20	0.30
L	0.27	0.43
e	0.65 BSC	

Note:  
1. Ref: JEDEC MO-287A



DATE: 12/09/13

DESCRIPTION: 6-Pin, TDFN, 2X2

PACKAGE CODE: ZC (ZC6)

DOCUMENT CONTROL #: PD-2178

REVISION: --

**6-SOT23 (TA)**

PKG. DIMENSIONS(MM)		
SYMBOL	Min	Max
A	-	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.30	0.50
c	0.08	0.22
D	2.75	3.05
E	1.45	1.75
E1	2.60	3.00
e	0.95 BSC	
L	0.30	0.60
θ	0°	8°

**RECOMMENDED LAND PATTERN**

0.95 0.95  
1.60 3.40  
0.90  
0.70

**Note:**  
1. Ref: JEDEC MO-178C/AB  
2. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR  
3. LAND PATTERN REFERENCE DIODES SOT23(Type-A1) PACKAGE INFORMATION

<b>DIODES</b> INCORPORATED	<b>PERICOM</b> A PRODUCT LINE OF DIODES INCORPORATED ENABLING SERIAL CONNECTIVITY	DATE: 05/17/23
DESCRIPTION: 6-Pin, Small Outline Transistor Plastic Package (SOT23)		
PACKAGE CODE: TA (TA6)		
DOCUMENT CONTROL #: PD-2145	REVISION: B	

**For latest package info.**

Please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>.

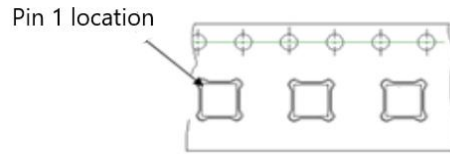
**Ordering Information**

Part Numbers	Package Code	Package Description
PT7M3808GxxxZCEX	ZC	6-pin, 2.0x2.0 (TDFN)
PT7M3808GxxxTAEX	TA	6-pin, Small Outline Transistor Plastic Package (SOT23)

**Notes:**

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- E = Pb-free and Green
- X suffix = Tape/Reel

## TDFN Pin 1 Location in Tape and Reel



## Function Comparison Table

Product	Nominal Supply Voltage	SENSE Threshold Voltage( $V_{IT}$ )
PT7M3808G01	adjustable	0.405V
PT7M3808G09	0.9V	0.84V
PT7M3808G12	1.2V	1.12V
PT7M3808G125	1.25V	1.16V
PT7M3808G15	1.5V	1.40V
PT7M3808G18	1.8V	1.67V
PT7M3808G19	1.9V	1.77V
PT7M3808G25	2.5V	2.33V
PT7M3808G30	3.0V	2.79V
PT7M3808G33	3.3V	3.07V
PT7M3808G50	5.0V	4.65V

## Mechanical Data

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per MIL-STD-202, Method 208 (e3)
- Weight: SOT23-6 0.009 grams (Approximate)  
TDFN-6 0.0075g grams (Approximate)

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