UG488: Si86SSxx EVB

The Si86SSxx-EVB evaluation board allows designers to evaluate representative members of Skyworks' family of CMOS ultra-low-power isolators, including SPI and QSPI digital isolators. These isolators are CMOS devices employing capacitive coupling technology to transmit digital information across an isolation barrier. Very high speed operation at low power levels is achieved. These products are based on Skyworks' proprietary capacitive coupling isolation technology and offer shorter propagation delays, lower power consumption, improved noise immunity, smaller installed size, and more stable operation with temperature and age versus optocouplers.

KEY FEATURES

- SPI and QSPI digital isolators
- Test setup
- Demo tests
- Schematic
- Layout
- Bill of Materials

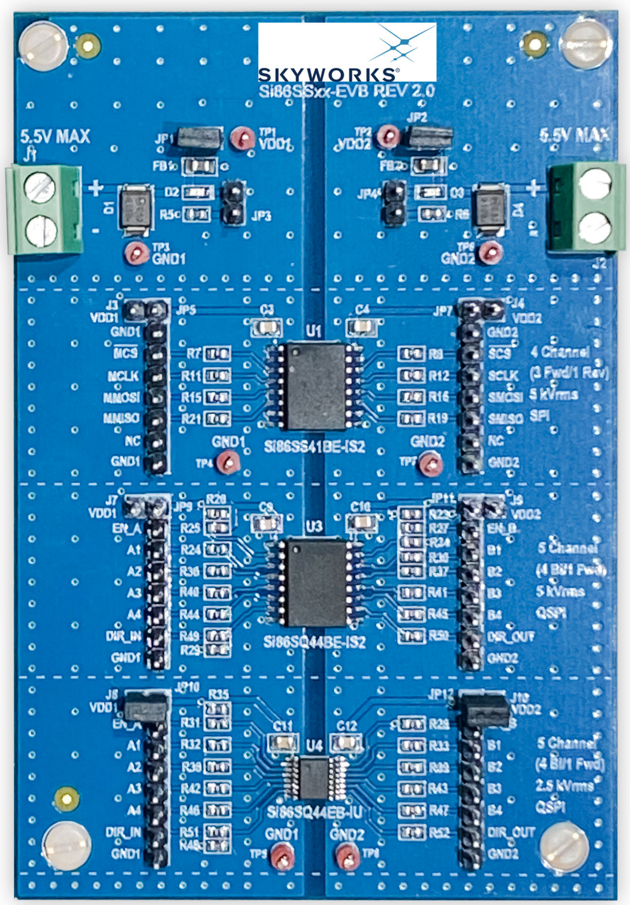

Table of Contents

1. Required Equipment

- Si86SSxx-EVB Rev 2.0
- UG488: Si86SSxx-EVB (this document)
- Two 5 V power supplies
- Two DMMs in current mode
- 0 V to +5 V signal source, up to 150 Mbps or 75 MHz capable, 50% duty cycle (the standard isolator devices can toggle at up to 150 Mbps rate; the signal source/oscillator need not be that fast.)
- Oscilloscope
- Various cables and probes

2. Test Setup

The board comes with jumpers applied to JP3 and JP4, which will allow LEDs D2 and D3 to illuminate indicating that power is active at J1 and J2.

Adjust the two power supplies to 5V out. Disable the outputs or turn them off.

Connect the power supply low outputs together. This is your system ground. This ground is common because you will use an oscilloscope with probe ground leads which are common. The two supply grounds may be separated if you have separate oscilloscopes for the left and right sides of the EVB.

Connect one power supply low output to GND1 at J1 pin 2, and the power supply high output to a DMM current input. Connect the DMM current output to VDD1 of the EVB, at J1 pin 1.

Connect the other power supply low output to GND2 at J2 pin 1, and the power supply high output to the other DMM current input. Connect the DMM current output to VDD2 of the EVB, at J2 pin 2.

Enable or turn on the power supplies. You may verify 5 V outputs at TP1 and TP2. Verify that LEDs D2 and D3 both turn on. You may remove the jumpers at JP3 and JP4 to disable the LEDs if you want to measure VDD current in the devices.

Set up the signal source with the low side to system ground, or to the input side ground depending on which side has the input being stimulated. Ground test points are provided on each side of the board for this purpose.

Each device section has headers for VDD1 and VDD2 connection to the board supply. Jumpers are provided for these headers to energize one device at a time.

2.1 Digital Isolator Considerations

The Si86SSxx-EVB evaluation board (see Figure 1) provides a means of evaluating the Si86SS41 and Si86SQ44 digital isolator devices. After power (2.5–5 V) has been supplied to the board, connect a digital input signal (5 Vpeak max, with desired clock frequency up to 150 Mbps) to the desired input channel. To view the isolated channel's data transmission, connect a scope probe to the output channel of interest. There are various inputs and outputs on either side of the board depending on the device one chooses to evaluate, as indicated by the silk screen. The board can be used to measure propagation delay, pulse-width distortion, channel-channel matching, pulse-width skew, and various other parameters.

The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the values of the on-chip series termination resistor and the channel resistance of the output driver FET. When driving loads where transmission line effects are a factor, output pins should be terminated with 50 Ω controlled impedance PCB traces.

The figure below illustrates the Si86SS41 transmitting a 500 kHz (3 Vpeak) signal through the Si86SS41. VDD1 and VDD2 were powered from 3 V. Channel 1 illustrates the input, and Channel 2 illustrates the output.

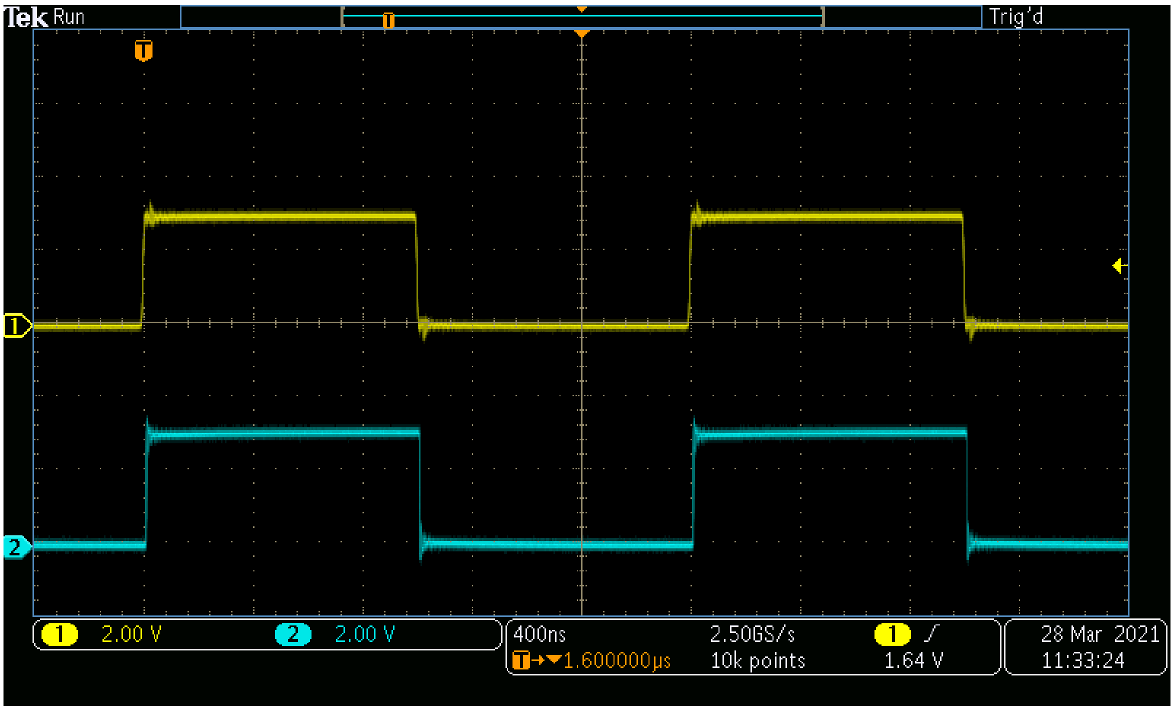

Figure 2.1. Si86SS41 Transmitting a 500 kHz (3 Vpeak) Signal through the Si86SS41

3. Si86SS41BE-IS2 (U1 Device) Setup and Demo Test

The Si86SS41 is a four-channel device with three forward channels and one reverse channel. The non-isolated or main side input pins are MCS/ (main side SPI chip select), MCLK (main side SPI clock), and MO (main side SPI MOSI). The non-isolated or main side output pin is MI (main side SPI MISO). The isolated or secondary side output pin is SCS/ (secondary side SPI chip select), SCLK (secondary side SPI clock), and SI (secondary side SPI MOSI). The isolated or secondary side input pin is SO (secondary side SPI MISO).

The MI pin is always driven by the device; there is no tristate option. In order to connect this output logically to a shared SDO bus line, the MI pin must be followed by a tristate or open drain/collector driver with an enable pin. Choose a device with an active-low enable pin; this can be driven by the MCS/ signal which will enable drive to the SDO bus line. A pull up resistor to an appropriate supply should be added to the SDO bus line somewhere along its length.

The board can be used to measure propagation delay, pulse-width distortion, channel-channel matching, pulse-width skew, and various other parameters.

Apply jumpers to J3 and J4 to connect the VDD supplies to the device. Verify an increase in VDDx current in both current meters.

Apply the signal to each device input successively, while monitoring the input and the corresponding output with oscilloscope probes. The output state should reflect the input state.

Table 3.1. U1 Channels

Input	Output
MCS/ (left side)	SCS/ (right side)
MCLK (left side)	SCLK (right side)
MO (left side)	SI (right side)
SO (right side)	MI (left side)

4. Si86SQ44BE-IS2 (U3 Device) Setup and Demo Test

The Si86SQ44BE-IS2 is a five-channel device with four bidirectional channels and one forward direction channel (DIR), in a wide body SOIC-16 package. The DIR pin when driven high configures the device for signal flow from A to B. The ISO_DIR pin provides an isolated copy of the DIR state. The DIR pin when driven low configures the device for signal flow from B to A. Each side of the device also has an enable pin (EN_A, EN_B) which when driven high enables the transmitter and receiver circuits, and when driven low configures the outputs as tristate. A 10 kΩ pull up resistor to the corresponding VDD is recommended for each enable pin.

Apply jumpers to J5 and J6 to connect the VDD supplies. Verify an increase in VDDx current in both current meters.

Apply the signal to each device input successively, while monitoring the input and the corresponding output with the oscilloscope probes. The output state should reflect the input state.

Table 4.1. U3 Channels

DIR	ENA	ENB	Input	Output	ISO_DIR
1	0	1	A1 (left side)	B1 (right side)	1
1	0	1	A2 (left side)	B2 (right side)	1
1	0	1	A3 (left side)	B3 (right side)	1
1	0	1	A4 (left side)	B4 (right side)	1
0	1	0	B1 (right side)	A1 (left side)	0
0	1	0	B2 (right side)	A2 (left side)	0
0	1	0	B3 (right side)	A3 (left side)	0
0	1	0	B4 (right side)	A4 (left side)	0

5. Si86SQ44EB-IU (U4 Device) Setup and Demo Test

The Si86SQ44EB-IU is a five-channel device with four bidirectional channels and one forward direction channel (DIR), in a QSOP-16 package. The DIR pin when driven high configures the device for signal flow from A to B. The ISO_DIR pin provides an isolated copy of the DIR state. The DIR pin when driven low configures the device for signal flow from B to A. Each side of the device also has an enable pin (EN_A, EN_B) which when driven high enables the transmitter and receiver circuits, and when driven low configures the outputs as tristate. A 10 kΩ pull up resistor to the corresponding VDD is recommended for each enable pin.

Apply jumpers to J7 and J10 to connect the VDD supplies. Verify an increase in VDDx current in both current meters.

Apply the signal to each device input successively, while monitoring the input and the corresponding output with the oscilloscope probes. The output state should reflect the input state.

Table 5.1. U4 Channels

DIR	ENA	ENB	Input	Output	ISO_DIR
1	0	1	A1 (left side)	B1 (right side)	1
1	0	1	A2 (left side)	B2 (right side)	1
1	0	1	A3 (left side)	B3 (right side)	1
1	0	1	A4 (left side)	B4 (right side)	1
0	1	0	B1 (right side)	A1 (left side)	0
0	1	0	B2 (right side)	A2 (left side)	0
0	1	0	B3 (right side)	A3 (left side)	0
0	1	0	B4 (right side)	A4 (left side)	0

6. Additional Board Features

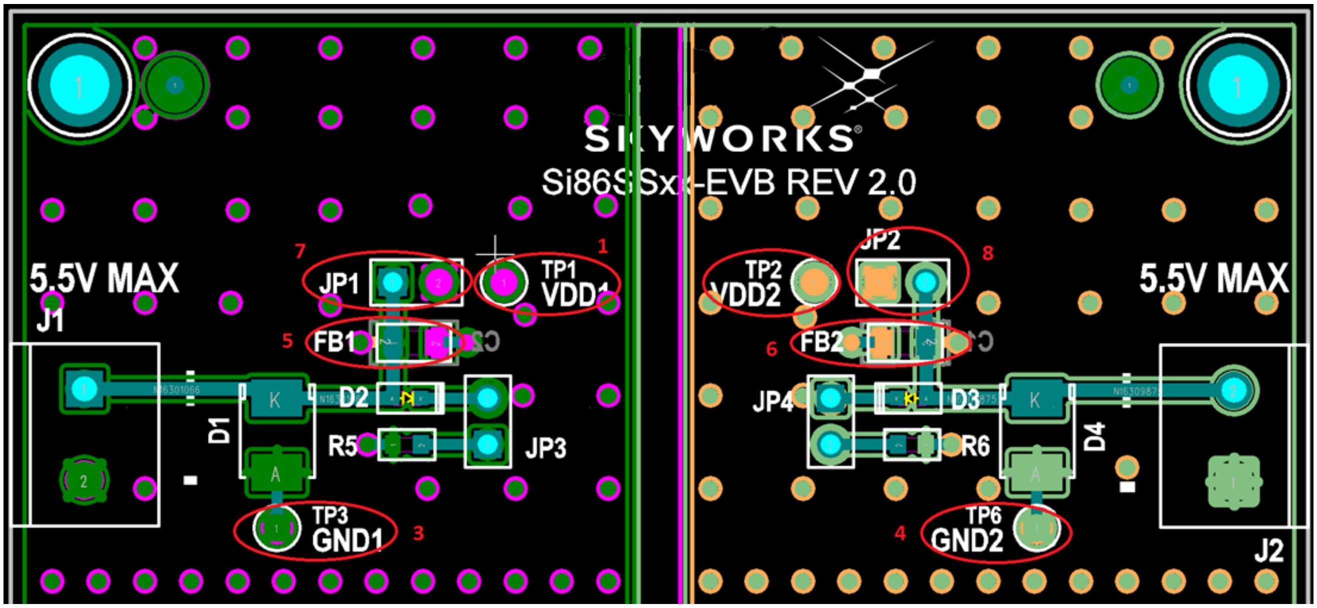

Figure 6.1. Board Features (Top End of Board)

1. **VDD Attachments:** If you prefer to attach VDD on either side using clip leads instead of stripped wires, you may use the test point, such as TP1 (1) for VDD1, TP3 (3) for GND1, TP2 (2) for VDD2, TP6 (4) for GND2. The indicator LEDs will still illuminate.
2. **Ferrite Beads:** Each VDD path at the top of the board contains a ferrite bead (5, 6). This may be shorted out with a jumper (7, 8), for instance at JP1. Alternatively, the ferrite bead may be replaced with a current sensing resistor, and its voltage measured across the header. A third use of the header would be to remove the ferrite bead and use the jumper to route the supply through a current meter and back to the board.
3. **Pin Series Resistors:** Each signal pin has a 0 Ω resistor in series. These may be replaced by a different value to limit input current or to provide termination.

7. Bill of Materials

Table 7.1. Si86SSxx-EVB Bill of Materials

Qty	Ref	Value	Rating	Voltage	Tol	Type	PCB Footprint	Mfr	Mfr PN
2	C1, C2	10 µF		10 V	±10%	X7R	C1206	Venkel	C1206X7R100-106K
6	C3, C4,C9, C10, C11,C12	0.1 µF		16 V	±10%	X7R	C0805	Venkel	C0805X7R160-104K
2	D1, D4	5.6 V	3 W	5.6 V	5%	Zener	DO-214AA	On Semi	1SMB5919BT3
2	D2, D3	Red					LED0603-KA	Lite-On Technology Corp	LTST-C190KRKT
2	FB1,FB2	600 Ω	200 mA			SMT	L0805	Murata	BLM21AG601SN1
4	JP1, JP2, JP3, JP4	Header 1x2				Header	CONN1X2	Samtec	TSW-102-07-T-S
6	JP5, JP7, JP9, JP10, JP11, JP12	Header 1x8				Header	CONN-1X8	Samtec	TSW-108-07-T-S
6	JS1, JS2, JS3, JS4, JS5, JS6	Jumper Shunt				Shunt	N/A	Samtec	SNT-100-BK-T
2	J1, J2	Connector TRBLK 2				Term Black	CONN-1X2-TB	Phoenix Contact	1729018
6	J3, J4, J7, J8, J9, J10	Header 1x1				Header	HDR1X1	Samtec	TSW-101-07-T-S
4	MH1, MH2, MH3, MH4	Apr-40				Screw	MH-125NP	Richco Plastic Co.	NSS-4-4-01
1	PCB1	Si86SSxx-EVB Rev 2.0				Bare PCB	N/A	Skyworks Solutions, Inc.	Si86SSxx-EVB REV 2.0
8	R5, R6, R23, R25, R29, R34, R35, R48	10 kΩ	1/10 W		±1%	Thick Film	R0603	Venkel	CR0603-10W-1002F
32	R7, R8, R11, R12, R15, R16, R19, R21, R24, R26, R27, R28, R30, R31, R32, R33, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46, R47, R49, R50, R51, R52	0 Ω	1 A			Thick Film	R0603	Venkel	CR0603-16W-000
4	SO1, SO2, SO3, SO4	Standoff				Stand-off		Keystone Electronics	1902D
8	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8	Red				Loop	Testpoint	Kobiconn	151-207-RC
1	U1	Si86SS41BE-IS2	5 kVrms			Isolator	SO16N10.3P1.27	Skyworks Solutions, Inc.	Si86SS41BE-IS2

Qty	Ref	Value	Rating	Voltage	Tol	Type	PCB Footprint	Mfr	Mfr PN
1	U3	Si86SQ44BE-IS2	5 kVrms			Isolator	SO16N10.3P1.27	Skyworks Solutions, Inc.	Si86SQ44BE-IS2
1	U4	Si86SQ44EB-IU	2.5 kVrms			Isolator	QSOP16N6.0P0.635	Skyworks Solutions, Inc.	Si86SQ44EB-IU
Not Installed Components									
3	C7, C13, C14	1000 pF	X2/Y3	250 V	±10%	Y3	C1808	Yageo	SC1808KKX7RTBB102

8. Ordering Guide

Table 8.1. Ordering Guide

Ordering Part Number (OPN)	Description
Si86SSxx-KIT	Si86SSxx Digital Isolator Evaluation Board Kit

9. Schematics

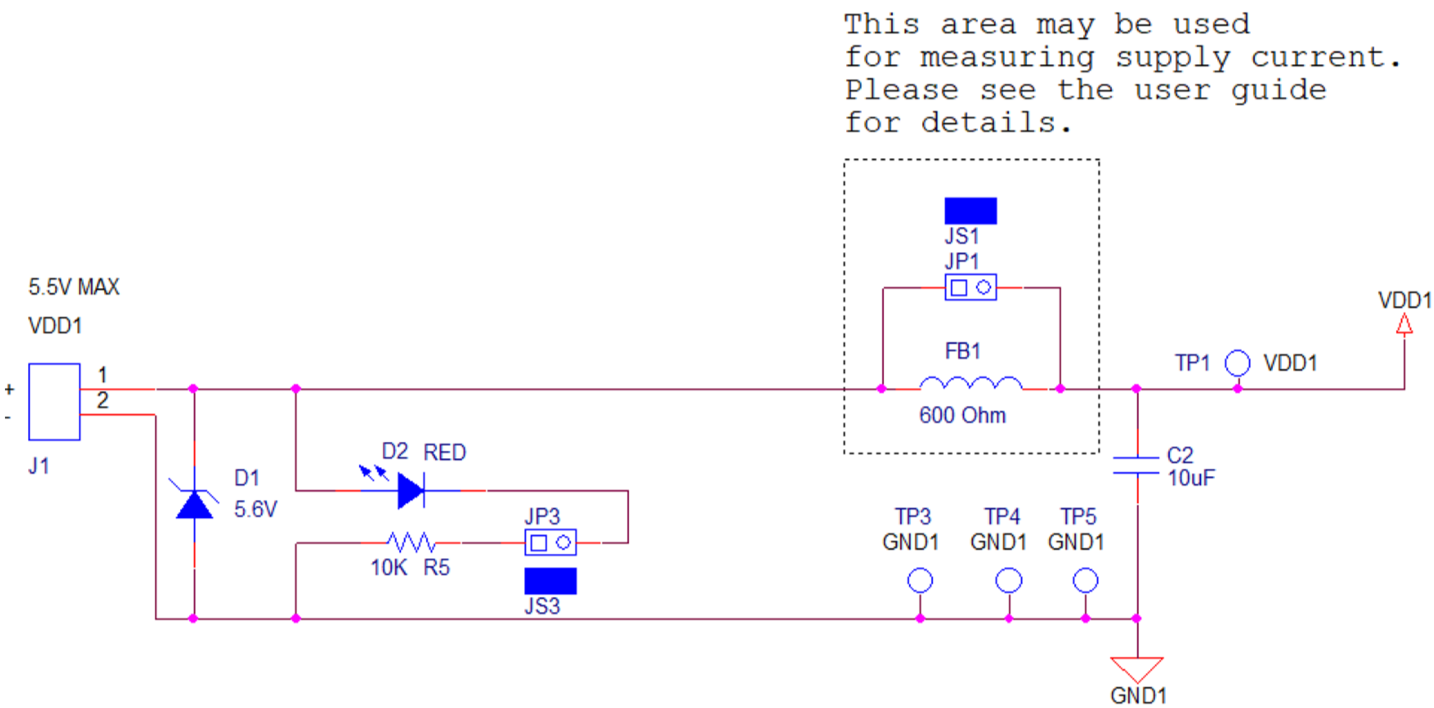

Figure 9.1. VDD1 Connection

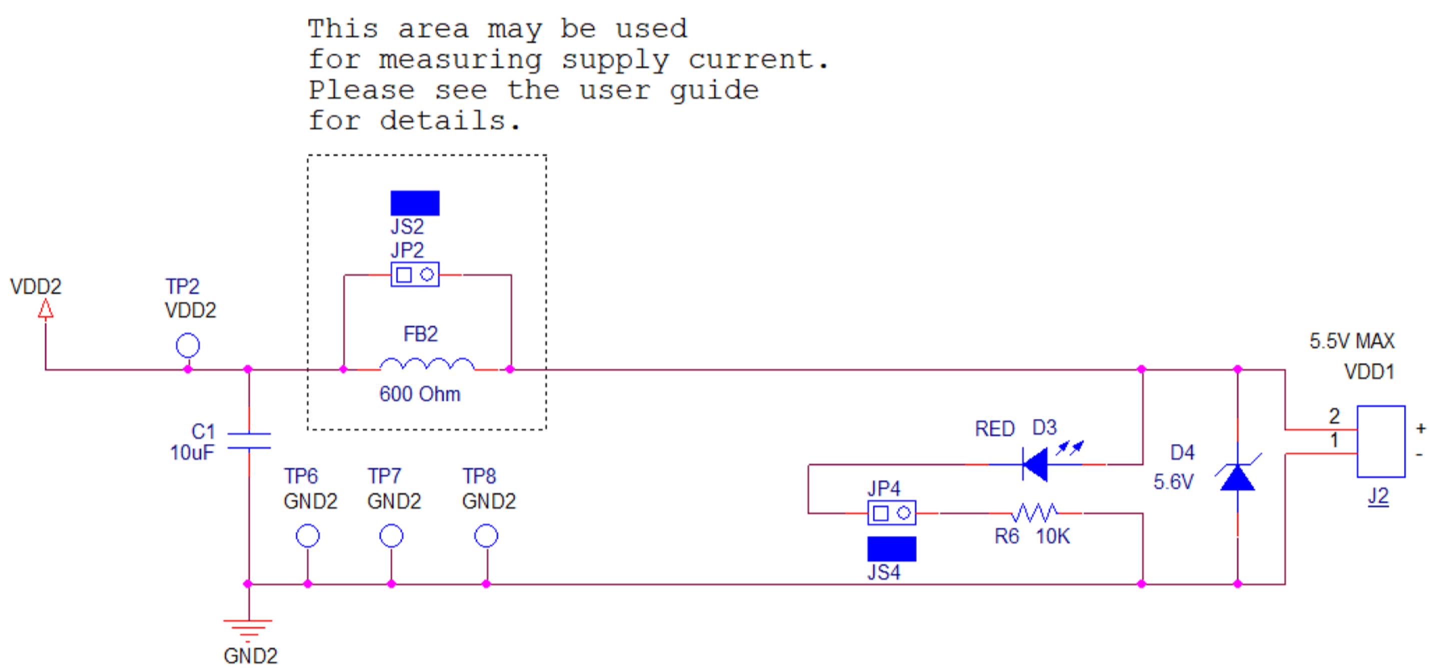

Figure 9.2. VDD2 Connection

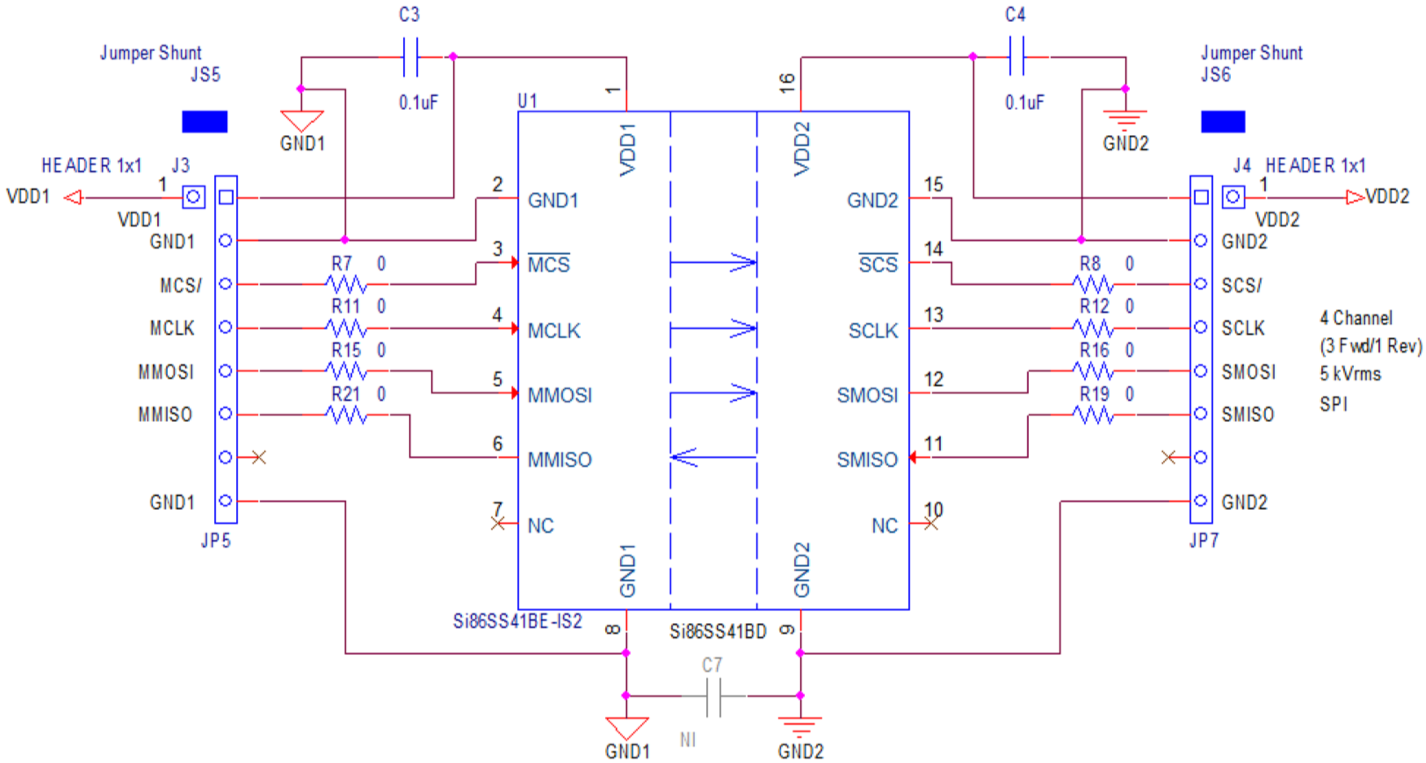

Figure 9.3. U1 Circuit

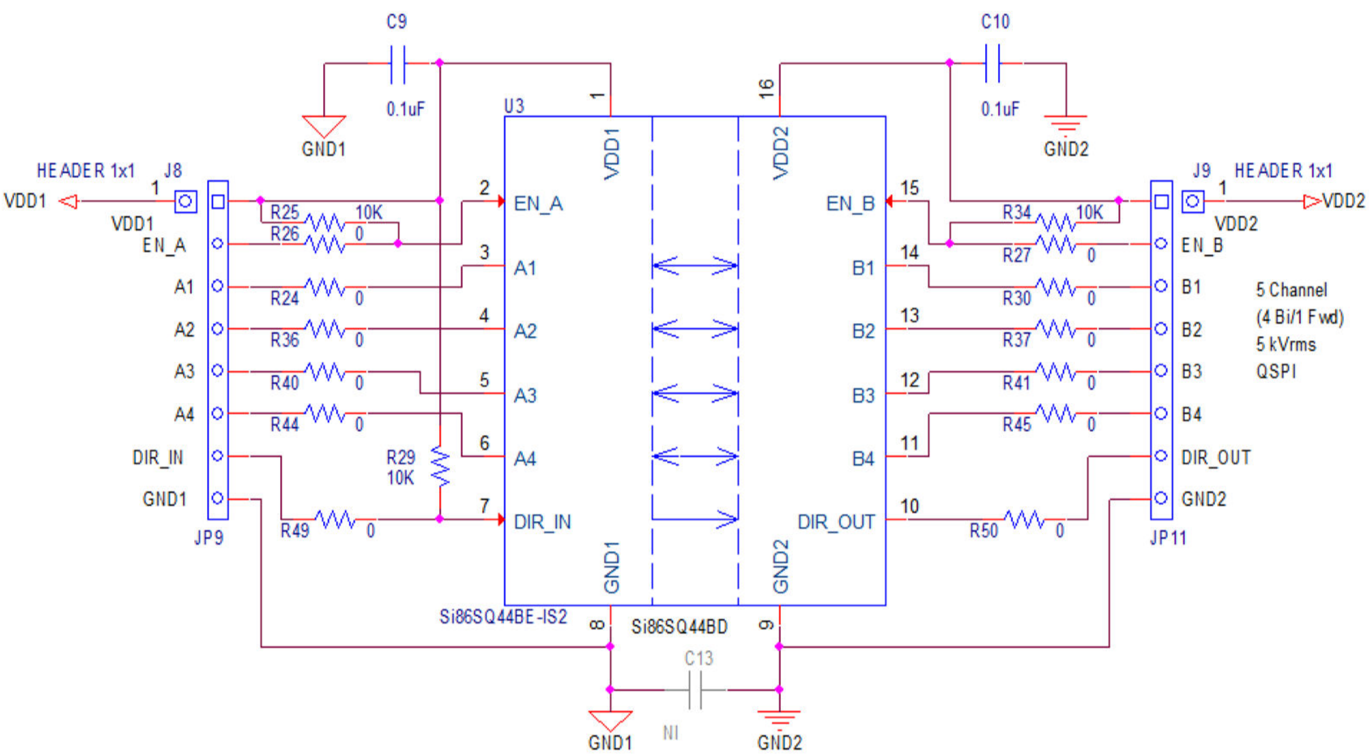

Figure 9.4. U3 Circuit

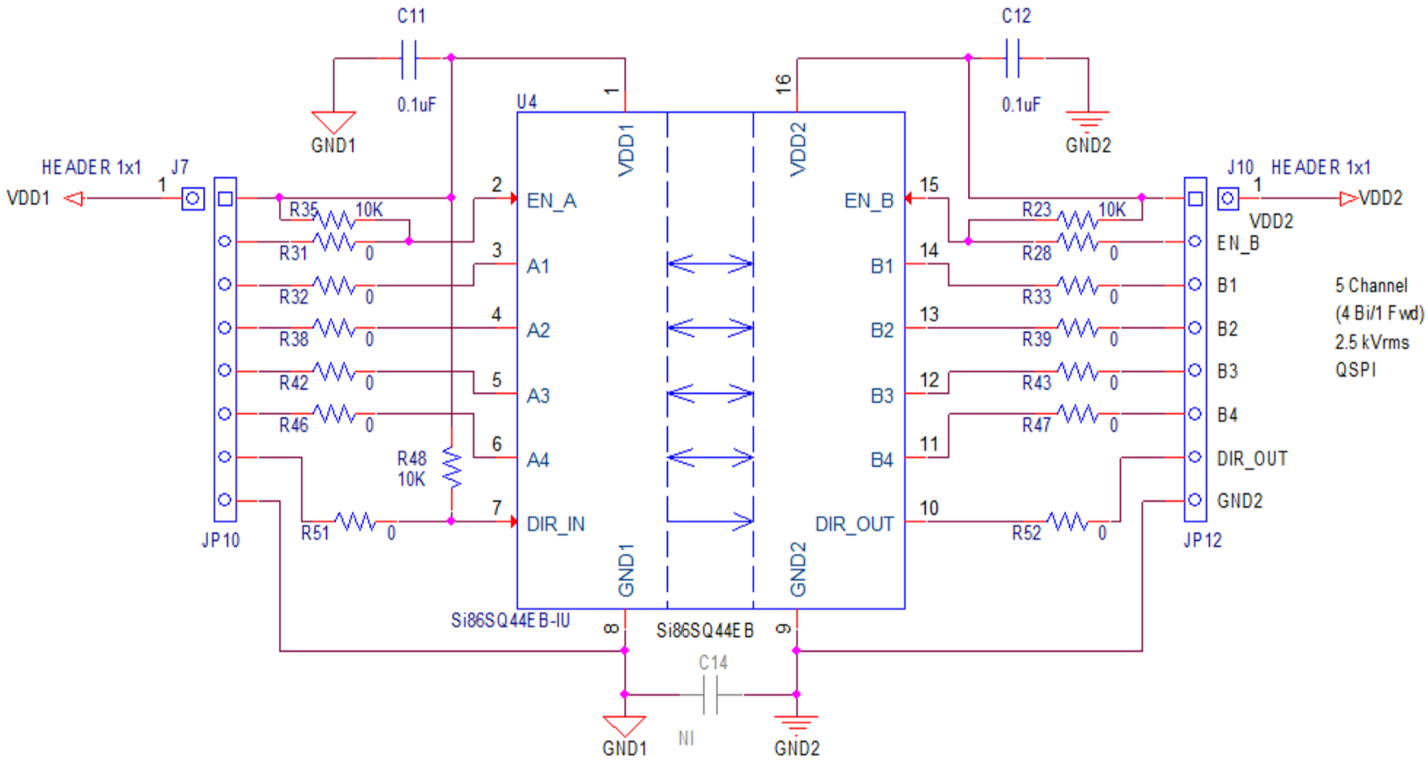

Figure 9.5. U4 Circuit

10. Layout

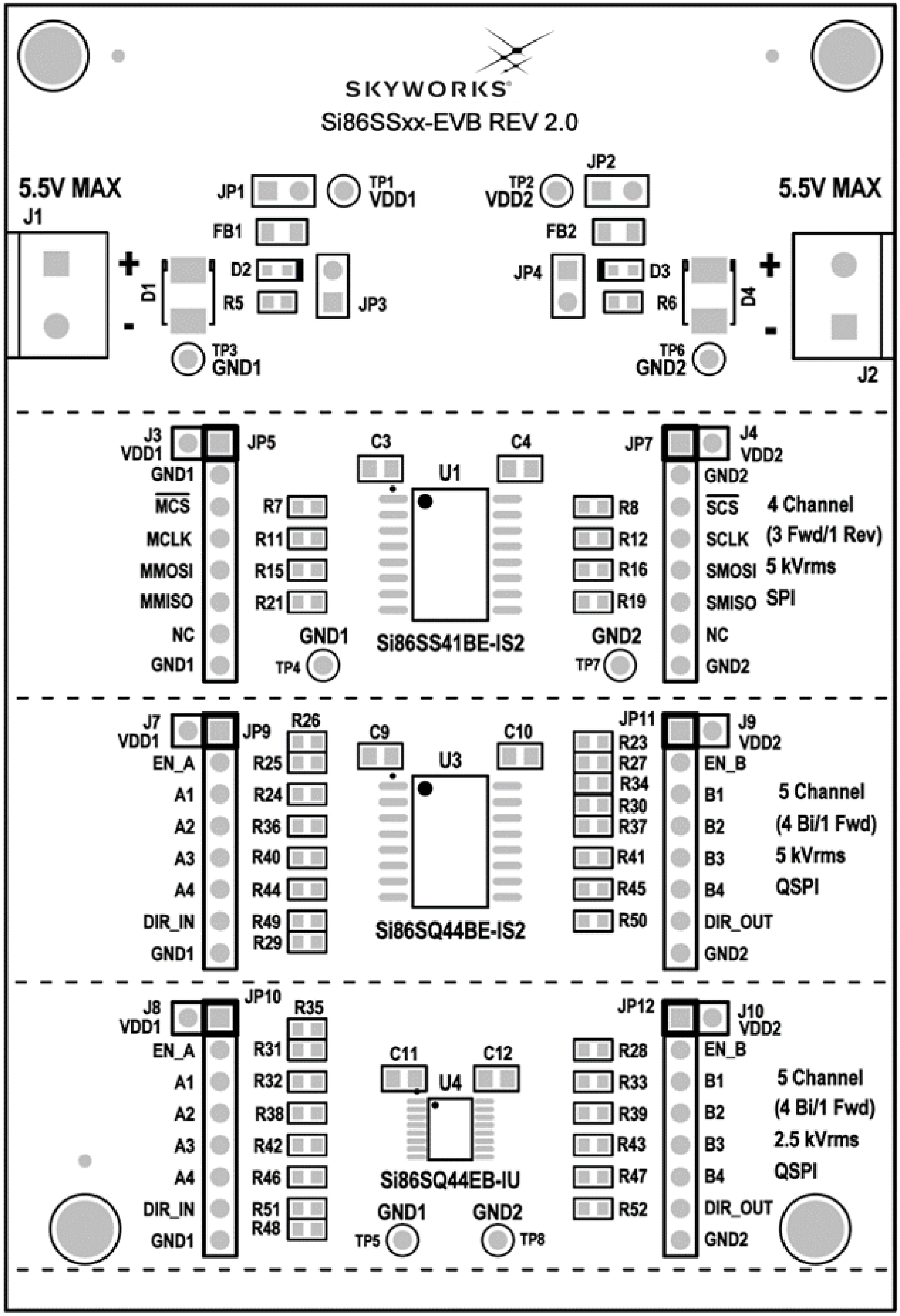

Figure 10.1. Primary Silkscreen

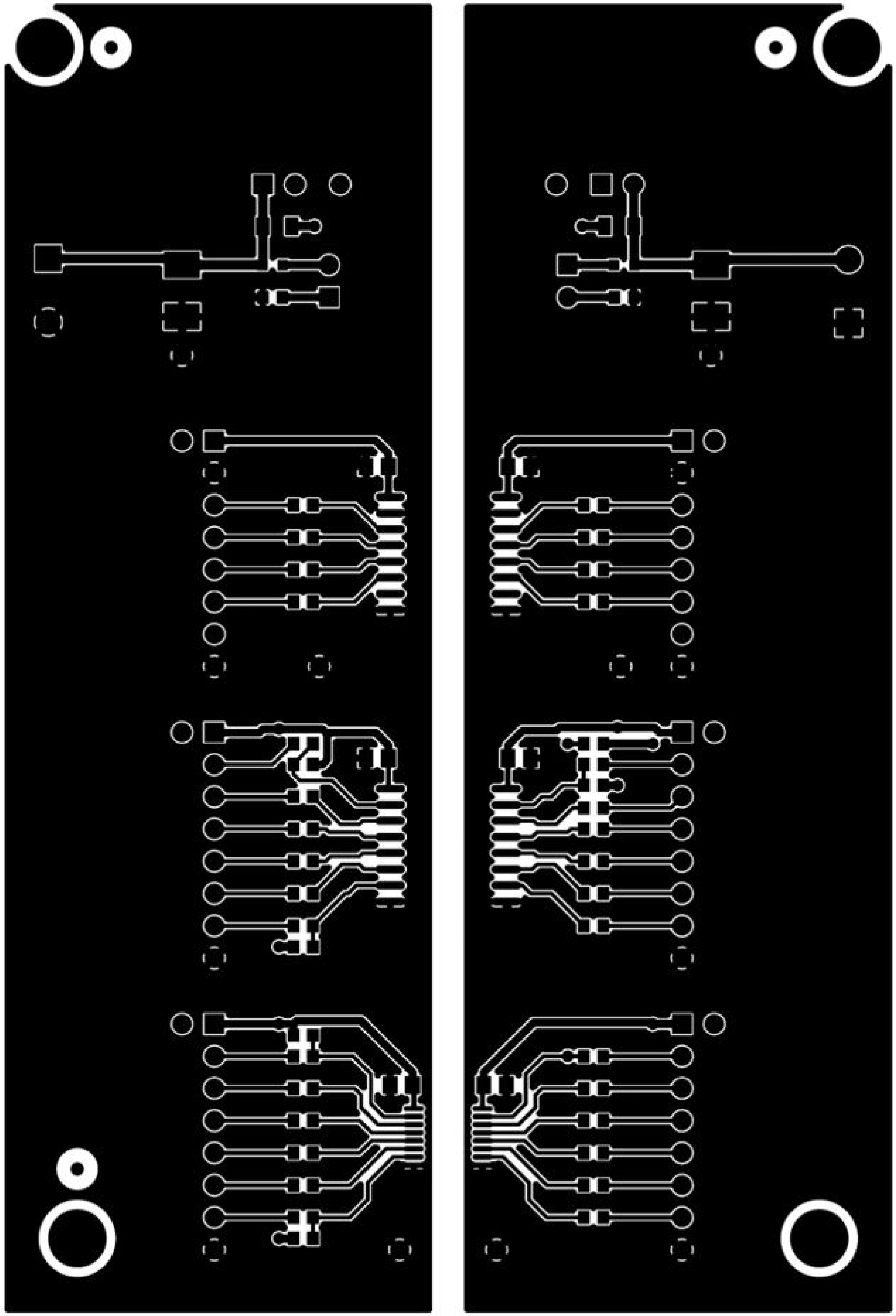

Figure 10.2. Top Interconnect Layer

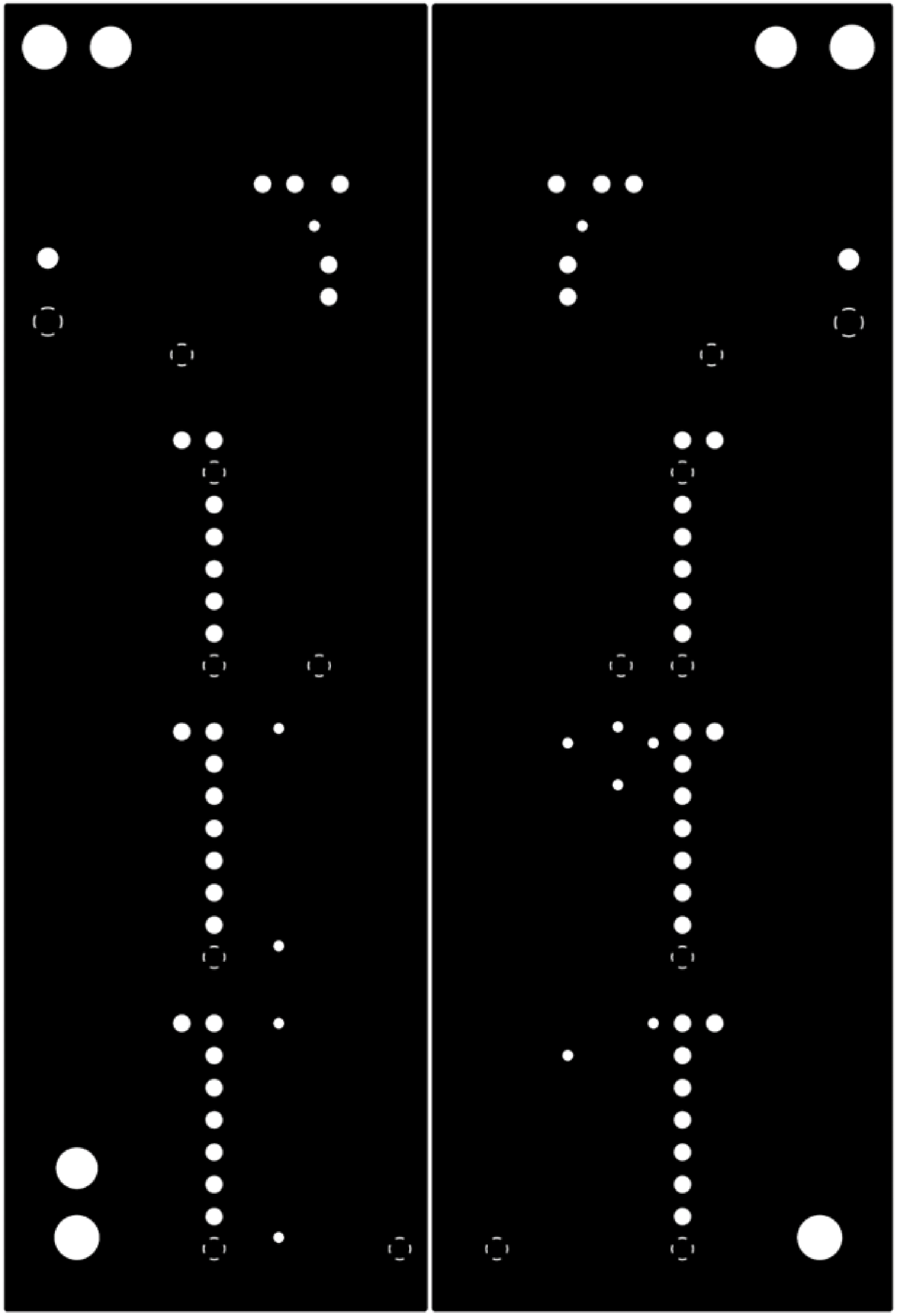

Figure 10.3. Ground Layer (2nd)

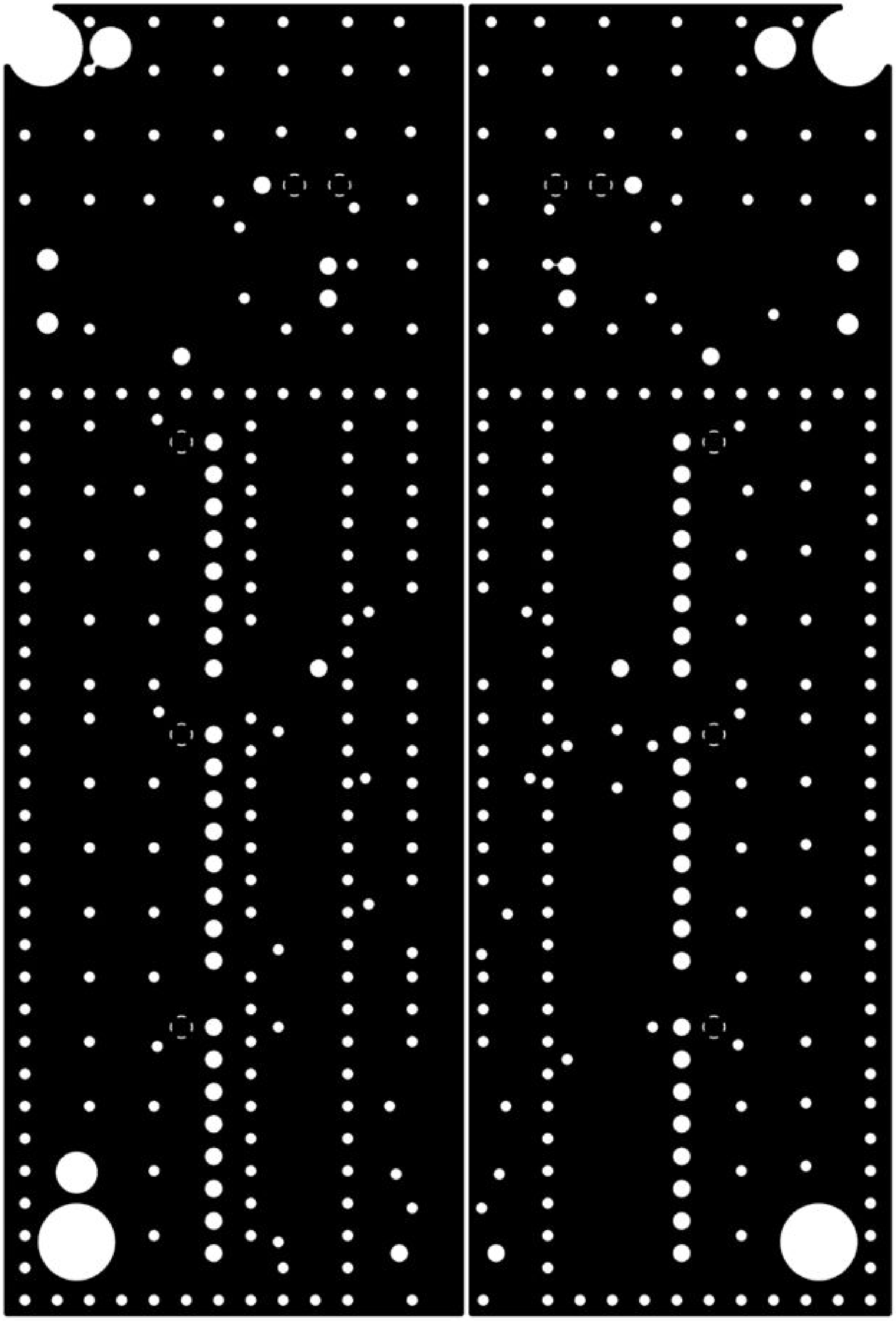

Figure 10.4. Power Layer (3rd)

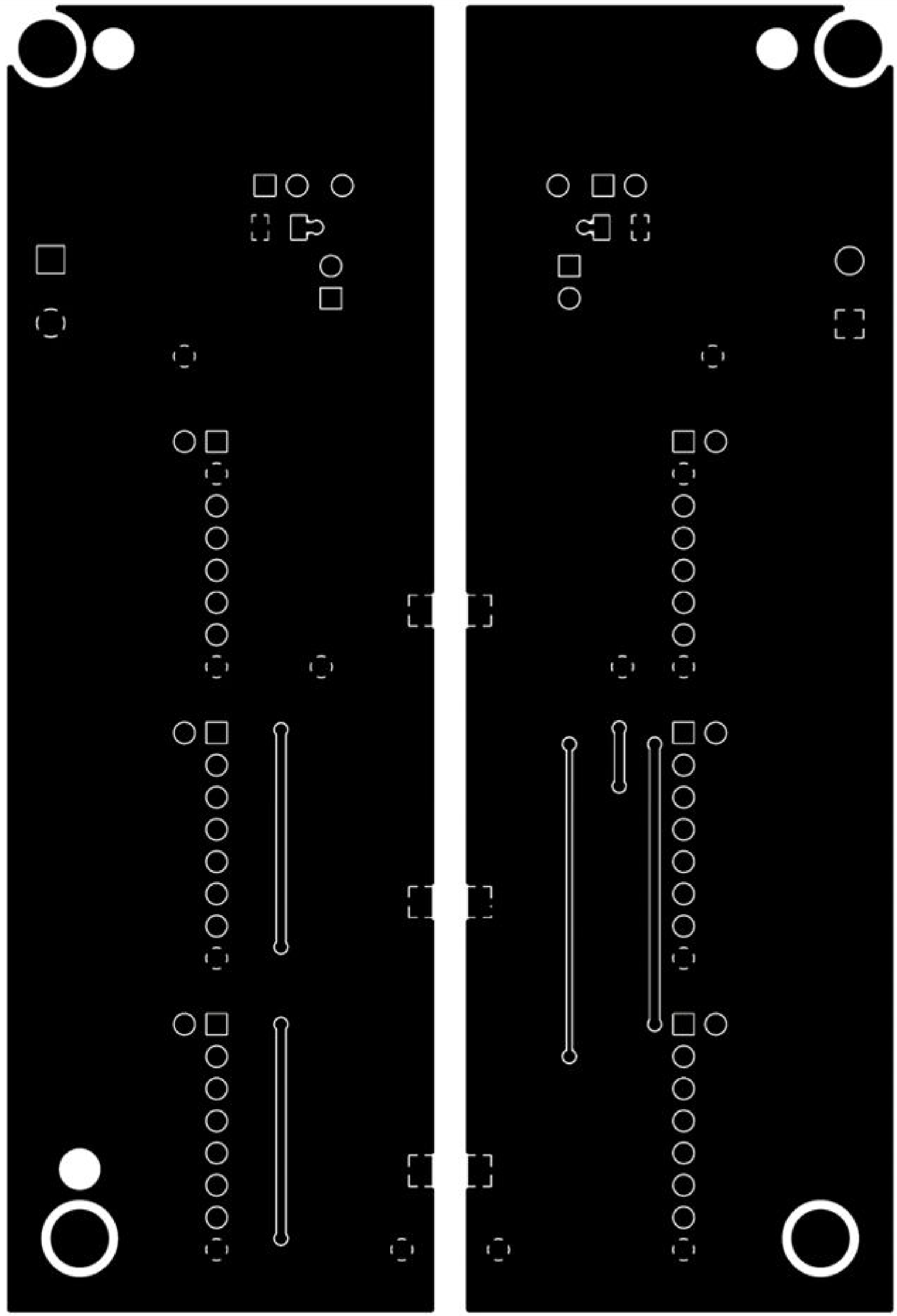

Figure 10.5. Bottom Side Interconnect

SKYWORKS®

Connecting Everyone

and Everything,

All the Time

Portfolio
skyworksinc.com

Quality
skyworksinc.com/quality

Support & Resources
skyworksinc.com/support

Skyworks Solutions, Inc. | Nasdaq: SWKS | sales@skyworksinc.com | www.skyworksinc.com
USA: 781-376-3000 | Asia: 886-2-2735 0399 | Europe: 33 (0)1 43548540