BMR510

2-phase integrated power stage up to 140 A peak

The BMR510 is a two-phase integrated power stage with a continuous output current of 80A, and a peak current of 140 A.

It comes in a compact footprint of just 0.9 cm^2 / 0.14 in^2 and is available with either LGA or solder bump termination.

The device is designed with the power stages located on top for the most effective top-side conducted cooling, and delivers excellent thermal results.

The BMR510 features protection mechanisms such as over-current protection and over-temperature protection. An enable input is provided, and the module accepts tri-state PWM inputs.

Key features

- High efficiency up to 92% at light load, 87.5% at full load.
- Paralleling with other units
- Remote control
- Reporting temperature and current for each phase
- Excellent thermal performance
- Halogen-free

Soldering methods

- Reflow soldering, LGA and solder bump options

Key electrical information

Parameter	Values
Input voltage range	4.5 - 15 V
Output voltage range	0.5 - 1.3 V
Max output current	80 A TDC/ 140 A peak

Mechanical

10 x 9 x 7.63 mm / 0.4 x 0.35 x 0.3 in

Application areas

- Designed for AI applications
- Used by CPU, GPUs, IPUs, high-performance ASICSs

Product options

The table below describes the different product options.

	BMR510	1	03	4	/002	C	Definitions
Product family	BMR510						
Mounting options		1					0 = solder bump 1 = LGA
Product variants			03				03 = standard electrical variant
Mechanical configuration				4			4 = standard mechanical configuration
Configuration code					/002		/002 = 2 phases
Packaging options						C	C = Antistaic tape and reel packaging

For more information, please refer to Part 2 Mechanical information.

If you do not find the variant you are looking for, please contact us at Flex Power Modules .

Order number examples

Part number	V_{in}	outputs	configuration
BMR5101034/001C	4.5-15 V	0.5-1.3 V	Standard 2 phases module, tape and reel package

Part 1: Electrical specifications

Absolute maximum ratings

Stress in excess of our defined *absolute maximum ratings* may cause permanent damage to the converter. Absolute maximum ratings, also referred to as *non-destructive limits,* are normally tested with one parameter at a time exceeding the limits in the electrical specification.

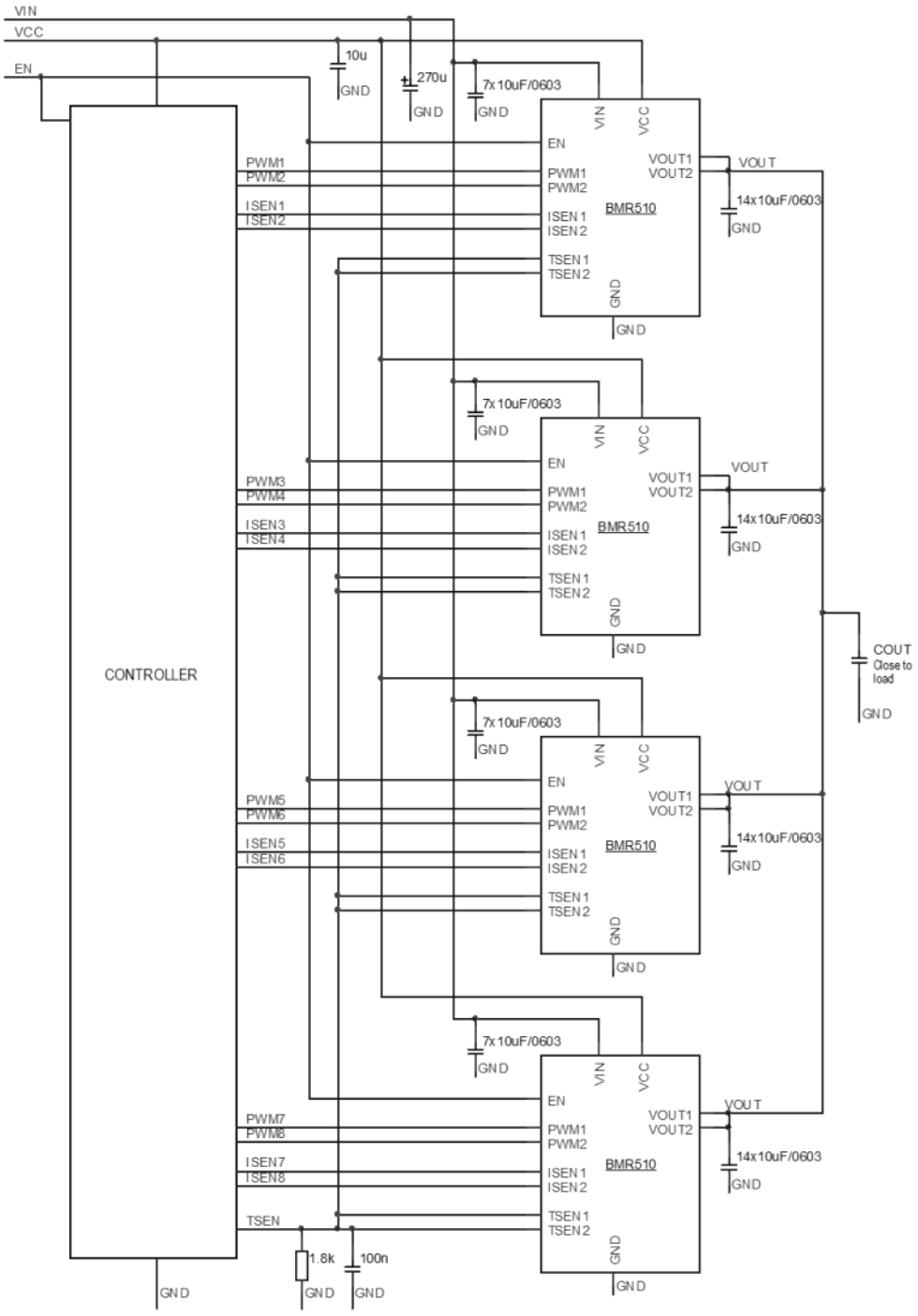
Characteristics		min	typ	max	Unit
Operating temperature (T_{P1})		-40		125	°C
Storage temperature		-40		125	°C
Input voltage (V_{in})		-0.3		20	V
Signal I/O voltage	EN, PWM,ISEN, TSEN	-0.3		VCC+0.3	V
Driver and logic supply	VCC	-0.3	3.3	4	V

Reliability

Failure rate (λ) and mean time (50%) between failures (MTBF= 1/ λ) are calculated based on *Telcordia SR-332 Issue 4: Method 1, Case 3, (80% of I_{out}, T_{P1}=40°C).*

	Mean	90% confidence level	Unit
Steady-state failure rate (λ)	13		nfailures/h
Standard deviation (σ)	5.3		nfailures/h
MTBF	76.3	50.3	MHr

Typical application diagram



Typical application circuit for 8 phases rail

Notes:

1. Value of output capacitance will depend on the application and load transient requirements.
2. TSEN filter values might be adjusted if connecting together TSEN of more than 16 phases.

Electrical specifications for BMR510 — Control and Monitoring

T_{P1} = -40 °C to 125 °C, VI = 12 V, VCC = VEN = 3.3 V, unless otherwise specified under Conditions.

Typical values given at: T_{P1} = +25 °C, unless otherwise specified under Conditions.

Characteristics		Conditions	min	typ	max	Unit
$UVLO_{VIN}$	VIN Under Voltage Lock-Out	Rising threshold		2.5	3.0	V
		Hysteresis		200		mV
$UVLO_{VCC}$	VCC Under Voltage Lock-Out	Rising threshold		2.75	2.95	V
		Hysteresis		200		mV
V_{IL_EN}	EN input low threshold				0.9	V
V_{IH_EN}	EN input high threshold		1.4			V
V_{IL_PWM}	PWM input low threshold				0.6	V
V_{IH_PWM}	PWM input high threshold		2.6			V
V_{TRI_PWM}	PWM tri-state region		1.1		2.1	V
V_{HiZ_PWM}	PWM high impedance voltage			1.6		V
I_{PWM}	PWM sink/source current	PWM = 0 V		500		µA
		PWM = 3.3 V		-500		µA
t_{PWM}	PWM minimum pulse width			15		ns
V_{O_TSEN}	TSEN voltage when fault		3.0	3.3		V
G_{TSEN}	TSEN gain			8		mV/°C
O_{TSEN}	TSEN offset	T_J = +25 °C		800		mV
T_{TSEN}	TSEN overtemperature shutdown and fault flag			160		°C
G_{ISEN}	ISEN gain			5		µA/A
		Accuracy	-2	0	2	%
O_{ISEN}	ISEN offset	I_O = 0 A, V_{ISEN} = 1.2 V T_J = +25 °C	-4	0	4	µA
V_{ISEN}	ISEN voltage range		0.7		2.1	V
I_{LIM_H}	High-side current limit	Threshold, cycle-by-cycle		120		A
		Shutdown counter		10		Times
I_{LIM_L}	Low-side current limit	Threshold, cycle-by-cycle No fault report		-50		A
		Off time		200		ns

Electrical specifications for BMR510 – Power Conversion

T_{P1} = -10 °C to 95 °C, V_I = 4.5 to 15 V, V_{CC} = 3.3 V, unless otherwise specified under Conditions.

Typical values given at: T_{P1} = +25 °C, V_I = 13.5 V, V_O = 0.8 V, I_O = 80 A, f_{sw} = 550 kHz, 2-phase single rail operation, otherwise specified under Conditions.
Measurements made on Reference board ROA 170 314.
External C_{IN} = 1 x 270 µF/22 mΩ OSCON + 28 x 10 µF ceramic.
External C_{OUT} = 10 x 470 µF/3 mΩ POSCAP + 356 x 10 µF ceramic.

Characteristics		Conditions	min	typ	max	Unit
V_I	Input supply	Continuous operation	4.5		15	V
		Peak			16	V
V_{CC}	Driver and logic supply		3.0	3.3	3.6	V
V_O	Output voltage range		0.5		1.3	V
V_{Oac}	Output ripple & noise	20 MHz BW		2		mVp-p
f_{sw}	Switching frequency	T_{P1} = +25 °C	500	550	600	kHz
C_I	Internal input capacitance	V_I = 0 V		33		µF
C_O	Internal output capacitance	V_O = 0 V		0		µF
L_O	Output inductance	I_O = 0 A		90		nH
I_O	Output current, peak	2-phase operation			140	A
		1-phase operation			70	A
	Output current, continuous, Note 2	2-phase operation	0	80		A
		1-phase operation	0	40		A
I_{IN}	VIN input current	Standby, EN = low		10		µA
I_{VCC}	VCC input current	1-phase operation I_O = 40 A		38		mA
		2-phase operation I_O = 80 A		71		mA
		Standby, PWM1 = PWM2 = low		3		mA

Note 1: Exclude V_{CC} losses.

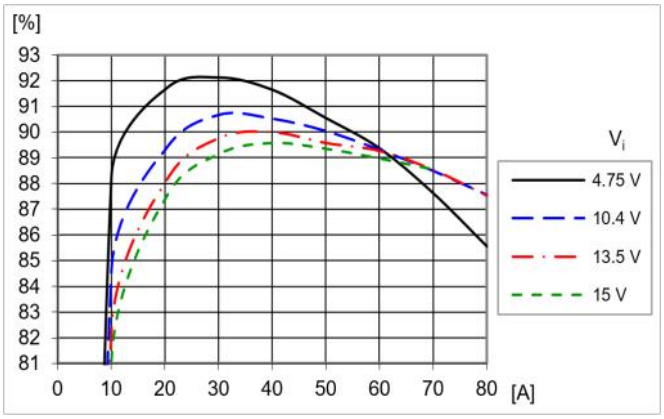
Note 2: The maximum continuous output current will also be limited by the thermal conditions.

See derating graphs and section Thermal Considerations.

Electrical graphs for BMR510

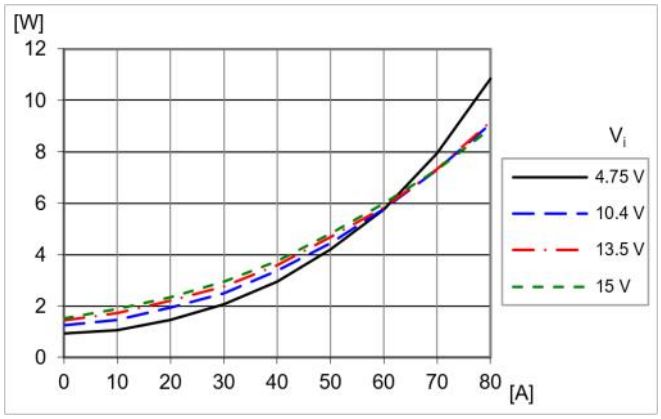
V_{out} = 0.8 V

Efficiency



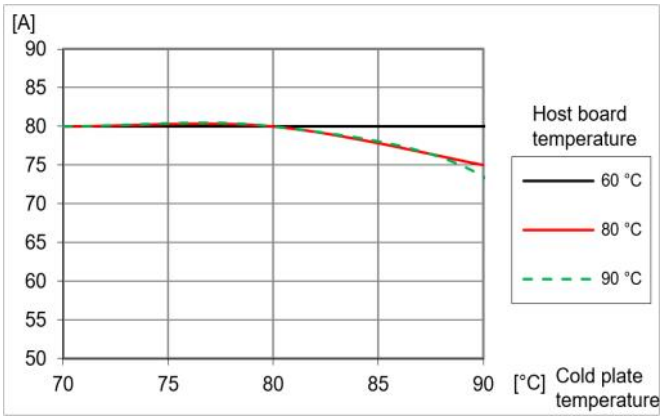
Driver losses excluded, 2 phases, fsw=550KHz

Power dissipation



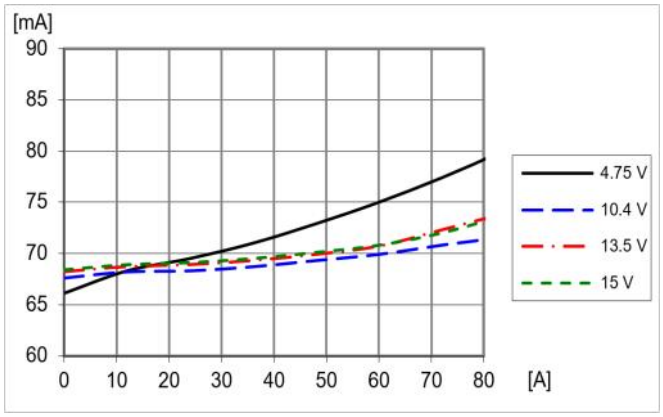
Driver losses excluded, 2 phases, fsw= 550KHz

Output Current Derating

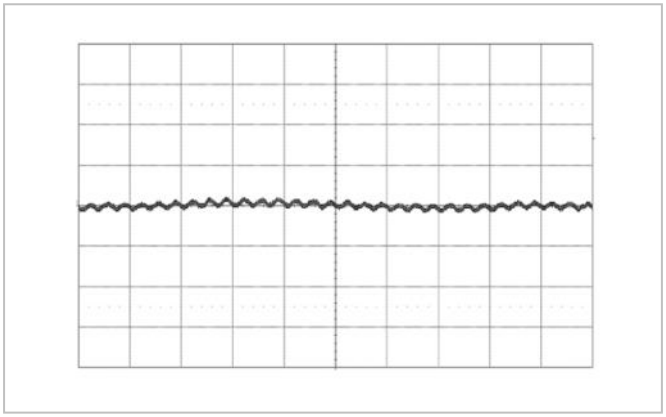


Thermal interface gap pad 0.5 mm, 3.5 W/mK. V_I= 13.5 V.

VCC input current



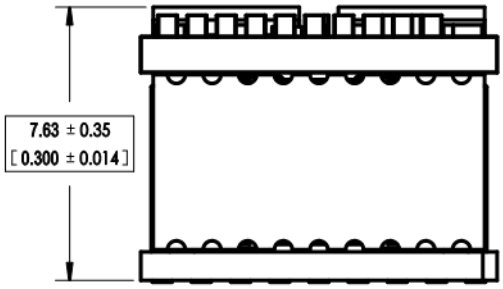
Output ripple



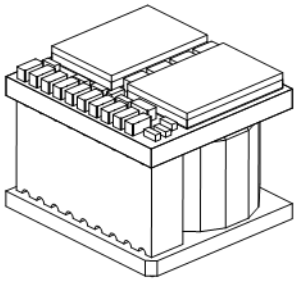
V_I = 13.5 V, I_O = 80 A, Scale: 5 mV/div, 1.5 µs/div, 20 MHz BW. C_{OUT} = 10 x 470 µF/3 mΩ POSCAP + 365 x 10 µF ceramic.

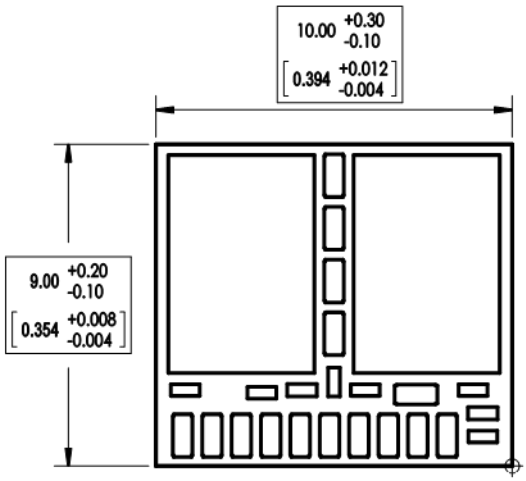
Part 2: Mechanical information

BMR510: Surface Mount Version

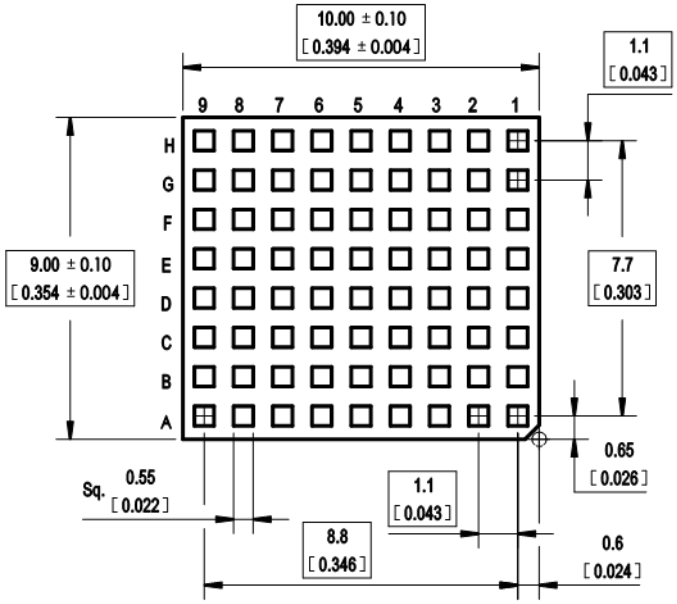


TOP VIEW
Product overall X/Y dimension including both top and bottom boards



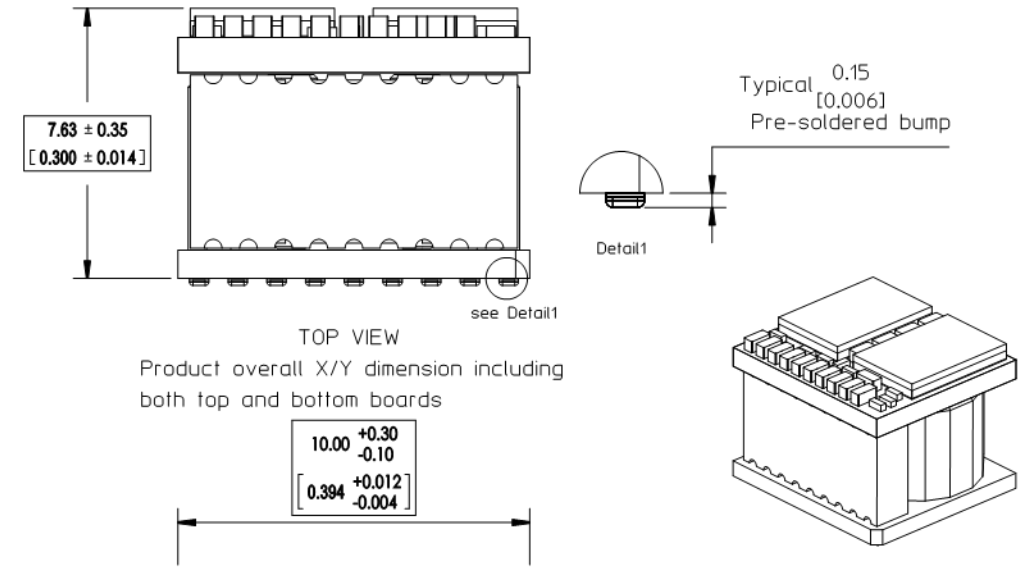


Pin layout and footprint top view through the product
Tolerances applicated for the bottom card

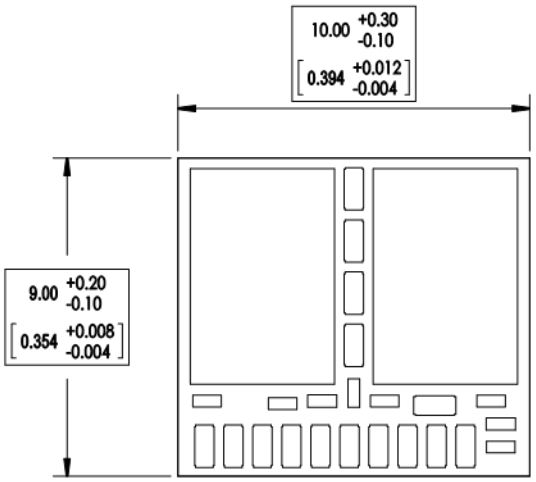


Weight: typical 2.2 g
All dimensions in mm [inches]
Tolerances unless specified:
x.x ±0.5 mm [0.02 inch]
x.xx ±0.25 mm [0.01 inch]
(not applied on footprint or typical values)

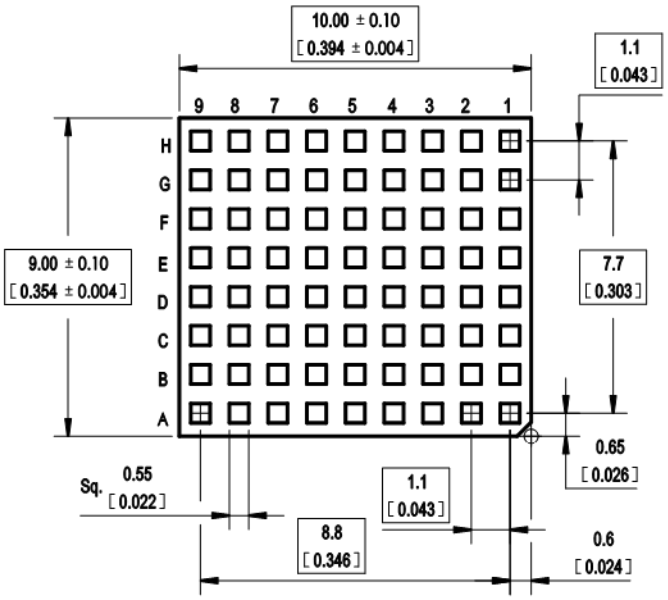
BMR510: Surface Mount Version with solder bumps



TOP VIEW
Product overall X/Y dimension including both top and bottom boards



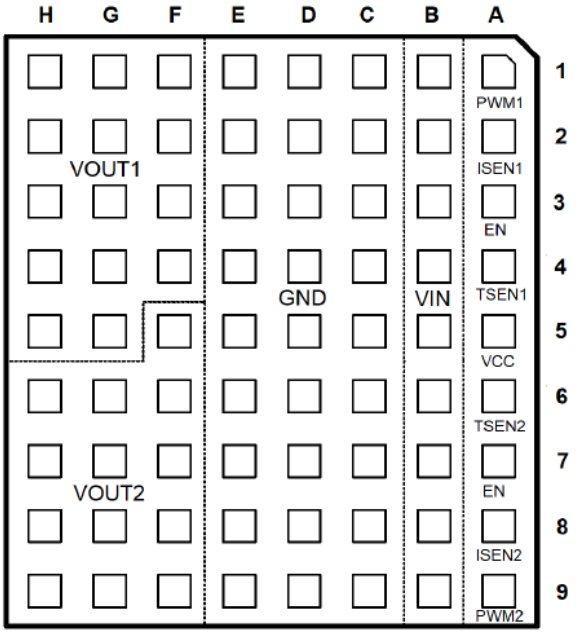
Pin layout and footprint top view through the product
Tolerances applicated for the bottom card



Notes:
Product height: Product height indicate module after soldered
Material: Solder bumps SAC305

Weight: typical 2.2 g
All dimensions in mm [inches]
Tolerances unless specified:
x.x ±0.5 mm [0.02 inch]
x.xx ±0.25 mm [0.01 inch]
(not applied on footprint or typical values)

Connections



Pin layout, top view

Pin	Designation	Type	Function
A1	PWM1	Input	Pulse-width modulation input, phase 1. The PWM1 signal shall be 180° phase shifted compared to the PWM2 signal.
A2	ISEN1	Output	Current sense output , phase 1. Use external resistor to adjust the voltage proportional to the inductor current .
A3, A7	EN	Input	Active high enable input, common for phase 1 and 2.
A4	TSEN1	Output	Temperature sense and fault reporting, phase 1.
A5	VCC	Input	Driver and internal circuitry supply. Connect to +3.3 V.
A6	TSEN2	Output	Temperature sense and fault reporting, phase 2.
A8	ISEN2	Output	Current sense output, phase 2. Use external resistor to adjust the voltage proportional to the inductor current.
A9	PWM2	Input	Pulse-width modulation input, phase 2. The PWM2 signal shall be 180° phase shifted compared to the PWM1 signal.
B1-B9	VIN	Power	Input voltage.
C1-C9, D1-D9 E1-E9	GND	Power	Power ground and digital ground.
F1-F4, G1-G5 H1-H5	VOUT1	Power	Output voltage, phase 1.
F5-F9, G6-G9 H6-H9	VOUT2	Power	Output voltage, phase 2.

Part 3: Thermal considerations

Thermal Consideration

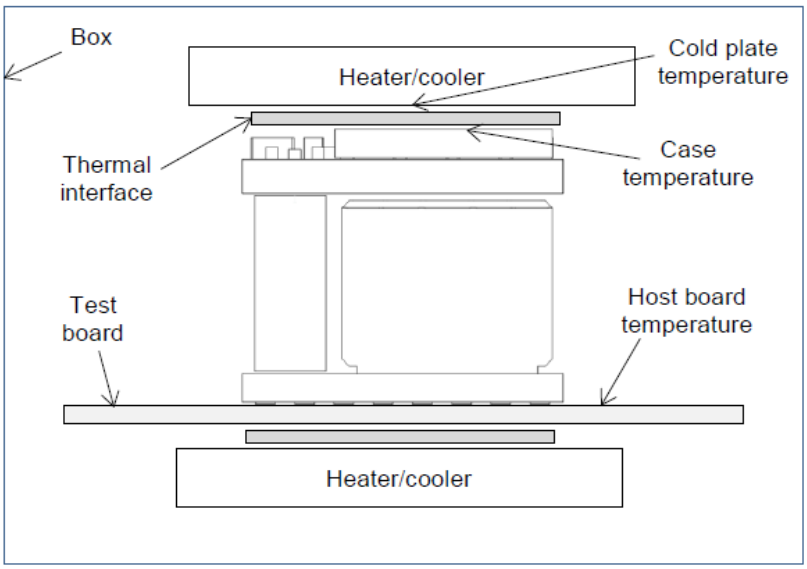
General

The product is designed with power switches on top. To operate with top side cooling towards a heat sink or a cold plate. This is required to handle operation with high load. Cooling is also achieved by conduction to the host board and surrounding air. Sufficient cooling must be provided to ensure reliable operation.

The Output Current Derating graph found in the Electrical Specification section provides the available output current versus cold plate temperature and host board temperature.

Test Setup – Cold Plate

The product is tested in a box with two heater/coolers; one as a cold plate to control the temperature at the top of the module, another on the bottom side of the test board to control the host board temperature. The test board used is 105 x 157 mm in size with 1.6 mm thickness and 4 layers of 2 oz.



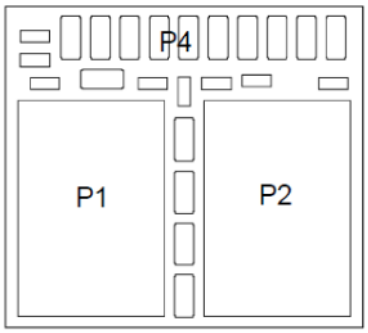
Test setup — Cold plate

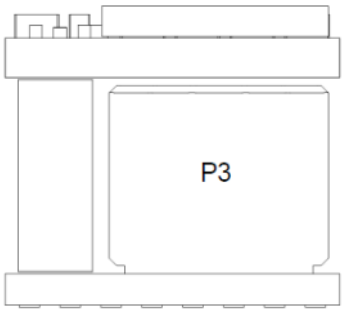
Definition of Product Operating Temperature

The temperature at positions P1-P4 should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology. Temperature above specified maximum measured at the specified position is not allowed and may cause permanent damage.

Note that the maximum value is the maximum operating temperature and that the provided Electrical Specification data is guaranteed up to T_{P1} = +95 °C.

Position	Description	Max temperature
P1	Power switch case phase 1 reference point	T_{P1}=125°C
P2	Power switch case phase 2	T_{P2}=125°C
P3	M1, Inductor core	T_{P3}=125°C
P4	capacitors	T_{P4}=105°C





Part 4: PCB layout considerations

PCB Layout Consideration

1. The radiated EMI performance of the product will depend on the PCB layout and ground layer design. A ground plane shall be used, to increase the stray capacitance in the PCB and improve the high frequency EMC performance. The ground plane shall connect to the GND pins of the devices and the equipment ground or chassis.

2. For a multiphase rail including several power modules, layout should be as symmetrical as possible in order to help balance the current between devices.

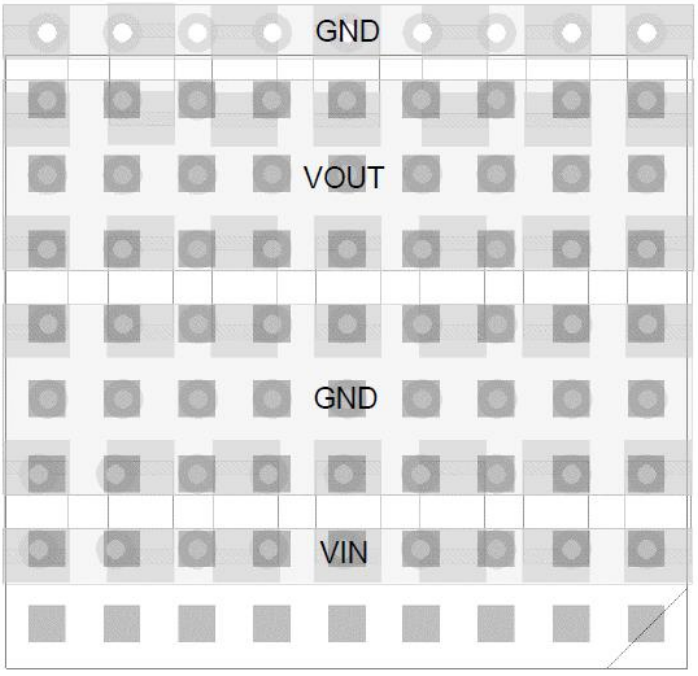
3. If possible, use planes on several layers to carry VI, VO and ground. There should be a large number of vias close to the VIN, VOUT and GND pins to lower input and output impedances and improve heat spreading between the product and the host board.

4. Care should be taken in the routing of the ISEN and TSEN connections. The routing should be along a GND plane and should avoid areas of switching signals or high electric or magnetic fields, e.g. keep away from PWM signals.

5. The external input capacitors, CI_EXT, shall be placed as close to the input pins as possible and with low impedance connections, e.g. using via stitching around capacitors' terminals. See AN323 for more details.

6. The external output capacitors, CO_EXT, should be placed close to the output pins to handle the output current ripple, and close to the load to handle the load transients. See AN321 for more details. Low impedance connections must be used, e.g. via stitching around capacitors' terminals.

Below picture shows a layout example where the module is mounted on the top side of the PCB and 7 pcs 0603 input capacitors and 14 pcs 0603 output capacitors are placed on the bottom side of the PCB, providing a short connection to the VIN, VOUT and GND pins through vias in module pads.

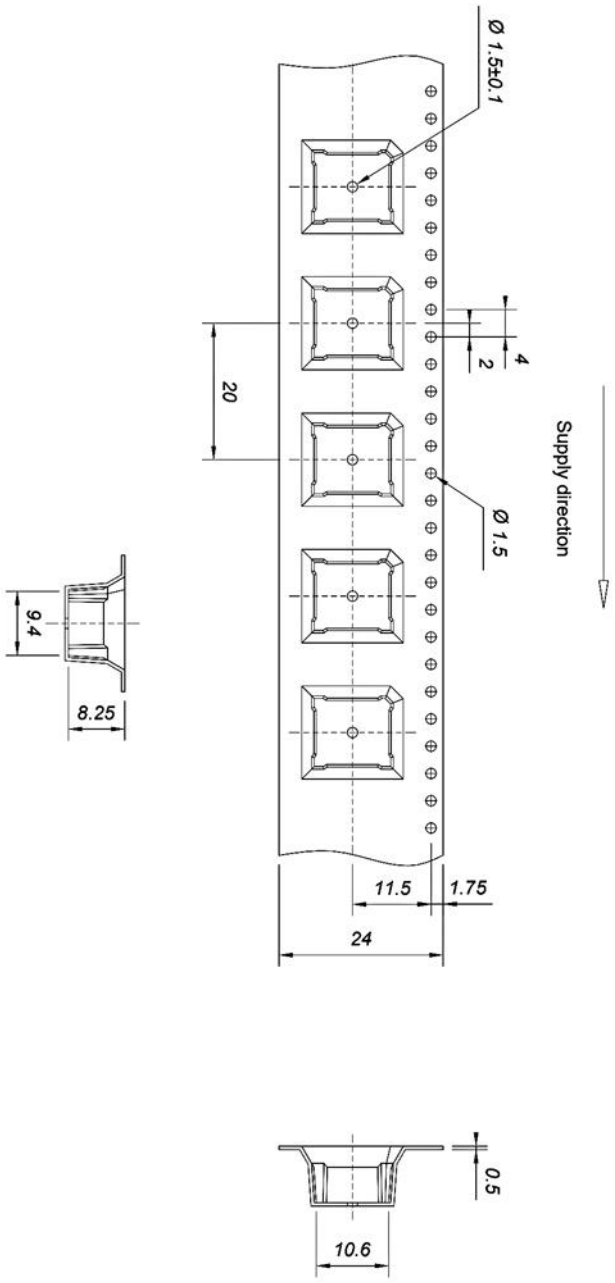


Layout example: Input and output capacitance placement close to the module (top view).

Part 5: Packaging

Packaging information

B option:	
Material	Antistatic Polyphenylene Ester (PPE)
Surface resistance	$10^5 <$ ohm/square $< 10^{11}$
Bakabilty	The tape is not bakeable
Tape width, W	24 mm [0.95 inch]
Pocket pitch, P_1	20 mm [0.79 inch]
Pocket depth, K_0	8.25 mm [0.32 inch]
Reel diameter	330 mm [13.0 inch]
Reel capacity	350 products /reel
Reel weight	1270 g/full reel



Part 6: Revision history

Revision table

Revision number	revision change	date	revisor
Rev. A	New document	2022/12/21	JIDDAYUE
Rev. B-D	Formatting updates	2023/01/10	KARTWAER

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