

NOT RECOMMENDED FOR NEW DESIGNS
 See HI1178

August 1997

Triple 8-Bit, 35 MSPS, RGB, 3-Channel D/A Converter

Features

- Resolution Triple 8-Bit
- Maximum Conversion Speed 35MHz
- RGB 3-Channel Input/Output
- Differential Linearity Error $\pm 1/2$ LSB
- Digital Input Voltage TTL Level
- Output Voltage Full-Scale 1V_{P-P} (Typ)
- Low Power Consumption 360mW (Typ)
- +5V Single Power Supply
- Direct Replacement for Sony CX20206

Applications

- Digital TV
- Graphics Display
- High Resolution Color Graphics
- Video Reconstruction
- Instrumentation
- Image Processing
- I/Q Modulation

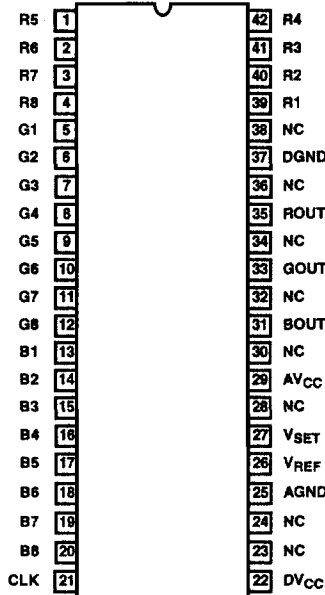
Description

The HI20206 is a triple 8-bit, high-speed, bipolar D/A converter designed for video band use. It has three separate, 8-bit pixel inputs, one each for red, green, and blue video data. A single 5.0V power supply and pixel clock input is all that is required to make the device operational. A bias voltage generator is internal. For lower CMOS power consumption, refer to the HI1178.

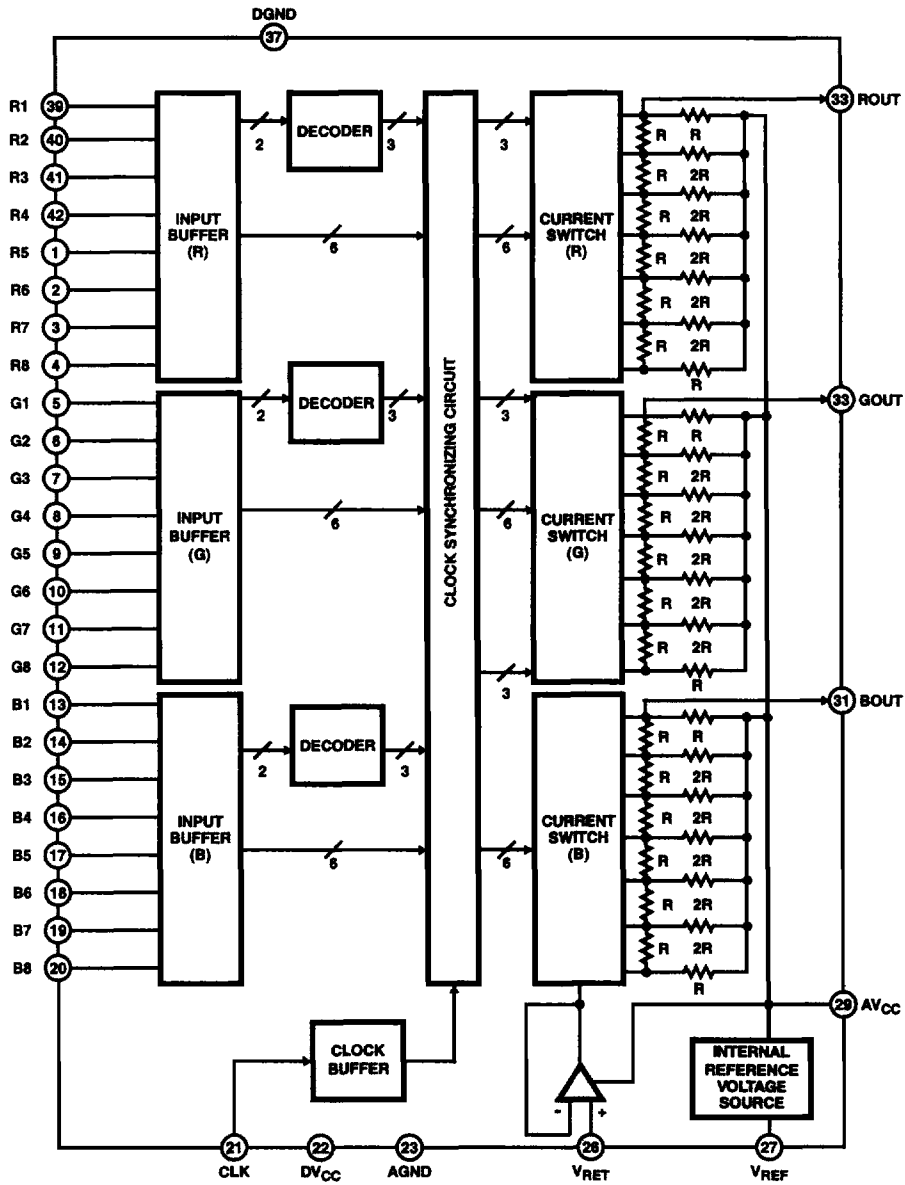
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HI20206JCP	-20 to 75	42 Ld PDIP	E42.6B-S

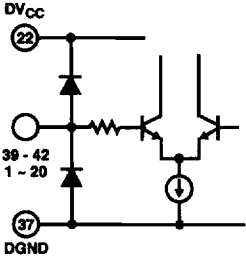
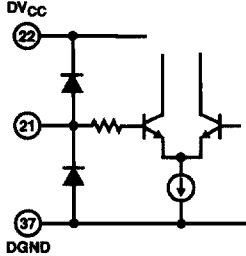
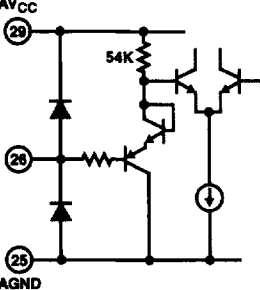
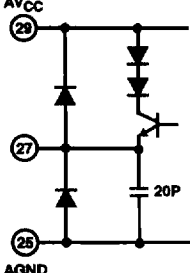
Pinout

 HI20206 (PDIP)
 TOP VIEW


Functional Block Diagram



Pin Descriptions

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 To 20 39 To 42	R1 To R8 G1 To G8 B1 To B8		Digital Input pin. From pins 39 to 42 and from 1 to 4 are for RED. R1 is MSB and R8 is LSB. From pins 5 to 12 are for GREEN. G1 is MSB and G8 is LSB. From pins 13 to 20 are for BLUE. B1 is MSB and B8 is LSB.
21	CLK		Clock Input pin.
22	DVCC		Digital VCC.
23 24	NC		No Connect.
25	AGND		Analog GND.
26	VSET		Bias Input pin. Normally, apply 0.8V.
27	VREF		Internal Reference Voltage Output pin 1.2V (Typ). A pulldown resistance is necessary externally.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
28	NC		No Connect.
29	AV _{CC}		Analog V _{CC} .
30	NC		Vacant pin but connect to AV _{CC} (Note 1).
31	BOUT		Analog Output pin for BLUE.
32	NC		Vacant pin but connect to AV _{CC} (Note 1).
33	GOUT		Analog Output pin for GREEN.
34	NC		Vacant pin but connect to AV _{CC} (Note 1).
35	ROUT		Analog Output pin for RED.
36	NC		Vacant pin but connect to AV _{CC} (Note 1).
37	DGND		Digital GND.
38	NC		No Connect.

NOTE:

1. Pins 30, 32, 34 and 36 are vacant, but in order to reduce interference between the individual RGB outputs, connect them to AV_{CC}.

Absolute Maximum Ratings

Supply Voltage (V _{CC})	0V to 7V
Input Voltage (Digital) (V _I , V _{CLK})	-0.3V to V _{CC}
Output Voltage (Analog) (V _{SET})	V _{CC} - 2.1V to V _{CC}
Output Current	
Analog (I _{OUT})	-3mA to 10mA
V _{REF} Pin (I _{REF})	-5mA to 0mA
Supply Voltage Range (Typ)	5V to 10V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ _{JA} (°C/W)
PDIP Package	70
Maximum Storage Temperature Range (T _{STG})	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C

Recommended Operating Conditions

Supply Voltage	
AV _{CC} , DV _{CC}	4.5V to 5.5V
AV _{CC} -DV _{CC}	-0.2V to 0.2V
AGND-DGND	-0.05V to 0.05V
Digital Input Voltage	
H Level (V _{IH} , V _{CLKH})	2.0V to DV _{CC}
L Level (V _{IL} , V _{CLKL})	DGND to 0.8V
V _{SET} Input Voltage (V _{SET})	0.7V to 0.9V
V _{REF} Pin Current (I _{REF})	-3mA to -0.4mA
Clock Pulse Width	
t _{PW1}	15ns
t _{PW0}	10ns
Temperature Range (T _{OPR})	-40°C to 85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications T_A = 25°C, AV_{CC} = DV_{CC} = 5V, AGND = DGND = 0V

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Resolution		RSL		-	8	-	Bit	
Monotonic		MNT		-	Guarantee	-	-	
Differential Linearity Error		DLE	V _{SET} - AGND = 0.8V, R _L > 10kΩ	-0.5	-	0.5	LSB	
Integral Linearity Error		ILE		-0.4	-	0.4	% of Full Scale	
Maximum Conversion Speed		f _{MAX}	V _{SET} - AGND = 0.8V, R _L > 10kΩ, C _L < 20pF	35	-	-	MHz	
Full Scale Output Voltage (Note 3)		V _{OF5}		0.85	1.0	1.15	V _{P-P}	
RGB Output Voltage Full Scale Ratio (Note 4)		FSR		0	4	8	%	
Output Zero Offset Voltage		V _{OFFSET}		-40	-6	0	mV	
Output Resistance		R _O		270	340	420	Ω	
Dissipation Current		I _D	V _{SET} - AGND = 0.8V, R _L > 10kΩ, I _{REF} = -400μA	54	72	90	mA	
Digital Data Input Current	H Level	Upper 2 Bits	V _I = DV _{CC}	-	1.2	20	μA	
		Lower 6 Bits						-
	L Level	Upper 2 Bits		V _I = DGND	-10	0	10	
		Lower 6 Bits						-10
Clock Input Current	H Level	I _{CLKH}	V _{CLK} = DV _{CC}	-	3	30	μA	
	L Level	I _{CLKL}	V _{CLK} = DGND	-10	0	10	μA	
V _{SET} Input Current		I _{SET}	V _{SET} - AGND = 0.8V	-5	-0.3	0	μA	
Internal Reference Voltage		V _{REF}	I _{REF} = -400μA	1.08	1.20	1.32	V	
Set-Up Time		t _S		12	-	-	ns	
Hold Time		t _H		3	-	-	ns	
Crosstalk Among R, G and B		CT	D/A OUT: 1V _{P-P} , R _L > 10kΩ, C _L < 20pF, f _{DATA} = 7MHz, f _{CLK} = 14MHz, See Figure 5	-	-40	-33	dB	

Electrical Specifications $T_A = 25^\circ\text{C}$, $AV_{CC} = DV_{CC} = 5\text{V}$, $AGND = DGND = 0\text{V}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Glitch Energy	GE	$V_{SET} - AGND = 0.8\text{V}$, $R_L > 10\text{k}\Omega$, $f_{CLK} = 1\text{MHz}$, Digital Ramp Output, See Figure 6 (Note 5)	-	160	-	pV/s
Rise Time (Note 6)	t_r	$V_{SET} - AGND = 0.8\text{V}$ See Figure 4	-	5.5	-	ns
Fall Time (Note 6)	t_f		-	5.0	-	ns
Settling Time	t_{SET}		-	16	-	ns

NOTES:

3. $AV_{CC} - V_O$.

4. Maximum value among $100 \times \left| \frac{V_{OFS(R)} - 1}{V_{OFS(G)}} \right|$, $100 \times \left| \frac{V_{OFS(G)} - 1}{V_{OFS(B)}} \right|$, or $100 \times \left| \frac{V_{OFS(B)} - 1}{V_{OFS(R)}} \right|$.

5. Observe the glitch which is generated when the digital input varies as follows:

```

0 0 1 1 1 1 1 1 1  — 0 1 0 0 0 0 0 0
0 1 1 1 1 1 1 1 1  — 1 0 0 0 0 0 0 0
1 0 1 1 1 1 1 1 1  — 1 1 0 0 0 0 0 0
    
```

6. The time required for the D/A OUT to arrive at 90% of its final value from 10%.

INPUT CORRESPONDING TABLE

INPUT CODE		OUTPUT VOLTAGE
MSB	LSB	
1 1 1 1 1 1 1		$V_{CC} + V_{OFFSET}$
.		.
.		.
1 0 0 0 0 0 0		$V_{CC} + V_{OFFSET} - 0.5\text{V}$
.		.
.		.
0 0 0 0 0 0 0		$V_{CC} + V_{OFFSET} - 1.0\text{V}$

NOTE: In case the output voltage full scale is 1V (1 LSB = 3.92mV).

Test Circuits

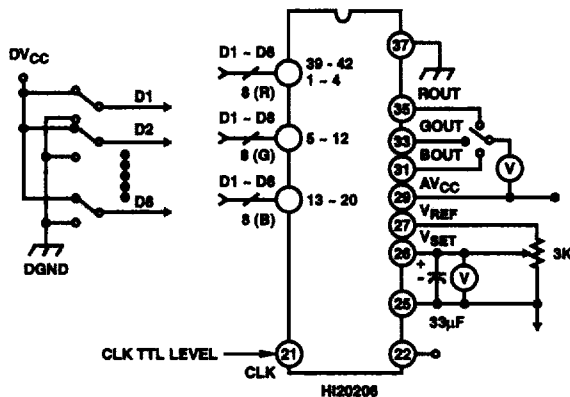


FIGURE 1. DIFFERENTIAL LINEARITY AND INTEGRAL LINEARITY TEST CIRCUITS

Test Circuits (Continued)

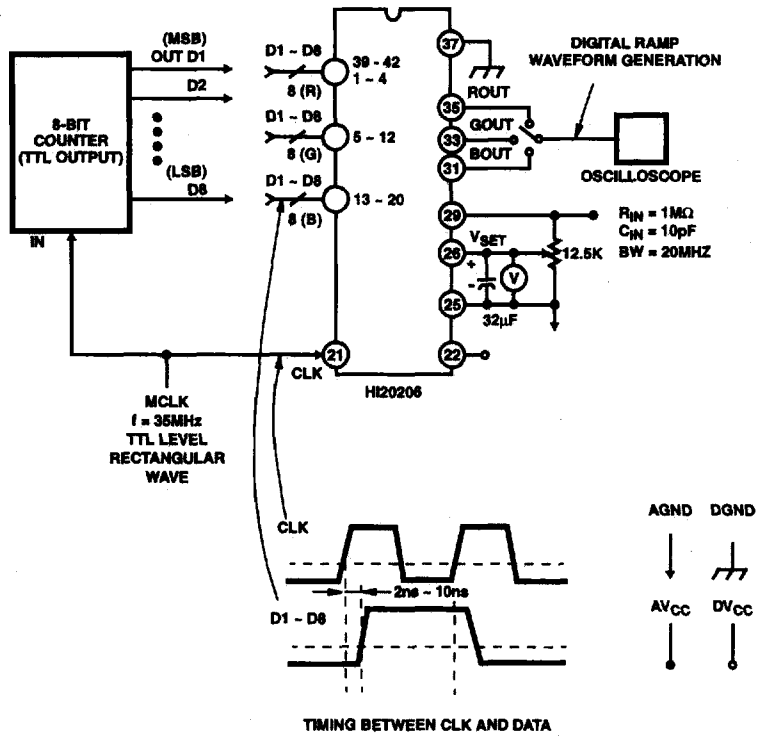


FIGURE 2. MAXIMUM CONVERSION RATE TEST CIRCUIT

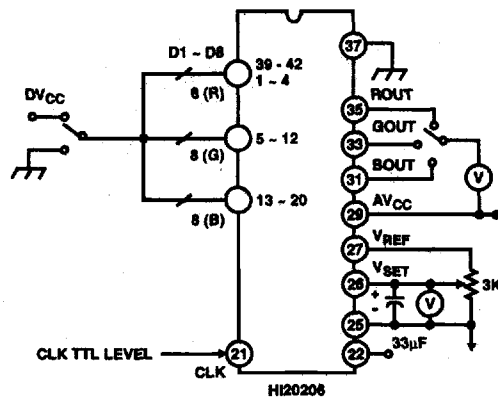


FIGURE 3. OUTPUT VOLTAGE FULL SCALE PRECISION, RGB OUTPUT VOLTAGE FULL SCALE RATIO, AND OUTPUT ZERO OFFSET VOLTAGE TEST CIRCUITS

Test Circuits (Continued)

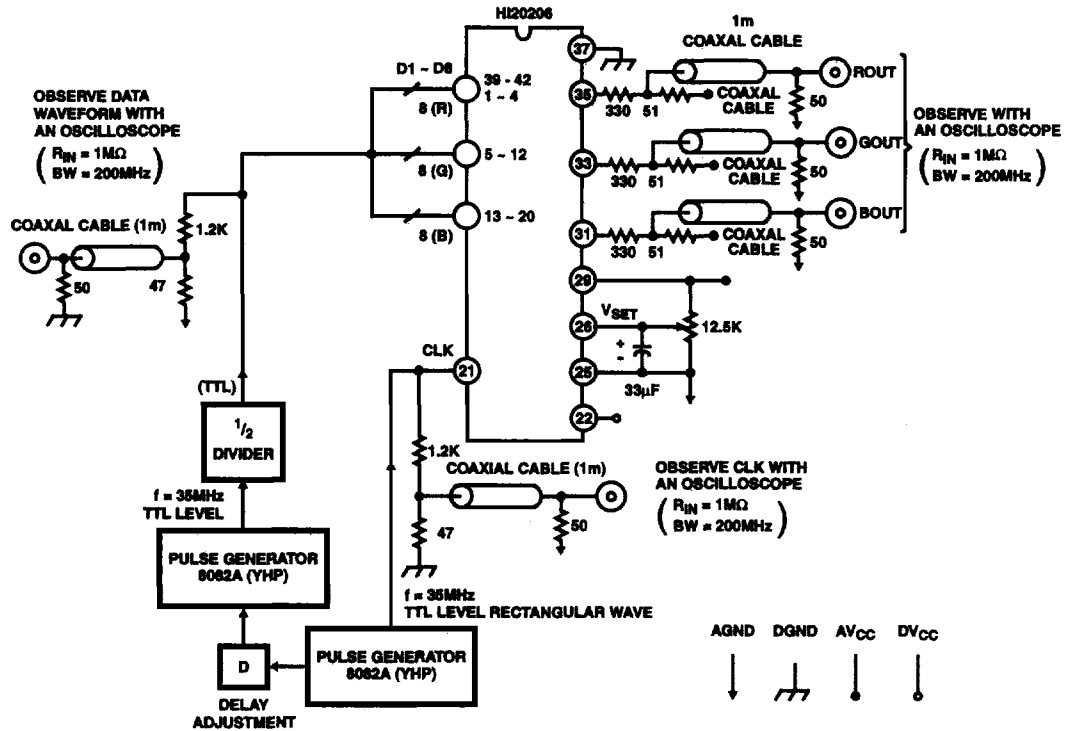
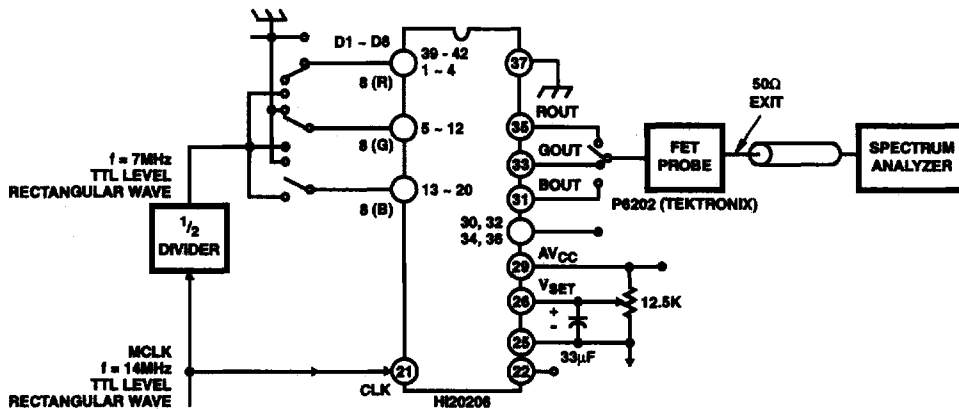


FIGURE 4. SET-UP TIME, HOLD TIME, AND RISE AND FALL TIME TEST CIRCUITS



Measuring Method, in case the measuring crosstalk of G → R:

1. Apply the data to G only, and measure the power of the frequency component of the data at R_{OUT}.
2. Apply the data to R only, and measure the power of the frequency component of the data at R_{OUT}.
3. Take the difference of the above two powers; the unit is in dB.

FIGURE 5. CROSSTALK AMONG R, G, AND B TEST CIRCUIT

Test Circuits (Continued)

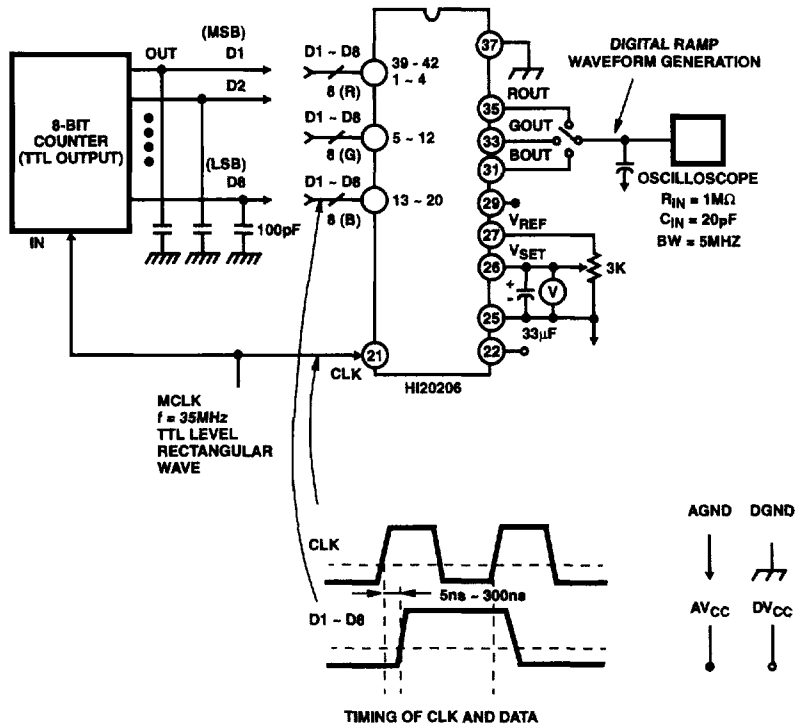


FIGURE 6. GLITCH ENERGY TEST CIRCUIT

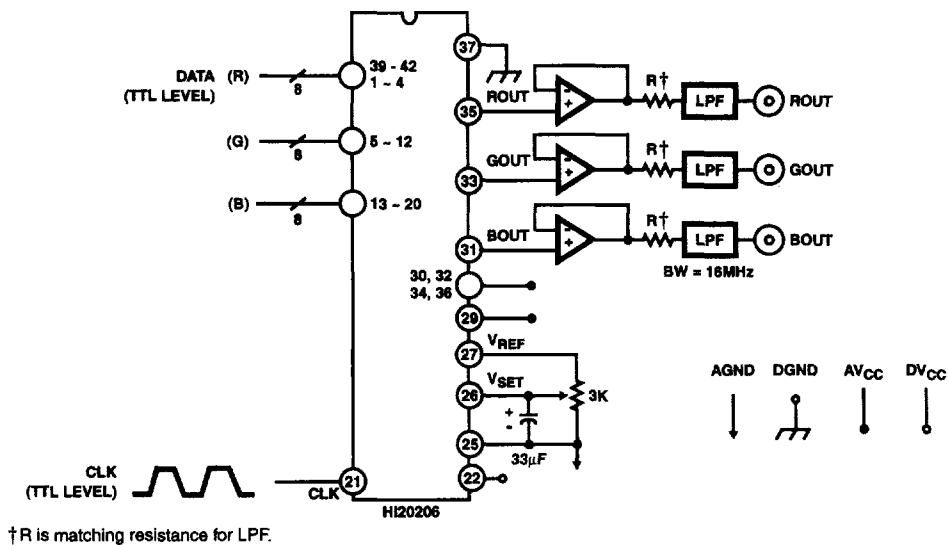
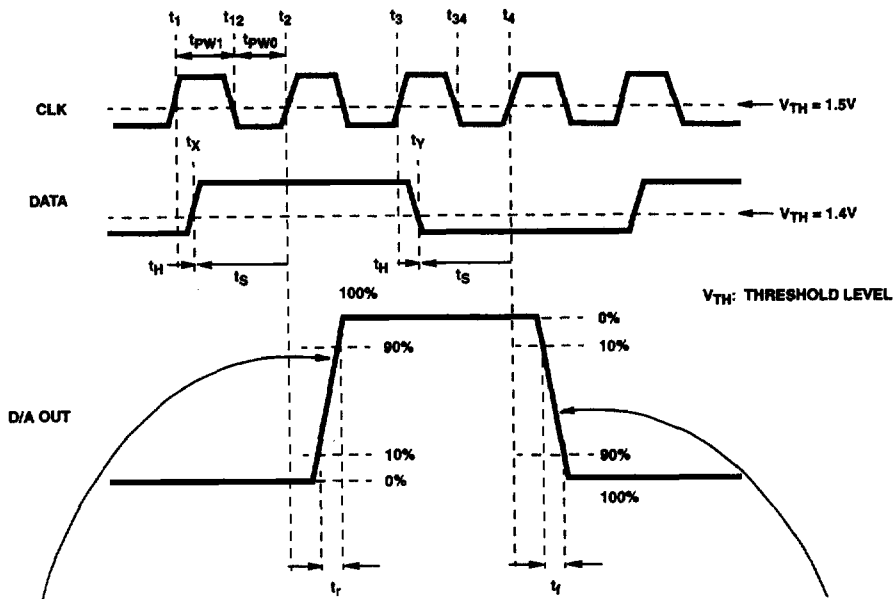


FIGURE 7. APPLIED CIRCUIT EXAMPLE

Timing Diagram



NOTE: At the time $t = t_x$, the data of individual bits are switched and thereafter, when the CLK becomes L → H at $t = t_2$, the D/A OUT is varied synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK. [In this case, fetching of the data is carried out at the fall of the CLK (at the time when $t = t_{12}$)].

NOTE: At the time $t = t_y$, the data of individual bits are switched and thereafter when the CLK becomes L → H at $t = t_4$, the D/A OUT is varied synchronous with it. That is, the D/A OUT is synchronous with the rise of the CLK. [In this case, fetching of the data is carried out at the fall of the CLK (at the time when $t = t_4$)].

FIGURE 8. TIMING CHART

Notes On Use

- (1) Setting of pin 26 (V_{SET})

The full scale of the D/A output voltage changes by applying voltage to pin 26 (V_{SET}). When load is connected to pin 27 (V_{REF}), DC voltage of 1.2V is issued and the said voltage is dropped to 0.8V by resistance division.

When the 0.8V is applied to pin 26 (V_{SET}), the D/A output of 1V_{p-p} can be obtained.

(Example of use):

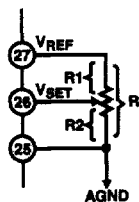


FIGURE 9.

(Adjustment Method)

1. The resistance R is determined in accordance with the recommended operating condition of I_{REF} . (current flowing through resistance R).

See R vs I_{REF} of Figure 14. The calculation expression is as follows:

$$R = V_{REF} / I_{REF}$$

2. Adjust the volume so that the RGB output voltage full scale becomes 1V.

(At this point, it becomes $R_1 : R_2 = 1 : 2$).

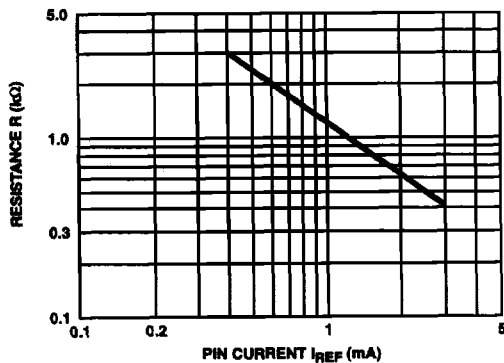


FIGURE 10. RESISTANCE vs V_{REF} PIN CURRENT

(2) Phase Relationship Between Data and Clock

In order to obtain the desired characteristics as a D/A converter, it is necessary to set the phase relationship correctly between the externally applied data and clock.

Satisfy the standard of the set-up time (t_S) and hold time (t_H) indicated in the electrical characteristics. As to the meaning of t_S and t_H , see the timing chart.

Moreover, the clock pulse width is desired to be as indicated in the recommended operating condition.

(3) Regarding the Load of D/A Output Pin

Receive the D/A output of the next stage with high impedance. In other words perform so that it becomes as follows:

$$R_L > 10k\Omega$$

$$C_L < 20pF$$

The temperature characteristics indicated in the characteristics diagram has been measured under this condition.

However, when it is made $R_L \leq 10k\Omega$ the temperature characteristics may change considerably. In addition, when it is made $C_L \geq 20pF$, the rise and fall of the D/A output become slow and will not operate at high speed.

(4) Noise Reduction Measures

As the D/A output voltage is a minute voltage of approximately 4mV per one step, ingenuity is required in reducing the noise entering from the outside of the IC as much as possible. Therefore, use the items given below as reference.

- When mounting onto the printed board, allow as much space as possible to the ground surface and the V_{CC} surface on the board and reduce the parasitic inductance and resistance.

- It is desirable that the AGND and DGND be separated in the pattern on the board. It is similar with AV_{CC} and DV_{CC} . As shown in the diagram below, for example, it is recommended that the wiring to the electric supply of AGND and DGND as also AV_{CC} and DV_{CC} be conducted separately, and then making AGND and DGND as also AV_{CC} and DV_{CC} in common right near the power supply respectively.

- Insert in parallel a 47 μ F tantalum capacitor and a 100pF ceramic capacitor between the V_{CC} surface on the printed board and the nearest ground surface. (A of diagram below). It is also desirable to insert the above between the V_{CC} surface near the pin of the IC and the ground surface (see Figure 11). They are bypass capacitors to prevent bad effects from occurring to the characteristics when the power supply voltage fluctuates due to the clock, etc.

It is recommended to reduce noise which overlaps the D/A output by inserting a capacitor of over 0.1 μ F between pin 25 (AGND) and pin 26 (V_{SET}).

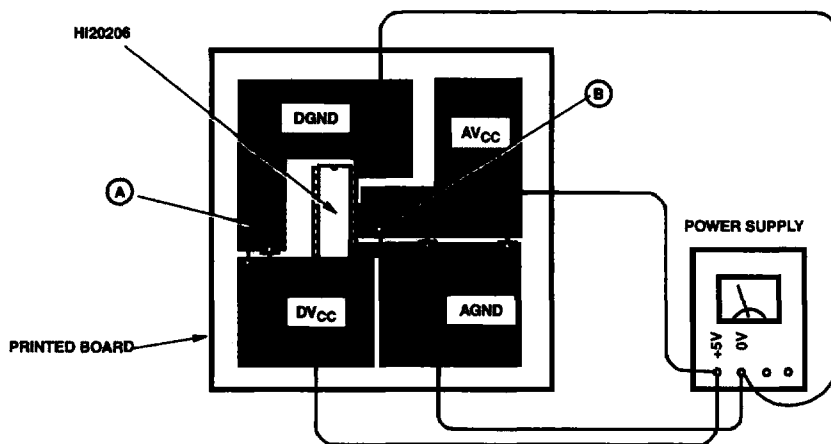


FIGURE 11.

Typical Performance Curves

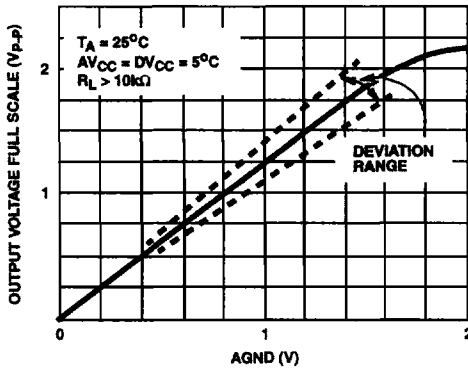


FIGURE 12. OUTPUT VOLTAGE FULL SCALE vs $V_{SET} - AGND$

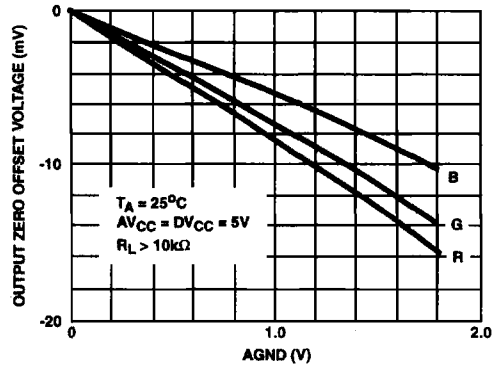


FIGURE 13. OUTPUT ZERO OFFSET VOLTAGE vs $V_{SET} - AGND$

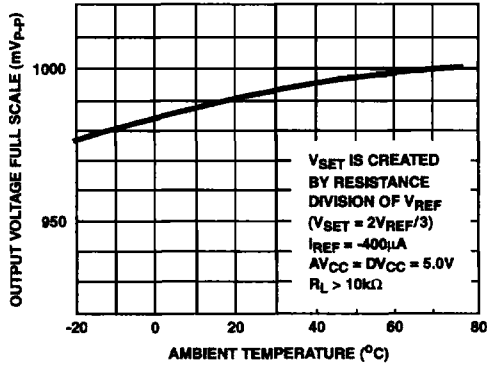


FIGURE 14. OUTPUT VOLTAGE FULL SCALE vs AMBIENT TEMPERATURE

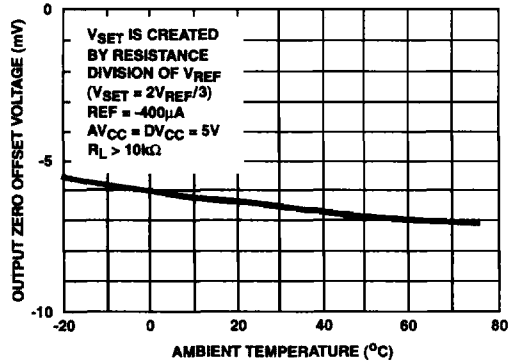


FIGURE 15. OUTPUT ZERO OFFSET vs AMBIENT TEMPERATURE

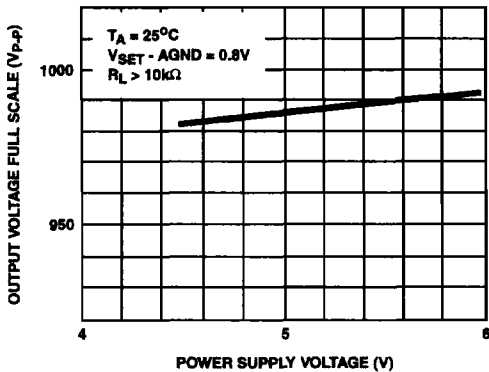


FIGURE 16. OUTPUT VOLTAGE FULL SCALE vs POWER SUPPLY VOLTAGE

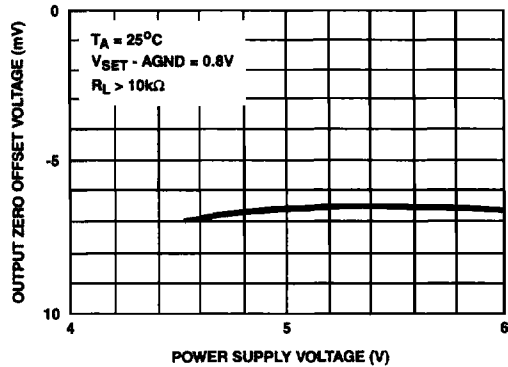


FIGURE 17. OUTPUT ZERO OFFSET VOLTAGE vs POWER SUPPLY VOLTAGE

Typical Performance Curves (Continued)

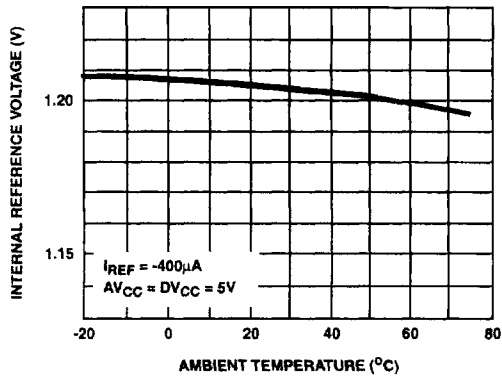


FIGURE 18. INTERNAL REFERENCE VOLTAGE vs AMBIENT TEMPERATURE

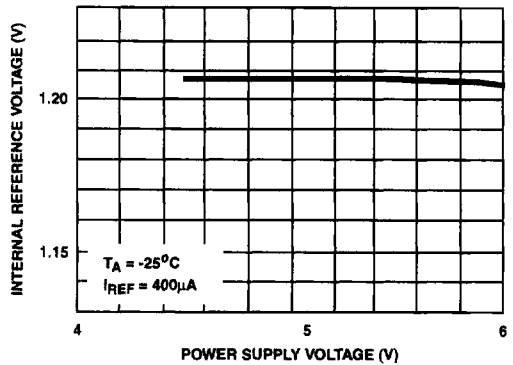


FIGURE 19. INTERNAL REFERENCE VOLTAGE vs POWER SUPPLY VOLTAGE

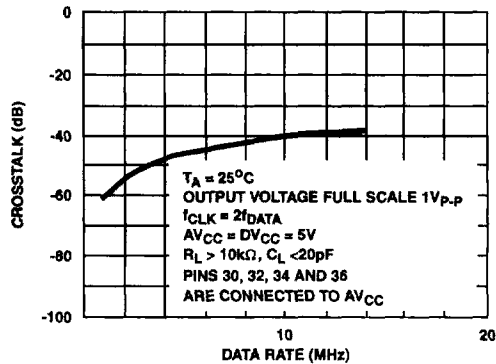


FIGURE 20. CROSSTALK AMONG R, G, AND B vs DATA RATE