

## **Description**

The RD3P050SNTL1 uses advanced trench technology and design to provide excellent  $R_{\text{DS(ON)}}$  with low gate charge. It can be used in a wide variety of applications.

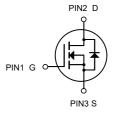


TO-252-2L

#### **General Features**

V<sub>DS</sub> =100V,I<sub>D</sub> =15A

 $R_{DS(ON)}$  <112m  $\Omega$  @  $V_{GS}$ =10V



# **Application**

Power switch

DC/DC converters

N-Channel MOSFET

## **Package Marking and Ordering Information**

Product ID	Pack	Brand	Qty(PCS)
RD3P050SNTL1	TO-252-2L	HXY MOSFET	2500

## Absolute Maximum Ratings (Tc=25 ℃ unless otherwise noted)

Symbol	Parameter	Rating	Units
VDS	Drain-Source Voltage	100	V
Vss	Gate-Source Voltage	±20	V
In@Tc=25°C	Continuous Drain Current, V <sub>☉</sub> @ 10V¹	15	А
I <sub>D</sub> @T <sub>C</sub> =100°C	Continuous Drain Current, V <sub>☉</sub> @ 10V¹	7.7	А
Ірм	Pulsed Drain Current <sup>2</sup>	24	А
EAS	Single Pulse Avalanche Energy <sup>3</sup>	6.1	mJ
las	Avalanche Current	11	А
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation <sup>3</sup>	34.7	W
Тѕтс	Storage Temperature Range	-55 to 150	°C
TJ	Operating Junction Temperature Range	-55 to 150	°C
Reja	Thermal Resistance Junction-ambient <sup>1</sup>	62	°C/W
Rejc	Thermal Resistance Junction-Case <sup>1</sup>	3.6 °C/V	

## Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BVpss	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	100			V
$\triangle BV_{DSS}/\triangle T_{J}$	BVDSS Temperature Coefficient	Reference to 25°C , I <sub>D</sub> =1mA		0.098		V/°C
_	0.1. 0.1. 0. 0. 0. 1	V <sub>GS</sub> =10V , I <sub>D</sub> =10A		100	112	mΩ
RDS(ON)	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =4.5V , I <sub>D</sub> =8A		117	130	$m\Omega$
VGS(th)	Gate Threshold Voltage		1.0		2.5	V
		V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA				
$\triangle V_{\text{GS(th)}}$	V <sub>GS(th)</sub> Temperature Coefficient			-4.57		mV/°C
		V <sub>DS</sub> =80V , V <sub>GS</sub> =0V , T <sub>J</sub> =25 °C			1	•
loss	Drain-Source Leakage Current	V <sub>DS</sub> =80V , V <sub>GS</sub> =0V , T <sub>J</sub> =55°C			5	uA
Igss	Gate-Source Leakage Current	$V_{GS}$ = $\pm 20V$ , $V_{DS}$ = $0V$			±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =10A		13		S
Rg	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		2		Ω
Qg	Total Gate Charge (10V)			26.2		
Qgs	Gate-Source Charge	V <sub>DS</sub> =80V , V <sub>GS</sub> =10V , I <sub>D</sub> =10A		4.6		nC
Qgd	Gate-Drain Charge			5.1		
Td(on)	Turn-On Delay Time			4.2		
Tr	Rise Time	V <sub>DD</sub> =50V , V <sub>GS</sub> =10V , —R <sub>G</sub> =3.3		8.2		ns
Td(off)	Turn-Off Delay Time	I <sub>D</sub> =10A		35.6		
T <sub>f</sub>	Fall Time	ID- TOA		9.6		
Ciss	Input Capacitance			1535		
Coss	Output Capacitance	V <sub>DS</sub> =15V , V <sub>GS</sub> =0V , f=1MHz		60		pF
Crss	Reverse Transfer Capacitance			37		
ls	Continuous Source Current <sup>1,5</sup>				12	Α
lsм	Pulsed Source Current <sup>2,5</sup>	−V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			24	Α
VsD	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =1A , T <sub>J</sub> =25°C			1.2	V
t <sub>rr</sub>	Reverse Recovery Time	I=-400 - 41/4t-4000		37		nS
Qrr	Reverse Recovery Charge	lF=10A , dl/dt=100A/μs , T <sub>J</sub> =25°C		27.3		nC

#### Note:

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width  $\leqq$  300us , duty cycle  $\leqq$  2%
- 3. The EAS data shows Max. rating . The test condition is  $V_{DD}$ =25V,  $V_{GS}$ =10V, L=0.1mH,  $I_{AS}$ =11A
- 4.The power dissipation is limited by 150°C junction temperature
- 5 .The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.

## **Typical Characteristics**

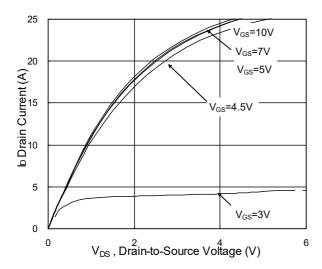


Fig.1 Typical Output Characteristics

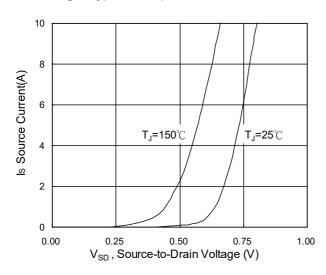


Fig.3 Forward Characteristics Of Reverse

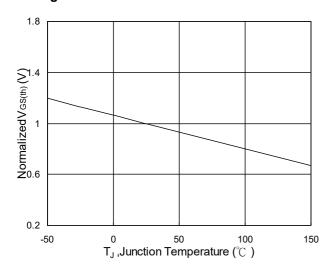


Fig.5 Normalized V<sub>GS(th)</sub> vs. T<sub>J</sub>

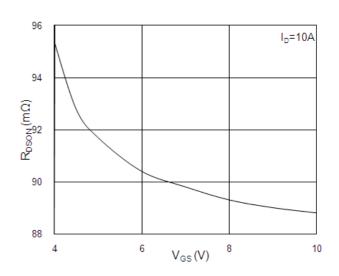


Fig.2 On-Resistance vs. Gate-Source

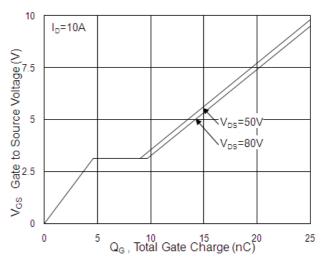


Fig.4 Gate-Charge Characteristics

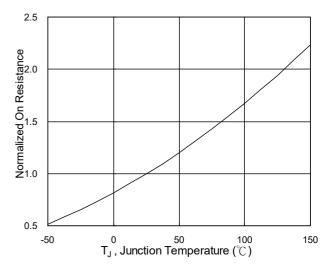
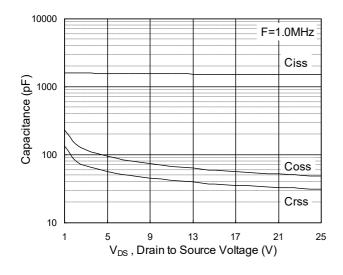


Fig.6 Normalized R<sub>DSON</sub> vs. T<sub>J</sub>



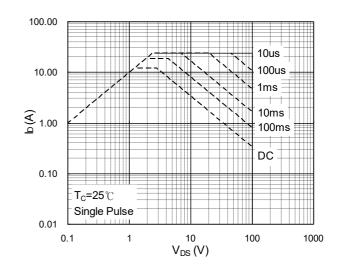


Fig.7 Capacitance

Fig.8 Safe Operating Area

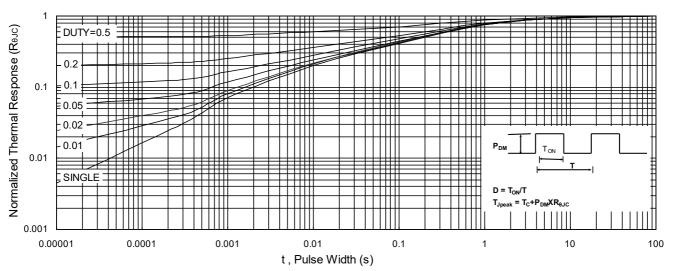


Fig.9 Normalized Maximum Transient Thermal Impedance

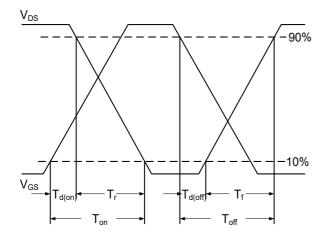


Fig.10 Switching Time Waveform

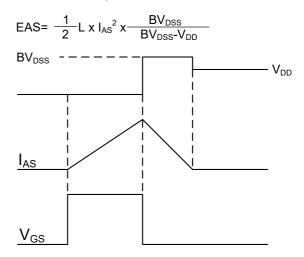
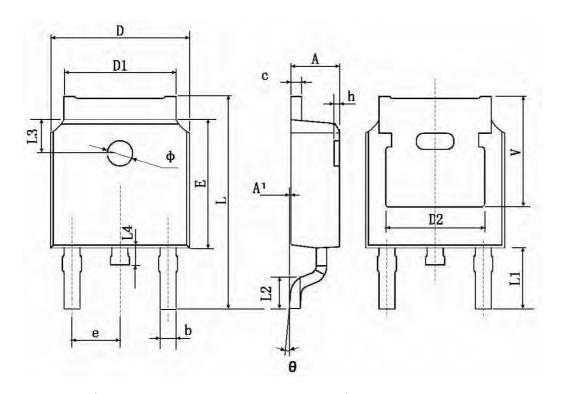


Fig.11 Unclamped Inductive Switching Waveform

## N-Channel Enhancement Mode MOSFET

# **TO-252-2L Package Information**



Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min.	Max.	Min.	Max.	
Α	2.200	2.400	0.087	0.094	
A1	0.000	0.127	0.000	0.005	
b	0.660	0.860	0.026	0.034	
С	0.460	0.580	0.018	0.023	
D	6.500	6.700	0.256	0.264	
D1	5.100	5.460	0.201	0.215	
D2	0.483	0.483 TYP.		0.190 TYP.	
Е	6.000	6.200	0.236	0.244	
е	2.186	2.386	0.086	0.094	
L	9.800	10.400	0.386	0.409	
L1	2.900 TYP.		0.114 TYP.		
L2	1.400	1.700	0.055	0.067	
L3	1.600 TYP.		0.063 TYP.		
L4	0.600	1.000	0.024	0.039	
Ф	1.100	1.300	0.043	0.051	
θ	0°	8°	0°	8°	
h	0.000	0.300	0.000	0.012	
V	5.350 TYP. 0.211 TYP.		TYP.		



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