

N-Channel Power MOSFET

600V, 11A, 390mΩ

FEATURES

- Super-Junction technology
- High performance due to small figure-of-merit
- High ruggedness performance
- High commutation performance
- 100% UIS & Rg tested
- RoHS Compliant
- Halogen-free according to IEC 61249-2-21

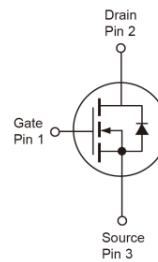
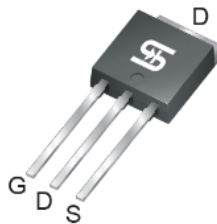
APPLICATIONS

- Power Supply
- Lighting

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
V_{DS}	600	V
$R_{DS(on)}$ (max)	390	mΩ
Q_g	21	nC



TO-251 (IPAK)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	600	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current (Note 1)	I_D	$T_C = 25^\circ\text{C}$	11
		$T_C = 100^\circ\text{C}$	7
Pulsed Drain Current (Note 2)	I_{DM}	33	A
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	125	W
Single Pulse Avalanche Energy (Note 3)	E_{AS}	300	mJ
Single Pulse Avalanche Current (Note 3)	I_{AS}	3.5	A
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150	$^\circ\text{C}$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	1	$^\circ\text{C/W}$
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	45	$^\circ\text{C/W}$

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0\text{V}, I_D = 1\text{mA}$	BV_{DSS}	600	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1\text{mA}$	$V_{GS(TH)}$	3	4.5	5	V
Gate Body Leakage	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	I_{GSS}	--	--	± 100	nA
Zero Gate Voltage Drain Current	$V_{DS} = 600\text{V}, V_{GS} = 0\text{V}$	I_{DSS}	--	--	100	μA
Drain-Source On-State Resistance	$V_{GS} = 10\text{V}, I_D = 3.8\text{A}$	$R_{DS(on)}$	--	350	390	m Ω
Dynamic (Note 5)						
Total Gate Charge	$V_{DS} = 300\text{V}, I_D = 11\text{A},$ $V_{GS} = 10\text{V}$	Q_g	--	21.4	--	nC
Gate-Source Charge		Q_{gs}	--	6.1	--	
Gate-Drain Charge		Q_{gd}	--	10.1	--	
Input Capacitance	$V_{DS} = 300\text{V}, V_{GS} = 0\text{V},$ $f = 1.0\text{MHz}$	C_{iss}	--	813	--	pF
Output Capacitance		C_{oss}	--	27	--	
Reverse Transfer Capacitance		C_{rss}	--	12	--	
Gate Resistance	$f = 1.0\text{MHz}$	R_g	0.52	1.73	3.46	Ω
Switching (Note 6)						
Turn-On Delay Time	$V_{DD} = 300\text{V}, R_G = 10\Omega,$ $I_D = 5.7\text{A}, V_{GS} = 10\text{V}$	$t_{d(on)}$	--	22	--	ns
Turn-On Rise Time		t_r	--	3.8	--	
Turn-Off Delay Time		$t_{d(off)}$	--	20	--	
Turn-Off Fall Time		t_f	--	8.1	--	
Source-Drain Diode (Note 4)						
Forward Voltage	$I_S = 11\text{A}, V_{GS} = 0\text{V}$	V_{SD}	--	--	1.5	V
Reverse Recovery Time	$I_S = 11\text{A}$	t_{rr}	--	320	--	ns
Reverse Recovery Charge		$dI_F/dt = 100\text{A}/\mu\text{s}$	Q_{rr}	--	4.85	--

Notes:

1. Current limited by package.
2. Pulse width limited by the maximum junction temperature.
3. $L = 50\text{mH}, V_{DD} = 50\text{V}, R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
4. Pulse test: $PW \leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

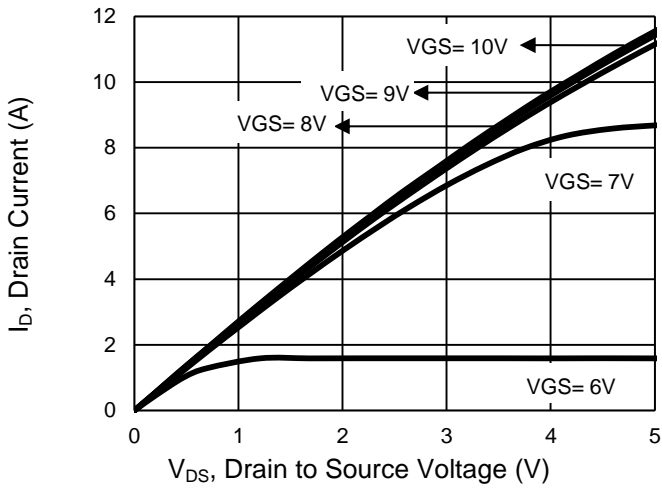
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TSM60NC390CH C5G	TO-251 (IPAK)	75pcs / Tube

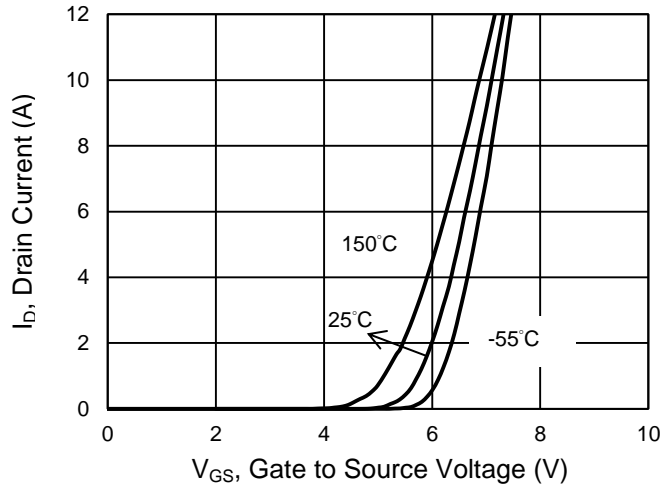
CHARACTERISTICS CURVES

($T_c = 25^\circ\text{C}$ unless otherwise noted)

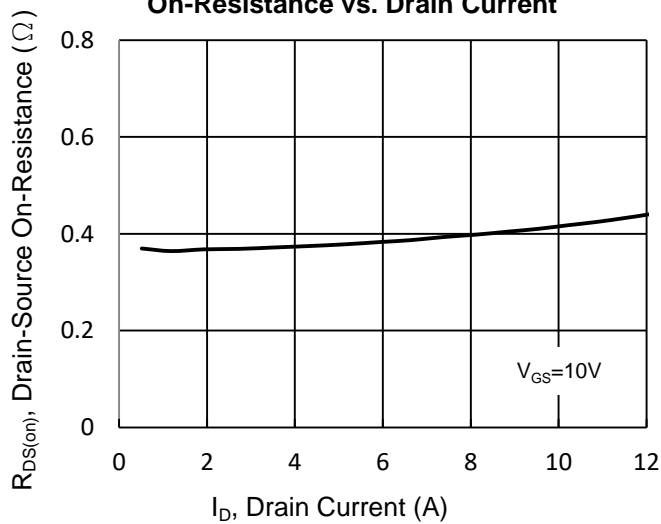
Output Characteristics



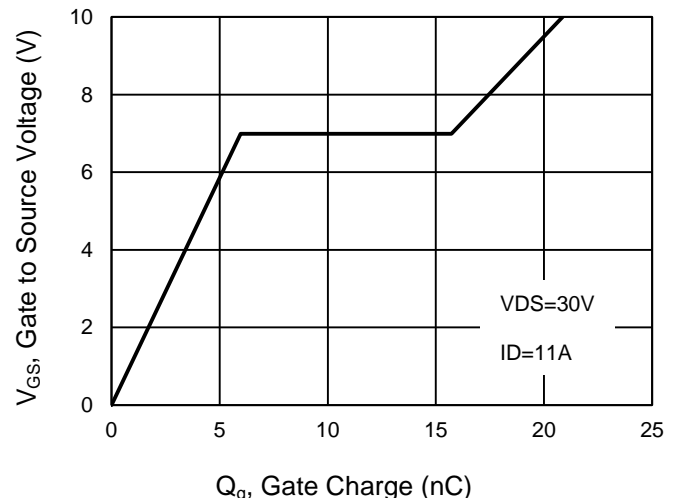
Transfer Characteristics



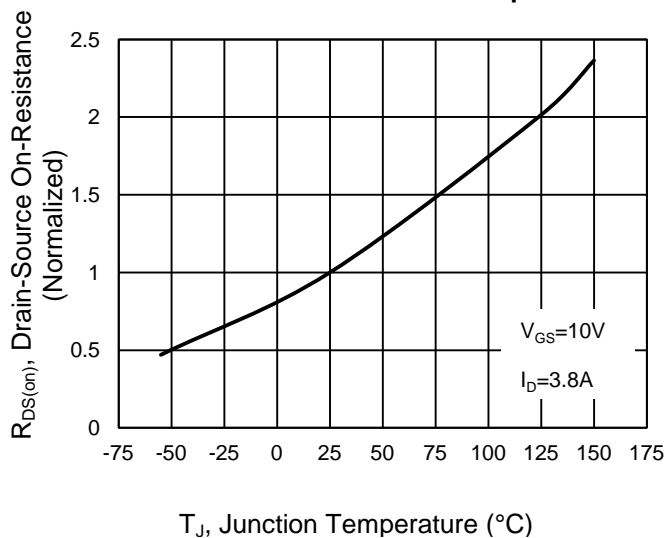
On-Resistance vs. Drain Current



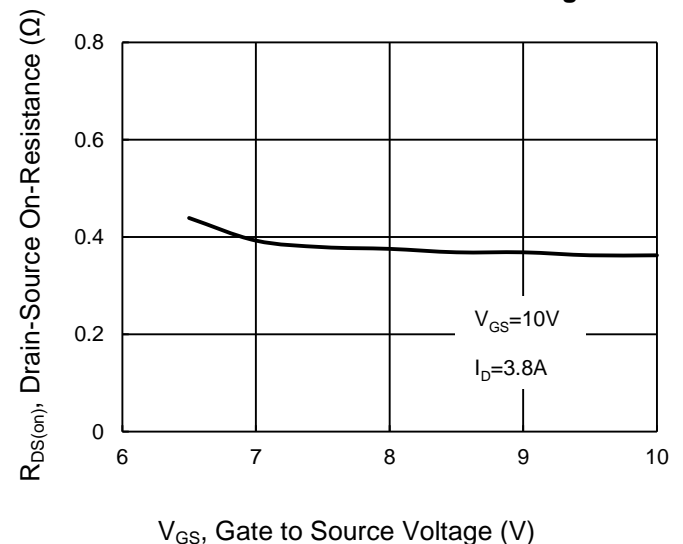
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



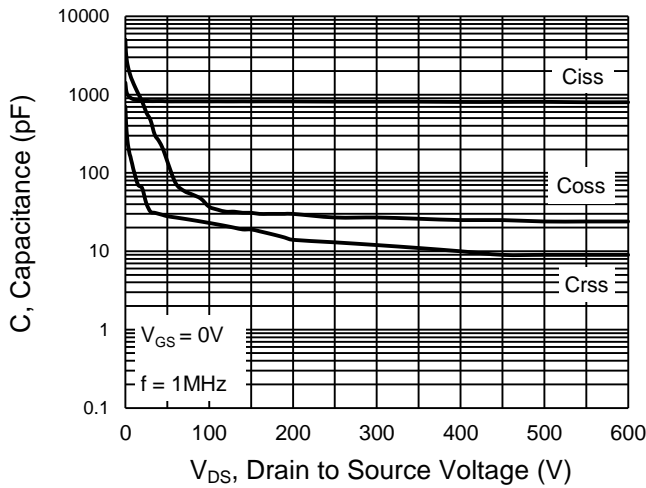
On-Resistance vs. Gate-Source Voltage



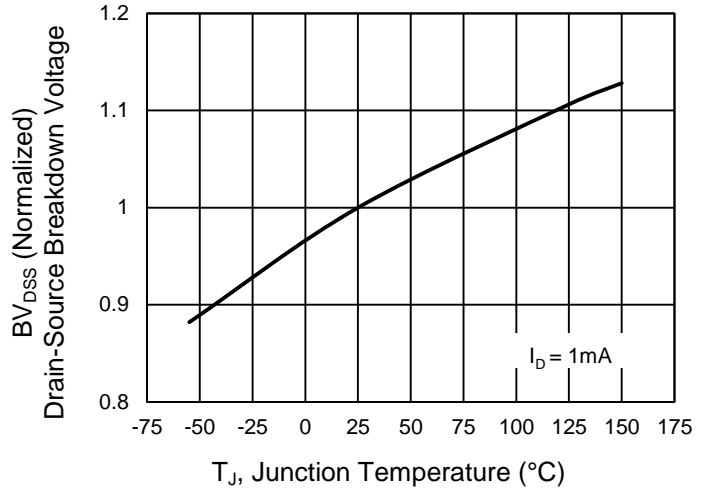
CHARACTERISTICS CURVES

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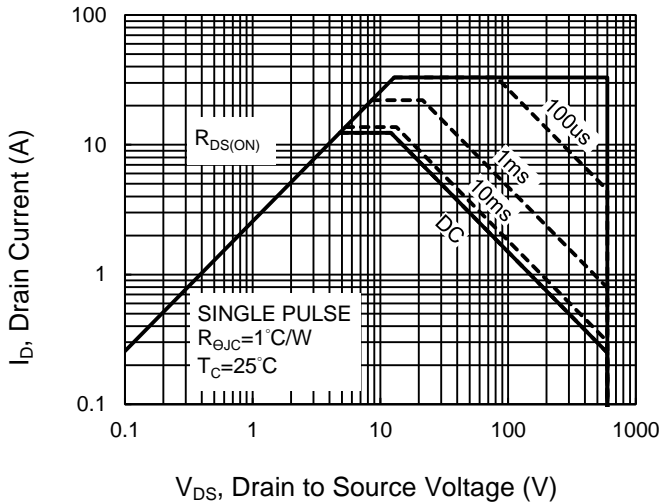
Capacitance vs. Drain-Source Voltage



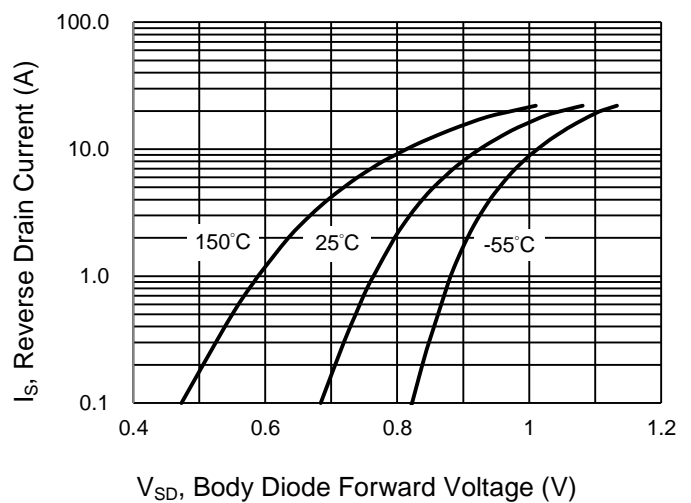
BV_{DSS} vs. Junction Temperature



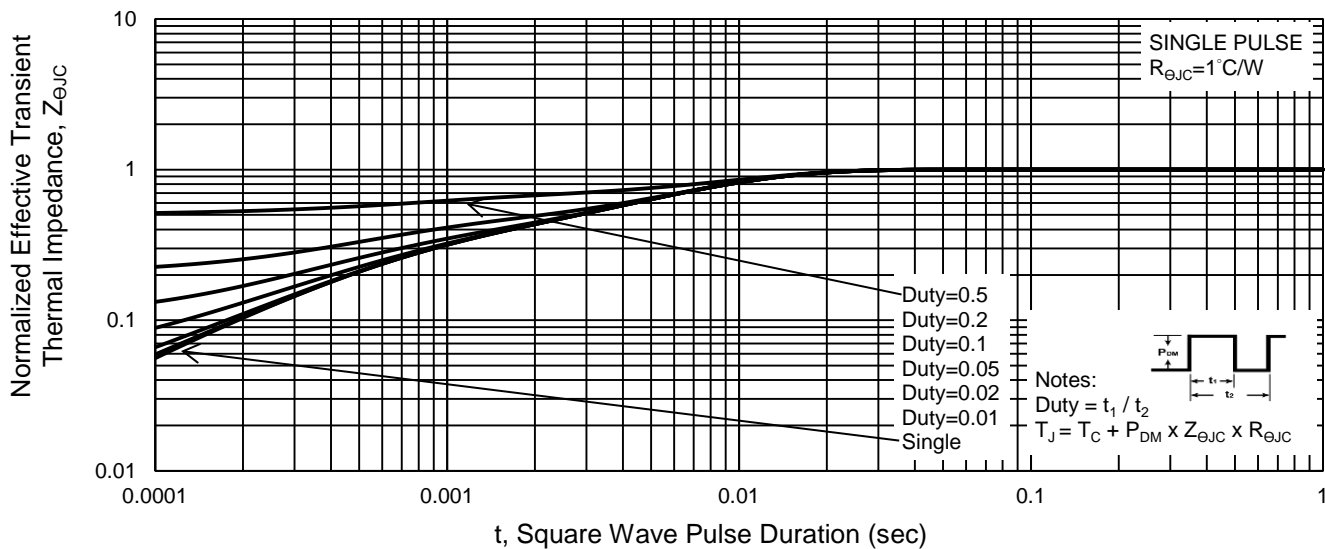
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

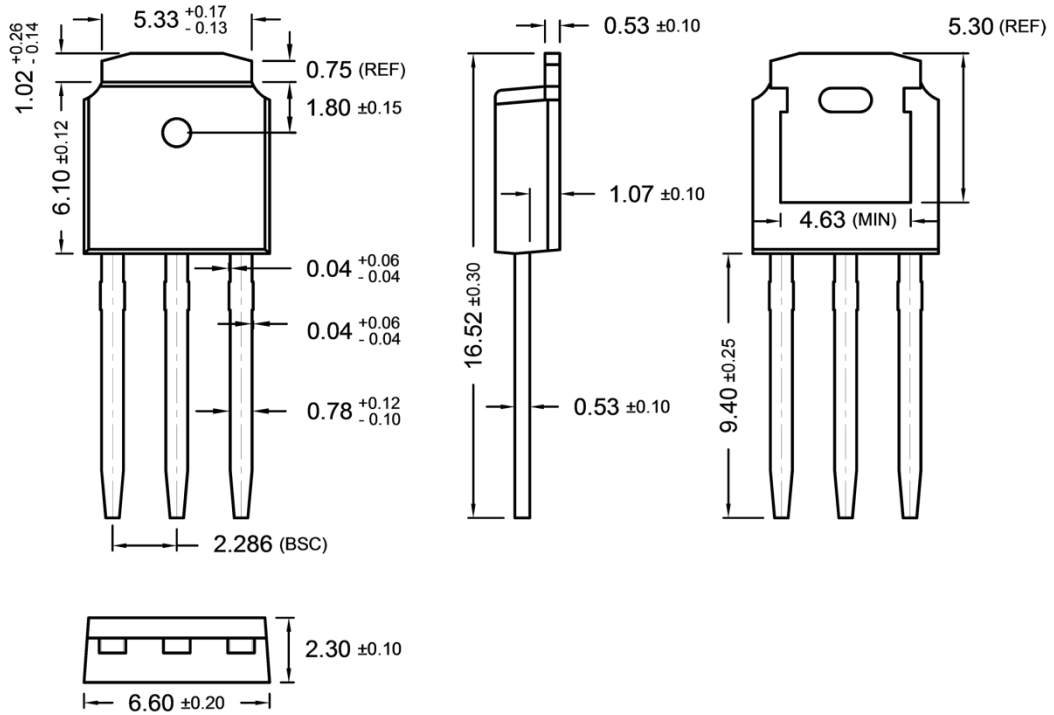


Normalized Thermal Transient Impedance, Junction-to-Case

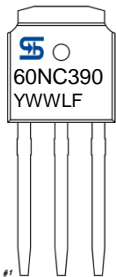


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

TO-251 (IPAK)



MARKING DIAGRAM



- Y** = Year Code
- WW** = Week Code (01~52)
- L** = Lot Code (1~9, A~Z)
- F** = Factory Code

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