BURR-BROWN®

OPA104

For a /883B version of this product, see OPA106/883B in the Military Products section.

Ultra-Low Bias Current Low Drift FET Input OPERATIONAL AMPLIFIER

FEATURES

- SPECIFICATIONS GUARANTEED OVER TEMPERATURE
- ULTRA-LOW BIAS CURRRENT, 75fA, max
- HIGH INPUT IMPEDANCE, $10^{15}\Omega$
- LOW DRIFT, $10\mu V/°C$, max
- LOW OFFSET VOLTAGE, 0.5mV, max
- LOW QUIESCENT CURRENT, 1.5mA, max

APPLICATIONS

- CURRENT TO VOLTAGE CONVERSION
- LONG TERM PRECISION INTEGRATION
- PRECISION VOLTAGE AMPLIFICATION FOR HIGH INPUT IMPEDANCE APPLICATIONS SUCH AS:
  - photo current detectors
  - pH electrodes
  - biological probes/transducers

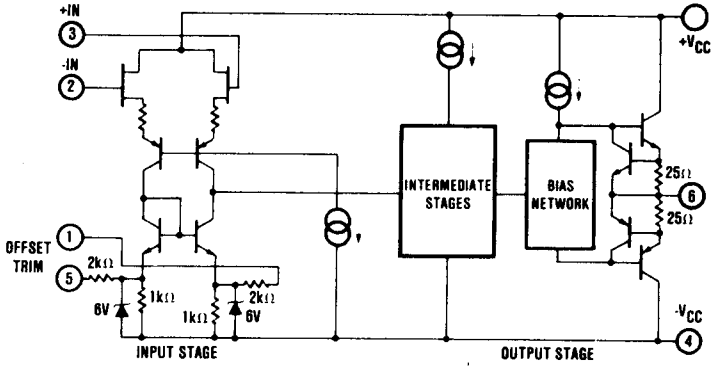
DESCRIPTION

The OPA104 is a precision low bias current operational amplifier. Guaranteed low initial offset voltage (0.5mV, max) and associated drift versus temperature ($10\mu V/°C$, max) is achieved by laser-adjusting the amplifier during manufacturing. The low offset, in addition to the guaranteed low bias current (75fA, max), allows greater system accuracy with no external components.

Quiescent current (1.5mA, max) is unaffected by changes in ambient temperature or power supply voltage. Other characteristics of the OPA104 include internal compensation for unity-gain stability and rapid thermal response for quick stabilization after turn-on or ambient temperature changes.

The amplifier is free from latch-up and is protected for continuous output shorts to common. As an added protection feature, either of the trim pins can be accidently shorted to a potential greater than the negative supply voltage without damage.

The standard pin configuration (741 type) of the OPA104 allows the user drop-in replacement capability. A pin 8 case connection permits the reduction of noise and leakage by employing guarding techniques.



International Airport Industrial Park · P.O. Box 11400 · Tucson, Arizona 85734 · Tel. (602) 746-1111 · Twx: 910-952-1111 · Cable: BBRCORP · Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and $\pm V_{CC}$ = ±15VDC unless otherwise noted.

MODEL	OPA104AM			OPA104BM			OPA104CM			
PARAMETERS	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
OPEN-LOOP GAIN, DC, V_{OUT} = ±10V										
Rated Load, $R_L \geq 2k\Omega$	100	108		•	•		•	•		dB
$R_L \geq 10k\Omega$	106	112		•	•		•	•		dB
T_A = -25°C to +85°C, $R_L \geq 2k\Omega$	92	100		•	•		•	•		dB
RATED OUTPUT										
Voltage at R_L = 2kΩ, T_A = -25°C to +85°C	±10	±12		•	•		•	•		V
R_L = 10kΩ, T_A = -25°C to +85°C	±12	±13		•	•		•	•		V
Current T_A = -25°C to +85°C	±5	±10		•	•		•	•		mA
Output Impedance		3			•			•		kΩ
Load Capacitance[1]	500	1000		•	•		•	•		pF
Short Circuit Current	10	25		•	•		•	•		mA
FREQUENCY RESPONSE										
Unity Gain, Small Signal		1			•			•		MHz
Full Power Response	25	35		•	•		•	•		kHz
Slew Rate	1.6	2.2		•	•		•	•		V/µsec
Settling Time (0.1%), Av = -1, Vo = 0 to ±10V		6			•			•		µsec
Settling Time (0.01%), Av = -1, Vo = 0 to ±10V		18			•			•		µsec
Overload Recovery[2], 50% overdrive		4	15		•	•		•	•	µsec
INPUT OFFSET VOLTAGE										
Initial Offset, T_A = +25°C		±200	±1000		±200	±500		±200	±500	µV
vs Temperature, T_A = -25°C to +85°C		±15	±25		±10	±15		±5	±10	µV/°C
vs Supply Voltage, T_A = +25°C		±10	±100		•	•		•	•	µV/V
vs Supply Voltage, T_A = -25°C to +85°C		±20	±150		•	•		•	•	µV/V
INPUT BIAS CURRENT[3]										
Initial Bias, T_A = +25°C			-300			-150			-75	fA
vs Supply Voltage		1				•			•	fA/V
INPUT DIFFERENCE CURRENT										
Initial Difference, T_A = +25°C		±80			±80			±40		fA
INPUT IMPEDANCE										
Differential		10^{14} || 0.5			•			•		Ω || pF
Common-mode		10^{15} || 1.0			•			•		Ω || pF
INPUT NOISE										
Voltage, f_O = 10Hz		75			•			•		nV/√Hz
f_O = 100Hz		55			•			•		nV/√Hz
f_O = 1kHz		35			•			•		nV/√Hz
f_O = 10kHz		35			•			•		nV/√Hz
f_B = 0.1Hz to 10Hz		6			•			•		µV, p-p
Current, f_B = 0.1Hz to 10Hz		3			•			•		fA, p-p
f_B = 10Hz to 10kHz		10			•			•		fA, rms
f_O = 1kHz		0.25			•			•		fA/√Hz
INPUT VOLTAGE RANGE										
Differential	±20			•	•		•	•		V
Common-mode, T_A = -25°C to +85°C	±10	±12		•	•		•	•		V
Common-mode Rejection at V_{IN} = ±10V	66	76		•	•		80	90		dB
Maximum Safe Input Voltage		±Vs			•			•		V
POWER SUPPLY										
Rated Voltage		±15		•	•	•	•	•	•	VDC
Voltage Range, derated performance	±5		±20			•			•	VDC
Current, quiescent T_A = -25°C to +85°C		1.0	1.5		•	•		•	•	mA
TEMPERATURE RANGE (ambient)										
Specification	-25		+85	•		•	•		•	°C
Operating	-55		+125	•		•	•		•	°C
Storage	-65		+150	•		•	•		•	°C
θ junction - ambient		235			•			•		°C/W

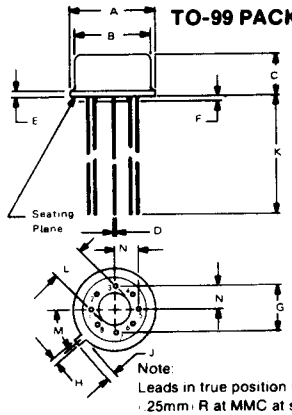
*Specifications same as for OPA104AM.

NOTES:

1. Stability guaranteed with load capacitance ≤ 500pF
2. Overload recovery is defined as the time required for the output to return from saturation to linear operation following the removal of a 50% input overdrive signal.
3. Bias current is tested and guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperature the bias current doubles approximately every +10°C

MECHANICAL

TO-99 PACKAGE



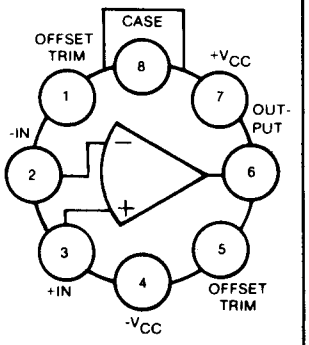
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.335	.370	8.51	9.40
B	.305	.335	7.75	8.51
C	.165	.185	4.19	4.70
D	.016	.021	0.41	0.53
E	.010	.040	0.25	1.02
F	.010	.040	0.25	1.02
G	.200 BASIC		5.08 BASIC	
H	.028	.034	0.71	0.86
J	.029	.045	0.74	1.14
K	.500	—	12.7	—
L	.110	.160	2.79	4.06
M	45° BASIC		45° BASIC	
N	.095	.105	2.41	2.67

Weight: 1 gram

Note:
Leads in true position within .010" (.25mm) R at MMC at seating plane.
Pin numbers shown for reference only. Numbers may not be marked on package

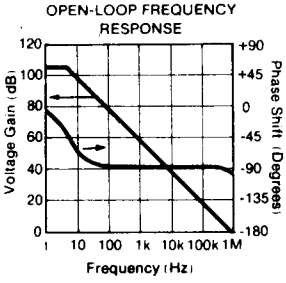
Pin material and plating composition conform to Method 2003 (solderability of MIL-STD-883 (except paragraph 3.2

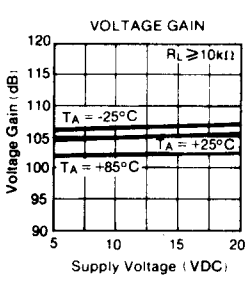
CONNECTION DIAGRAM

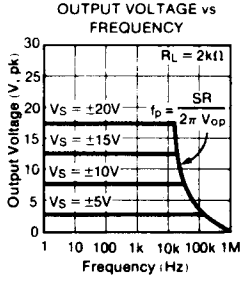


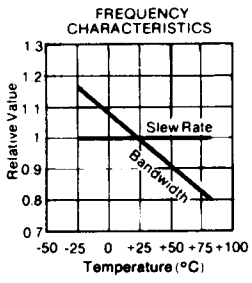
(TOP VIEW)

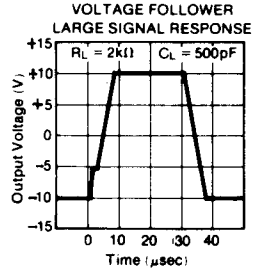
TYPICAL PERFORMANCE CURVES

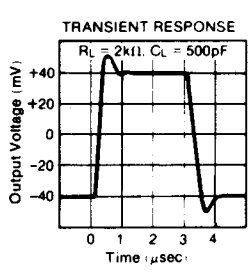


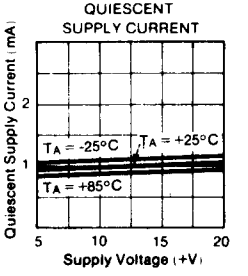


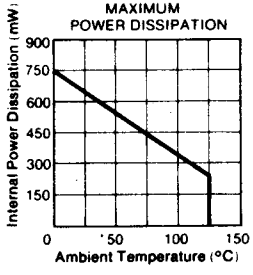


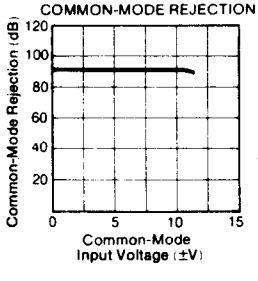


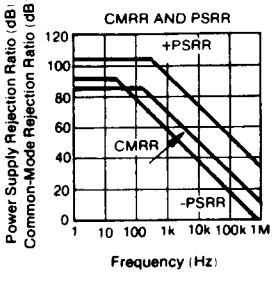


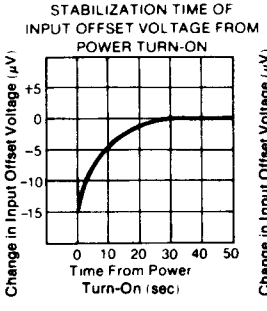


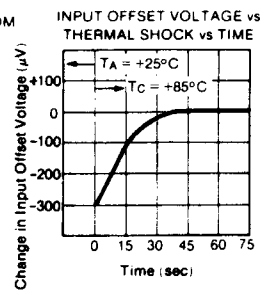












APPLICATIONS INFORMATION

THERMAL RESPONSE TIME

Thermal response time is an important parameter in low drift operational amplifiers like the OPA104. A low drift specification would be of little value if the amplifier took a long time to stabilize after turn-on or ambient temperature change. The TO-99 package and careful circuit design provide the necessary quick thermal response. Typical warm-up drift of the OPA104 is approximately 20 seconds (see Typical Performance Curves).

GUARDING AND SHIELDING

The ultra-low bias current and high input impedance of the OPA104 are well-suited to a number of stringent applications. However, careless signal wiring of printed circuit board layout can degrade circuit performance several orders of magnitude below the capability of the OPA104.

As in any situation where high impedances are involved, careful shielding is required to reduce "hum" pickup in input leads. If large feedback resistors are used, they should also be shielded along with the external input circuitry.

Leakage currents across printed circuit boards can easily exceed the bias current of the OPA104. To avoid leakage problems, it is recommended that the signal input lead of the OPA104 be wired to a Teflon standoff. If the OPA104 is to be soldered directly into a printed circuit board, utmost care must be used in planning the board layout. A "guard" pattern should completely surround the two amplifier input leads and should be connected to a low impedance point which is at the signal input potential.

The amplifier case should be connected to any input shield or guard via pin 8. This insures that the amplifier itself is fully surrounded by guard potential, minimizing both leakage and noise pickup. Figure 1 illustrates the use of the guard.

OFFSET VOLTAGE ADJUSTMENT

Although the OPA104 has a low initial offset voltage (500μV), some applications may require external nulling of this small offset. Figure 2 shows the recommended circuit for adjustment of the offset voltage. External offset voltage adjustment changes the laser adjusted offset voltage temperature drift slightly. The drift will change approximately 0.3μV/°C, for every 100μV of offset adjustment.

TYPICAL APPLICATION

The circuit in Figure 3 is a common application of a low noise FET amplifier. Noise calculations are often important when using low current photodiodes.

CR1 is a PIN photodiode connected in the photovoltaic mode (no bias voltage) which produces an output current i_{in} when exposed to the light, λ.

A more complete circuit is shown in Figure 4. The values shown for C_1 and R_1 are typical for small geometry PIN diodes with sensitivities in the range of 0.5 A/W. The value of C_2 (0.5pF to 2pF) is what would be typically required to compensate for the pole generated by the capacitance at the input node. A larger value of C_2 could be used to limit the bandwidth and reduce the voltage noise at higher frequencies.

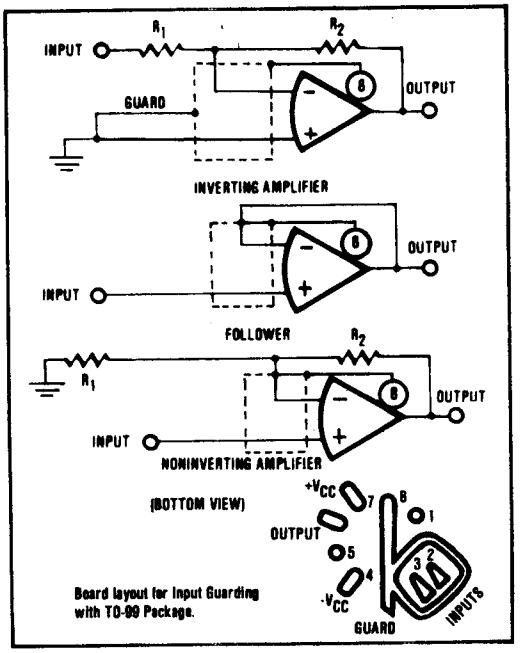


FIGURE 1. Connection of Input Guard.

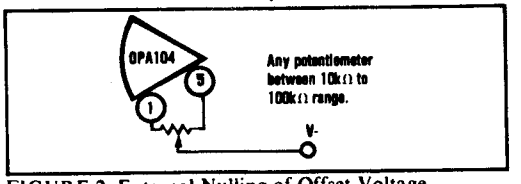


FIGURE 2. External Nulling of Offset Voltage.

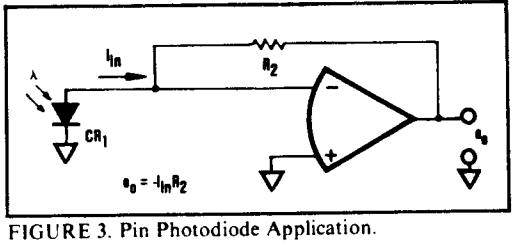


FIGURE 3. Pin Photodiode Application.

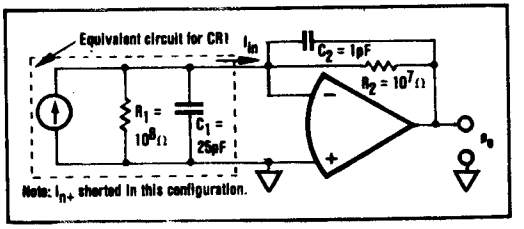


FIGURE 4. Model of Photodiode Application.