General Description

The MC14017 is a 5 - stage Johnson decade counter with ten spike- free decoded active HIGH outputs (Q0 to Q9) , an active LOW carry output from the most significant flip- flop (Q5— - 9) , active HIGH and active LOW clock inputs (CP0 , —CP1) and an overriding asynchronous master reset input (MR) .
The counter is advanced by either a LOW- to- HIGH transition at CP0 while P1 is LOW or a HIGH- to- LOW transition at CP1 while CP0 is HIGH.
When cascading counters, the Q5 - 9 output, which is LOW while the counter is in states 5 , 6 , 7 , 8 , and 9 , can be used to drive the CP0 input of the next counter. A HIGH on MR resets the counter to zero (Q0= Q—5 -9= HIGH; Q1 to Q9= LOW) independent of the clock inputs (CP0 , CP1) .
Automatic counter code correction is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 1 1 clock pulses.
It operates over a recommended VDD power supply range of3 V to 1 5 V referenced to VSS (usually ground) .
Unused inputs must be connected to VDD, VSS, or another input.

Features

- Wide supply voltage range from 3V to 15V
- Automatic counter correction
- Tolerant of slow clock rise and fall times
- 5V, 10V, and 15V parametric ratings
- Standardized symmetrical output characteristics
- Specified from -40℃ to +85℃
- Packaging information: SOP16

Ordering Information

Product Model	Package Type	Marking	Packing	Packing Qty
XBLW MC14017BDR2G	SOP-16	14017	Tape	2500Pcs/Reel

Block DiagramAndPinDescription

2．1 Block Diagram

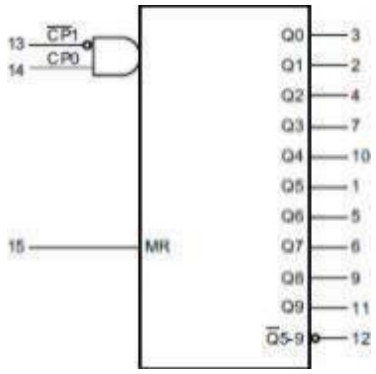


Figure 1 . Logic symbol

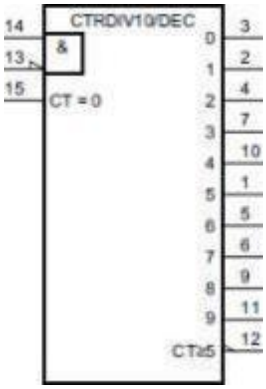


Figure 2 . IEE logic symbol

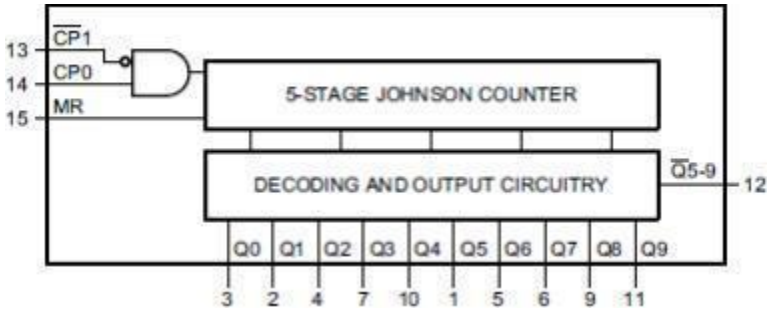


Figure 3 . Functional diagram

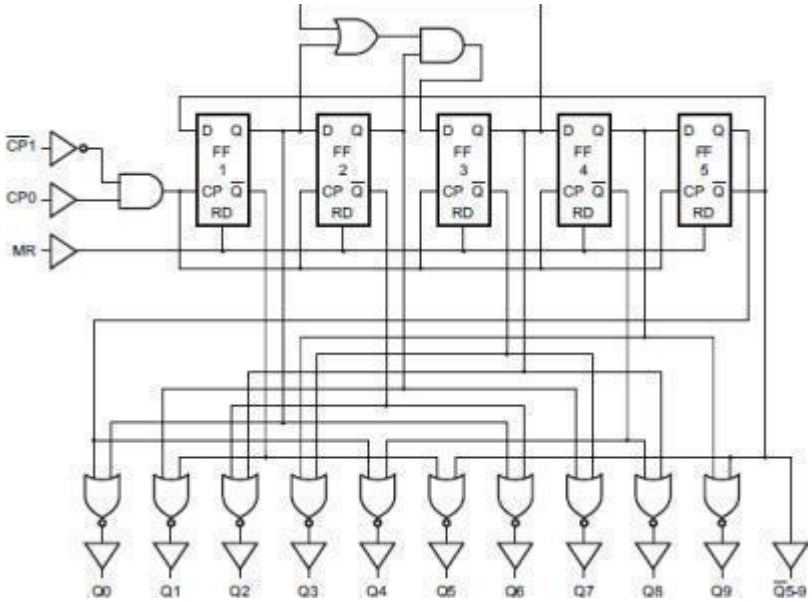


Figure 4 . Logic diagram

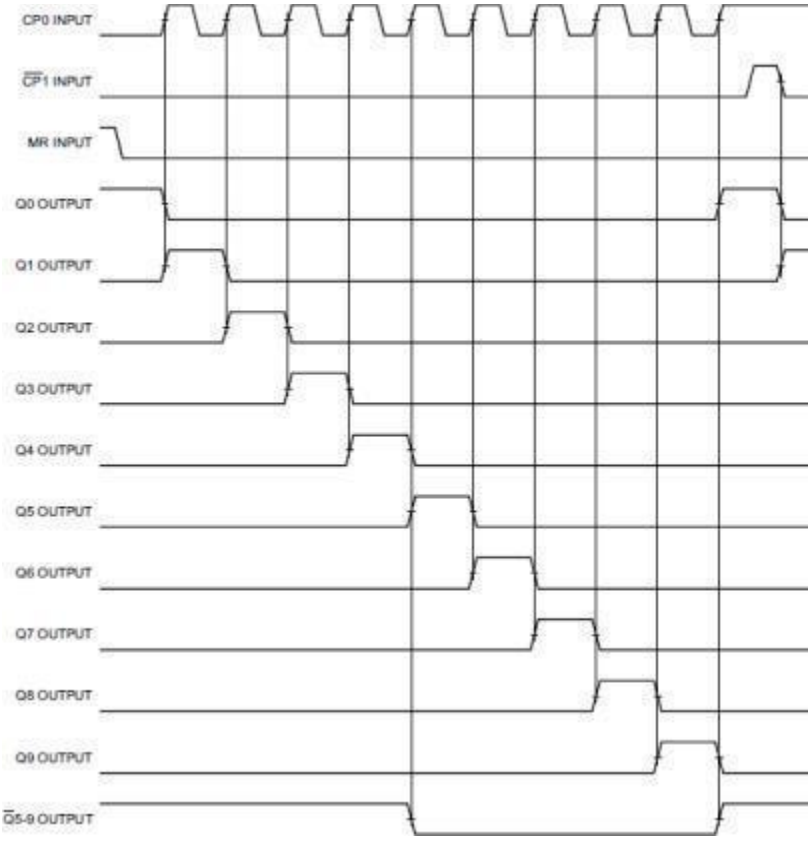
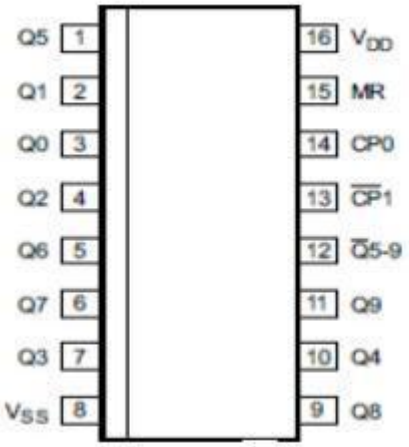


Figure 5 . Timing diagram

2 .2 Pin Configurations



2 . 3 Pin Description

Pin No.	Pin Name	Description
1	Q5	decoded output
2	Q1	decoded output
3	Q0	decoded output
4	Q2	decoded output
5	Q6	decoded output
6	Q7	decoded output
7	Q3	decoded output
8	V_{SS}	ground (0 V)
9	Q8	decoded output
10	Q4	decoded output
11	Q9	decoded output
12	$\overline{Q}$5-9	carry output (active LOW)
13	$\overline{CP}$1	clock input (HIGH- to- LOW edge- triggered)
14	CP0	clock input (LOW- to- HIGH edge- triggered)
15	MR	master reset input
16	V_{DD}	supply voltage

2 .4 Function Table

Input			Operation
MR	CP0	$\overline{CP}$1	
H	X	X	Q0= $\overline{Q}$5 - 9 = H; Q1 to Q9= L
L	H	↓	counter advances
L	↑	L	counter advances
L	L	X	no change
L	X	H	no change
L	H	↑	no change
L	↓	L	no change

Electrical Parameter

Absolute Maximum Ratings

(Voltages are referenced to V_{SS} (ground=0 V) , unless otherwise specified.)

Paramet er	Symbol	Condition s		Min.	Max.	Unit
supply voltage	V_{DD}	-		-0 5	+ 18	V
DC input current	I_{IK}	any one input		-	± 10	mA
input voltage	V_I	all inputs		-0 5	V_{DD}+ 0 5	V
storage temperature	T_{stg}	-		-65	+ 150	℃
total power dissipation	P_{tot}	-		-	500	mW
device dissipation	P	per output transistor		-	100	mW
Soldering temperature	T_L	10s	DIP	245		℃
			SOP	250		

Note:

[1] For DIP16 packages: above 70℃ the value of P_{tot} derates linearly with 12 mW/ K.

[2] For SOP16 packages: above 70 ℃ the value of Ptot derates linearly with 8 mW/ K.

[3] For (T) SSOP16 packages: above 60 ℃ the value of Ptot derates linearly with 5 . 5 mW/ K.

Recommended Operating Conditions

Paramet er	Symbol	Conditions				Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-				3	-	15	V
ambient temperature	T_{amb}	in free air				-40	-	+85	℃
clock input frequency	f_{CL}	V_{DD}= 5 V				-	-	2.5	MHz
		V_{DD}= 10V				-	-	5	MHz
		V_{DD}= 15 V				-	-	5.5	MHz
clock pulse width	t_w	V_{DD}= 5 V				200	-	-	ns
		V_{DD}= 10V				90	-	-	ns
		V_{DD}= 15V				60	-	-	ns
clock rise and fall time	t_{rCL}, t_{fCL}	V_{DD}= 5 V				unlimited			-
		V_{DD}= 10V							-
		V_{DD}= 15V							-
clock inhibit setup time	t_s	V_{DD}= 5 V				230	-	-	ns
		V_{DD}= 10V				100	-	-	ns
		V_{DD}= 15V				70	-	-	ns
reset pulse width	t^{RW}	V_{DD}= 5 V				260	-	-	ns
		V_{DD}= 10 V				110	-	-	ns
		V_{DD}= 15V				60	-	-	ns
reset removal time	t_{rec}	V_{DD}= 5 V				400	-	-	ns
		V_{DD}= 10V				280	-	-	ns
		V_{DD}= 15 V				150	-	-	ns
		-	0, 15	15	-	0.05	-	0.05	V
HIGH- level output voltage	V_{OH}	-	0, 5	5	4.95	-	4.95	-	V
		-	0, 10	10	9.95	-	9.95	-	V
		-	0, 15	15	14.95	-	14.95	-	V
LOW- level input voltage	V_{IL}	0.5, 4.5	-	5	-	1.5	-	1.5	V
		1, 9	-	10	-	3	-	3	V
		1.5, 13.5	-	15	-	4	-	4	V
HIGH- level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	3.5	-	V
		1, 9	-	10	7	-	7	-	V
		1.5, 13.5	-	15	11	-	11	-	V
input leakage current	I_I	-	0, 15	15	-	±0. 1	-	±1	uA

AC Characteristics

(T_{amb}=25℃, V_{SS}=0V, t_r, t_f=20ns, C_L=50pF, R_L=200kΩ, unless otherwise specified.)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
propagation delay time	t_{PHL}, t_{PLH}	$\overline{CP0}$, $\overline{CP1}$ to Q0 to Q9; see Figure 7	V_{DD}=5V	-	325	650	ns
			V_{DD}=10V	-	135	270	ns
			V_{DD}=15V	-	85	170	ns
		CP0, $\overline{CP1}$ to Q5-9; see Figure 7	V_{DD}=5V	-	300	600	ns
			V_{DD}=10V	-	125	250	ns
			V_{DD}=15V	-	80	160	ns
		MR to Q0 to Q9; see Figure 7	V_{DD}=5V	-	265	530	ns
			V_{DD}=10V	-	115	230	ns
			V_{DD}=15V	-	85	170	ns
transition time	t_t	see Figure 7	V_{DD}=5V	-	100	200	ns
			V_{DD}=10V	-	50	100	ns
			V_{DD}=15V	-	40	80	ns
pulse width	t_W	see Figure 8	V_{DD}=5V	-	100	200	ns
			V_{DD}=10V	-	45	90	ns
			V_{DD}=15V	-	30	60	ns
clock rise and fall time	t_{rCL}, t_{fCL}	-	V_{DD}=5V	unlimited			-
			V_{DD}=10V				-
			V_{DD}=15V				-
maximum clock frequency	f_{CL}	see Figure 8	V_{DD}=5V	2.5	5	-	MHz
			V_{DD}=10V	5	10	-	MHz
			V_{DD}=15V	5.5	11	-	MHz
setup time	t_s	$\overline{CP0}$ to $\overline{CP1}$; see Figure 9	V_{DD}=5V	-	115	230	ns
			V_{DD}=10V	-	50	100	ns
			V_{DD}=15V	-	35	70	ns
reset removal time	t_{rec}	MR input; see Figure 8	V_{DD}=5V	-	200	400	ns
			V_{DD}=10V	-	140	280	ns
			V_{DD}=15V	-	75	150	ns
input capacitance	C_I	any input		-	5	-	pF

Note: t_t is the same as t_{TLH} and t_{THL}.

Testing Circuit

AC Testing Circuit

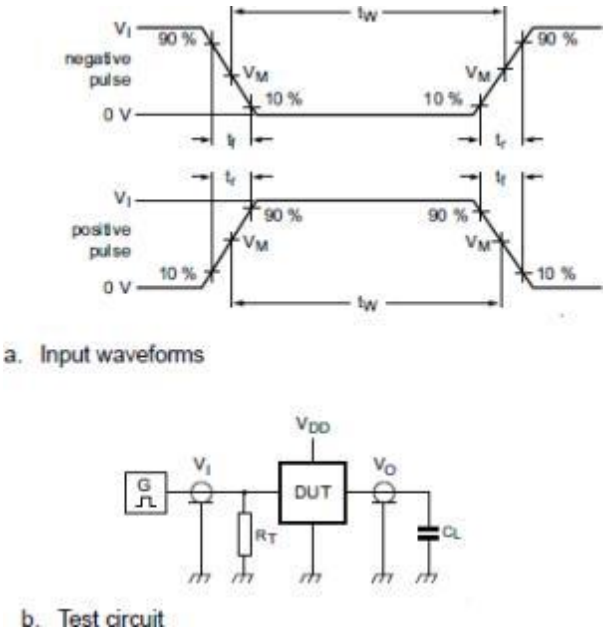


Figure 6. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

AC Testing Waveforms

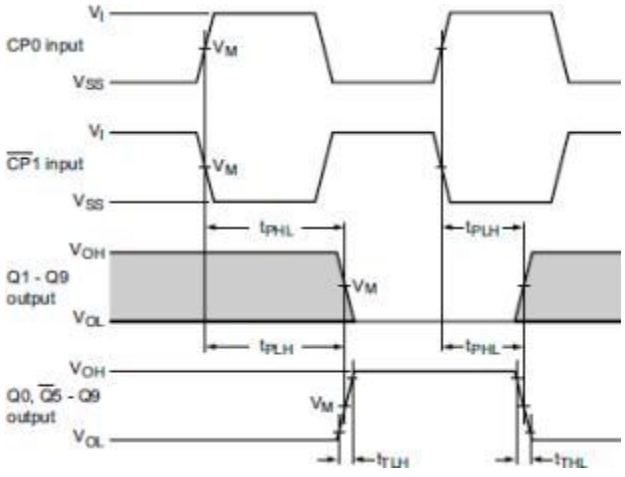


Figure 7. Waveforms showing the propagation delays for CP0, CP1 to Qn, Q5-9 outputs and the output transition times

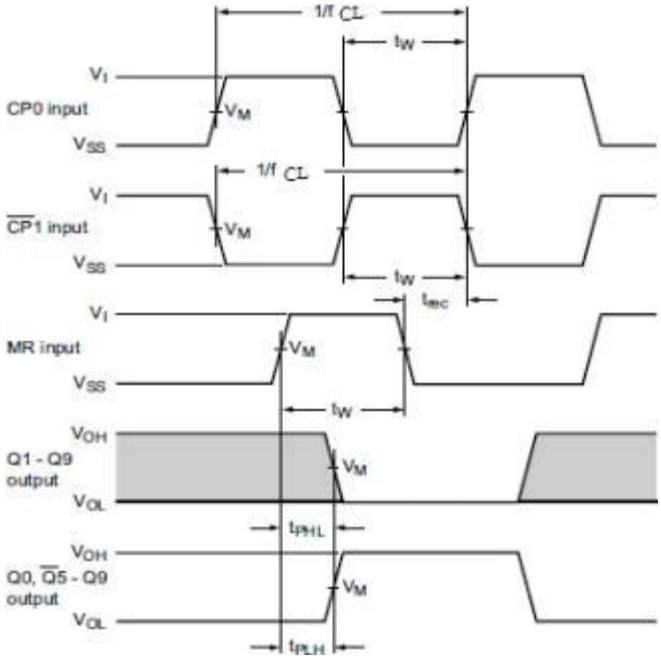


Figure 8. Waveforms showing the minimum pulse width for CP0, $\overline{CP1}$ and MR input; the maximum frequency for CP0 and $\overline{CP1}$ input; the recovery time for MR and the MR input to Qn and Q5-9 output propagation dela

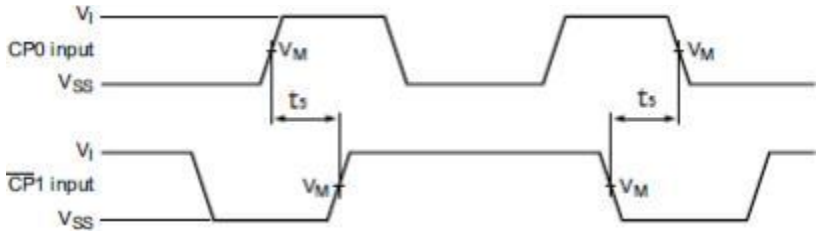


Figure 9. Waveforms showing hold times for CP0 to $\overline{CP1}$ and $\overline{CP1}$ to CP0

Measurement Points

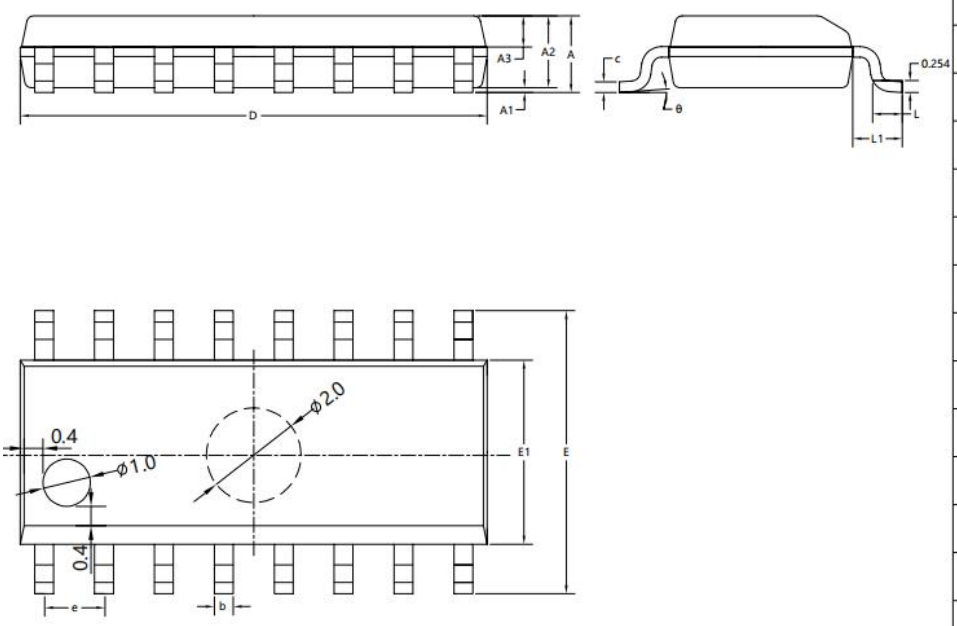
Supply voltage	Input	Output
V_{DD}	V_M	V_M
5V to 15V	$0.5\times V_{DD}$	$0.5\times V_{DD}$

Test Data

Supply voltage	Input		Load
V_{DD}	V_I	t_r , t_f	C_L
5V to 15V	V_{SS} or V_{DD}	≤ 20ns	50pF

Package Information

SOP16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.50	1.60	1.70
A1	0.10	0.15	0.25
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.85	3.90	3.95
e	1.27BSC		
L	0.50	0.60	0.70
L1	1.05BSC		
θ	0°	4°	8°

Statement：

✧ Shenzhen xinbole electronics co., ltd. reserves the right to change the product specifications, without notice! Before placing an order, the customer needs to confirm whether the information obtained is the latest version, and verify the integrity of the relevant information.

✧ Any semiconductor product is liable to fail or malfunction under certain conditions, and the buyer shall be responsible for complying with safety standards in the system design and whole machine manufacturing using Shenzhen xinbole electronics co., ltd products, and take appropriate security measures to avoid the potential risk of failure may result in personal injury or property losses of the situation occurred!

✧ This document is for referenceonly,and the actual use should be based on the application test results.

✧ Product performance is never ending, Shenzhen xinbole electronics co., ltd will be dedicated to provide customers with better performance, better quality of integrated circuit products.