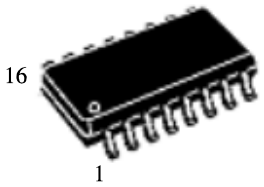
DESCRIPTION

The MAX202 device consists of two line drivers, two line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND).
The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 5-V supply. The device operates at data signaling rates up to 120 kbit/s and a maximum of 30-V/μs driver output slew rate.



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FEATURES

- ESD Protection for RS-232 Bus Pins
  - ±15-kV - Human-Body Model
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards
- Operates at 5-V VCC Supply
- Operates Up To 120 kbit/s
- External Capacitors...4 × 0.1 μF
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II·

APPLICATIONS

- Battery-Powered System
- Notebooks
- Hand-Held devices
- Portable computer

FUNCTION TABLE

Each Driver

INPUT DIN	OUTPUT DOUT
L	H
H	L

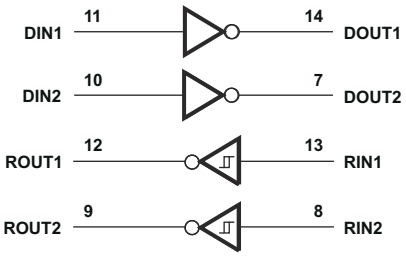
H = high level, L = low level

Each Receiver

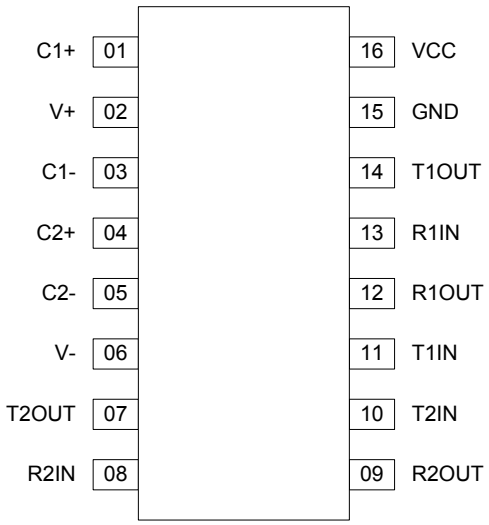
INPUT RIN	OUTPUT ROUT
L	H
H	L
Open	H

H = high level, L = low level,
Open = input disconnected or connected driver off

Logic Diagram (Positive Logic)



PIN CONFIGURATION



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PIN DESCRIPTION

Pin No.	Pin Name	Pin Description
1	C1+	Terminal for Positive Charge-Pump C1 Capacitor
2	V+	Positive Voltage Generated by the Charge-Pump
3	C1-	Terminal for Negative Charge-Pump C1 Capacitor
4	C2+	Terminal for Positive Charge-Pump C2 Capacitor
5	C2-	Terminal for Negative Charge-Pump C2 Capacitor
6	V-	Negative Voltage Generated by the Charge-Pump
7	T2OUT	RS-232 Driver Output (Levels RS-232)
8	R2IN	RS-232 Receiver Input (Levels RS-232)
9	R2OUT	RS-232 Receiver Output (Levels TTL/CMOS)
10	T2IN	RS-232 Driver Input (Levels TTL/CMOS)
11	T1IN	RS-232 Driver Input (Levels TTL/CMOS)
12	R1OUT	RS-232 Receiver Output (Levels TTL/CMOS)
13	R1IN	RS-232 Receiver Input (Levels RS-232)
14	T1OUT	RS-232 Driver Output (Levels RS-232)
15	GND	Ground
16	VCC	Supply Voltage Input

SPECIFICATIONS

Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Supply Voltage	V_{CC}	-0.3	6.0	V
Transmitter High Output Voltage	V_+	V_{CC}-0.3	14	V
Transmitter Low Output Voltage	V_-	-0.3	-14	V
Transmitter Input Voltage	V_{TIN}	-0.3	V_++0.3	V
Receiver Input Voltage	V_{RIN}	-30	30	V
Voltage Applied to Transmitter Output	V_{TOUT}	V_--0.3	V_++0.3	V
Voltage Applied to Receiver Output	V_{ROUT}	-0.3	V_{CC}+0.3	V
Storage Temperature Range	T_{STG}	-65	150	°C

ESD protection

PIN	TEST CONDITIONS	TYP	UNIT
D_{OUT}, R_{IN}	Human-Body Model	±15	kV

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted(1))

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
	Supply voltage	4.5	5	5.5	V
V_{IH}	Driver high-level input voltage (D_{IN})	2			V
V_{IL}	Driver low-level input voltage (D_{IN})			0.8	V
V_I	Driver input voltage (D_{IN})	0		5.5	V
	Receiver input voltage	-30		30	

(1) Test conditions are C1 – C4 = 0.1μF at V_{CC} = 5V ±0.5V.

Thermal Information

SYMBOL	THERMAL METRIC	TYP	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	°C/W

Electrical Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
I_{CC}	Supply current	No load, V_{CC} = 5 V		8	15	mA

(1) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

Driver Section

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	D_{OUT} at R_L = 3kΩ to GND, D_{IN} = GND	5	9		V
V_{OL}	Low-level output voltage	D_{OUT} at R_L = 3kΩ to GND, D_{IN} = V_{CC}	−5	−9		V
I_{IH}	High-level input current	V_I = V_{CC}		0	200	μA
I_{IL}	Low-level input current	V_I at 0V		0	−200	μA
I_{OS} (1)	Short-circuit output current	V_{CC} = 5.5V, V_O = 0V		±10	±60	mA
r_O	Output resistance	V_{CC}, V+, and V− = 0V, V_O = ±2V	300			Ω

(1) Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.

Receiver Section

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −1mA	3.5	V_{CC} − 0.4		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 5V, T_A = 25°C		1.7	2.4	V
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 5V, T_A = 25°C	0.8	1.2		V
V_{hys}	Input hysteresis (V_{IT+} − V_{IT-})		0.2	0.5	1	V
r_i	Input resistance	V_I = ±3V to ±25V	3	5	7	kΩ

SWITCHING CHARACTERISTICS

Driver Section

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Maximum data rate	C_L = 50pF to 1000pF, R_L = 3kΩ to 7kΩ one D_{OUT} switching	120			kbit/s
$t_{PLH(D)}$	Propagation delay time, low- to high-level output	C_L = 2500pF, R_L = 3kΩ, all drivers loaded		2		μs
$t_{PHL(D)}$	Propagation delay time, high- to low-level output	C_L = 2500pF, R_L = 3kΩ, all drivers loaded		2		μs
$t_{sk(p)}$	Pulse skew(1)	C_L = 150 to 2500pF, R_L = 3kΩ to 7 kΩ		300		ns
SR(tr)	Slew rate, transition region	C_L = 50 to 1000pF, R_L = 3kΩ to 7 kΩ, V_{CC} = 5V	3	6	30	V/μs

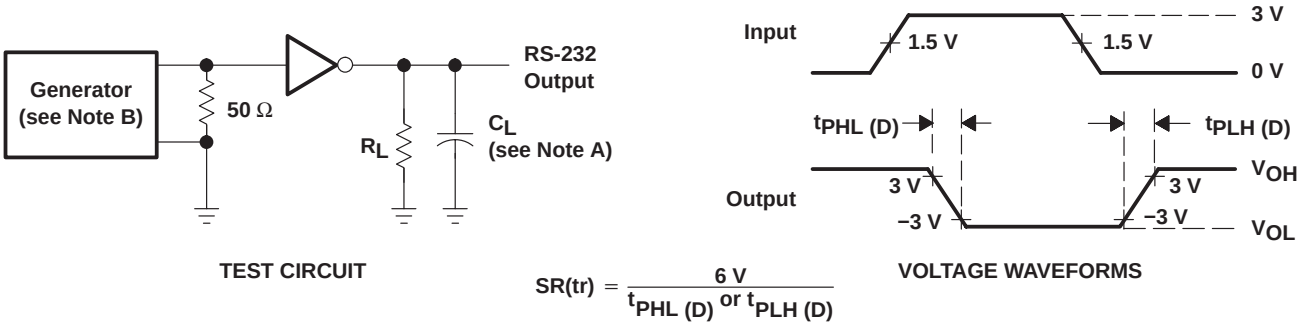
(1) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

Receiver Section

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(R)}$	Propagation delay time, low- to high-level output	C_L = 150pF		0.5	10	μs
$t_{PHL(R)}$	Propagation delay time, high- to low-level output	C_L = 150pF		0.5	10	μs
$t_{sk(p)}$	Pulse skew(1)	C_L = 150pF		300		ns

(1) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

PARAMETER MEASUREMENT INFORMATION



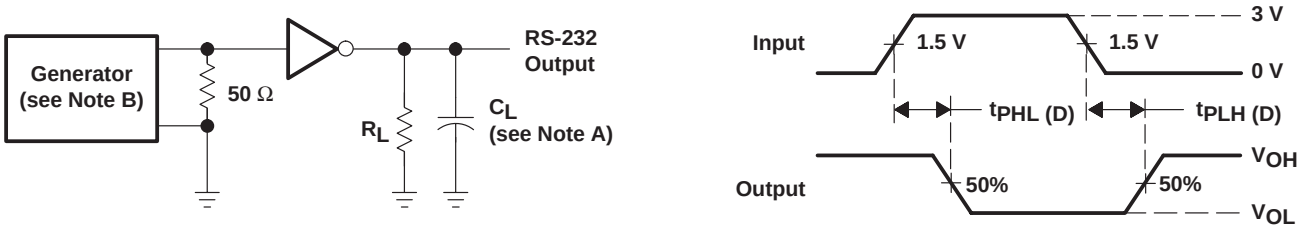
TEST CIRCUIT

VOLTAGE WAVEFORMS

$$SR(tr) = \frac{6\ V}{t_{PHL\ (D)} \text{ or } t_{PLH\ (D)}}$$

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 120 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 1. Driver Slew Rate

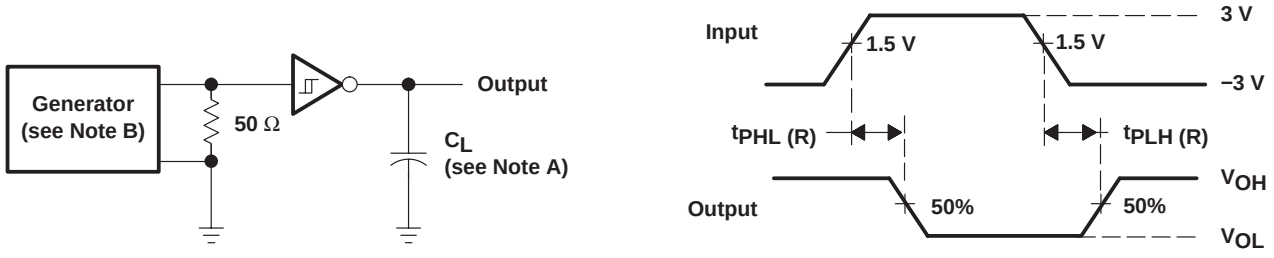


TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 120 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 2. Driver Pulse Skew



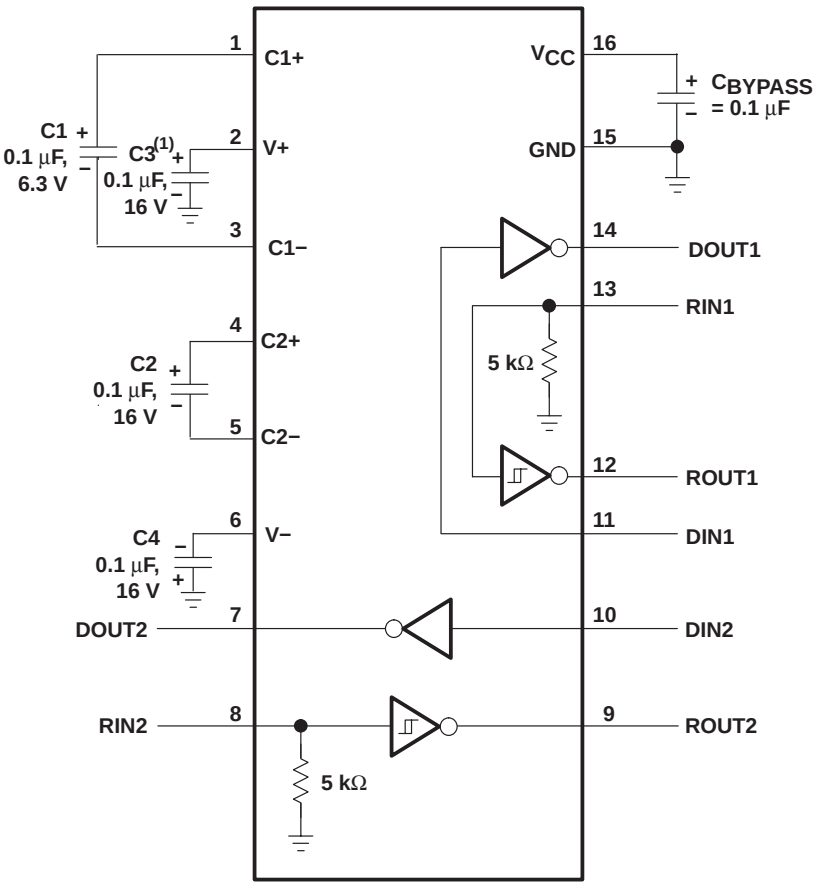
TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 3. Receiver Propagation Delay Times

APPLICATION INFORMATION



(1) C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

Figure 4. Typical Operating Circuit and Capacitor Values

APPLICATION INFORMATION

Capacitor Selection

The capacitor type used for C1 through C4 is not critical for proper operation. The MAX202 requires 0.1µF capacitors. Capacitors up to 10µF can be used without harm. Ceramic dielectrics are suggested for the 0.1µF capacitors. When using the minimum recommended capacitor values, make sure the capacitance value does not degrade excessively as the operating temperature varies. If in doubt, use capacitors with a larger (for example, 2×) nominal value. The capacitors' effective series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V－.

Use larger capacitors (up to 10µF) to reduce the output impedance at V+ and V－.

Bypass V_{CC} to ground with at least 0.1µF. In applications sensitive to power-supply noise generated by the charge pumps, decouple V_{CC} to ground with a capacitor the same size as (or larger than) the charge-pump capacitors (C1 to C4).

ESD Protection

MAX202 devices have standard ESD protection structures incorporated on all pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS-232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ±15kV when powered down.

ESD Test Conditions

Stringent ESD testing is performed by TI based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

Human-Body Model (HBM)

The HBM of ESD testing is shown in Figure 5,Figure 6 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the device under test (DUT) through a 1.5-kΩ resistor.

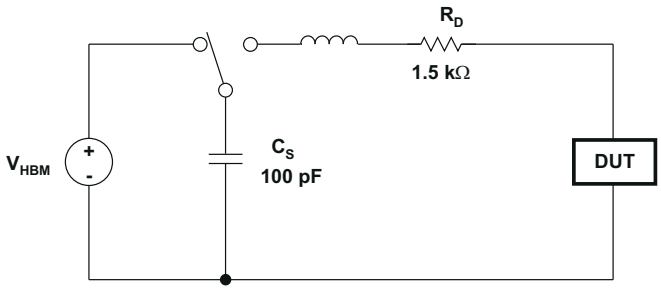


Figure 5. HBM ESD Test Circuit

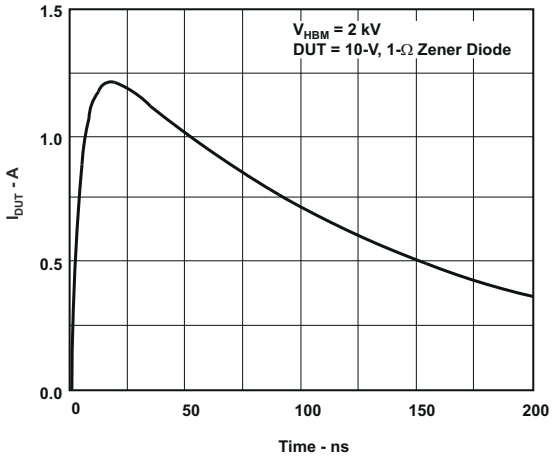


Figure 6. Typical HBM Current Waveform

Machine Model (MM)

The MM ESD test applies to all pins using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test no longer is as pertinent to the RS-232 pins.

PACKAGE OUTLINE DIMENSIONS

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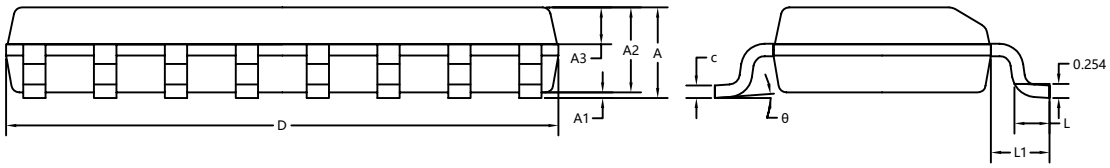

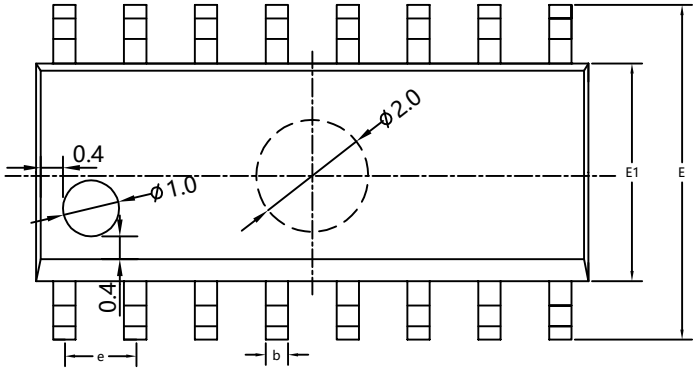

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.50	1.60	1.70
A1	0.10	0.15	0.25
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.85	3.90	3.95
e	1.27BSC		
L	0.50	0.60	0.70
L1	1.05BSC		
θ	0°	4°	8°

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