NOT RECOMMENDED FOR NEW DESIGNS

HI5816

May 1997

CMOS 12-Bit Sampling A/D Converter with Serial Data Output and Internal Track and Hold

Features

- 20µs Conversion Time
- 50KSPS Throughput Rate
- Built-In Track and Hold
- Guaranteed No Missing Codes Over Temperature
- Single +5V Supply Voltage
- 15mW Maximum Power Consumption
- Internal or External Conversion Clock
- Direct Three Wire Interface to Most MPU Serial Ports
  - SPI™ and QSPI™
  - Microwire™
- Available in 16 Lead Small Shrink Outline Plastic Package (SSOP)
- Flexible Conversion Modes

Applications

- Remote Low Power Data Acquisition Systems
- µP Controlled Measurement Systems
- DSP Modems
- General Purpose DSP Front End

Description

The HI5816 is a fast, low power, 12-bit successive approximation analog-to-digital converter. It can operate from a single 3V to 6V supply and typically draws just 2.0mA when operating at 5V. The HI5816 features a built-in track and hold.
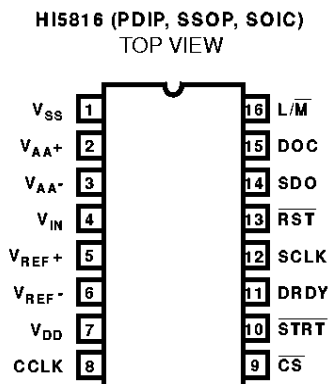
The serial data output features full high speed CMOS three-state bus driver capability. Data is output at the SDO output in two different modes. With DOC = 1 the data is output as the conversion takes place. With DOC = 0 the data is available after a complete conversion and can be read at up to 5MHz in either MSB first or LSB first format. The chip select input enables/disables the SDO pin and a data ready flag signals the end of a conversion.

An internal conversion clock is provided and is available as an output. The conversion clock may also be over-driven by an external source.

Pinout

HI5816 (PDIP, SSOP, SOIC)
TOP VIEW

V$_{SS}$	1	16	L/$\overline{M}$
V$_{AA}$+	2	15	DOC
V$_{AA}$-	3	14	SDO
V$_{IN}$	4	13	$\overline{RST}$
V$_{REF}$+	5	12	SCLK
V$_{REF}$-	6	11	DRDY
V$_{DD}$	7	10	$\overline{STRT}$
CCLK	8	9	$\overline{CS}$

Ordering Information

PART NUMBER	INL (LSB) (MAX OVER TEMP)	TEMPERATURE RANGE	PACKAGE
HI5816KIP	±0.75	-40°C to +85°C	16 Lead Plastic DIP
HI5816KIA†	±0.75	-40°C to +85°C	16 Lead SSOP
HI5816KIB	±0.75	-40°C to +85°C	16 Lead SOIC (W)

W = Wide body package

† Consult factory for availability

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SPI™, QSPI™ are trademarks of Motorola

File Number **3664.1**

Functional Block Diagram
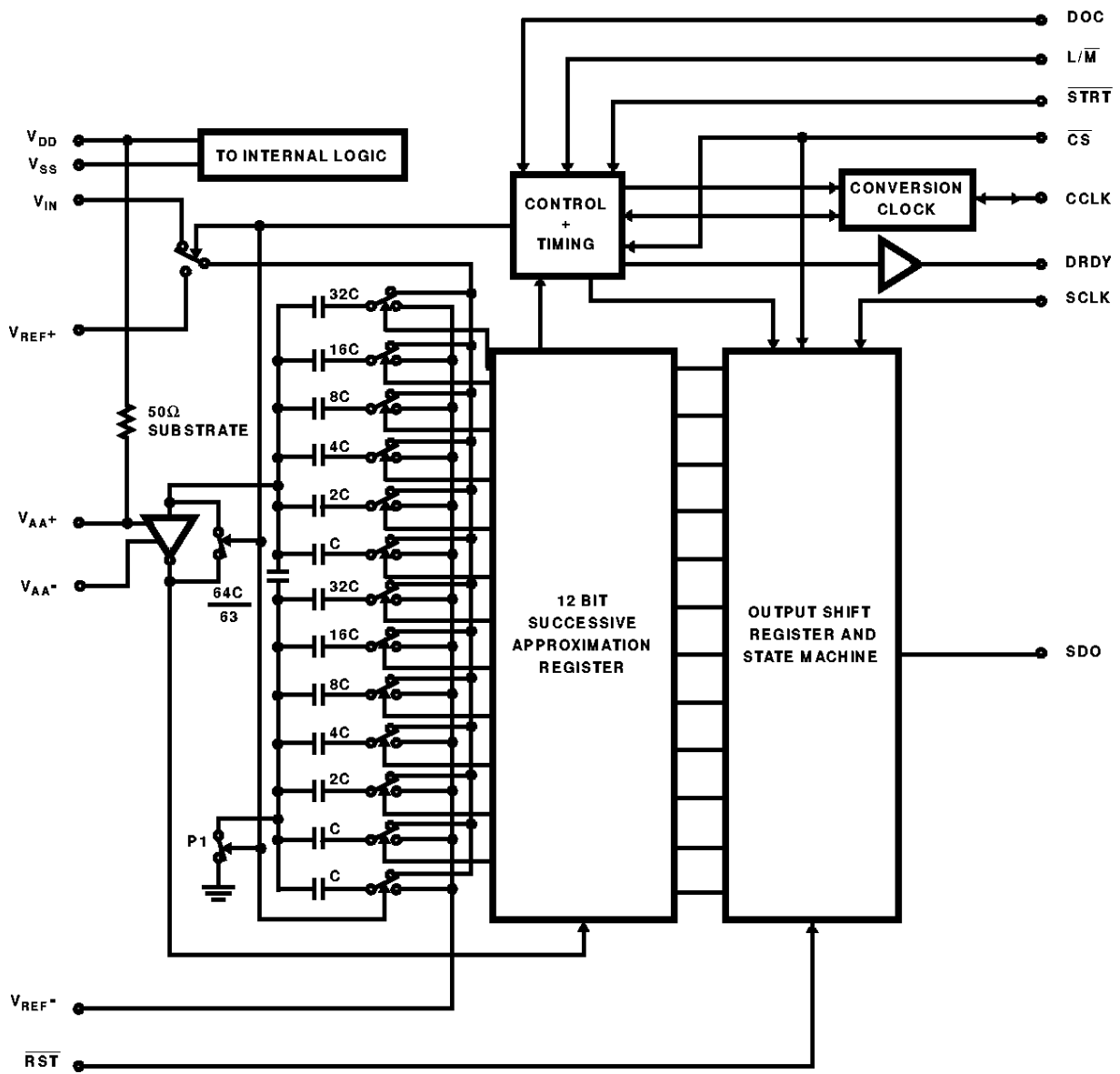
Absolute Maximum Ratings

Supply Voltage

V_{DD} to V_{SS} . . . . (V_{SS} -0.5V) < V_{DD} < +6.5V

V_{AA}+ to V_{AA}- . . . . (V_{SS} -0.5V) to (V_{SS} +6.5V)

V_{AA}+ to V_{DD}. . . . .±0.3V

Analog and Reference Inputs

V_{IN}, V_{REF}+, V_{REF}- . . . . (V_{SS} -0.2V) < V_{INA} < (V_{DD} +0.2V)

Digital I/O Pins . . . . (V_{SS} -0.2V) < VI/O < (V_{DD} +0.2V)

Operating Temperature Range

Plastic DIP, SSOP, SOIC. . . . . -40°C to +85°C

Junction Temperature

Plastic DIP, SSOP, SOIC. . . . . +150°C

Storage Temperature Range . . . . -65°C to +150°C

Lead Temperature (Soldering, 10s) . . . . 300°C

Thermal Information

Thermal Resistance θ_{JA}

Plastic DIP . . . . 90°C/W

Plastic SSOP . . . . 155°C/W

Plastic SOIC . . . . 100°C/W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $V_{DD} = V_{AA}+ = V_{REF}+ = 5V$, $V_{SS} = V_{AA}- = V_{REF}- = GND$, CCLK = External 750kHz, (Conversion Time = 20µs) Unless Otherwise Specified

PARAMETER	TEST CONDITION	+25°C			-40°C TO +85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
ACCURACY							
Resolution		12	-	-	12	-	Bits
Integral Linearity Error, INL (End Point)		-	0.35	±0.75	-	±0.75	LSB
Differential Linearity Error, DNL		-	0.35	±1.0	-	±1.0	LSB
Gain Error, FSE (Adjustable to Zero)		-	-0.4	±2.0	-	±2.0	LSB
Offset Error, V_{OS} (Adjustable to Zero)		-	0.8	±2.0	-	±2.0	LSB
Power Supply Rejection, PSRR Offset Error PSRR	$V_{REF} = 4V$ $V_{DD} = V_{AA}+ = 5V ±5\%$	-	0.1	±0.5	-	±0.5	LSB
Gain Error PSRR		-	0.1	±0.5	-	±0.5	LSB
ANALOG INPUT							
Input Current, Dynamic	At $V_{IN} = V_{REF}+$, 0V	-	±50	±100	-	±100	µA
Input Current, Static	Conversion Stopped	-	±0.4	±10	-	±10	µA
Input Bandwidth -3dB		-	1	-	-	-	MHz
Reference Input Current		-	160	-	-	-	µA
Input Series Resistance, R_S	In Series with Input C_{SAMPLE}	-	420	-	-	-	Ω
Input Capacitance, C_{SAMPLE}	During Sample State	-	380	-	-	-	pF
Input Capacitance, C_{HOLD}	During Hold State	-	20	-	-	-	pF
DIGITAL INPUTS							
High-Level Input Voltage, V_{IH}		2.4	-	-	2.4	-	V
Low-Level Input Voltage, V_{IL}		-	-	0.8	-	0.8	V
Input Leakage Current, I_{IL}	Except CCLK, V_{IN} = 0V, 5V	-	-	±10	-	±10	µA
Input Capacitance, C_{IN}		-	10	-	-	-	pF

Electrical Specifications $V_{DD} = V_{AA^+} = V_{REF^+} = 5V$, $V_{SS} = V_{AA^-} = V_{REF^-} = GND$, CCLK = External 750kHz, (Conversion Time = 20µs) Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	+25°C			-40°C TO +85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
DIGITAL OUTPUTS							
High-Level Output Voltage, V_{OH}	I_{SOURCE} = -400µA	4.6	-	-	4.6	-	V
Low-Level Output Voltage, V_{OL}	I_{SINK} = 1.6mA	-	-	0.4	-	0.4	V
Three-State Leakage, I_{OZ}	V_{OUT} = 0V, 5V	-	-	±10	-	±10	µA
Output Capacitance, C_{OUT}		-	20	-	-	-	pF
CONVERSION CLOCK							
High-Level Output Voltage, V_{OH}	I_{SOURCE} = -100µA (Note 2)	4	-	-	4	-	V
Low-Level Output Voltage, V_{OL}	I_{SINK} = 100µA (Note 2)	-	-	1	-	1	V
Input Current	CCLK Only, V_{IN} = 0V, 5V	-	-	±5	-	±5	mA
TIMING							
Conversion Time (t_{CONV} + t_{ACQ}) (Includes Acquisition Time)		20	-	-	20	-	µs
Conversion Clock Frequency	Internal Clock, (CCLK = Open)	200	300	400	150	550	kHz
	External CCLK (Note 2)	0.05	2	1.5	0.05	1.5	MHz
Conversion Clock Pulse Width, t_{LOW}, t_{HIGH}	External CCLK (Note 2)	100	-	-	100	-	ns
Conversion Clock to Data Ready Delay, t_{D1}DRDY	(Note 2)	-	105	150	-	180	ns
Conversion Clock to Data Ready Delay, t_{D2}DRDY	(Note 2)	-	100	160	-	195	ns
Start Removal Time, $t_R\overline{STRT}$	(Note 2)	75	30	-	75	-	ns
Start Setup Time, $t_{SU}\overline{STRT}$	(Note 2)	85	60	-	100	-	ns
Start Pulse Width, $t_W\overline{STRT}$	(Note 2)	10	4	-	15	-	ns
Start to Data Ready Delay, t_{D3} DRDY	(Note 2)	-	65	105	-	120	ns
Conversion Clock Delay from Start, $t_D\overline{STRT}$	(Note 2)	-	60	-	-	-	ns
SCLK to SDO Valid, t_{DV}	(Note 2)	-	50	55	-	65	ns
$\overline{CS}$ to SCLK Falling Setup Time, t_{ESU}	(Note 2)	20	-	-	25	-	ns
$\overline{CS}$ Active to SDO Valid, t_{ELOV}	(Note 2)	-	-	40	-	45	ns
$\overline{CS}$ Inactive to SDO Three-State, t_{EHOZ}	(Note 2)	-	-	35	-	40	ns
Read Time Without Losing a Data Word, t_{READ}	(Notes 2, 3)	-	-	20	-	20	µs
SCLK Period, T_{SCLK}	(Note 2)	200	-	-	200	-	ns
POWER SUPPLY CHARACTERISTICS							
Supply Current, I_{DD} + I_{AA}		-	2.0	3.0	-	3.5	mA

NOTES:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

2. Parameter guaranteed by design or characterization, not production tested.

3. $t_{READ} = \dfrac{15}{F_{CCLK}}$ (starting at rising edge of DRDY).
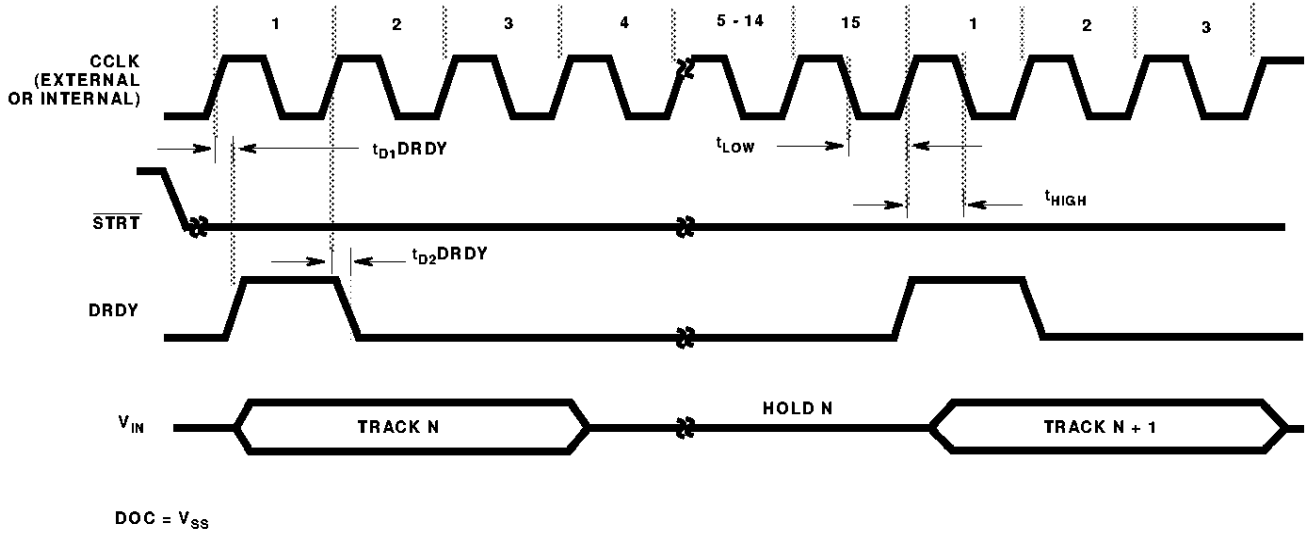
Timing Diagrams

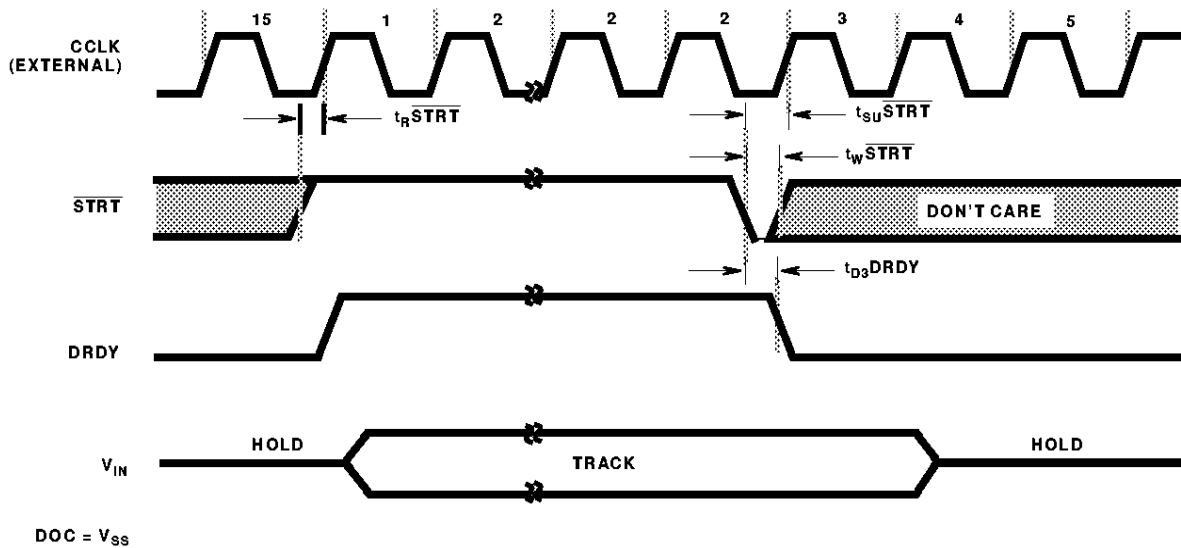**FIGURE 1. CONTINUOUS CONVERSION MODE**

FIGURE 2. SINGLE SHOT MODE EXTERNAL CONVERSION CLOCK
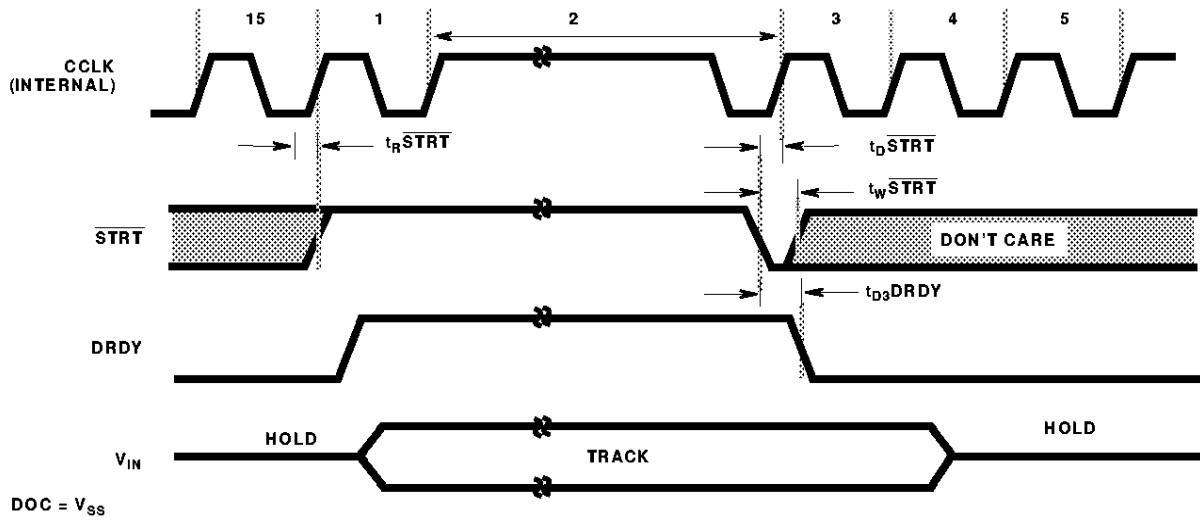
Timing Diagrams (Continued)

FIGURE 3. SINGLE SHOT MODE INTERNAL CLOCK
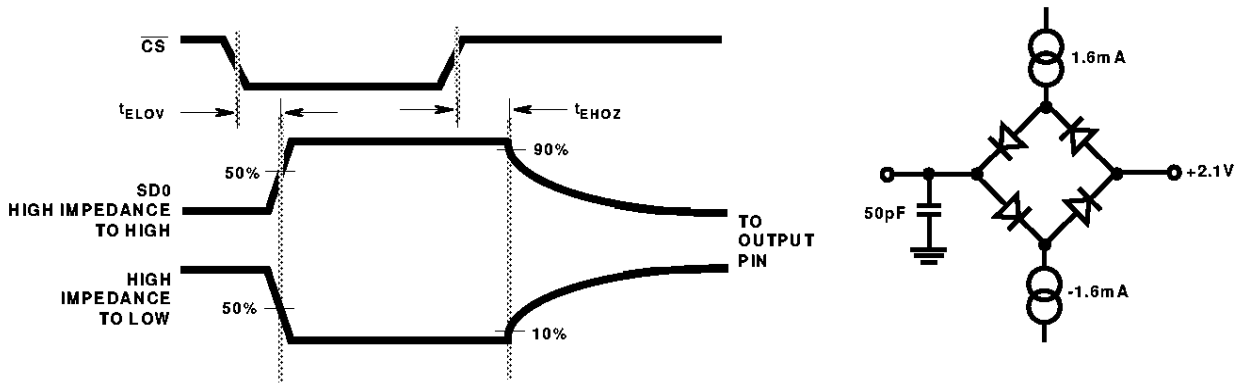

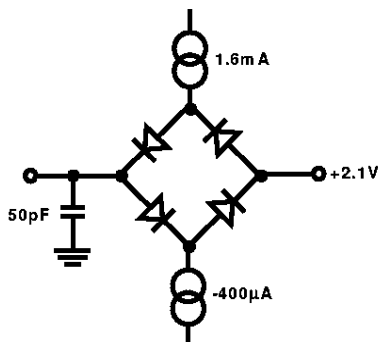FIGURE 4. OUTPUT ENABLE/DISABLE TIMING DIAGRAM

FIGURE 5. GENERAL TIMING LOAD CIRCUIT
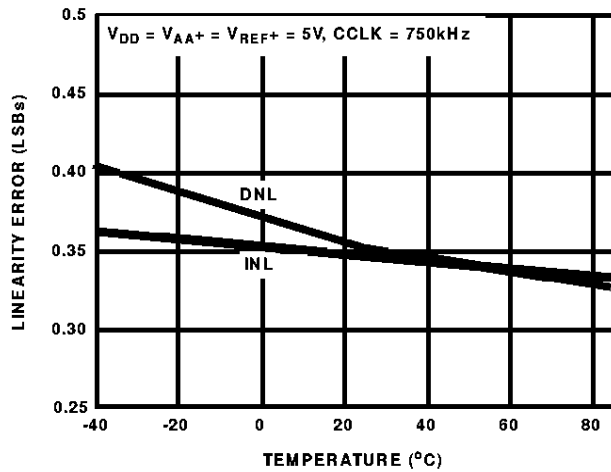
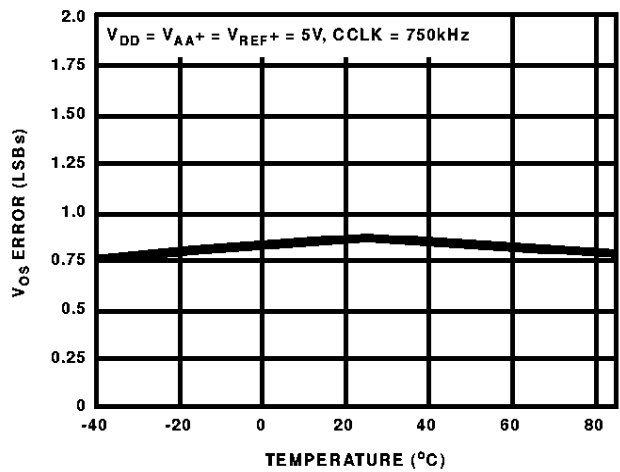## *Typical Performance Curves*

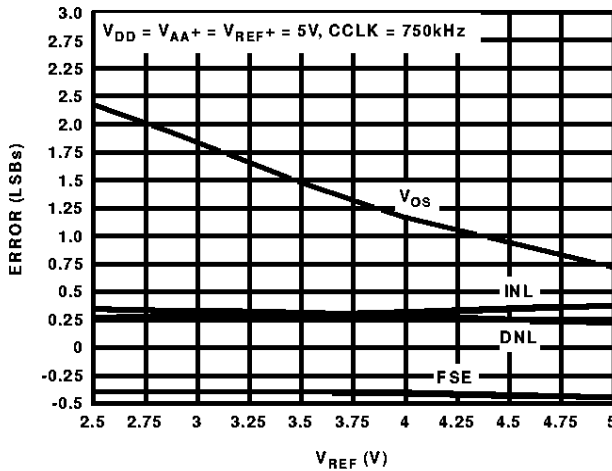FIGURE 6. LINEARITY vs TEMPERATURE

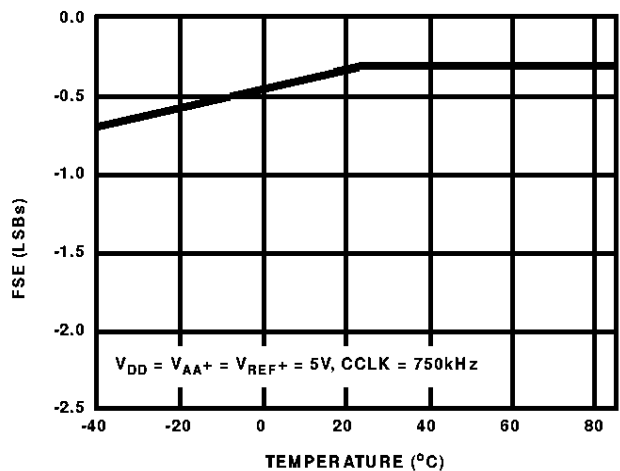FIGURE 7. OFFSET ERROR vs TEMPERATURE

FIGURE 8. ACCURACY vs REFERENCE VOLTAGE
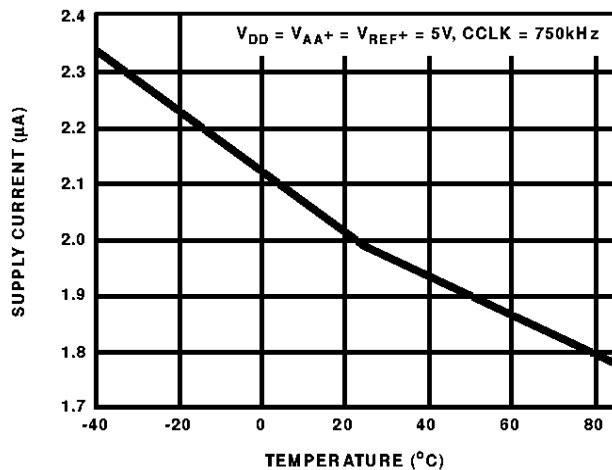

FIGURE 9. FULL SCALE ERROR vs TEMPERATURE

FIGURE 10. SUPPLY CURRENT vs TEMPERATURE

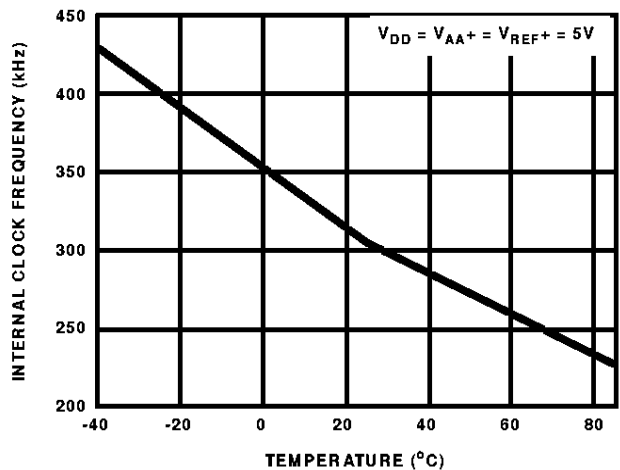FIGURE 11. INTERNAL CLOCK FREQUENCY vs TEMPERATURE

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TABLE 1. PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	V_{SS}	Digital ground, (0V).
2	$V_{AA}+$	Analog positive supply. (+5V) (See text)
3	$V_{AA}-$	Analog ground (0V).
4	V_{IN}	Analog input.
5	$V_{REF}+$	Reference voltage positive input, sets 4095 code end of input range.
6	$V_{REF}-$	Reference voltage negative input, sets 0 code end of input range.
7	V_{DD}	Digital positive supply (+5V).
8	CCLK	CCLK input or output. Conversion functions are synchronized to positive going edge. (See text) (Valid for DOC = 0 only)
9	$\overline{CS}$	Chip Select. Low; SDO enabled. High; SDO three-stated.
10	$\overline{STRT}$	Start conversion input (active low), recognized after end of conversion clock period 15. (Valid for DOC = 0 only)
11	DRDY	Output flag signifying new data is available. Goes high at end of conversion clock period 15. Goes low when new conversion is started.
12	SCLK	Serial Data Clock. Clocks data out at SDO. Also acts as conversion clock when DOC is high. (See text)
13	$\overline{RST}$	Active low I/O state machine reset. Does not affect converter state machine
14	SDO	Serial Data Out
15	DOC	Data On Conversion. High; data output to SDO as it is determined. Low; normal operation. (See text)
16	$L/\overline{M}$	Serial Data Out format control. High; LSB first. Low; MSB first. (Valid for DOC = 0 only)

Theory of Operation

A/D Conversion

HI5816 is a CMOS 12-Bit Analog-to-Digital Converter that uses capacitor-charge balancing to successively approximate the analog input. A binary weighted capacitor network forms the heart of the A/D converter (see Block Diagram).

The capacitor network has a common node which is connected to a comparator. The second terminal of each capacitor is individually switchable to the input, $V_{REF}+$ or $V_{REF}-$.

During the first three conversion clock periods of a conversion cycle, the switchable end of every capacitor is connected to the input and the comparator is being auto-balanced at the capacitor common node.

During the fourth period, all capacitors are disconnected from the input; the one representing the MSB (b11) is connected to the $V_{REF}+$ terminal; and the remaining

capacitors to $V_{REF}-$. The capacitor-common node, after the charges balance out, will indicate whether the input was above $^{1}/_{2}$ of ($V_{REF}+$ - $V_{REF}-$). At the end of the fourth period, the comparator output is stored and the MSB capacitor is either left connected to $V_{REF}+$ (if the comparator was high) or returned to $V_{REF}-$. This allows the next comparison to be at either $^{3}/_{4}$ or $^{1}/_{4}$ of ($V_{REF}+$ - $V_{REF}-$).

At the end of periods 5 through 14, capacitors representing b10 through b1 are tested, the result stored, and each capacitor either left at $V_{REF}+$ or at $V_{REF}-$.

The conversion is completed at the end of the 15th period when the LSB (b0) capacitor is tested. The capacitors are then reconnected to the input, the comparator returned to the balance state, and the data-ready output goes active. The conversion cycle is finished and data can be read out at the SDO pin.

Operational Modes

The HI5816 supports two operational modes controlled by the state of the DOC input pin.

The Data On Convert mode (DOC = 1), produces data at the SDO pin as the conversion is occurring. That is, data is available on every clock cycle and is shifted out in MSB first format.

When DOC = 0, the Serial Interface mode is operational and the data is accessible after a conversion has been completed. The serial interface for the HI5816 is a 3-wire interface which is compatible with standard SPI, QSPI, and Microwire interfaces. The three pins used for the interface are the SDO, SCLK, and $\overline{CS}$ pins.

Both modes have unique advantages and are discussed in detail below.

Serial Interface Mode (DOC = 0)

With DOC = 0, the HI5816 may be synchronized from an external source by using the $\overline{STRT}$ (Start Conversion) input to initiate conversion. If $\overline{STRT}$ is tied low, the HI5816 will free run in the continuous conversion mode. The CCLK pin is used for the conversion clock and the SCLK pin is used to read the data.

When the $\overline{STRT}$ input is used to initiate conversions, operation is slightly different depending on whether an internal or external conversion clock is used. Figure 3 illustrates operation with an internal conversion clock. If the $\overline{STRT}$ signal is removed (at least $T_R\overline{STRT}$) before conversion clock period 1, and is not reapplied during that period, the conversion clock will shut off after entering period 2. The input will continue to track during this time. A low signal applied to $\overline{STRT}$ (at least $T_W\overline{STRT}$ wide) can now initiate a new conversion. The $\overline{STRT}$ signal (after a delay of ($T_D\overline{STRT}$)) causes the conversion clock to restart. Depending on how long the conversion clock was shut off, the low portion of conversion clock period 2 may be longer than during the remaining cycles. The input will continue to track until the end of period 3, the same as when free running.

Figure 2 illustrates the same operation as above but with an external conversion clock. If the $\overline{STRT}$ signal is removed (at least $T_R\overline{STRT}$) before conversion clock period 1, and is not

reapplied during that period, the converter will stall after entering period 2. The HI5816 will continue to track the input while the $\overline{\text{STRT}}$ pin is continuously sampled. A signal applied to $\overline{\text{STRT}}$ (at least $T_W\overline{\text{STRT}}$ wide) can now initiate a new conversion. The input will continue to track until the end of period 3, the same as when free running.

After a conversion is complete, the DRDY (Data Ready) status output goes high (specified by T_{D1}DRDY) indicating a valid result is available for reading. In continuous conversion mode, DRDY returns low (specified by T_{D2}DRDY) after one conversion clock period (See Figure 1). If conversion has been stalled, DRDY remains high until the converter is restarted (See Figures 2 and 3)

After a DRDY interrupt has been issued, with $\overline{\text{CS}}$ low, the SDO line is now driven by the HI5816 and conversion data is transferred out on falling edges of SCLK. The first falling edge of SCLK after $\overline{\text{CS}}$ goes low (specified by T_{ESU}) drives the first data bit on the SDO line and each successive falling SCLK edge transfers the next data bit. The L/$\overline{\text{M}}$ pin is used to control whether the serial data is output in LSB first or MSB first format (see Figure 12).

The HI5816 maintains data integrity until a data read is complete. That is, if a data read has begun ($\overline{\text{CS}}$ has been driven low and at least one falling edge of SCLK has occurred), but has not completed before another conversion is finished, the output shift register is not updated, the DRDY pulse is suppressed, and that conversion result is lost. The maximum read time allowed without losing a data word is 15 x T_{CCLK} (from the rising edge of DRDY). In order for the output shift register to be updated and the DRDY line to go high after each conversion is complete, there must have been 16 x N SCLK falling edges since the last DRDY rising edge (where N is 0 or a positive integer).

SCLK #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DATA BIT	0	0	0	0	MSB	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	LSB

FIGURE 12A. L/$\overline{\text{M}}$ = 0

SCLK #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DATA BIT	LSB	b1	b2	b3	b4	b5	b6	b7	b8	b9	b10	MSB	0	0	0	0

FIGURE 12B. L/$\overline{\text{M}}$ = 1

FIGURE 12. DOC = 0 DATA FORMAT

When $\overline{\text{CS}}$ goes high (inactive) the SDO pin is three-stated and the SCLK functionality is disabled. If $\overline{\text{CS}}$ goes high during a data read, the data read continues where it left off when $\overline{\text{CS}}$ is driven low again. This means that the SCLK can be free running and the processor can drive $\overline{\text{CS}}$ high during a read. If at any time the controller becomes "lost", the $\overline{\text{RST}}$ line can be pulsed low to synchronize the internal I/O state

machine. This has the affect of "completing" a data read allowing the next conversion result to be read following the next DRDY rising edge.

Serial interface timing for DOC = 0 is shown in Figure 15.

Data On Convert (DOC = 1)

When DOC = 1, SCLK acts as both the conversion clock and the data output clock. Each data bit is output immediately after being determined by the conversion process. A data bit is registered at the output on each falling edge of SCLK and it takes fifteen conversion clock cycles (SCLK cycles) for a complete conversion. The first two data bits and the last (fifteenth) data bit are always 0 (these occur during the sample period of the converter). The third through fourteenth data bits contain the actual conversion data in MSB first format (see Figure 16). Please note that the CCLK specifications apply to SCLK when operating in the DOC = 1 mode.

$\overline{\text{CS}}$ now serves the same function that $\overline{\text{START}}$ did for DOC = 0, but $\overline{\text{CS}}$ still controls the SDO pin. Bringing $\overline{\text{CS}}$ low will start a conversion and tieing $\overline{\text{CS}}$ low puts the HI5816 in the continuous conversion mode (see Figures 1, 2, and 3 for the converter timing). Data is output at SDO when $\overline{\text{CS}}$ is low and SDO is three-stated when $\overline{\text{CS}}$ is high.

The DRDY flag is fully operational in this mode (goes high when a conversion is complete).

The states of the $\overline{\text{START}}$ and L/$\overline{\text{M}}$ pins do not matter, but they should be tied either high or low.

The internal clock can be used to drive the HI5816 in the DOC = 1 mode by connecting the CCLK and SCLK pins together. The internal CCLK output is very weak and should be buffered if it is used to drive more than the SCLK input. If CCLK is left unused it should be tied either high or low.

Serial interface timing for DOC = 1 is shown in Figure 17.

8 Pin Functionality

Although the HI5816 is not available in an 8 pin package, it can be configured to have the functionality of an 8 pin device. For example, Figure 19 shows the HI5816 configured to have the same "look and feel" as the Texas Instrument TLV1549C. The HI5816 can be configured to have the same functionality of other 8 pin converters by simply tieing certain pins to either V_{DD} or GND (V_{SS}).

Analog Input

The analog input pin is a predominately capacitive load that changes between the track and hold periods of the conversion cycle. During hold, conversion clock period 4 through 15, the input loading is leakage and stray capacitance, typically less than 5μA and 20pF.

At the start of input tracking, conversion clock period 1, some charge is dumped back to the input pin. The input source must have low enough impedance to dissipate the current spike by the end of the tracking period as shown in Figure 13. The amount of charge is dependent on supply and input voltages. The average current is also proportional to conversion clock frequency.
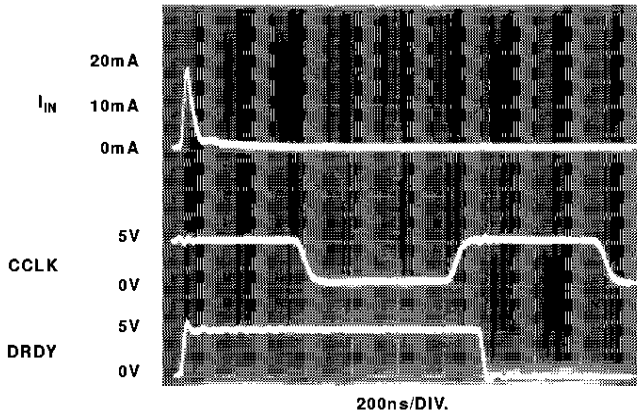
Conditions: $V_{DD} = V_{AA}+ = 5.0V$, $V_{REF}+ = 5.0V$,
$V_{IN} = 5.0V$, CCLK = 750kHz, $T_A = +25^oC$

FIGURE 13. TYPICAL ANALOG INPUT CURRENT

As long as these current spikes settle completely by end of the signal acquisition period, converter accuracy will be preserved. The analog input is tracked for 3 conversion clock cycles. With an external conversion clock of 750kHz the track period is 4µs.

A simplified analog input model is presented in Figure 14. During tracking, the A/D input (V_{IN}) typically appears as a 380pF capacitor being charged through a 420Ω internal switch resistance. The time constant is 160ns. To charge this capacitor from an external "zero Ω" source to $^1/_2$ LSB (1/8192), the charging time must be at least 9 time constants or 1.4µs. The maximum source impedance (R_{SOURCE} Max) for a 4µs acquisition time settling to within $^1/_2$ LSB is 750Ω.

If the conversion clock frequency was slower, or the converter was not restarted immediately (causing a longer sample time), a higher source impedance could be tolerated.
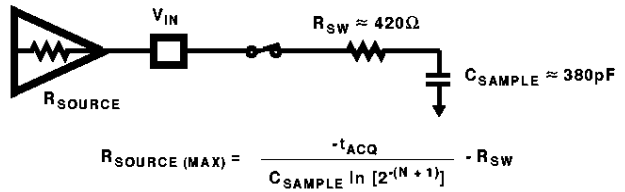

$$R_{SOURCE\,(MAX)} = \frac{-t_{ACQ}}{C_{SAMPLE}\,\ln\,[2^{-(N+1)}]} - R_{SW}$$

FIGURE 14. ANALOG INPUT MODEL IN TRACK MODE
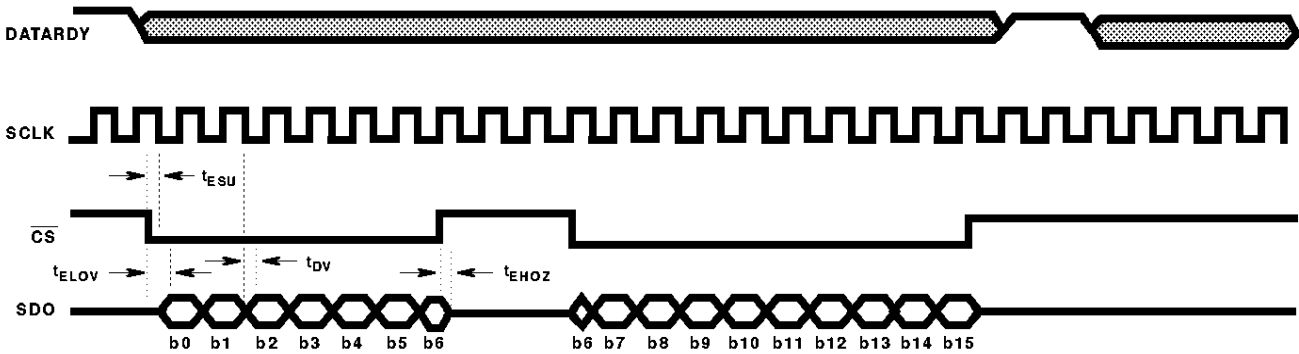
FIGURE 15. SERIAL INTERFACE TIMING, DOC = 0

SCLK#	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DATA BIT	0	0	MSB	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	LSB	0

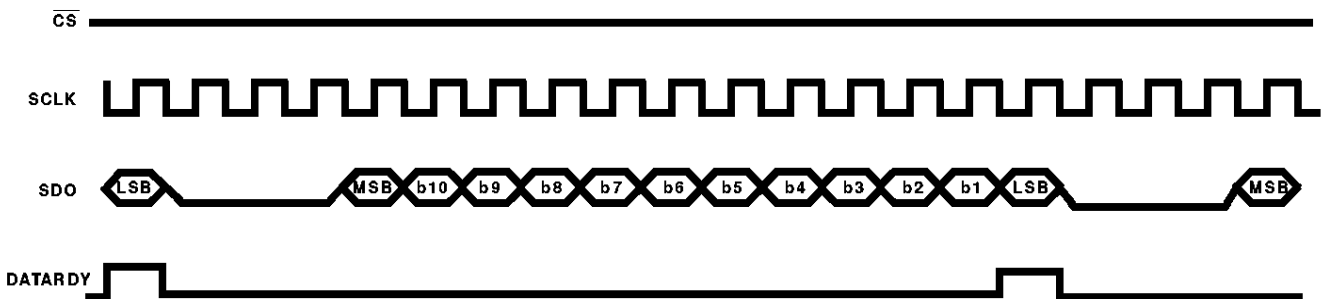**FIGURE 16. DOC = 1 DATA FORMAT**

FIGURE 17. SERIAL INTERFACE TIMING, DOC = 1

Reference Input

The reference input $V_{REF}+$ should be driven from a low impedance source and be well decoupled.

As shown in Figure 18, current spikes are generated on the reference pin during each bit test of the successive approximation part of the conversion cycle as the charge-balancing capacitors are switched between $V_{REF}-$ and $V_{REF}+$ (conversion clock periods 5 - 14). These current spikes must settle completely during each bit test of the conversion to not degrade the accuracy of the converter. Therefore $V_{REF}+$ and $V_{REF}-$ should be well bypassed. Reference input $V_{REF}-$ is normally connected directly to the analog ground plane. If $V_{REF}-$ is biased for nulling the converters offset it must be stable during the conversion cycle.
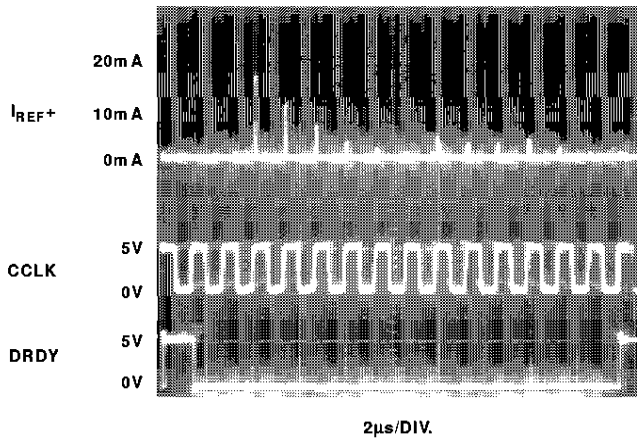
Conditions: $V_{DD} = V_{AA}+ = 5.0V$, $V_{REF}+ = 5.0V$,
$V_{IN} = 2.3V$, CCLK = 750kHz, $T_A = +25^oC$

**FIGURE 18. TYPICAL REFERENCE INPUT CURRENT**

The HI5816 is specified with a 5.0V reference, however, it will operate with a reference down to 2.5V having a slight degradation in performance. A typical graph of accuracy vs reference voltage is presented (see Figure 8).

Full Scale and Offset Adjustment

In many applications the accuracy of the HI5816 would be sufficient without any adjustments. In applications where accuracy is of utmost importance full scale and offset errors may be adjusted to zero.

The $V_{REF}+$ and $V_{REF}-$ pins reference the two ends of the analog input range and may be used for offset and full scale adjustments. In a typical system the $V_{REF}-$ might be returned to a clean ground, and the offset adjustment done on an input amplifier. $V_{REF}+$ would then be adjusted to null out the full scale error. When this is not possible, the $V_{REF}-$ input can be adjusted to null the offset error, however, $V_{REF}-$ must be well decoupled.

Full scale and offset error can also be adjusted to zero in the signal conditioning amplifier driving the analog input (V_{IN}).
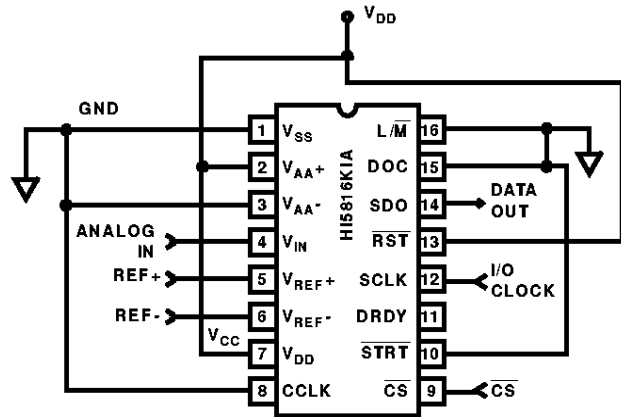
(For space savings SSOP 16 pin package used)

FIGURE 19. 8 PIN FUNCTIONALITY

Conversion Clock

The HI5816 can operate either from its internal conversion clock or from one externally supplied. The CCLK pin functions either as the conversion clock output or input.

Figure 20 shows the configuration of the internal conversion clock. The conversion clock output drive is low power: if used as an output, it should not have more than 1 CMOS gate load applied, and stray wiring capacitance should be kept to a minimum.
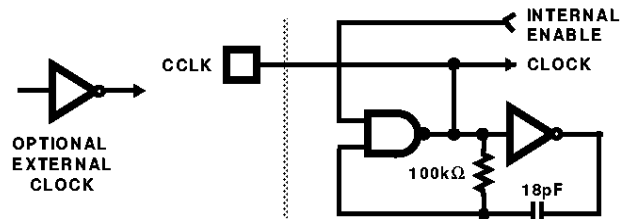

FIGURE 20. INTERNAL CONVERSION CLOCK CIRCUITRY

The internal conversion clock will shut down if the A/D is not restarted after a conversion. The conversion clock could also be shut down with an open collector driver applied to the CCLK pin. This should only be done during the sample portion (the first three conversion clock periods) of a conversion cycle, and might be useful for using the device as a digital sample and hold.

If an external conversion clock is supplied to the CCLK pin, it must have sufficient drive to overcome the internal conversion clock source. The external conversion clock can be shut off, but again, only during the sample portion of a conversion cycle. At other times, it must be above the minimum frequency shown in the specifications. In the above two cases, a further restriction applies in that the conversion clock should not be shut off during the third sample period for more than 1ms. This might cause an internal charge-pump voltage to decay.

If the internal or external conversion clock was shut off during the conversion time (conversion clock cycles 4 through 15) of the A/D, the output might be invalid due to balancing capacitor droop.

An external conversion clock must also meet the minimum T_{LOW} and T_{HIGH} times shown in the specifications. A violation may cause an internal miscount and invalidate the results.

Power Supplies and Grounding

V_{DD} and V_{SS} are the digital supply pins: they power all internal logic and the output drivers. Because the output drivers can cause fast current spikes in the V_{DD} and V_{SS} lines, V_{SS} should have a low impedance path to digital ground and V_{DD} should be well bypassed.

Except for $V_{AA}+$, which is a substrate connection to V_{DD}, all pins have protection diodes connected to V_{DD} and V_{SS}. Input transients above V_{DD} or below V_{SS} will get steered to the digital supplies.

The $V_{AA}+$ and $V_{AA}-$ terminals supply the charge-balancing comparator only. Because the comparator is auto-balanced between conversions, it has good low-frequency supply rejection. It does not reject well at high frequencies however; $V_{AA}-$ should be returned to a clean analog ground and $V_{AA}+$ should be RC decoupled from the digital supply as shown in Figure 21.

There is approximately 50Ω of substrate impedance between V_{DD} and $V_{AA}+$. This can be used, for example, as part of a low-pass RC filter to attenuate switching supply noise. A $10\mu F$ capacitor from $V_{AA}+$ to ground would attenuate 30kHz noise by approximately 40dB. Note that back-to-back diodes should be placed from V_{DD} to $V_{AA}+$ to handle supply to capacitor turn-on or turn-off current spikes.
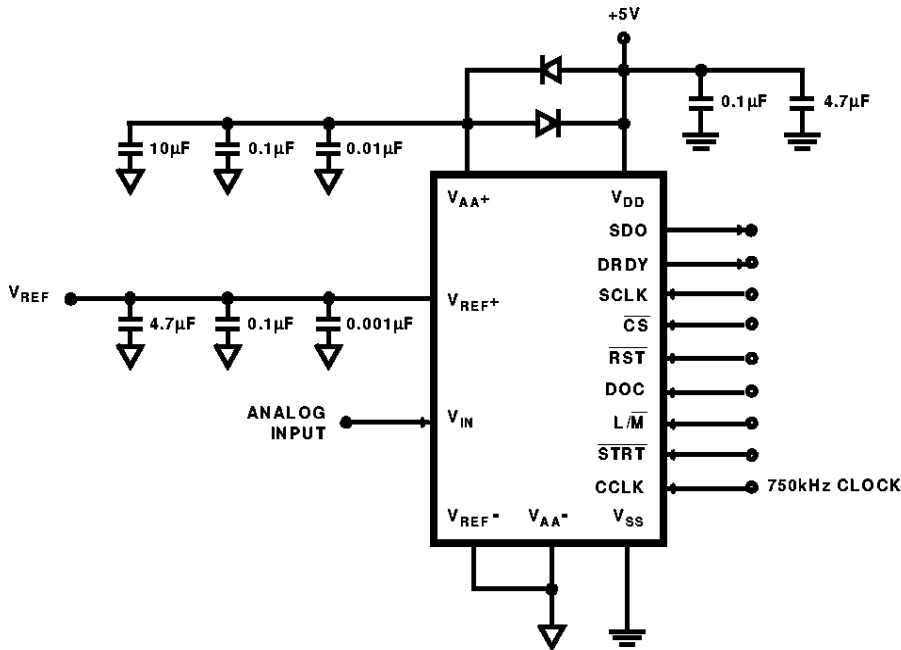

FIGURE 21. GROUND AND SUPPLY DECOUPLING

TABLE 3. CODE TABLE

CODE DESCRIPTION	(NOTE 1) INPUT VOLTAGE $V_{REF}+ = 5.0V$ $V_{REF}- = 0.0V$ (V)	DECIMAL COUNT	BINARY OUTPUT CODE MSB											LSB
			b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Full Scale (FS)	4.9988	4095	1	1	1	1	1	1	1	1	1	1	1	1
FS - 1 LSB	4.9976	4094	1	1	1	1	1	1	1	1	1	1	1	0
$^3/_4$ FS	3.7500	3072	1	1	0	0	0	0	0	0	0	0	0	0
$^1/_2$ FS	2.5000	2048	1	0	0	0	0	0	0	0	0	0	0	0
$^1/_4$ FS	1.2500	1024	0	1	0	0	0	0	0	0	0	0	0	0
1 LSB	0.001221	1	0	0	0	0	0	0	0	0	0	0	0	1
Zero	0	0	0	0	0	0	0	0	0	0	0	0	0	0

NOTE:

1. The voltages listed above represent the ideal lower transition of each output code shown as a function of the reference voltage.

Die Characteristics

DIE DIMENSIONS:
3220μm x 3510μm

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
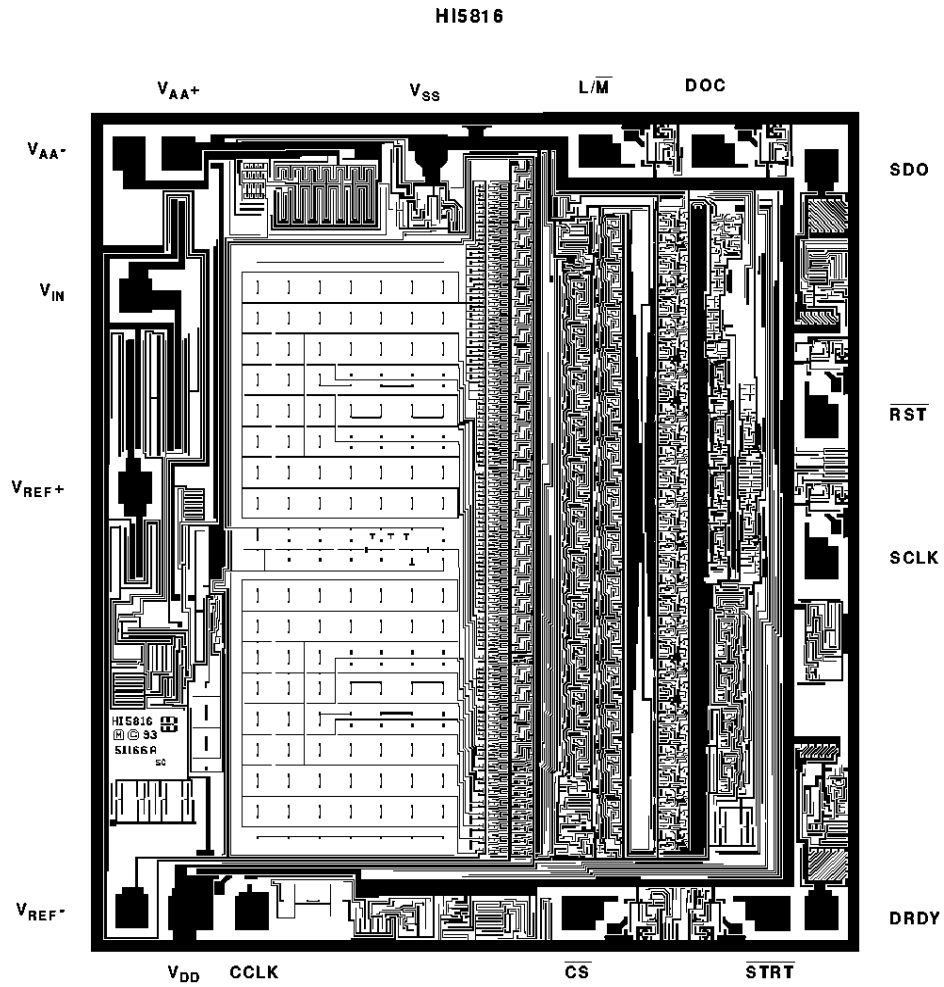Type: PSG
Thickness: 13kÅ ± 2.5kÅ

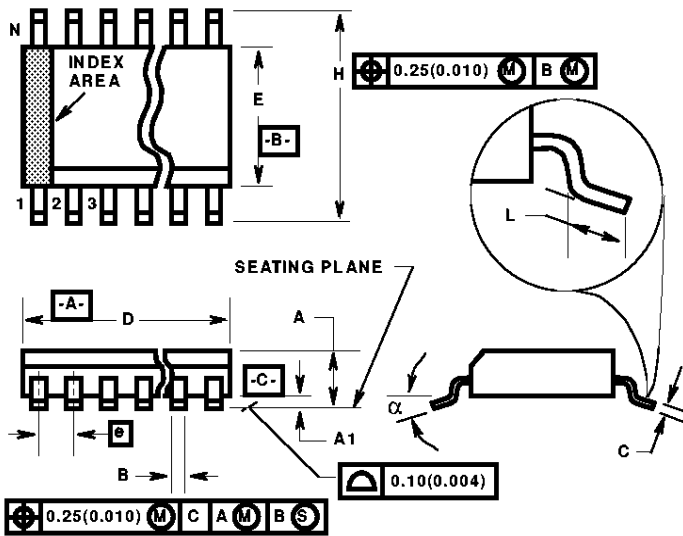**WORST CASE CURRENT DENSITY:**
1.84×10^5 A/cm^2

Metallization Mask Layout

HI5816

Shrink Small Outline Plastic Packages (SSOP)

M16.209 (JEDEC MO-150-AC ISSUE A)
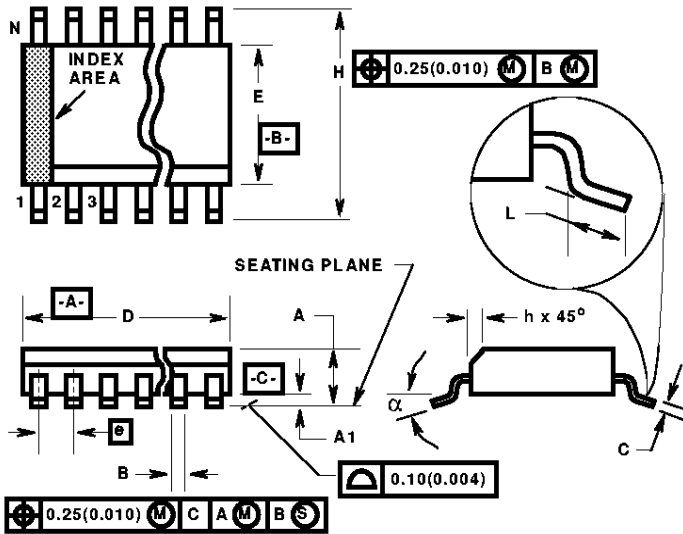**16 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.083	-	2.13	-
A1	0.002	0.009	0.05	0.25	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.007	0.09	0.20	-
D	0.233	0.255	5.90	6.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.025	0.040	0.63	1.03	-
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 0 2/94

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.

2. Dimensioning and tolerancing per ANSI Y14.5M-1982.

3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.

4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.

5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

6. "L" is the length of terminal for soldering to a substrate.

7. "N" is the number of terminal positions.

8. Terminal numbers are shown for reference only.

9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.51mm (0.020 inch).

10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline Plastic Packages (SOIC)

M16.3 (JEDEC MS-013-AA ISSUE C)
**16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.

2. Dimensioning and tolerancing per ANSI Y14.5M-1982.

3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.

4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.

5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

6. "L" is the length of terminal for soldering to a substrate.

7. "N" is the number of terminal positions.

8. Terminal numbers are shown for reference only.

9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)

10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Dual-In-Line Plastic Packages (PDIP)
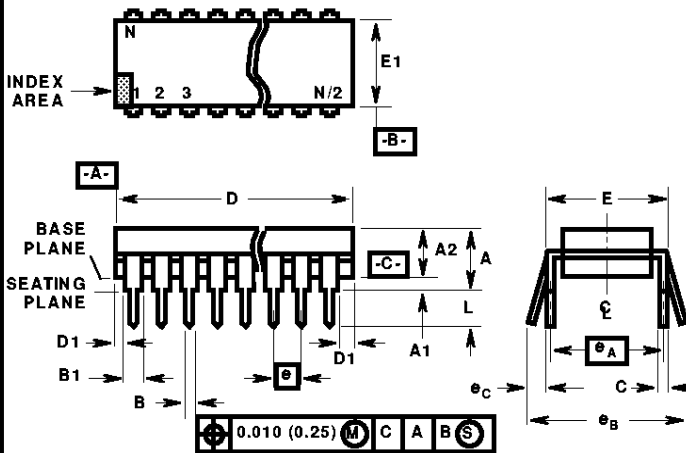
E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.

2. Dimensioning and tolerancing per ANSI Y14.5M-1982.

3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.

4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.

5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).

6. E and e_A are measured with the leads constrained to be perpendicular to datum -C- .

7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.

8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).

9. N is the maximum number of terminal positions.

10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

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