

## Dual Channel Bidirectional I<sup>2</sup>C Bus Level Shift and Repeater

### Features

- Dual channel level shift and repeater for SDA/SCL Lines in I<sup>2</sup>C Applications and SMBus Compatible
- Support multi-mode: Standard-mode (SM), Fast-mode (FM), and Fast-mode Plus (FM+)
- Open-Drain I<sup>2</sup>C Input/Output
- Latching free operation
- Allows Voltage-Level Translation Between
  - V<sub>REF1</sub> range 0.8 V to 5.5 V
  - V<sub>REF2</sub> range 2.2 V to 5.5 V
- 5 V tolerant I<sup>2</sup>C-bus and enable pins
- High-impedance SCL1, SDA1, SCL2 and SDA2 pins for EN = LOW
- Support Low level output current up to 30 mA
- Latch-Up performance exceeds 600 mA
- ESD Protection:
  - 7000-V Human-Body Model
  - 1500-V Charged-Device Model

### Applications

- I<sup>2</sup>C, SMBus, PMBus, MDIO, UART, Low-Speed SDIO, GPIO, and Other Two-Signal Interfaces
- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer handsets
- Industrial Automation

### Description

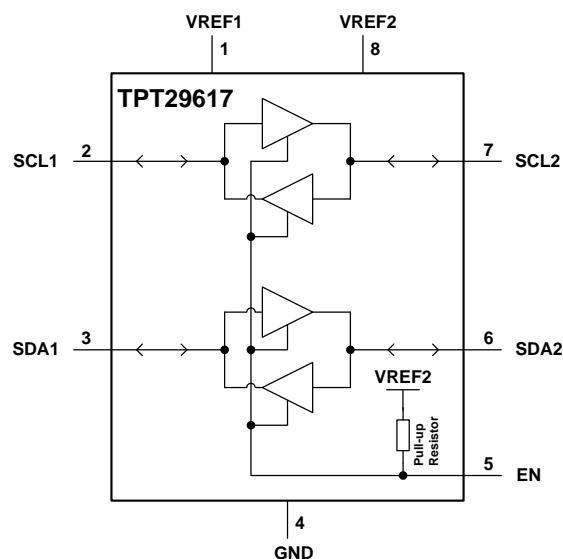
The TPT29617A device is a dual channel I<sup>2</sup>C level shift and repeater function with an enable (EN) input, and work from 0.8 V to 5.5 V V<sub>REF1</sub> and 2.2 V to 5.5 V V<sub>REF2</sub>.

The SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, will allow bidirectional data flow between ports. If EN is low, the translator switch is off, and a high-impedance state exists between ports to isolate both sides.

Dual channel, bidirectional buffer isolates capacitance and allows 540 pF on either side of the device at 1 MHz and up to 4000 pF at lower speeds.

TPT29617A is available in SOP8 and MSOP8 package, and is characterized from -40°C to +125°C.

### Functional Block Diagram



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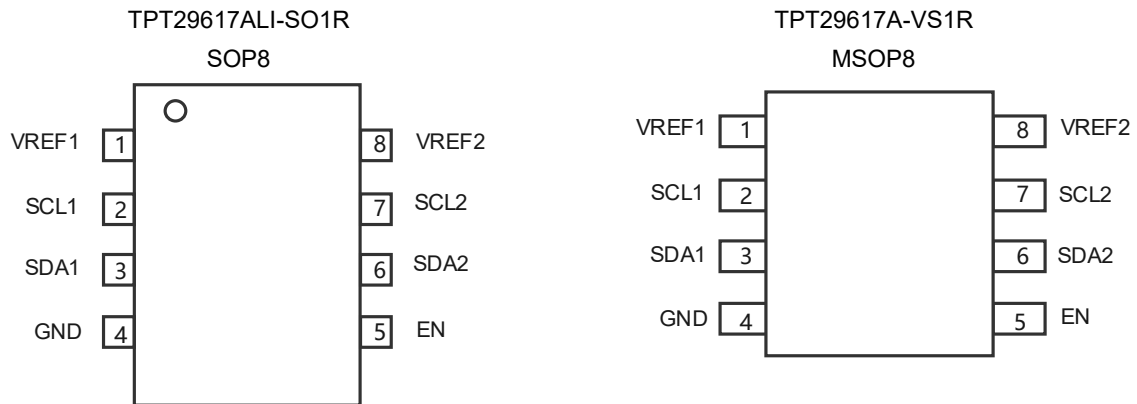
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**Dual Channel Bidirectional I<sup>2</sup>C Bus  
Level Shift and Repeater****Revision History**

Date	Revision	Notes
2019-06-10	Rev.Pre.0	Initial Version
2019-09-12	Rev.Pre.1	Added ESD data
2019-12-04	Rev.Pre.2	Added electrical data
2020-01-10	Rev.Pre.3	Updated function block diagram and application circuit
2020-02-27	Rev.A.0	Fixed datasheet
2020-04-24	Rev.A.1	Updated latch up 600 mA
2020-07-21	Rev.B.0	Updated $V_{OL} - V_{IL}$ value
2022-02-09	Rev.B.1	Added tape and reel information
2022-03-21	Rev.B.2	Added the description of Latching free operation

## Dual Channel Bidirectional I<sup>2</sup>C Bus Level Shift and Repeater

### Pin Configuration and Functions



### Pin Functions

Pin		I/O	Description
No.	Name		
1	VREF1	I	Side-1 supply voltage (0.8 V to 5.5 V)
2	SCL1	I/O	I <sup>2</sup> C SCL line, side-1. Connect to VREF1 through a pull-up resistor.
3	SDA1	I/O	I <sup>2</sup> C SDA line, side-1. Connect to VREF1 through a pull-up resistor.
4	GND	I	Supply ground
5	EN	I	Active-high repeater enable input, internal pull high to VREF2
6	SDA2	I/O	I <sup>2</sup> C SDA line, side-2. Connect to VREF2 through a pull-up resistor.
7	SCL2	I/O	I <sup>2</sup> C SCL line, side-2. Connect to VREF2 through a pull-up resistor.
8	VREF2	I	Side-2 and device supply voltage (2.2 V to 5.5 V)

## Specifications

### Absolute Maximum Ratings

Parameter		Min	Max	Unit
V <sub>REF1</sub>	DC reference voltage range	-0.5	7	V
V <sub>REF2</sub>	DC reference bias voltage range	-0.5	7	V
V <sub>I</sub>	Input voltage range	-0.5	7	V
V <sub>I/O</sub>	Input/output voltage range	-0.5	7	V
I <sub>IK</sub>	Input clamp current, V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current, V <sub>I/O</sub> < 0		-50	mA
T <sub>J</sub>	Maximum Junction Temperature		150	°C
T <sub>STG</sub>	Storage Temperature Range	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

(2) This data was taken with the JEDEC low effective thermal conductivity test board.

(3) This data was taken with the JEDEC standard multilayer test boards.

### ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	7	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	1.5	kV

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### Recommended Operating Conditions

Parameter		Min	Max	Max
V <sub>I/O</sub>	Input/output voltage, SCL1, SDA1, SCL2, SDA2	0	5.5	V
V <sub>REF1</sub>	Reference voltage	0.8	5.5	V
V <sub>REF2</sub>	Reference voltage	2.2	5.5	V
I <sub>input</sub>	Input clamp current	0	50	mA
I <sub>output</sub>	Output clamp current	0	50	mA
T <sub>A</sub>	Operating ambient temperature	-40	125	°C

### Thermal Information

Package Type	θ <sub>JA</sub>	θ <sub>JC</sub>	Unit
MSOP8	180	72	°C/W
SOP8	148	48	°C/W

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### Electrical Characteristics

All test conditions:  $V_{REF1} = 0.8\text{ V to }5.5\text{ V}$ ,  $V_{REF2} = 2.2\text{ V to }5.5\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+125^\circ\text{C}$ , unless otherwise noted.

Symbol	Parameter		Conditions	Min	Typ	Max	Unit	
<b>Supply Voltage and Current</b>								
$V_{IK}$	Input clamp voltage		$I_I = -18\text{ mA}$ , $V_{CC} \times 2.2\text{ V to }5.5\text{ V}$	-1.2		-0.3	V	
$V_{OL}$	Low-level output voltage	SDA1, SCL1	$I_{OL} = 13\text{ mA}$ , $V_{CC} \times 0.8\text{ V to }5.5\text{ V}$		0.1	0.2	V	
		SDA2, SCL2	$I_{OL} = 150\text{ }\mu\text{A or }13\text{ mA}$ , $V_{ILA} = 0\text{ V}$ , $V_{CC} \times 2.2\text{ V to }5.5\text{ V}$		0.5	0.6		
$V_{IH}$	High-level input voltage	SDA1, SCL1	$V_{CC} \times 0.8\text{ V to }5.5\text{ V}$	$0.7 \times V_{REF1}$		5.5	V	
		SDA2, SCL2	$V_{CC} \times 2.2\text{ V to }5.5\text{ V}$	$0.7 \times V_{REF2}$		5.5		
		EN	$V_{CC} \times 2.2\text{ V to }5.5\text{ V}$	$0.7 \times V_{REF2}$		5.5		
$V_{IL}$	Low-level input voltage	SDA1, SCL1	$V_{CC} \times 0.8\text{ V to }5.5\text{ V}$			$0.3 \times V_{REF1}$	V	
		SDA2, SCL2	$V_{CC} \times 2.2\text{ V to }5.5\text{ V}$			0.4		
		EN	$V_{CC} \times 2.2\text{ V to }5.5\text{ V}$			$0.3 \times V_{REF2}$		
$V_{OL} - V_{IL}$	Difference between Low-level output and Low-level input voltage		$V_{OL}$ at $I_{OL} = 1\text{ mA}$ ;		90	140	mV	
$I_{CC1}$	Quiescent supply current for $V_{REF1}$		Both channels low, SDA1 = SCL1 = GND and SDA2 = SCL2 = open, or SDA1 = SCL1 = open and SDA2 = SCL2 = GND	$V_{REF1} = 0.8\text{ V}$		1.5	5	$\mu\text{A}$
				$V_{REF1} = 5.5\text{ V}$		10	20	
$I_{CC2}$	Quiescent supply current		Output Low Level	$V_{CC} \times 2.2\text{ V to }5.5\text{ V}$		9	15	mA
			Output High Level			1.2	5	
$I_I$	Input leakage current	SDA2, SCL2	$V_I = V_{REF2}$	$V_{CC} \times 2.2\text{ V to }5.5\text{ V}$	-1	+1	$\mu\text{A}$	
			$V_I = 0.2\text{ V}$ , EN = 0		-1	+1		
		SDA1, SCL1	$V_I = V_{REF1}$		-1	+1		
			$V_I = 0.2\text{ V}$		-1	+1		
		EN	$V_I = V_{REF2}$		-1	+1		
			$V_I = 0.2\text{ V}$		-18	-7		
$C_I$	Input capacitance <sup>(1)</sup>	SCL1, SCL2	$V_I = 3\text{ V or }0\text{ V}$ , $V_{CC} \times 3.3\text{ V or }0\text{ V}$		7		pF	
		EN	$V_I = 3\text{ V or }0\text{ V}$ , $V_{CC} \times 3.3\text{ V}$		5			
$C_{IO}$	Input/output capacitance <sup>(1)</sup>	SDA1, SDA2	$V_I = 3\text{ V or }0\text{ V}$ , $V_{CC} \times 3.3\text{ V}$		10		pF	

(1) Test data based on bench test and design simulation.

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### AC Timing Requirements

All test conditions:  $V_{REF1} = 0.8\text{ V to }5.5\text{ V}$ ,  $V_{REF2} = 2.2\text{ V to }5.5\text{ V}$ ,  $GND = 0\text{ V}$ ,  $T_A = -40^{\circ}\text{C to }+125^{\circ}\text{C}$ , unless otherwise noted.

Symbol	Parameter		From (input)	To (output)	Conditions	Min	Typ	Max	Unit
t <sub>PLH</sub>	Propagation delay		SDA2, SCL2	SDA1, SCL1			80	150	ns
			SDA1, SCL1	SDA2, SCL2	$V_{REF2} = 2.2\text{ to }5.5\text{ V}$		85	150	ns
t <sub>PHL</sub>	Propagation delay		SDA2, SCL2	SDA1, SCL1			55	100	ns
			SDA1, SCL1	SDA2, SCL2			90	150	ns
t <sub>TLH</sub>	Transition time	2 side	30% Level	70% Level			90	150	ns
		1 side					75	100	ns
t <sub>THL</sub>	Transition time	2 side	70% Level	30% Level			10	30	ns
		1 side					10	30	
t <sub>en</sub>	Setup time, EN high before Start condition							100	ns
t <sub>dis</sub>	Disable time							100	ns

## Dual Channel Bidirectional I<sup>2</sup>C Bus Level Shift and Repeater

### Typical Performance Characteristics

All test conditions:  $V_{REF1} = 0.9V$ ,  $V_{REF2} = 2.2V$ .

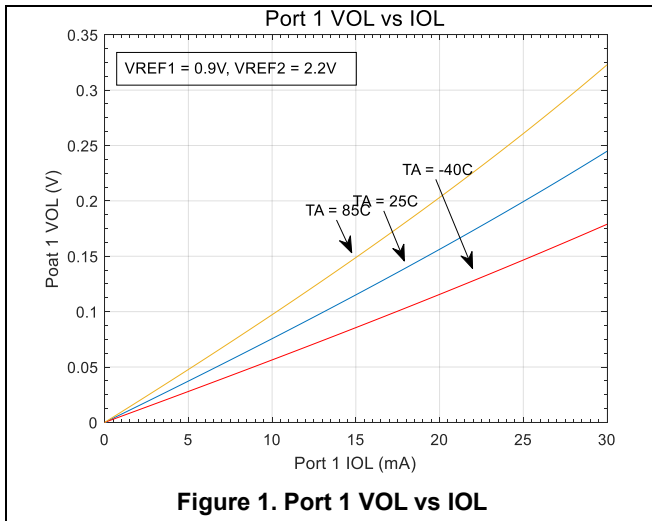


Figure 1. Port 1 VOL vs IOL

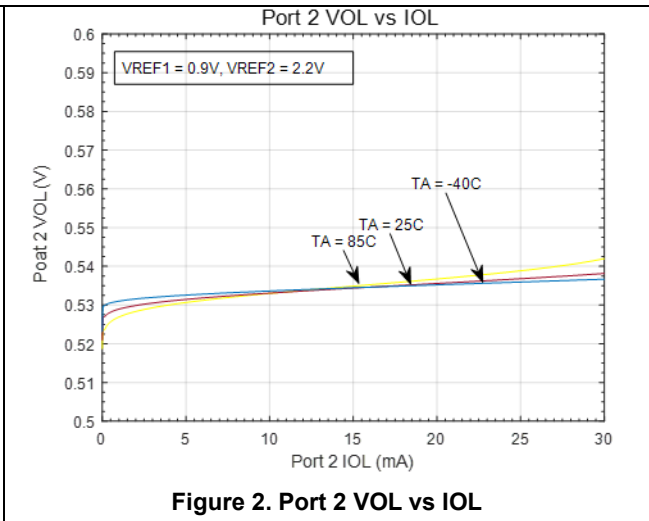


Figure 2. Port 2 VOL vs IOL

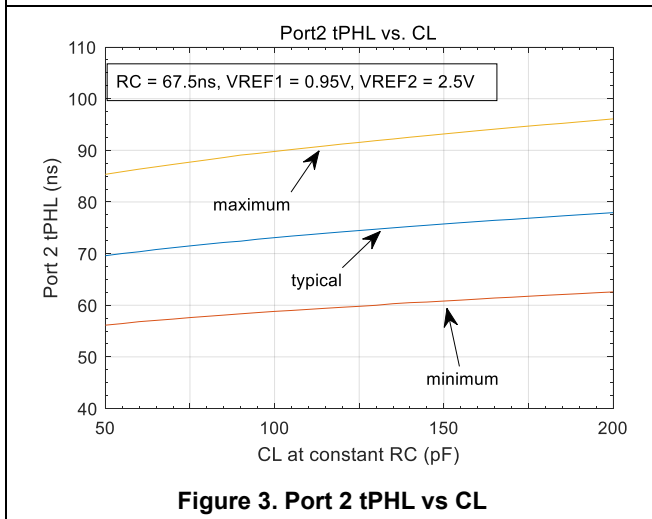


Figure 3. Port 2 tPHL vs CL



## Dual Channel Bidirectional I<sup>2</sup>C Bus Level Shift and Repeater

### Parameter measurement waveforms

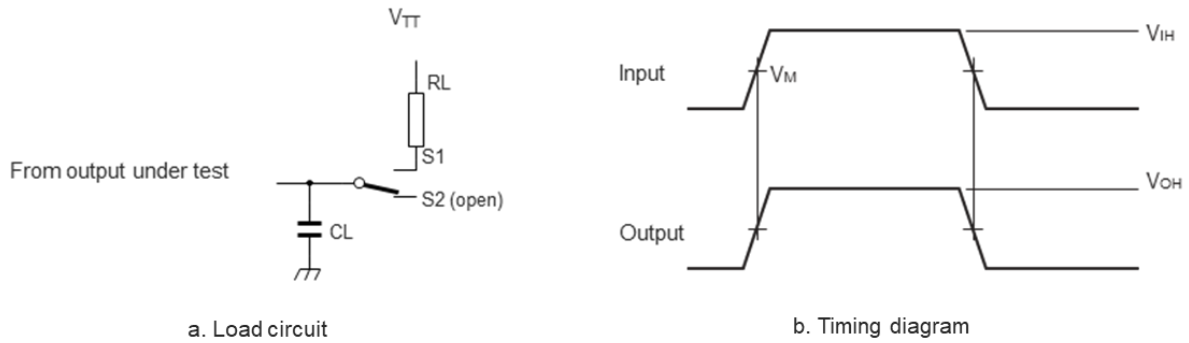


Figure 4 Load circuit for outputs

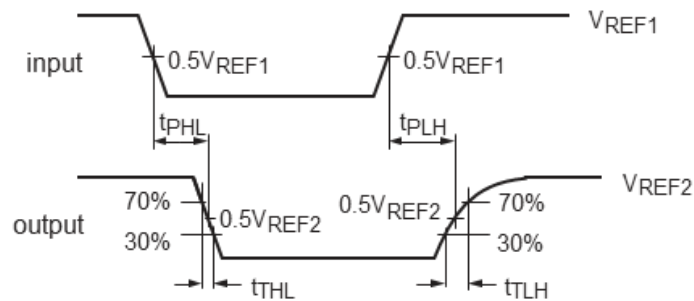


Figure 5 Propagation delay and transition times, side1 to side2

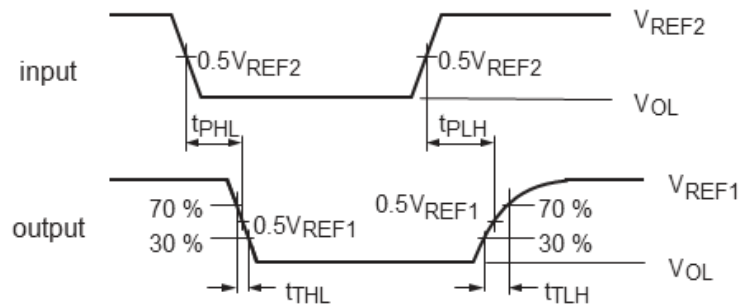


Figure 6 Propagation delay and transition times, side2 to side1

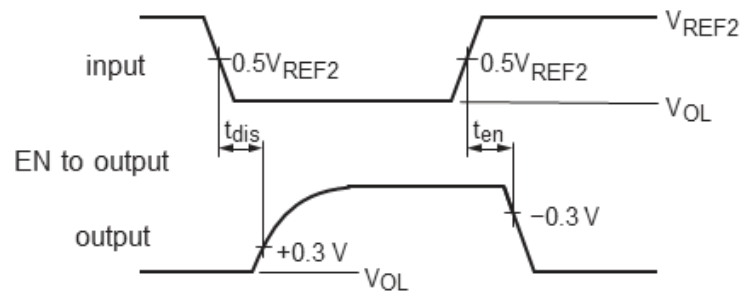


Figure 7 Enable and disable times

## Dual Channel Bidirectional I<sup>2</sup>C Bus Level Shift and Repeater

### Detailed Description

#### Overview

The TPT29617A is a dual channel level shift and repeater for SDA/SCL Lines in I<sup>2</sup>C Applications and SMBus Compatible, which supports I<sup>2</sup>C-bus or SMBus translation down to  $V_{REF1}$  as 0.8 V with normal system performance. The TPT29617A builds in two bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage (down to 0.8 V) and a 2.5 V, 3.3 V or 5 V I<sup>2</sup>C-bus or SMBus. All inputs and I/Os are tolerant to 5.5 V level.

The TPT29617A includes a power-up circuit that keeps the output drivers turned off until  $V_{REF2}$  is above 2.2 V and until after the internal reference circuits have settled  $\sim 400$   $\mu$ s, and the  $V_{REF1}$  is above 0.8 V.  $V_{REF2}$  and  $V_{REF1}$  can be applied in any sequence at power-up. After power-up and with the enable (EN) HIGH, a LOW level on port-1 ( $< 0.3 \cdot V_{REF1}$ ) turns the corresponding port-2 driver (SDA or SCL) on and drives port-2 down to  $\sim 0.55$  V. When port-1 rises above  $0.3 \cdot V_{REF1}$ , the port-2 pull-down driver is turned off and the external pull-up resistor pulls the pin HIGH. When port-2 falls first and goes below 0.4 V, the port-1 driver is turned on and port-1 pulls down to  $\sim 0$  V. The port-1 pull-down is not enabled unless the port-2 voltage goes below 0.4 V. If the port-2 low voltage goes below 0.4 V, the port-2 pull-down driver is enabled and port-2 will only be able to rise to 0.55 V until port-1 rises above  $0.3 \cdot V_{REF1}$ , then port-2 will continue to rise being pulled up by the external pull-up resistor. The  $V_{REF1}$  is only used to provide the  $0.35 \cdot V_{REF1}$  reference to the port-1 input comparators and for the power good detect circuit. The TPT29617A includes a  $V_{REF1}$  overvoltage disable that turns the channel off if  $0.4 \cdot V_{REF1} + 0.8 \text{ V} > V_{REF2}$ .

### Functional Block Diagram

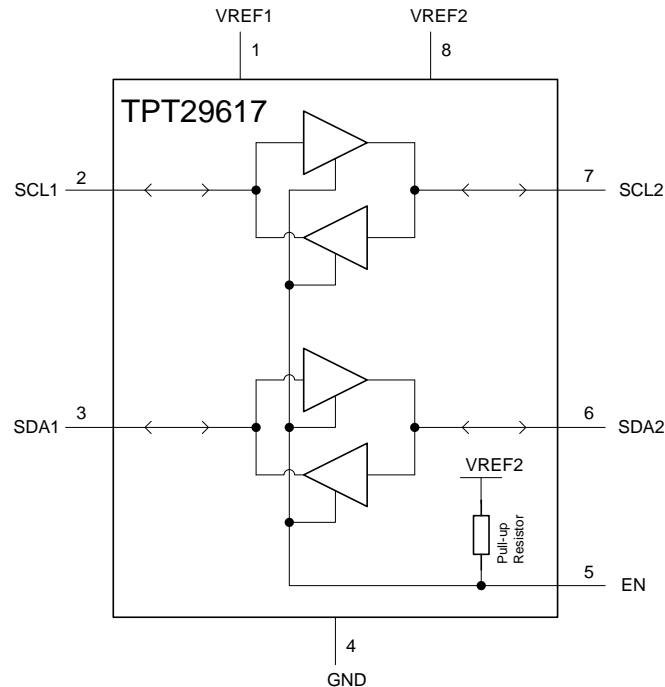


Figure 8. Functional Block Diagram

## Dual Channel Bidirectional I<sup>2</sup>C Bus Level Shift and Repeater

### Feature Description

#### Enable (EN)

The EN pin is active HIGH with thresholds referenced to  $V_{REF2}$  and an internal pull-up to  $V_{REF2}$  that maintains the device active unless the user selects to disable the TPT29617A to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I<sup>2</sup>C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I<sup>2</sup>C-bus parts being enabled. The enable does not switch the internal reference circuits so the ~400 us delay is only seen when  $V_{REF2}$  comes up.

The EN pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

**Table 1. Device Function table**

Input EN <sup>(1)</sup>	Translator Function
H	SCL1 = SCL2, SDA1 = SDA2
L	Disconnect

(1) The SCL switch conducts if EN is  $\geq 1$  V higher than SCL1 or SCL2. The same is true of SDA.

(2) EN = Floating, or the GPIO goes Hi-z which control the EN from I<sup>2</sup>C master, and TPT29617A status refer to EN = H.

#### Latching free operation

The output on the port 2 internal buffer is set the pull-down LOW as 0.55 V, while the input threshold of the internal buffer is set about 90 mV lower ( around 0.45 V). When the port 2 I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a latching condition from occurring. The output pull-down on port 1 drives a hard LOW and the input level is set at 0.35VCC(port 1) to accommodate the need for a lower LOW level in systems where the low voltage side supply voltage is as low as 0.8 V.

#### I<sup>2</sup>C-bus systems

As the standard I<sup>2</sup>C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus (standard open-collector configuration of the I<sup>2</sup>C-bus). The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part designed to work with Standard mode, Fast-mode and Fast-mode Plus I<sup>2</sup>C-bus devices in addition to SMBus devices. Standard mode and Fast-mode I<sup>2</sup>C-bus devices only specify 3 mA output drive; this limits the termination current to 3 mA in a generic I<sup>2</sup>C-bus system where Standard-mode devices, Fast-mode devices and multiple masters are possible. When only Fast-mode Plus devices are used with 20 mA at 5 V drive strength, then lower value pull-up resistors can be used. The side-2 RC should not be less than 67.5 ns because shorter RCs increase the turnaround bounce when the side-2 transitions from being externally driven to pulled down by its offset buffer.

Please see Application information, the pull up resistors value, which contains typical, star network and series network circuits.

## Dual Channel Bidirectional I<sup>2</sup>C Bus Level Shift and Repeater

### Application and Implementation

#### NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

#### Application Information

The TPT29617A is a dual channel level shift and repeater for SDA/SCL Lines in I<sup>2</sup>C Applications and SMBus Compatible, which supports I<sup>2</sup>C-bus or SMBus translation down to  $V_{REF1}$  as 0.8 V with normal system performance.

- I<sup>2</sup>C, SMBus, PMBus, MDIO, UART, Low-Speed SDIO, GPIO, and Other Two-Signal Interfaces
- Servers/Storages
- Routers (Telecom Switching Equipment)
- Personal Computers/Consumer handsets
- Industrial Automation

#### Typical Application

A typical application is shown in Figure 9. In this example, the system master is running on a 1.8 V I<sup>2</sup>C-bus while the slave is connected to a 3.3 V bus. Both buses run at 1000 kHz. Master devices can be placed on either bus.

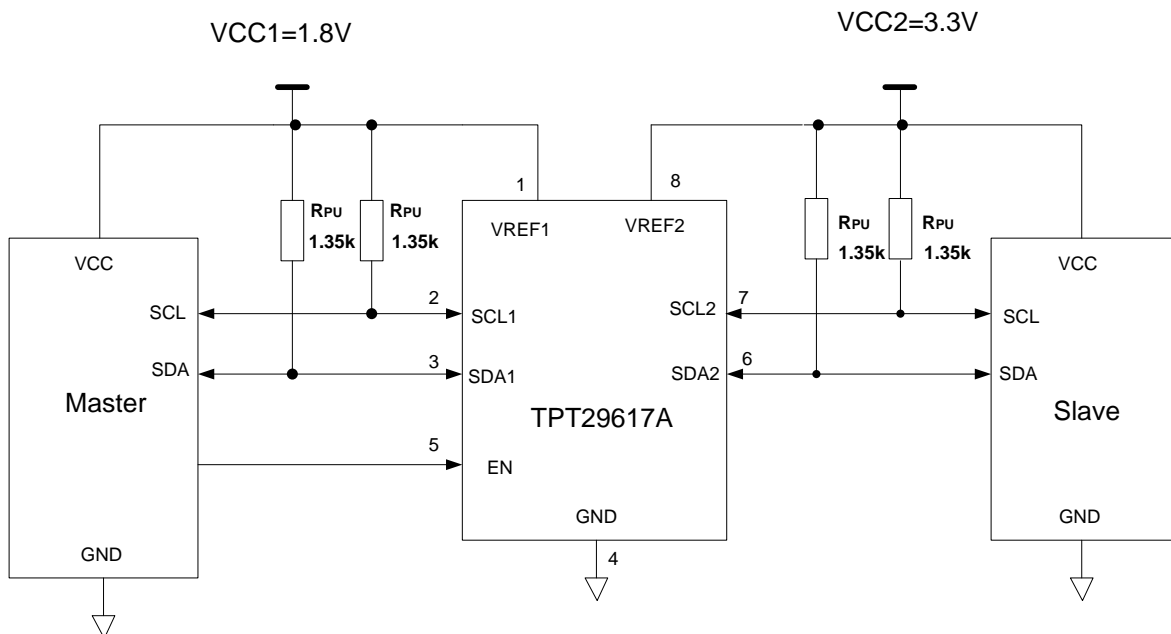


Figure 9. Typical Application Circuit

The TPT29617A is 5 V tolerant, so it does not require any additional circuitry to translate between 0.8 V to 5.5 V bus voltages and 2.2 V to 5.5 V bus voltages.

When port-1 of the TPT29617A is pulled LOW by a driver on the I<sup>2</sup>C-bus, a comparator detects the falling edge when it goes below  $0.3 \cdot V_{REF1}$  and causes the internal driver on port-2 to turn on, causing port-2 to pull down to

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about 0.5 V. When port-2 of the TPT29617A falls, first a CMOS hysteresis type input detects the falling edge and causes the internal driver on port-1 to turn on and pull the port-1 pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 10 and Figure 11. If the bus master in Figure 9 were to write to the slave through the TPT29617A, waveforms shown in Figure 10 would be observed on the port-1. This looks like a normal I<sup>2</sup>C-bus transmission except that the HIGH level may be as low as 0.8 V, and the turn on and turn off of the acknowledge signals are slightly delayed.

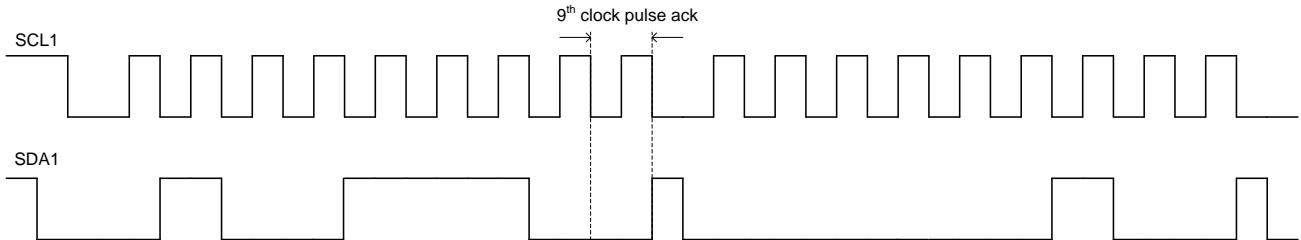


Figure 10 PORT-1 (0.8 V ~ 5.5 V) waveform

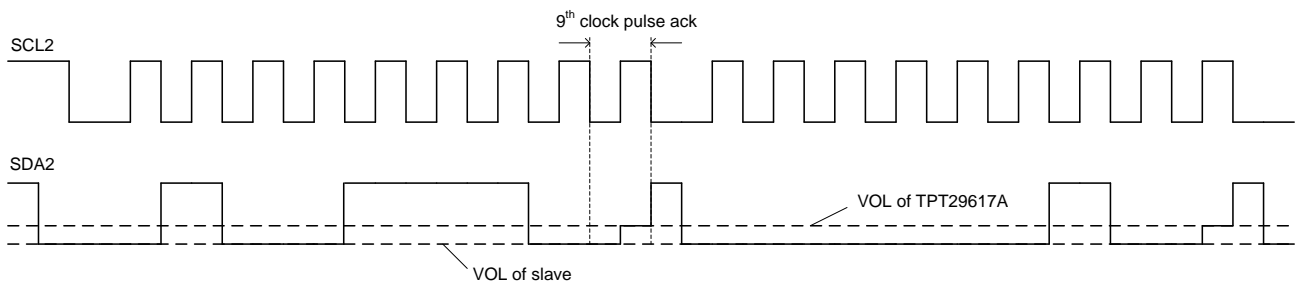


Figure 11 PORT-2 (2.2 V ~ 5.5 V) waveform

The internal comparator requires that  $0.4 \cdot V_{REF1}$  be less than or equal to  $V_{REF2} - 0.8 \text{ V}$  for the device to operate. Since A port is 5 V tolerant, the  $V_{REF1}$  can be lowered to support device spectrum while still supporting 5 V signals on the port-1.

On the port-2 side of the TPT29617A, the clock and data lines would have a positive offset from ground equal to the  $V_{OL}$  of the TPT29617A. After the eighth clock pulse, the data line will be pulled to the  $V_{OL}$  of the slave device which is very close to ground in this example. At the end of the acknowledge, the level rises only to the LOW level set by the driver in the port-2.

TPT29617A for a short delay while the port-1 side rises above  $0.3 \cdot V_{REF1}$  then it continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the B bus side at the input of the TPT29617A ( $V_{IL}$ ) be at or below 0.4 V to be recognized by the TPT29617A and then transmitted to the port-1 side.

## Dual Channel Bidirectional I<sup>2</sup>C Bus Level Shift and Repeater

Multiple TPT29617A port-1 sides can be connected in a star configuration (Figure 12), allowing all nodes to communicate with each other.

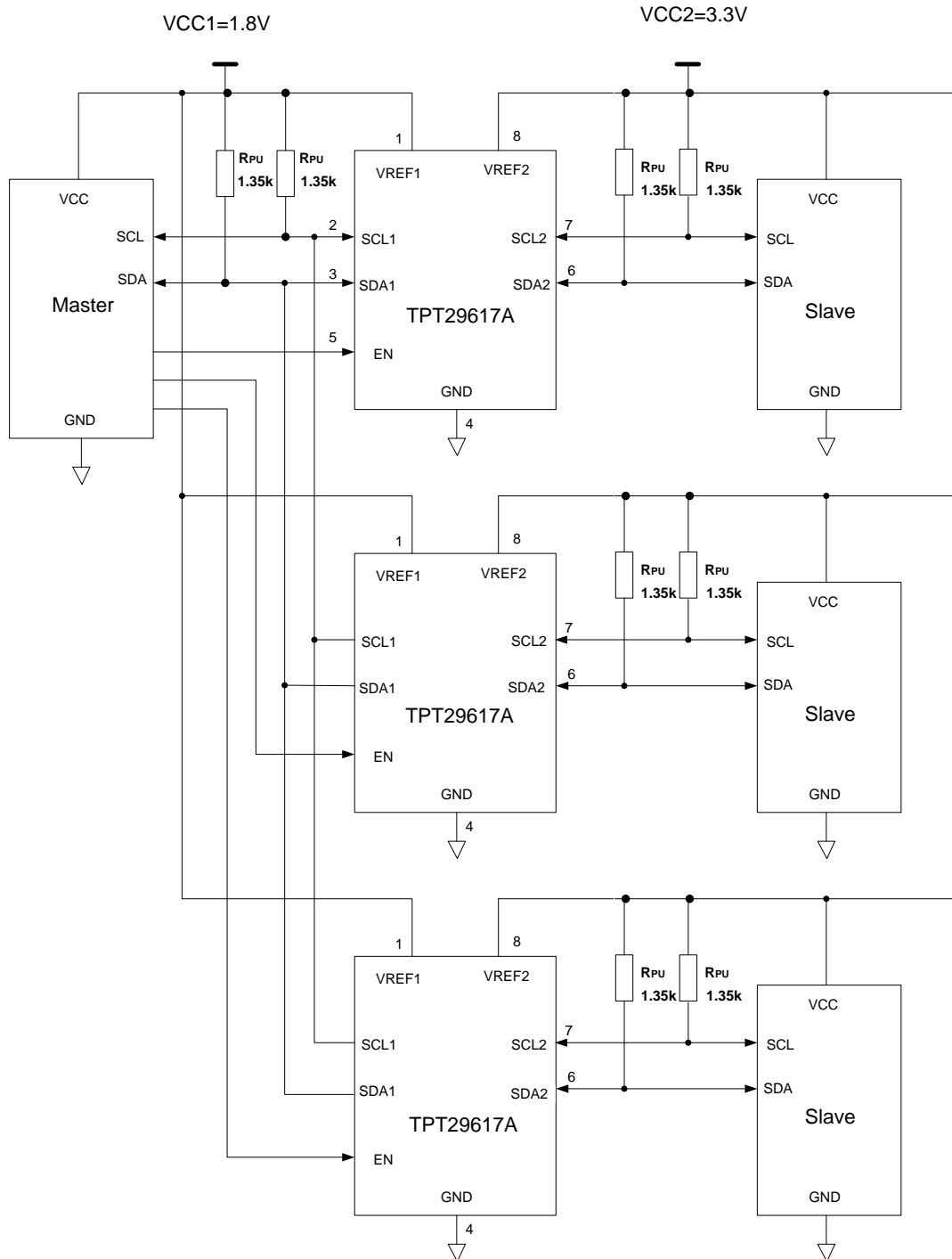
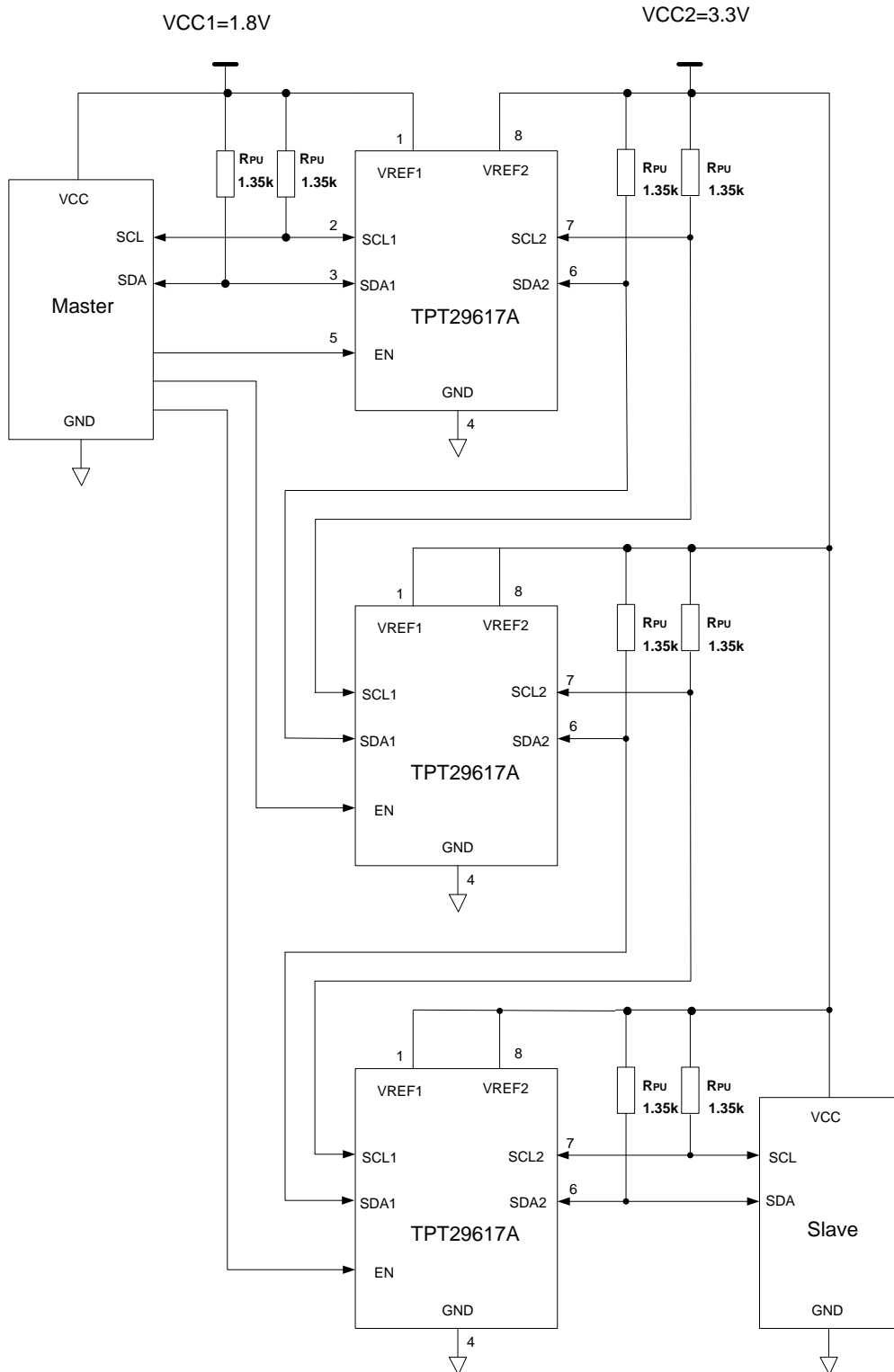


Figure 12 Typical application circuit, star network

Multiple TPT29617As can be connected in series (Figure 13) as long as port-1 is connected to port-2. I<sup>2</sup>C-bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.

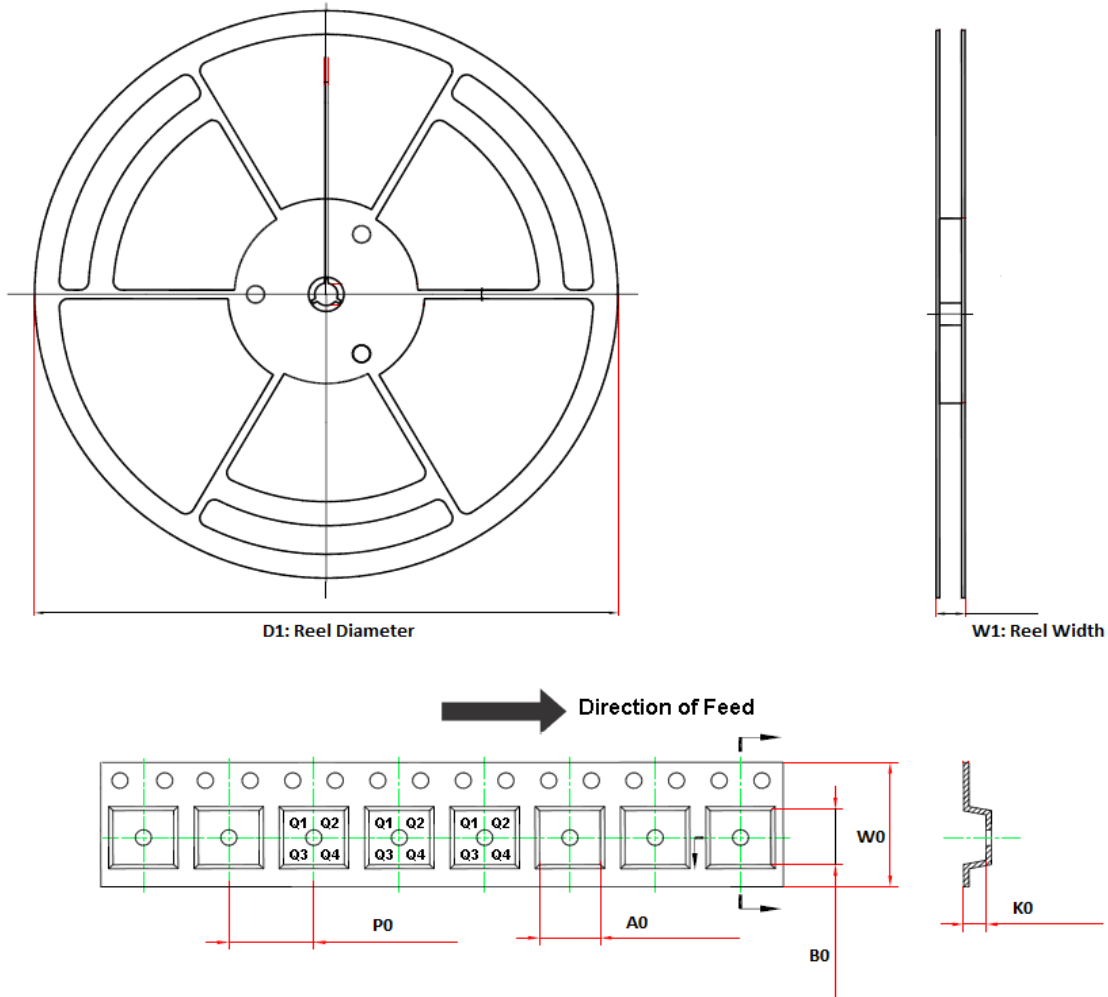
**Dual Channel Bidirectional I<sup>2</sup>C Bus  
Level Shift and Repeater**



**Figure 13 Typical application circuit, series network**

Decoupling capacitors not shown for simplicity, but they are required. It is especially important that the decoupling for the TPT29617A VREF2 be close to the VREF2 pin.

Tape and Reel Information

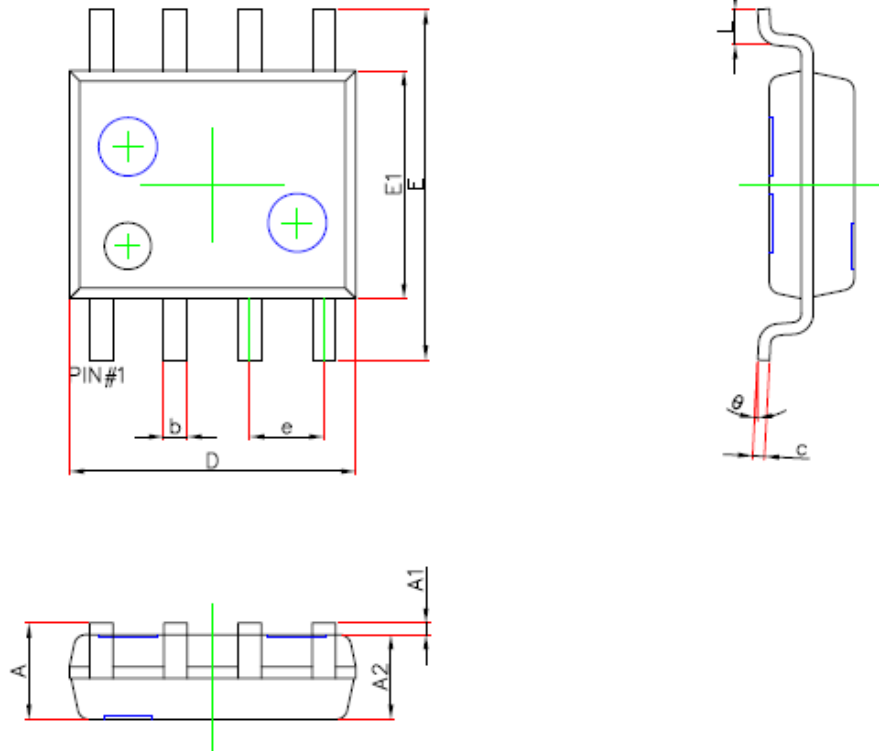


Order Number	Package	D1 (mm)	A0 (mm)	K0 (mm)	W0 (mm)	W1 (mm)	B0 (mm)	P0 (mm)	Pin1 Quadrant
TPT29617A-VS1R	8-Pin MSOP	330.0	5.2	1.5	12.0	17.6	3.3	8.0	Q1
TPT29617AL1-SO1R	8-Pin SOP	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1



Package Outline Dimensions

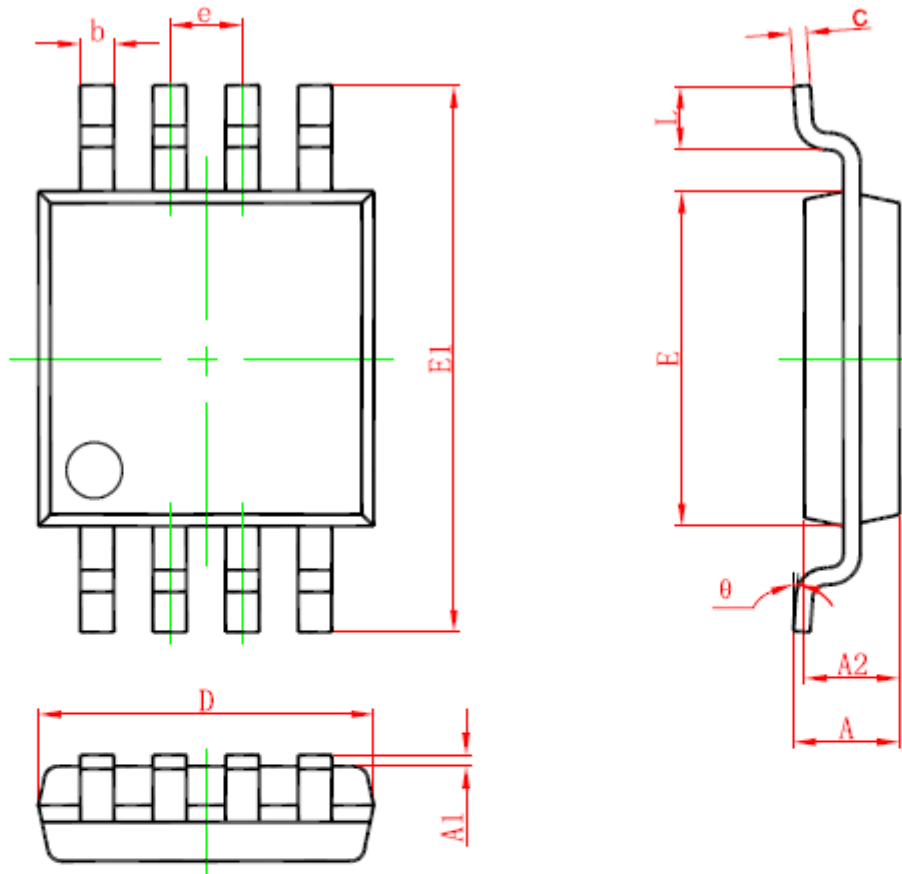
SO1R (SOP8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	0.800	0.016	0.031
$\theta$	0°	8°	0°	8°

Dual Channel Bidirectional I<sup>2</sup>C Bus  
Level Shift and Repeater

VS1R (MSOP8)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650(BSC)		0.026(BSC)	
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

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**Dual Channel Bidirectional I<sup>2</sup>C Bus Level Shift and Repeater****Order Information**

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPT29617A-VS1R	-40 to 125°C	8-Pin MSOP	9617A	MSL3	Tape and Reel, 3000	Green
TPT29617AL1-SO1R	-40 to 125°C	8-Pin SOP	9617A	MSL1	Tape and Reel, 4000	Green

**Green:** 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

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