IBM PowerPC 750GX RISC Microprocessor Revision Level DD1.X

Datasheet

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List of Figures

List of Tables

1. General Information

The IBM PowerPC® 750GX RISC[1] Microprocessor is a 32-bit implementation of the IBM PowerPC family. This document contains pertinent physical and electrical characteristics of the IBM PowerPC 750GX RISC Microprocessor Revision DD1.X Single Chip Module (SCM). The IBM PowerPC 750GX RISC Microprocessor is also referred to as the 750GX throughout this document.

1.1 Features

This section summarizes the features of the 750GX implementation of the PowerPC Architecture™. Major features of the 750GX include the following:

- Branch processing unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving two speculations)
  - Up to one speculative stream in execution, one additional speculative stream in fetch
  - 512-entry branch history table (BHT) for dynamic prediction
  - 64-entry, 4-way set associative branch target instruction cache (BTIC) for eliminating branch delay slots
- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Load/store unit
  - One cycle load or store cache access (byte, half-word, word, double-word)
  - Effective address generation
  - Hits under miss (four outstanding misses)
  - Single-cycle misaligned access within double-word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating-point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations
  - Store gathering
  - Cache and translation lookaside buffer (TLB) instructions
  - Big-endian and little-endian byte addressing supported
  - Misaligned little-endian support in hardware
- Dispatch unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, or floating-point)
  - 4-stage pipeline: fetch, dispatch, execute, and complete
  - Serialization control (predispatch, postdispatch, execution, serialization)
- Fixed-point units
  - Fixed-point unit 1 (FXU1): multiply, divide, shift, rotate, arithmetic, logical
  - Fixed-point unit 2 (FXU2): shift, rotate, arithmetic, logical
  - Single-cycle arithmetic: shift, rotate, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
  - Thirty-two 32-bit general purpose registers
- Floating-point unit
  - Support for IEEE®-754 standard single-precision and double-precision floating-point arithmetic
  - Optimized for single-precision multiply/add
  - Thirty-two 64-bit floating-point registers
  - Enhanced reciprocal estimates
  - 3-cycle latency, 1-cycle throughput, single-precision multiply-add
  - 3-cycle latency, 1-cycle throughput, double-precision add
  - 4-cycle latency, 2-cycle throughput, double-precision multiply-add
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Time deterministic non-IEEE mode

1. Reduced instruction set computer

- System unit
  - Executes Condition Register (CR) logical instructions and miscellaneous system instructions
  - Special register transfer instructions
- Level 1 (L1) cache structure
  - 32-KB, 8-way set associative instruction and data caches
  - Single-cycle cache access
  - Pseudo-least-recently-used (PLRU) replacement
  - Cache write-back or write-through operations programmable on a virtual-page or BAT-block basis
  - Parity on L1 tags and caches
  - 3-state modified/exclusive/invalid (MEI) memory coherency
  - Hardware support for data coherency
  - Non-blocking instruction cache (one outstanding miss)
  - Non-blocking data cache (four outstanding misses)
  - No snooping of instruction cache
- Memory management unit
  - 64-entry, 2-way set associative instruction TLB (total 128)
  - 64-entry, 2-way set associative data TLB (total 128)
  - Hardware reload for TLBs
  - Eight instruction block address translation (BAT) arrays and eight data BAT arrays
  - Virtual memory support for up to 4 exabytes (2^{52}) virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
  - Support for big-endian/little-endian addressing
- Dual phase-locked loops (PLLs)
  - Allow seamless frequency switching
- Level 2 (L2) cache
  - Integrated 1-MB L2 cache with on-chip controller and 8-KB entry tags
  - 4-way set-associative; supports locking by way
  - Ability to restrict the cache for instruction-only or data-only operation
  - Copy-back or write-through data cache on a page basis, or for entire L2 cache
  - 64-byte sectored line size
  - L2 frequency at core speed
  - Error checking and correction (ECC) protection on SRAM array
  - Parity on L2 tags
  - Supports up to four outstanding misses (four data or three data and one instruction)
- Power
  - Low power consumption with low voltage application at lower frequency
  - Dynamic power management
  - Three static power save modes: doze, nap, and sleep
  - Thermal assist unit (TAU)
- Bus interface
  - 32-bit address bus
  - 64-bit data bus (also supports 32-bit mode)
  - Up to 200-MHz 60x bus frequency
  - Four load/store requests, plus one snoop are supported for a total of five outstanding bus requests. Load/store requests can be a combination of three data and one instruction, or four data requests
  - Core-to-bus multipliers are supported in half-step integer increments from 2 through 10, and in full-step increments from 10 through 20. Ratios of 3.5x and lower are not supported with miss-under-miss enabled
  - Supports 1.8-V, 2.5-V, or 3.3-V I/O modes
- Reliability and serviceability
  - Parity checking on 60× bus interface
  - ECC detection and correction on L2 cache
  - Parity on the L1 caches
  - Parity on the L1 and L2 tags
- Testability
  - Level-sensitive scan design (LSSD) testing
  - Powerful diagnostic and test interface through Common On-Chip Processor (COP) and IEEE 1149.1 (JTAG) interface

1.2 Design Highlights

The 750GX supports several unique features including:

- Pin compatible with the PowerPC 750FX RISC Microprocessor
- 1-MB L2 cache, 4-way set associative, operating at core frequency
- Independent L2 cache locking of all four ways
- L2 cache may be configured to contain instructions only or data only
- Enhanced 60× bus to support up to five pipelined transactions
- Up to 1-GHz operation at embedded application specifications

1.3 Processor Version Register

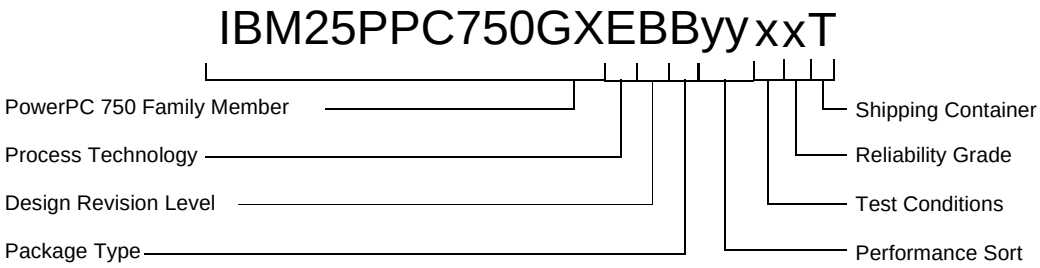
The IBM PowerPC 750GX RISC Microprocessor has the following processor version register (PVR) values for the respective design revision levels.

Table 1-1. 750GX Processor Version Register (PVR)

750GX Design Revision Level	750GX PVR
DD1.0	0x700201r0
DD1.1	0x700201r1
DD1.2	0x700201r2

Note: r = reserved nibble; reserved bits can be either '0' or '1', and should be masked in application software.

1.4 Part Number Information



Process Technology	E = 9S2, 0.13 µm
Design Revision Level	A = DD1.0 B = DD1.1 C = DD1.2
Package Type	B = Ceramic Ball Grid Array R = Reduced Lead CBGA
Performance Sort	10 = 733 MHz[1] 25 = 800 MHz 50 = 933 MHz 65 = 1.0 GHz 2H = 800 MHz, half-mode good (2) 5H = 933 MHz, half-mode good (2) 6H = 1G Hz, half-mode good (2)
Test Conditions	3 = 1.45 ±.05 V (733 MHz[1] and 800 MHz) 4 = 1.50 ±.05 V (933 MHz and 1.0 GHz) 6 = (dd1.1 only. See Erratum #8 for details) 7 = (dd1.1 only. See Erratum #8 for details) 8 = 1.50 +/- 0.05V with low-power screen (933 MHz and 1.0 GHz) 9 = (dd1.1 only. See Erratum #8 for details)
Reliability Grade	3 = Grade 3, <100 failures in time (FIT) average failure rate (AFR) 2 = Grade 2, < 25 FIT AFR
Shipping Container	T = Tray

Notes:

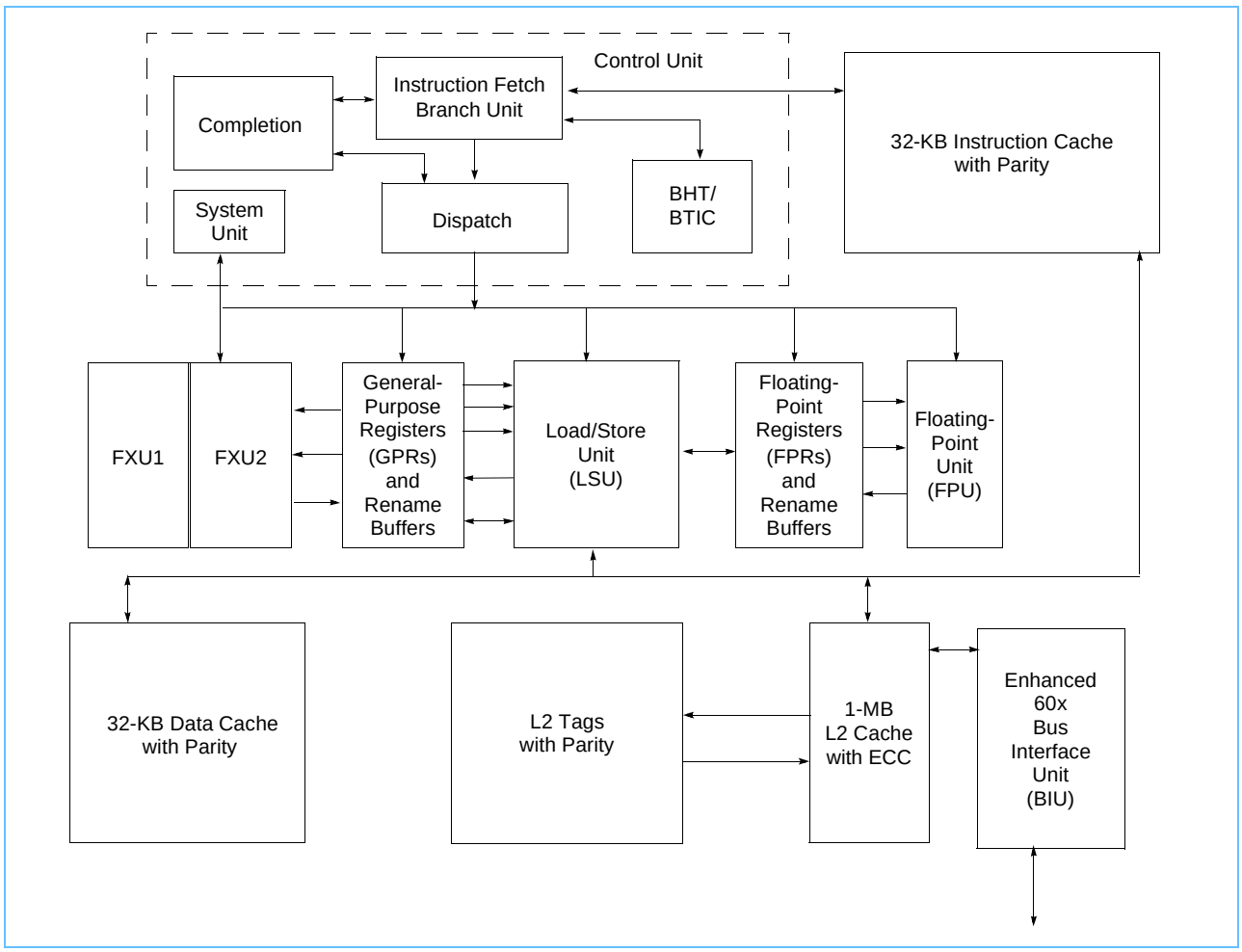
1. The 733MHz parts had limited availability in DD1.1 and are not offered in DD1.2.
2. Errata #9 does not apply to half-mode good parts.

2. Overview

The IBM PowerPC 750GX RISC Microprocessor, also called the 750GX, is targeted for high-performance, low-power systems using a 60× bus. The 750GX also includes an internal 1-MB L2 cache with on-board error correction circuitry (ECC).

2.1 Block Diagram

Figure 2-1. IBM PowerPC 750GX RISC Microprocessor Block Diagram



2.2 General Parameters

Table 2-1. 750GX General Parameters

Item	Description	Notes
Technology	0.13-µm copper silicon-on-insulator (CSOI) technology 6-layer metallization plus one level of local interconnect	
Die Size	52.5 sq. mm (diced 7.6 mm × 6.9 mm)	
Logic design	Fully static	
Package	292-pin ceramic ball grid array (CBGA) 21 × 21 mm (1.0-mm pitch) 0.8-mm ball size	
Core power supply	1.45 V ±50 mV for 733 and 800 MHz 1.5 V ±50 mV for 933 MHz and 1.0 GHz	1
I/O power supply	3.3 V ±165 mV (BVSEL = 1, L1_TSTCLK = 0) or 2.5 V ±125 mV (BVSEL = 1, L1_TSTCLK = 1) or 1.8 V ±100 mV (BVSEL = 0, L1_TSTCLK = 1)	2

Notes:

1. Lower core voltages are offered to allow slower operation at substantial power savings (see the *IBM PowerPC 750GX RISC Microprocessor Supplement* for power reduction trade-offs).
2. BVSEL = 0, L1_TSTCLK = 0 is an *invalid* setting.

3. Electrical and Thermal Characteristics

This section provides AC and DC electrical specifications and thermal characteristics for the 750GX.

3.1 DC Electrical Characteristics

The tables in this section describe the DC electrical characteristics for the 750GX.

Table 3-1. Absolute Maximum Ratings [1]

Characteristic	Symbol	1.8 V	2.5 V	3.3 V	Unit	Notes
Core supply voltage	V_{DD}	-0.3 to 1.6	-0.3 to 1.6	-0.3 to 1.6	V	3, 4
PLL supply voltage	$A1V_{DD}$, $A2V_{DD}$	-0.3 to 1.6	-0.3 to 1.6	-0.3 to 1.6	V	3, 4, 5
60x bus supply voltage	OV_{DD}	-0.3 to 2.0	-0.3 to 2.75	-0.3 to 3.7	V	3, 4
Input voltage	V_{IN}	-0.3 to 2.0	-0.3 to 2.75	-0.3 to 3.7	V	2
Storage temperature range	T_{STG}	-55 to 150	-55 to 150	-55 to 150	°C	

Notes:

1. Functional and tested operating conditions are given in *Table 3-2 Recommended Operating Conditions*. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed above may affect device reliability or cause permanent damage to the device.
2. **Caution:** Transient V_{IN} overshoots of up to OV_{DD} + 0.8 V, with a maximum of 4.0 V for 3.3 V operation, and undershoots down to GND - 0.8 V, are allowed for up to 5 ns.
3. **Caution:** OV_{DD} must not exceed V_{DD}/AV_{DD} by more than 2.5 V continuously. OV_{DD} may exceed V_{DD}/AV_{DD} by up to 2.65 V for up to 20 ms during power-on or power-off. OV_{DD} must not exceed V_{DD}/AV_{DD} by more than 2.65 V for any amount of time.
4. **Caution:** V_{DD}/AV_{DD} must not exceed OV_{DD} by more than 1.0 V continuously. V_{DD}/AV_{DD} may exceed OV_{DD} by up to 1.6 V for up to 20 ms during power-on or power-off. V_{DD}/AV_{DD} must not exceed OV_{DD} by more than 1.6 V for any amount of time.
5. **Caution:** AV_{DD} must not exceed V_{DD} by more than 0.5 V at any time.

Table 3-2. Recommended Operating Conditions

Characteristic	Symbol	Value	Unit	Notes
Core supply voltage (733 MHz–800 MHz)	V_{DD}	1.4 to 1.5	V	1, 2, 4
Core supply voltage (933 MHz–1.0 GHz)	V_{DD}	1.45 to 1.55	V	1, 2
PLL supply voltage (733 MHz–800 MHz)	AV_{DD}	1.4 to 1.5	V	1, 3, 4
PLL supply voltage (933 MHz–1.0 GHz)	AV_{DD}	1.45 to 1.55	V	1, 3
60× bus supply voltage (1.8 V)	OV_{DD}	1.7 to 1.9	V	2
60× bus supply voltage (2.5 V)	OV_{DD}	2.375 to 2.625	V	2
60× bus supply voltage (3.3 V)	OV_{DD}	3.135 to 3.465	V	2
Input voltage	V_{IN}	GND to OV_{DD}	V	2
Die-junction temperature	T_J	-40 to 105	°C	

Notes:

1. Lower core voltages are supported to allow slower operation at substantial power savings.
2. These are recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
3. AV_{DD} should be set to the same value as V_{DD} for single PLL operation.
4. Operation with Vdd up to 1.55V is supported, but the power dissipation will increase.

Table 3-3. Package Thermal Characteristics

Characteristic	Symbol	Value	Unit
CBGA package thermal resistance, junction-to-case thermal resistance (typical)	θ_{JC}	0.1	°C/W
CBGA package thermal resistance, junction-to-lead thermal resistance (typical)	θ_{JB}	7.6	°C/W

Note: θ_{JC} is the internal resistance from the junction to the back of the die. A heat sink customized to the end user application and ambient operating environment is required to ensure the die junction temperature is maintained within the limits defined in *Table 3-2* on page 15. For more information about thermal management, see *Section 5.7* on page 61.

Table 3-4. DC Electrical Specifications
See *Table 3-2* on page 15 for recommended operating conditions.

Characteristic	Symbol	Voltage		Unit	Notes
		Min.	Max.		
Input high voltage (all inputs except system clock [SYSCLK])	$V_{IH\ (1.8\ V)}$	1.20	—	V	
	$V_{IH\ (2.5\ V)}$	1.70	—	V	
	$V_{IH\ (3.3\ V)}$	2.4	—	V	
Input low voltage (all inputs except SYSCLK)	$V_{IL\ (1.8\ V)}$	—	0.60	V	
	$V_{IL\ (2.5\ V)}$	—	0.70	V	
	$V_{IL\ (3.3\ V)}$	—	0.80	V	
SYSCLK input high voltage	$CV_{IH\ (1.8\ V)}$	1.20	—	V	
	$CV_{IH\ (2.5\ V)}$	1.90	—	V	
	$CV_{IH\ (3.3\ V)}$	2.1	—	V	
SYSCLK input low voltage	$CV_{IL\ (1.8\ V,\ 2.5\ V,\ 3.3\ V)}$	—	0.40	V	
Input leakage current, V_{IN} = applies to all OV_{DD} levels	I_{IN}	—	300	µA	2
Hi-Z (off state) leakage current, V_{IN} = applies to all OV_{DD} levels	I_{TSI}	—	20	µA	2
Output high voltage, I_{OH} = -4 mA	$V_{OH\ (1.8\ V)}$	1.30	—	V	
	$V_{OH\ (2.5\ V)}$	2.00	—	V	
	$V_{OH\ (3.3\ V)}$	2.40	—	V	
Output low voltage, I_{OL} = 4 mA	$V_{OL\ (1.8\ V,\ 2.5\ V,\ 3.3\ V)}$	—	0.4	V	
Capacitance, V_{IN} = 0 V, f = 1 MHz	C_{IN}	—	7	pF	1

Notes:
1. Capacitance values are guaranteed by design and characterization, and are not tested.
2. Additional input current may be attributed to the Level Protection Keeper Lock circuitry. For details, see *Section 5.9, Operational and Design Considerations,* on page 69.

Table 3-5. Power Consumption for DD1.1
See *Table 3-2* on page 15 for recommended operating conditions.

Mode	T_j	Processor Frequency				Unit	Notes
		733 MHz	800 MHz	933 MHz	1.0 GHz		
Core Voltage	—	1.45	1.45	1.5	1.5	V	
Maximum Power	105°C	9.5	9.75	12.5	14.0	W	1, 2
Typical Power	65°C	4.90	5.0	7.35	8.3	W	1, 3
Nap Power, Maximum	50°C	4.3	4.3	5.2	6.3	W	1
Sleep Power, Maximum	50°C	4.3	4.3	5.2	6.0	W	1

Notes:
1. These values apply for all valid 60× buses. The values do not include I/O supply power (OV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} power is system dependent, but is typically less than 2% of V_{DD} power.
2. Maximum power is measured at the indicated V_{DD} and T_J using parts with worst-case process parameters and running RC5-72. RC5-72 runs hotter than typical production code, but it is possible to design code that runs even hotter than RC5-72. See *Reducing PowerPC 750GX Power Dissipation* Application Note for more information.
3. Typical power is an estimate of the average value modeled in a system executing typical applications with V_{DD} and typical process parameters. Note that typical power cannot be used in the design of the power supply or cooling system.

Table 3-6. Power Consumption for DD1.2
See *Table 3-2* on page 15 for recommended operating conditions.

Mode	T_j	Processor Frequency					Unit	Notes
		800 MHz Standard	933 MHz Low Power	933 MHz Standard	1.0 GHz Low Power	1.0 GHz Standard		
Core Voltage	—	1.45	1.5	1.5	1.5	1.5	V	
Maximum Power	105°C	11.5	10.75	13.75	11	14	W	1, 2
Typical Power	65°C	6.5	6.5	8.0	6.75	8.3	W	1, 3
Nap Power, Maximum	50°C	5.2	4.5	6.2	4.5	6.3	W	1
Sleep Power, Maximum	50°C	5.2	4.3	6.0	4.3	6.0	W	1

Notes:
1. These values apply for all valid 60× buses. The values do not include I/O supply power (OV_{DD}) or PLL supply power (AV_{DD}). OV_{DD} power is system dependent, but is typically less than 2% of V_{DD} power.
2. Maximum power is measured at the indicated V_{DD} and T_J using parts with worst-case process parameters and running RC5-72. RC5-72 runs hotter than typical production code, but it is possible to design code that runs even hotter than RC5-72. See *PowerPC 750GX Power Dissipation* Application Note for more information.
3. Typical power is an estimate of the average value modeled in a system executing typical applications with V_{DD} and typical process parameters. Note that typical power cannot be used in the design of the power supply or cooling system.

3.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the 750GX. After fabrication, parts are sorted by maximum processor core frequency as shown in *Section 3.3, Clock AC Specifications,* on page 18, and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL configuration (PLL_CFG[0-4]) signals.

3.3 Clock AC Specifications

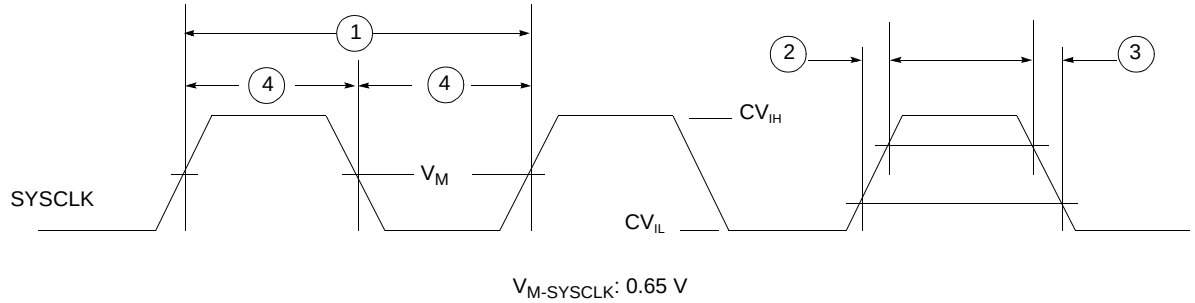
Table 3-7 provides the clock AC timing specifications as defined in *Figure 3-1*.

Table 3-7. Clock AC Timing Specifications
See *Table 3-2* on page 15 for recommended operating conditions.[1, 3, 6]

Figure 3-1 Timing Reference	Characteristic	Value		Unit	Notes
		Min.	Max.		
	Processor frequency	500	1000	MHz	
	SYSCLK frequency	25	200	MHz	
1	SYSCLK cycle time	5.0	40	ns	
2, 3	SYSCLK slew rate	1.0	4.0	V/ns	2
4	SYSCLK duty cycle measured at 0.65 V	25	75	%	
	SYSCLK cycle-to-cycle jitter	—	±150	ps	4
	Internal PLL relock time	—	100	µs	5

Notes:
1. **Caution:** The SYSCLK frequency and the PLL_CFG[0:4] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in *Table 5-2, 750GX Microprocessor PLL Configuration,* on page 48 for valid PLL_CFG[0:4] settings.
2. Slew rate for the SYSCLK inputs is measured from 0.4 to 1.0 V.
3. Timing is guaranteed by design and characterization, and is not tested.
4. See *Section 3.4, Spread Spectrum Clock Generator,* on page 19 for long-term jitter.
5. Relock timing is guaranteed by design and characterization, and is not tested. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that hard reset ($\overline{\text{HRESET}}$) must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
6. Lower voltage and frequency operation will be available based on characterization results. See the *IBM PowerPC 750GX RISC Microprocessor Supplement* for more information.

Figure 3-1. SYSCLK Input Timing Diagram



3.4 Spread Spectrum Clock Generator

3.4.1 Design Considerations

When designing with the Spread Spectrum Clock Generator (SSCG), there are a number of design issues that must be taken into account.

SSCG creates a controlled amount of long-term jitter. In order for a receiving PLL in the 750GX to operate in this environment, it must be able to accurately track the SSCG clock jitter.

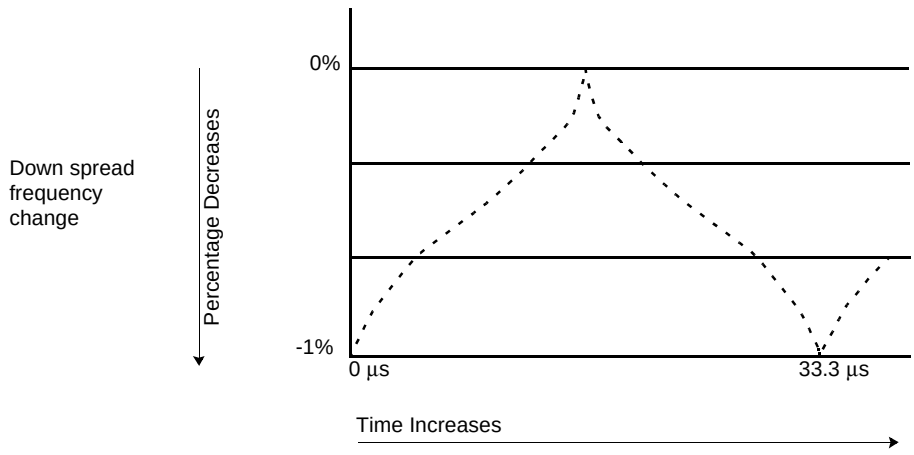
The accuracy to which the 750GX PLL can track the SSCG clock is referred to as tracking skew. When performing system timing analysis, the tracking skew must be added or subtracted to the I/O timing specifications because the tracking skew appears as a static phase error between the internal PLL and the SSCG clock.

To minimize the impact on I/O timings, the following SSCG configuration is recommended:

- Down spread mode, less than or equal to 1% of the maximum frequency.
- A modulation frequency of 30 kHz.
- Linear sweep modulation or “Hershey’s Kiss” (as in a Lexmark[1] profile) modulation profile as shown in *Figure 3-2*.

In this configuration, the tracking skew is less than 100 ps.

Figure 3-2. Linear Sweep Modulation Profile



1. See patent 5,631,920.

3.5 60x Bus Input AC Specifications

Table 3-8 provides the 60x bus AC timing specifications defined in *Figure 3-4* and *Figure 3-5* on page 22.

Table 3-8. 60x Bus Input AC Timing Specifications
See *Table 3-2* on page 15 for operating conditions.[1, 5, 6]

Figure 3-4 and 3-5 Timing Reference	Characteristic	1.8 V Mode		2.5 V Mode		3.3 V Mode		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
10a	Input setup: SYSCLK to inputs valid.	1.0	—	1.1	—	1.6	—	ns	
10c	Mode select input setup to HRESET (TLBISYNC, DRTRY, L2_TSTCLK, DBDIS, QACK, and DBWO)	8	—	8	—	8	—	sysclk cycles	2, 3, 4
11a	Input hold: SYSCLK to inputs invalid	0.45	—	0.3	—	0.3	—	ns	
11c	HRESET to mode select input hold (TLBISYNC, DRTRY, L2_TSTCLK, DBDIS, QACK, and DBWO)	0	4	0	4	0	4	sysclk cycles	2, 4
V_M	Measurement reference voltage for inputs	$OV_{DD}/2$						—	
V_{IL-AC}	AC timing reference levels	—	0.2	—	0.2	—	0.2	V	7
V_{IH-AC}		$OV_{DD - 0.2}$	—	$OV_{DD - 0.2}$	—	$OV_{DD - 0.2}$	—		
Slew Rate	Reference input slew rate	1.0	—	1.5	—	2.0	—	V/ns	

Notes:
1. Input specifications are measured from the midpoint voltage (V_M) of the signal in question to the V_M of the rising edge of the input SYSCLK. Timings are measured at the pin (see *Figure 3-4* on page 21).
2. The setup and hold time is with respect to the rising edge of HRESET (see *Figure 3-5* on page 22).
3. t_{SYSCLK} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. This specification is for configuration mode select only. Also note that the HRESET must be held asserted for a *minimum of 255 bus clocks* after the PLL relock time during the power-on reset sequence.
5. All values are guaranteed by design, and are not tested.
6. Refer to *Section 3.5.1* on page 20 and *Figure 3-3* on page 21 for input setup timing definitions.
7. Input reference signal levels used to establish the timings defined in this table.

3.5.1 Input Setup Timing

The information in this subsection is provided to clarify the criteria used to establish the timings in *Table 3-8*. The DC Electrical Specifications shown in *Table 3-4* on page 16 are not altered by this clarification. The valid input signal levels remain V_{IH} and V_{IL}.

The input setup times shown as 10a in *Table 3-8* specify the required time from the input signal crossing V_M to the rising edge of SYSCLK crossing V_M.

For the timings in *Table 3-8* to be valid, the falling edge of the input signal shown in *Table 3-8* is assumed to transition through V_M and cross V_{IL-AC} at the slew rate specified in *Table 3-8*. Input signals that do not reach the V_{IL-AC} boundary, or slew from V_M to V_{IL-AC} more slowly than specified, will result in longer input setup times.

In the same way, on the rising edge, the input signal must continue past V_M and cross the V_{IH-AC} boundary within the specified minimum slew rate. Input signals that do not reach the V_{IH-AC} boundary within the slew rate specified will result in longer input setup times.

Figure 3-4 provides the input timing diagram for the 750GX.

Figure 3-3. Input Timing Definition

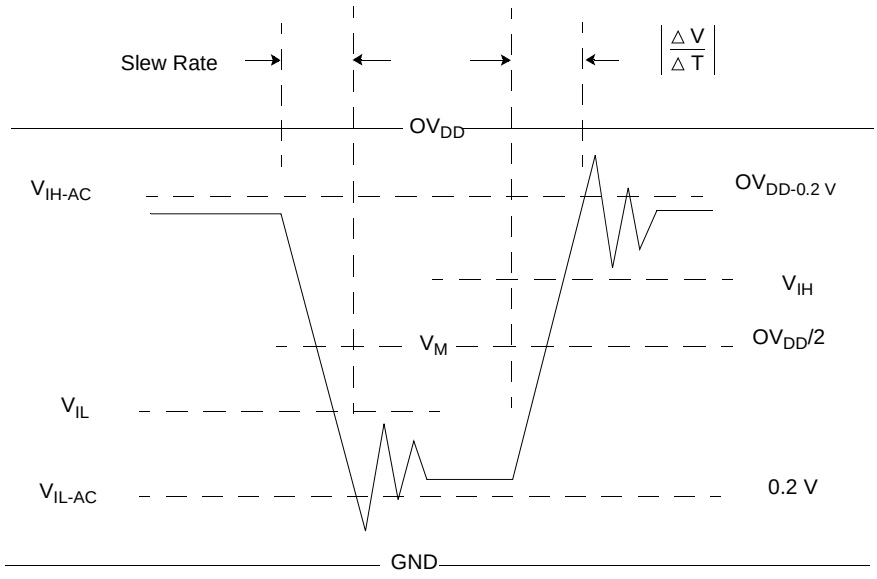
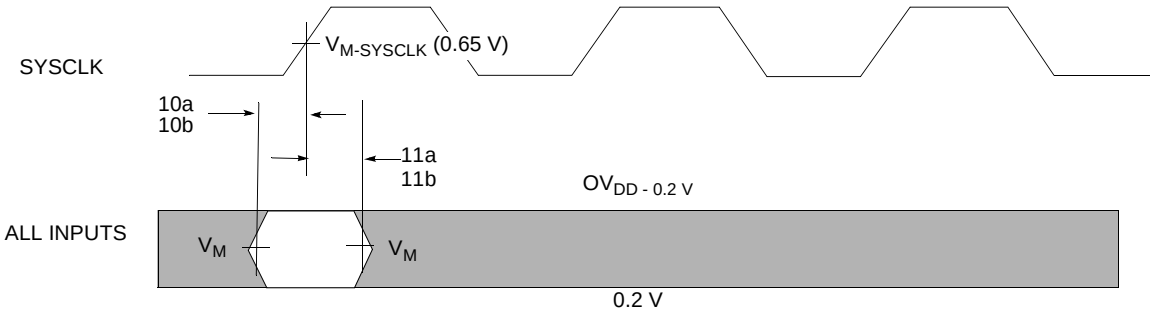


Figure 3-4. Input Timing Diagram

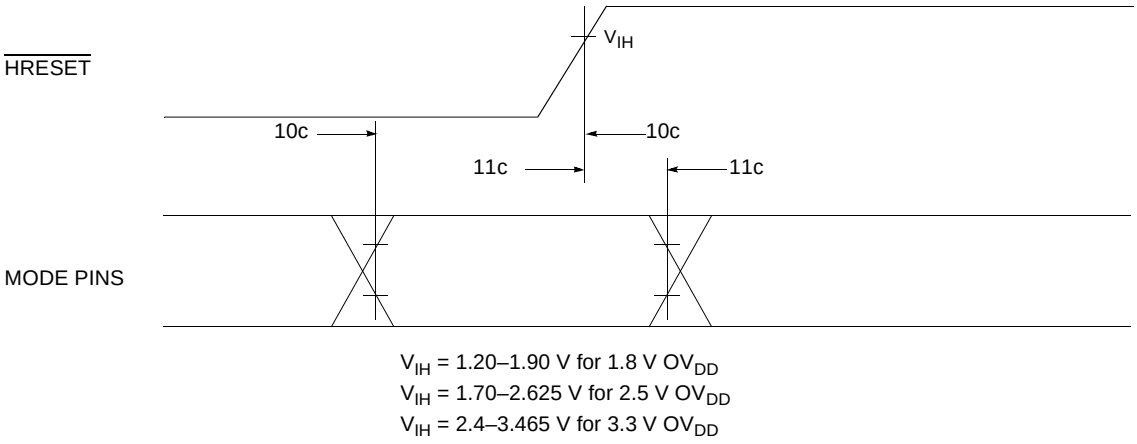


V_M = Midpoint Voltage (OV_{DD}/2)

Note: The minimum slew rate specified in *Table 3-8* on page 20 is required to achieve the input timings specified. See *Section 3.5.1, Input Setup Timing,* on page 20 and *Figure 3-3* for additional information.

Figure 3-5 provides the mode select input timing diagram for the 750GX.

Figure 3-5. Mode Select Input Timing Diagram



3.6 60x Bus Output AC Specifications

Table 3-9 provides the 60× bus output AC timing specifications for the 750GX as defined in *Figure 3-7* on page 25.

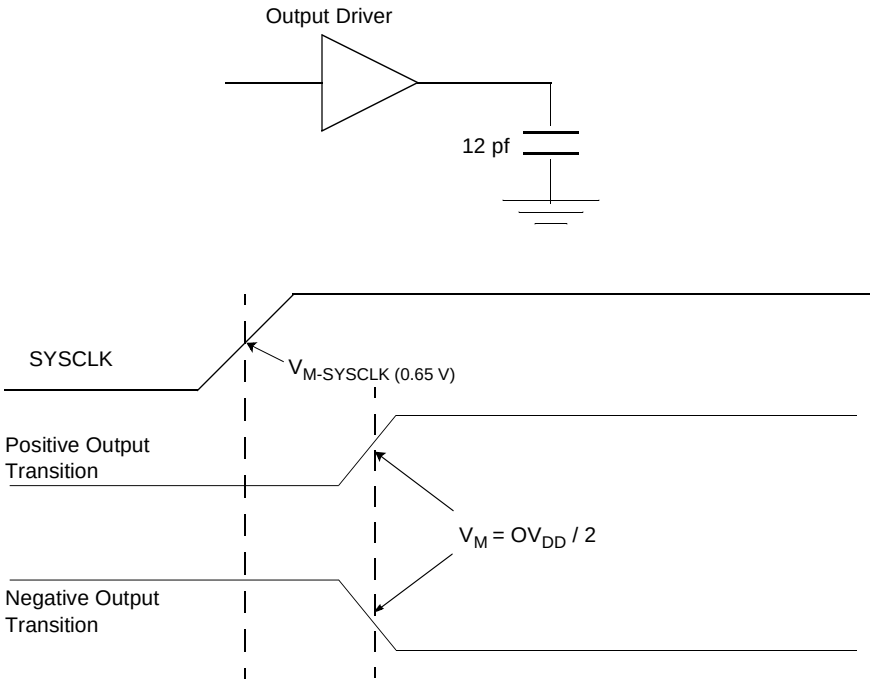
Table 3-9. 60x Bus Output AC Timing Specifications
See *Table 3-2* on page 15 for operating conditions.[1, 4, 6]

Figure 3-7 Timing Reference	Characteristic	1.8 V		2.5 V		3.3 V		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
12	SYSCLK to Output Driven (Output Enable Time)	0.3	—	0.3	—	0.3	—	ns	
13	SYSCLK to Output Valid	—	2.4	—	2.3	—	2.4	ns	5
14	SYSCLK to Output Invalid (Output Hold)	1.0	—	0.6	—	0.6	–	ns	
15	SYSCLK to Output High Impedance (all signals except address retry [ARTRY], address bus busy [ABB], and data bus busy [DBB])	—	2.5	—	2.5	—	2.5	ns	
16	SYSCLK to $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ high impedance after precharge	—	1.0	—	1.0	—	1.0	t_{SYSCLK}	2
17	SYSCLK to $\overline{\text{ARTRY}}$ high impedance before precharge	—	3.0	—	3.0	—	3.0	ns	
18	SYSCLK to $\overline{\text{ARTRY}}$ precharge enable	$0.2 \times t_{SYSCLK} + 1.0$		$0.2 \times t_{SYSCLK} + 1.0$	—	$0.2 \times t_{SYSCLK} + 1.0$	—	ns	3
19	Maximum delay to $\overline{\text{ARTRY}}$ precharge	—	1.0	—	1.0	—	1.0	t_{SYSCLK}	2, 3
20	SYSCLK to $\overline{\text{ARTRY}}$ high impedance after precharge	—	2.0	—	2.0	—	2.0	t_{SYSCLK}	2, 3

Notes:

1. All output specifications are measured from the V_M of the rising edge of SYSCLK to the midpoint of the output signal in question using a test load as shown in *Figure 3-6* on page 24. Both input and output timings are measured at the pin. Timings are determined by design.
2. t_{SYSCLK} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration of the parameter in question.
3. Nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}.
4. Guaranteed by design and characterization, and not tested.
5. Output Valid timing increases as the V_{DD} is reduced. These values assume a V_{DD} minimum of 1.4 V.
6. See *Figure 3-6* on page 24 and *Figure 3-7* on page 25 for output loading and timing definitions.

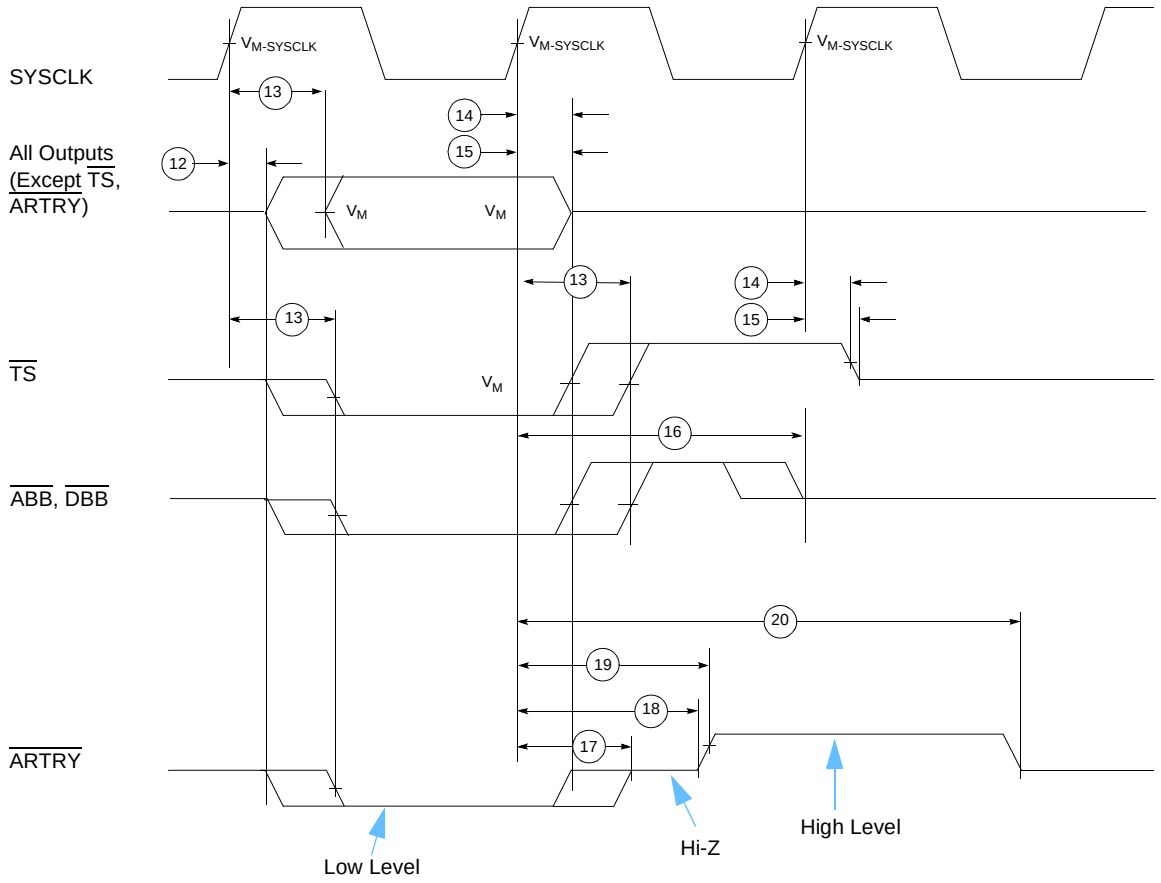
Figure 3-6. Output Valid Timing Definition



Output Transition defined between SYSCLK at V_M and the respective transition level.

Note: The timing definition is valid using the termination model shown here with timings referenced to the respective pin of the specified output driver.

Figure 3-7. Output Timing Diagram for IBM PowerPC 750GX RISC Microprocessor



Note: SYSCLK V_M as defined in *Section 3.3, Clock AC Specifications,* on page 18.
Output V_M as defined in *Figure 3-6, Output Valid Timing Definition,* on page 24.

3.6.1 IEEE 1149.1 AC Timing Specifications

Table 3-10 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in the following figures:

To find out more about...	See...
JTAG Clock Input Timing Diagram	*Figure 3-8* on page 27.
TRST Timing Diagram	*Figure 3-9* on page 27.
Boundary-Scan Timing Diagram	*Figure 3-10* on page 27.
Test Access Port Timing Diagram	*Figure 3-11* on page 28.

The five JTAG signals are: test data input (TDI), test data output (TDO), test mode select (TMS), test clock (TCK), and test reset ($\overline{\text{TRST}}$).

Table 3-10. JTAG AC Timing Specifications (Independent of SYSCLK)
See *Table 3-2* on page 15 for operating conditions.

Figures 3-8 through 3-11 Timing Reference	Characteristic	Min.	Max.	Unit	Notes
	TCK frequency of operation	0	25	MHz	
1	TCK cycle time	40	—	ns	
2	TCK clock pulse width measured at 1.1 V	15	—	ns	
3	TCK rise and fall times	0	2	ns	4
4	Specification obsolete, intentionally omitted	—	—	—	
5	$\overline{\text{TRST}}$ assert time	25	—	ns	1
6	Boundary-scan input data setup time	0	—	ns	2
7	Boundary-scan input data hold time	13	—	ns	2
8	TCK to output data valid	—	8	ns	3, 5
9	TCK to output high impedance	3	19	ns	3, 4
10	TMS, TDI data setup time	0	—	ns	
11	TMS, TDI data hold time	15	—	ns	
12	TCK to TDO data valid	2.0	12	ns	5
13	TCK to TDO high impedance	3	9	ns	4
14	TCK to output data invalid (output hold)	0	—	ns	

Notes:
1. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. Guaranteed by design.
2. Non-JTAG signal input timing with respect to TCK.
3. Non-JTAG signal output timing with respect to TCK.
4. Guaranteed by characterization and not tested.
5. Minimum specification guaranteed by characterization and not tested.

Figure 3-8 provides the JTAG clock input timing diagram.

Figure 3-8. JTAG Clock Input Timing Diagram

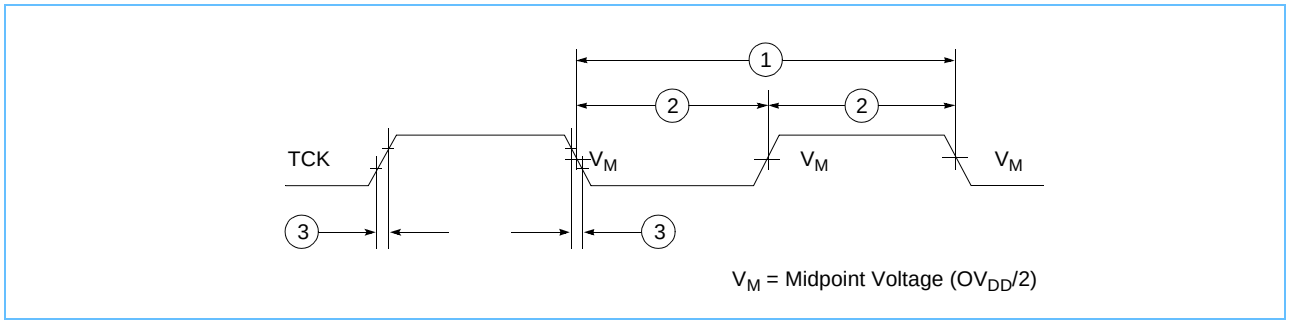


Figure 3-9 provides the $\overline{\text{TRST}}$ timing diagram.

Figure 3-9. $\overline{TRST}$ Timing Diagram

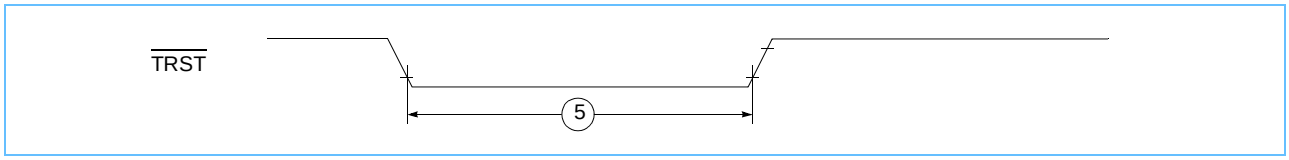


Figure 3-10 provides the boundary-scan timing diagram.

Figure 3-10. Boundary-Scan Timing Diagram

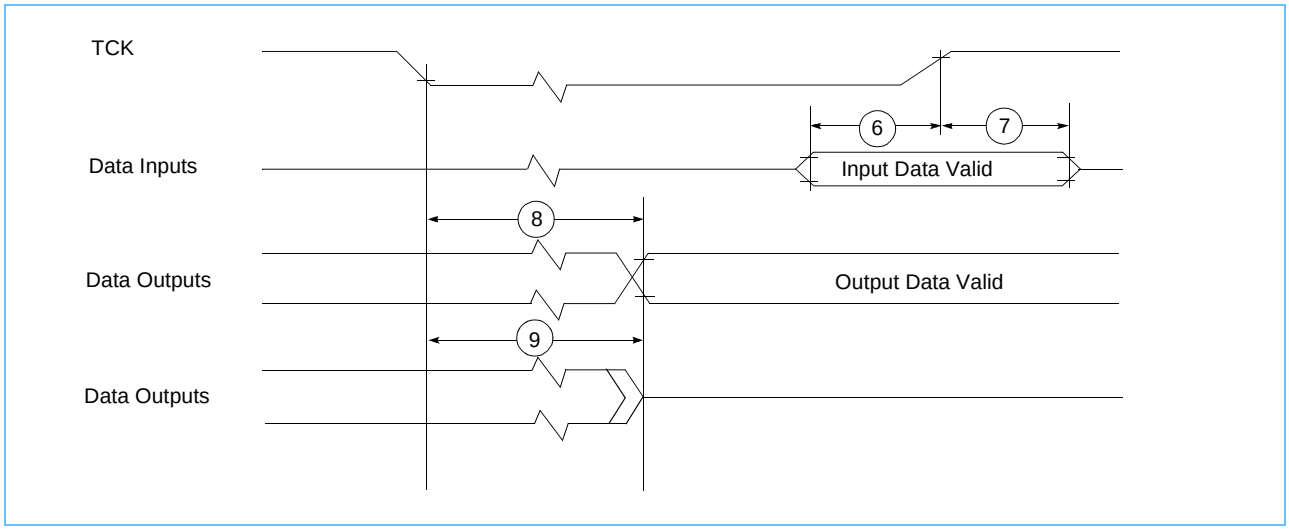
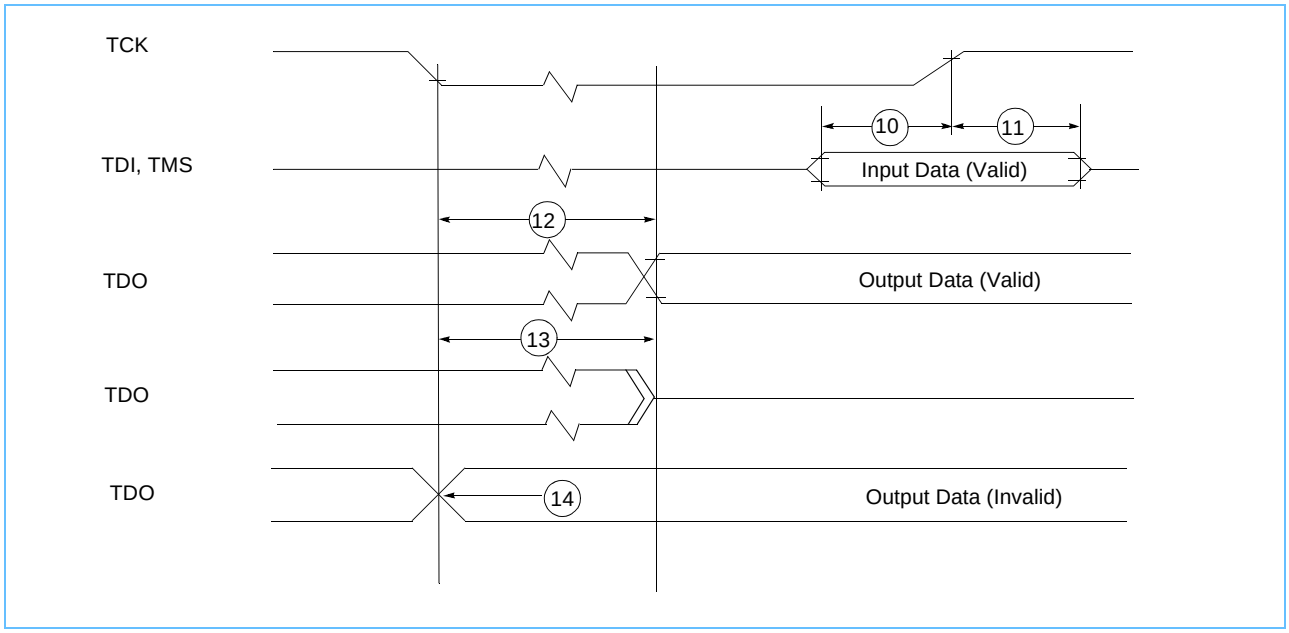


Figure 3-11 provides the test access port timing diagram.

Figure 3-11. Test Access Port Timing Diagram



4. Dimensions and Signal Assignments

IBM offers a ceramic ball grid array (CBGA) that supports 292 balls for the 750GX package. This is a signal and power compatible footprint to the PowerPC 750FX RISC Microprocessor module. Use A01 corner designation for correct placement. Use the five plated dots that form a right angle (|_) to locate the A01 corner.

4.1 Package

4.1.1 Reduced-Lead package

This section describes the reduced-lead package, as indicated by the ‘R’ in the Package code field of the part number. For the reduced lead package, lead-free solder is used for the substrate capacitors and the BGA balls on the bottom of the package. Standard high melting point 97Pb3Sn solder (exempted by EU RoHS legislation) is used for the C4 balls that connect the die to the substrate. The resulting module is RoHS compatible.

All Datasheet electrical specifications apply equally to standard and reduced-lead parts.

4.1.1.1 Mechanical Specifications

The reduced-lead 292-CBGA package uses the same signal pinout, ball center-to-center spacing, and 21x21mm package outline as the leaded package. The solder balls on the bottom of the reduced-lead package are slightly smaller, which will decrease the overall module height when assembled onto a board. Heatsink solutions should be modified accordingly.

Table 4-1. Standard and Reduced-Lead Package, Layout, and Assembly Differences

Package	JEDEC MSL	Solder Ball Composition	Solder Ball Diameter	CBGA Substrate I/O Pad Diameter	Card Solder Mask Opening Diameter	Card Solder Screen Diameter	Card Pad Diameter
Standard	1	Sn 10% Pb 90%	31.5 (0.80)	31.5 (0.80)	31.5 (0.80)	26.5mil opening in 7.5mil thick stencil, 2500-4600 cubic mils	27.5 (0.70)
Reduced Lead	3	Sn 95.5% Ag 3.8% Cu 0.7%	25 (0.635)	27.55 (0.71)	28 (0.72)	23mil opening in 4mil thick stencil, 1400-2000 cubic mils	24 (0.61)
Note: All dimensions in mils unless noted. Dimensions in parenthesis are in mm.							

4.1.1.2 Assembly Considerations

The reduced-lead package is compatible with a 260C lead-free card assembly reflow profile. Refer to the NEMI Consortium, www.nemi.org, for industry-standard assembly and rework information. The coplanarity specification for the reduced-lead CBGA, like other single melt BGA packages, is 0.20 mm (8mil).

The qualification testing included a lead-free water soluble solder paste with type 3 mesh size (-325/+500). The solder alloy is 95.5% Sn, 4.0% Ag, and 0.5% Cu, with a 90% metal loading. The paste viscosity range is 600 to 800 Kcps. The thickness of the stencil is 4 mils and the aperture size is 23 mil diameter. The target solder paste volume range is between 1400 to 2000 cubic mils. Achieving the correct paste volume is necessary for eliminating solder shorts and producing high reliability solder joints. The actual solder paste volume from the qualification build ranged from 1750 to 2000 cubic mils.

Another change is the JEDEC Moisture Sensitivity Level, which is MSL 3 for the reduced-lead package. Storage and assembly protocols should be modified accordingly.

4.1.1.3 Board Layout Considerations

As shown in *Table 4-1*, the smaller size of the reduced-lead ball is matched by a smaller pad on the module substrate, and requires a smaller recommendation for card pad size (for the ball end of the dogbone), solder mask opening, and solder screen diameter.

4.1.2 Package Mechanical Drawings

Figure 4-1. Mechanical Dimensions, Standard (Leaded) Package

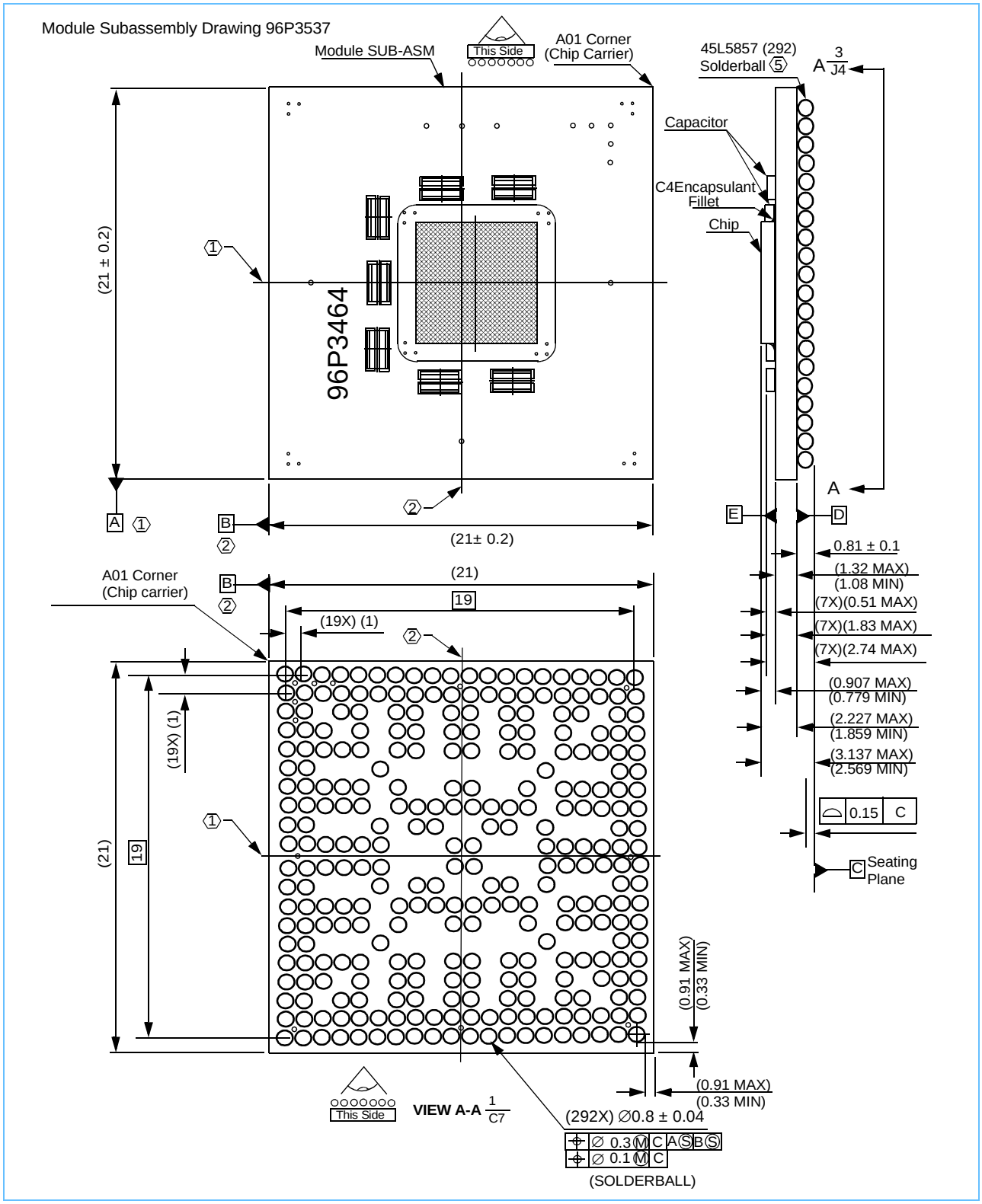


Figure 4-1. Mechanical Dimensions, Standard (Leaded) Package(Continued)

Notes:

1. DATUM A is the center plane of feature labeled DATUM A.
2. DATUM B is the Center plane of feature labeled DATUM B.
3. Unless otherwise specified, part is symmetrical about centerlines defined by DATUMs A and B.
4. Where not otherwise defined, centerlines indicated are to be interpreted as a DATUM framework established by DATUMs D, A, and B, respectively.
5. Eutectic solder 63/37 Sn/Pn is used to join ball to chip carrier.

Figure 4-2. Mechanical Dimensions, ROHS-Compatible Package

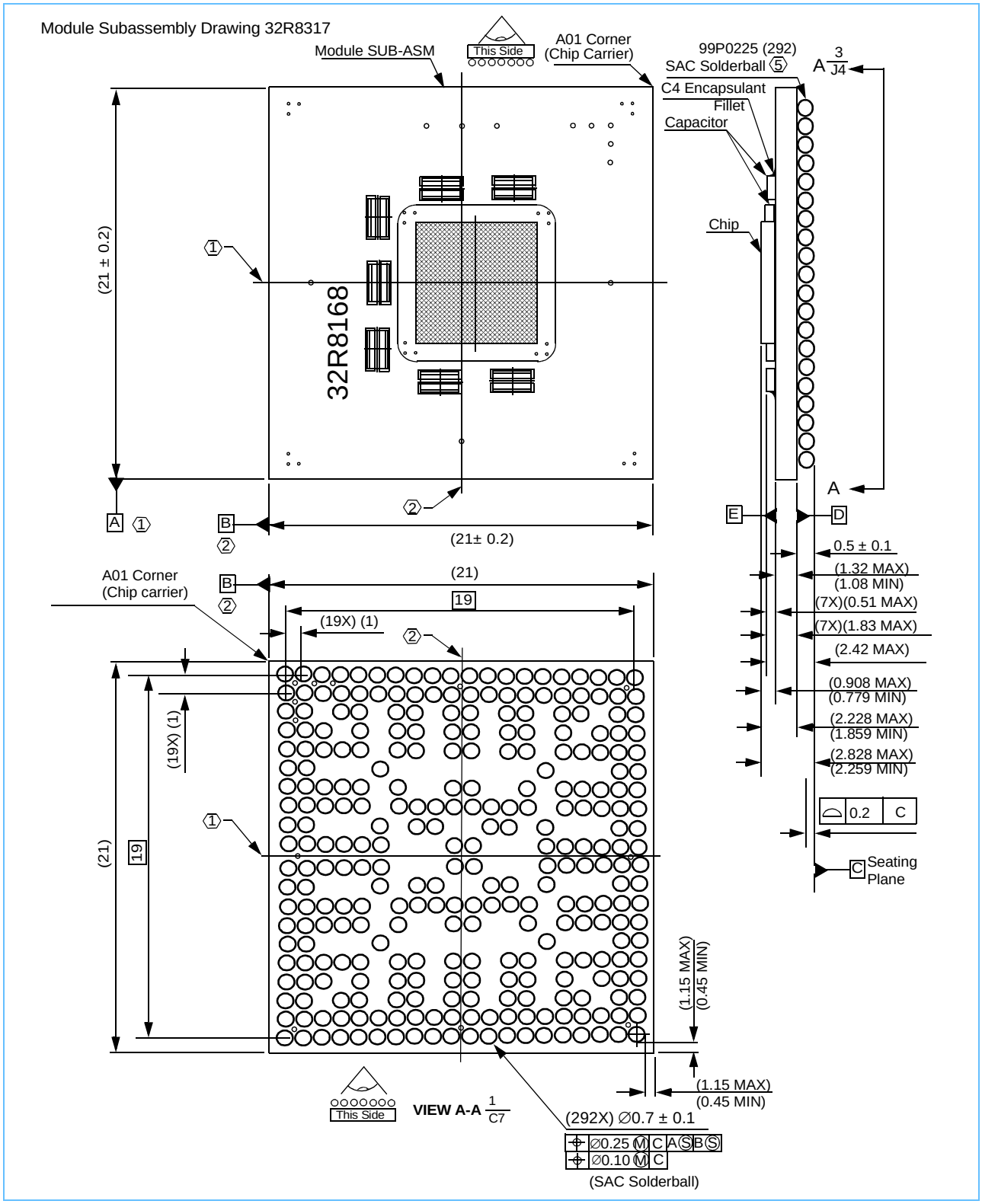


Figure 4-2. Mechanical Dimensions, ROHS-Compatible Package (Continued)

Notes:

〈1〉 DATUM A is the center plane of feature labeled DATUM A.

〈2〉 DATUM B is the Center plane of feature labeled DATUM B.

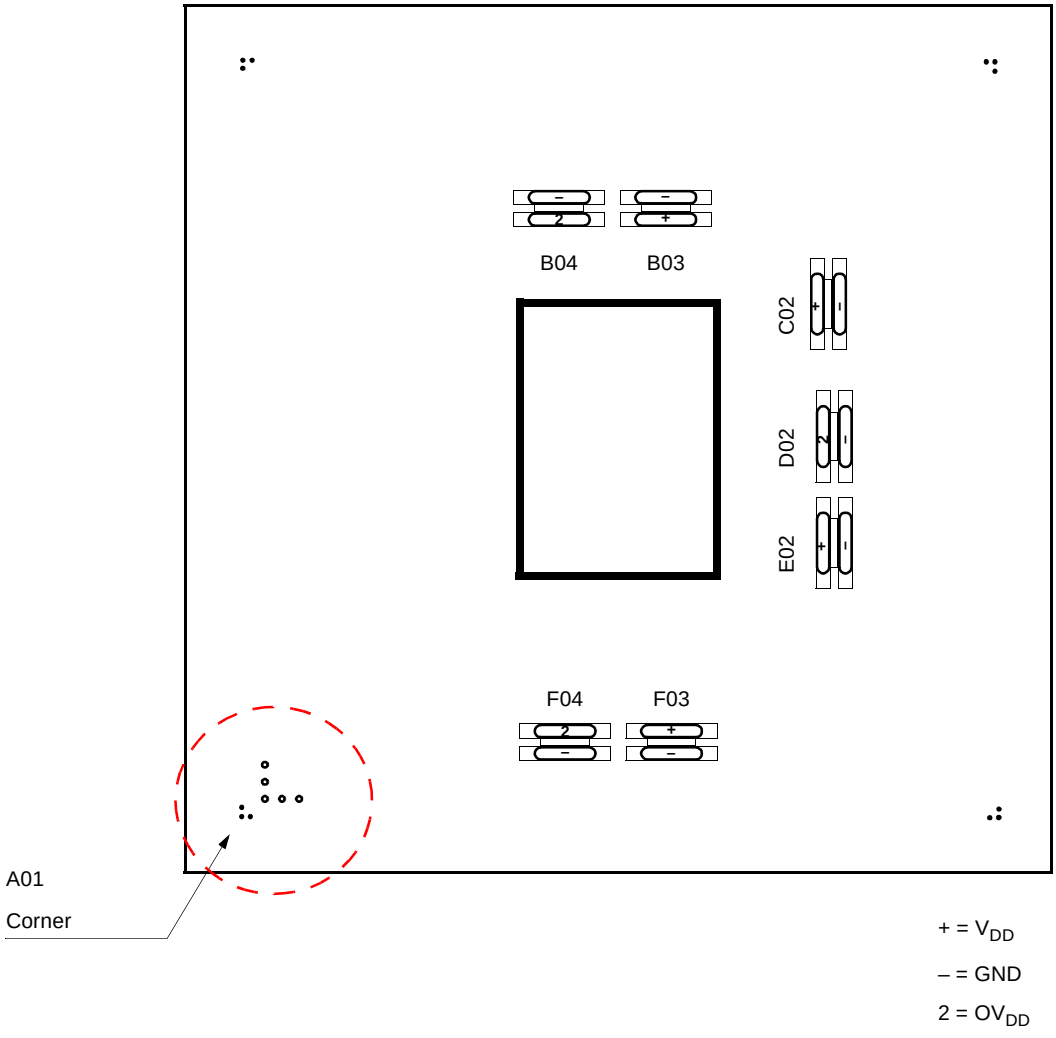
3. Unless otherwise specified, part is symmetrical about centerlines defined by DATUMs A and B.
4. Where not otherwise defined, centerlines indicated are to be interpreted as a DATUM framework established by DATUMs D, A, and B, respectively.

〈5〉 SnAgCu (SAC) balls joined to the chip carrier.

4.2 Module Substrate Decoupling Voltage Assignments

The on-board substrate voltage-to-ground assignments for the capacitor locations are shown in *Figure 4-3*.

Figure 4-3. Module Substrate Decoupling Voltage Assignments



4.3 Microprocessor Ball Placement

Figure 4-4. PowerPC 750GX Microprocessor Ball Placement

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y
20	A6	A8	A3	A2	A0	DH31	DH25	DH26	DP2	DH22	DH19	DH18	DH16	DH15	DH14	DP0	DH9	DH10	DH4	DH2
19	A13	GND	A5	A4	A1	DH29	DP3	DH28	DH23	DH24	DH21	DH20	DP1	DH17	DH11	DH8	DH6	DH5	GND	DH3
18	A11	A10		**OVDD**	GND		**OVDD**	GND		VDD	VDD		GND	**OVDD**		GND	**OVDD**		DH0	PLL_CFG0
17	A12	TT1	**OVDD**		A9		DH30	DH27		GND	GND		DH12	DH13		DH1		**OVDD**	PLL_CFG1	PLL_CFG2
16	A14	A15	GND	AP0	A7		GND	**OVDD**		**OVDD**	**OVDD**		**OVDD**	GND		DH7	PLL_CFG3	GND	SYSCLK	**A2VDD**
15	TT3	TS				VDD									VDD				PLL_RNG0	**A1VDD**
14	TSIZ0	TT2	**OVDD**	TT0	GND		**OVDD**			GND	GND			**OVDD**		GND	**PLL_RNG1**	**OVDD**	PLL_CFG4	**AGND**
13	AP2	TT4	GND	AP1	VDD		GND	GND	VDD	VDD	VDD	VDD	GND	GND		VDD	LLSD_ MODE	GND	L2_TSTCLK	L1_TSTCLK
12	TA	TSIZ1				VDD		GND	GND			GND	GND		VDD				MCP	CHECKSTOP
11	TBST	TSIZ2	VDD	GND	**OVDD**	GND				VDD	VDD				GND	**OVDD**	GND	VDD	TLBISYNC	HRESET
10	DBDIS	A16	VDD	GND	**OVDD**	GND				GND	GND				GND	**OVDD**	GND	VDD	SMI	CKSTP
9	A18	A17				VDD		GND	VDD			VDD	GND		VDD				BVSEL	INT
8	AACK	AP3	GND	A21	VDD		GND	GND	VDD	VDD	VDD	VDD	GND	GND		VDD	QREQ	GND	TBEN	QACK
7	A20	A19	**OVDD**	A24	GND		**OVDD**			GND	GND			**OVDD**		GND	DBB	**OVDD**	ARTRY	SRESET
6	DBWO	A23				VDD									VDD				TEA	ABB
5	A22	A26	GND	A25	A31		GND	**OVDD**		**OVDD**	**OVDD**		**OVDD**	GND		CLK_O UT	WT	GND	TDO	DBG
4	A28	A27	**OVDD**		DL3		DP5	DL13		GND	GND		DL23	DL26		CI		**OVDD**	BG	RSRV
3	A29	A30		**OVDD**	GND		**OVDD**	GND		VDD	VDD		GND	**OVDD**		GND	**OVDD**		DRTRY	BR
2	DL0	GND	DL2	DL6	DL5	DL11	DL10	DL12	DL16	DL15	DL19	DL20	DL22	DL27	DL28	TCK	DL30	TDI	GND	BLANK
1	DL1	DP4	DL4	DL8	DL7	DL9	DL14	DP6	DL18	DL17	DL21	DP7	DL24	DL25	DL29	DL31	TRST	TMS	GBL	BLANK

Note: This view is looking down from above the 750GX placed and soldered on the system board.

4.4 Pinout Listings

Table 4-2 contains the pinout listing for the 750GX CBGA package.

Table 4-2. Pinout Listing for the CBGA package

Signal Name	Pin Number	Active	Input/Output	Notes
A[0:31]	E20, E19, D20, C20, D19, C19, A20, E16, B20, E17, B18, A18, A17, A19, A16, B16, B10, B9, A9, B7, A7, D8, A5, B6, D7, D5, B5, B4, A4, A3, B3, E5.	High	Input/Output	
$A1V_{DD}$	Y15	—	—	
$A2V_{DD}$	Y16	—	—	
$\overline{AACK}$	A8	Low	Input	
$\overline{ABB}$	Y6	Low	Input/Output	
AGND	Y14	—	—	
AP[0:3]	D16, D13, A13, B8	High	Input/Output	6
$\overline{ARTRY}$	W7	Low	Input/Output	
$\overline{BG}$	W4	Low	Input	
BLANK	Y1, Y2	—	—	3
$\overline{BR}$	Y3	Low	Output	
BVSEL	W9	—	Input	4
$\overline{CHECKSTOP}$ (CKSTP_OUT)	Y12	Low	Output	
$\overline{CI}$	T4	Low	Output	
$\overline{CKSTP\_IN}$	Y10	Low	Input	
CLK_OUT	T5	High	Output	
$\overline{DBB}$	U7	Low	Input/Output	
$\overline{DBDIS}$	A10	Low	Input	
$\overline{DBG}$	Y5	Low	Input	
$\overline{DBWO}$	A6	Low	Input	
DH[0:31]	W18, T17, Y20, Y19, W20, V19, U19, T16, T19, U20, V20, R19, N17, P17, R20, P20, N20, P19, M20, L20, M19, L19, K20, J19, K19, G20, H20, H17, H19, F19, G17, F20	High	Input/Output	
DL[0:31]	A2, A1, C2, E4, C1, E2, D2, E1, D1, F1, G2, F2, H2, H4, G1, K2, J2, K1, J1, L2, M2, L1, N2, N4, N1, P1, P4, P2, R2, R1, U2, T1	High	Input/Output	
DP[0:7]	T20, N19, J20, G19, B1, G4, H1, M1	High	Input/Output	6
$\overline{DRTRY}$	W3	Low	Input	
$\overline{GBL}$	W1	Low	Input/Output	

Notes:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. OV_{DD} inputs supply power to the input/output drivers and V_{DD} inputs supply power to the processor core.
3. These pins are reserved for potential future use.
4. BVSEL and L1_TSTCLK select the input/output voltage mode on the 60x bus.
5. TCK must be tied high or low for normal machine operation.
6. Address and data parity should be left floating if unused in the design.

Table 4-2. Pinout Listing for the CBGA package (Continued)

Signal Name	Pin Number	Active	Input/Output	Notes
GND	B2, B19, C5, C8, C13, C16, D10, D11, E3, E7, E14, E18, F10, F11, G5, G8, G13, G16, H3, H8, H9, H12, H13, H18, J12, K4, K7, K10, K14, K17, L4, L7, L10, L14, L17, M12, N3, N8, N9, N12, N13, N18, P5, P8. P13, P16, R10, R11, T3, T7, T14, T18, U10, U11, V5, V8, V13,V16, W2, W19,	—	—	
$\overline{\text{HRESET}}$	Y11	Low	Input	
$\overline{\text{INT}}$	Y9	Low	Input	
L1_TSTCLK	Y13	High	Input	4
L2_TSTCLK	W13	High	Input	1
$\overline{\text{LSSD\_MODE}}$	U13	Low	Input	1
$\overline{\text{MCP}}$	W12	Low	Input	
OV_{DD}	C4, C7, C14, C17, D3, D18, E10, E11, G3, G7, G14, G18, H5, H16, K5, K16, L5, L16, N5, N16, P3, P7, P14, P18, T10, T11, U3, U18, V4, V7, V14, V17	—	—	2
PLL_CFG[0:4]	Y18, W17, Y17, U16, W14	High	Input	
PLL_RNG[0:1]	W15, U14	High	Input	
$\overline{\text{QACK}}$	Y8	Low	Input	
$\overline{\text{QREQ}}$	U8	Low	Output	
$\overline{\text{RSRV}}$	Y4	Low	Output	
$\overline{\text{SMI}}$	W10	Low	Input	
$\overline{\text{SRESET}}$	Y7	Low	Input	
SYSCLK	W16	High	Input	
$\overline{\text{TA}}$	A12	Low	Input	
TBEN	W8	High	Input	
$\overline{\text{TBST}}$	A11	Low	Input/Output	
TCK	T2	High	Input	5
TDI	V2	High	Input	
TDO	W5	High	Output	
$\overline{\text{TEA}}$	W6	Low	Input	
$\overline{\text{TLBISYNC}}$	W11	Low	Input	
TMS	V1	High	Input	
$\overline{\text{TRST}}$	U1	Low	Input	
$\overline{\text{TS}}$	B15	Low	Input/Output	
TSIZ[0:2]	A14, B12, B11	High	Output	

Notes:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. OV_{DD} inputs supply power to the input/output drivers and V_{DD} inputs supply power to the processor core.
3. These pins are reserved for potential future use.
4. BVSEL and L1_TSTCLK select the input/output voltage mode on the 60x bus.
5. TCK must be tied high or low for normal machine operation.
6. Address and data parity should be left floating if unused in the design.

Table 4-2. Pinout Listing for the CBGA package (Continued)

Signal Name	Pin Number	Active	Input/Output	Notes
TT[0:4]	D14, B17, B14, A15, B13	High	Input/Output	
V_{DD}	C10, C11, E8, E13, F6, F9, F12, F15, J8, J9, J13, K3, K8, K11, K13, K18, L3, L8, L11, L13, L18, M8, M9, M13, R6, R9, R12, R15, T8, T13, V10, V11	—	—	2
$\overline{WT}$	U5	Low	Output	

Notes:

1. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
2. OV_{DD} inputs supply power to the input/output drivers and V_{DD} inputs supply power to the processor core.
3. These pins are reserved for potential future use.
4. BVSEL and L1_TSTCLK select the input/output voltage mode on the 60x bus.
5. TCK must be tied high or low for normal machine operation.
6. Address and data parity should be left floating if unused in the design.

Table 4-3. Signal Listing for the CBGA Package

Signal Name	Pin Count	Active	Input/Output	Notes
A[0:31]	32	High	Input/Output	
$A1V_{DD}$	1	—	—	Supply for PLL0
$A2V_{DD}$	1	—	—	Supply for PLL1
$\overline{AACK}$	1	Low	Input	
$\overline{ABB}$	1	Low	Input/Output	
AGND	1	—	—	Ground for PLL
AP[0:3]	4	High	Input/Output	
$\overline{ARTRY}$	1	Low	Input/Output	
$\overline{BG}$	1	Low	Input	
$\overline{BR}$	1	Low	Output	
BVSEL	1	High	Input	I/O voltage mode select for 60x bus. See *Section 5.9.3* on page 70 for setup conditions.
$\overline{CI}$	1	Low	Output	
$\overline{CKSTP\_IN}$	1	Low	Input	
CKSTP_OUT	1	Low	Output	
CLK_OUT	1	High	Output	
$\overline{DBB}$	1	Low	Input/Output	
$\overline{DBDIS}$	1	Low	Input	Factory usage mode pin. Pull inactive (high) when HRESET transitions from low to high for normal machine operation.
$\overline{DBG}$	1	Low	Input	
$\overline{DBWO}$	1	Low	Input	Factory usage mode pin. Pull inactive (high) when HRESET transitions from low to high for normal machine operation.
DH[0:31]	32	High	Input/Output	
DL[0:31]	32	High	Input/Output	
DP[0:31]	8	High	Input/Output	
$\overline{DRTRY}$	1	Low	Input	*Optional* data retry mode select. This function will be set when HRESET transitions from low to high. DRTRY high indicates data-retry mode; DRTRY low indicates no data-retry mode.
$\overline{GBL}$	1	Low	Input/Output	
Ground	60	—	—	Common ground
$\overline{HRESET}$	1	Low	Input	See note 1.

Notes:

1. $\overline{QACK}$ in a logical high state at the transition of $\overline{HRESET}$ from asserted to negated enables standard pre-charge mode in the 750GX.
   $\overline{QACK}$ in a logical low state at the transition of $\overline{HRESET}$ from asserted to negated enables extended pre-charge mode in the 750GX.
2. $\overline{QACK}$, in a logical low state at the transition of $\overline{QREQ}$ from asserted to negated, enables the 750GX processor to enter the soft stop (Nap) state for proper JTAG emulator operation.

Table 4-3. Signal Listing for the CBGA Package (Continued)

Signal Name	Pin Count	Active	Input/Output	Notes
$\overline{\text{INT}}$	1	Low	Input	
L1_TSTCLK	1	High	Input	I/O voltage mode select for 60x bus. See *Section 5.9.3* on page 70 for setup conditions.
L2_TSTCLK	1	High	Input	These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
LSSD_MODE	1	Low	Input	These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
$\overline{\text{MCP}}$	1	Low	Input	
OV_{DD}	32	—	—	Supply for receivers/drivers
PLL_CFG[0:4]	5	High	Input	
PLL_RNG[0:1]	2	High	Input	
$\overline{\text{QACK}}$	1	Low	Input	See notes 1 and 2.
$\overline{\text{QREQ}}$	1	Low	Output	
$\overline{\text{RSRV}}$	1	Low	Output	
$\overline{\text{SMI}}$	1	Low	Input	
$\overline{\text{SRESET}}$	1	Low	Input	
SYSCLK	1	High	Input	
$\overline{\text{TA}}$	1	Low	Input	
TBEN	1	High	Input	
$\overline{\text{TBST}}$	1	Low	Input/Output	
TCK	1	High	Input	
TDI	1	High	Input	
TDO	1	High	Output	
$\overline{\text{TEA}}$	1	Low	Input	
$\overline{\text{TLBISYNC}}$	1	Low	Input	*Optional*: 64/32-Bit Data Bus mode select. This function will be set when $\overline{\text{HRESET}}$ transitions (low to high). TLBISYNC: high = 64-bit mode, low = 32-bit mode.
TMS	1	High	Input	
$\overline{\text{TRST}}$	1	Low	Input	
$\overline{\text{TS}}$	1	Low	Input/Output	
TSIZ[0:2]	3	High	Output	
TT[0:4]	5	High	Input/Output	
V_{DD}	32			Supply for core

Notes:

1. $\overline{\text{QACK}}$ in a logical high state at the transition of $\overline{\text{HRESET}}$ from asserted to negated enables standard pre-charge mode in the 750GX.
   $\overline{\text{QACK}}$ in a logical low state at the transition of $\overline{\text{HRESET}}$ from asserted to negated enables extended pre-charge mode in the 750GX.
2. $\overline{\text{QACK}}$, in a logical low state at the transition of $\overline{\text{QREQ}}$ from asserted to negated, enables the 750GX processor to enter the soft stop (Nap) state for proper JTAG emulator operation.

Table 4-3. Signal Listing for the CBGA Package (Continued)

Signal Name	Pin Count	Active	Input/Output	Notes
$\overline{\text{WT}}$	1	Low	Output	

Notes:

1. $\overline{\text{QACK}}$ in a logical high state at the transition of $\overline{\text{HRESET}}$ from asserted to negated enables standard pre-charge mode in the 750GX.
   $\overline{\text{QACK}}$ in a logical low state at the transition of $\overline{\text{HRESET}}$ from asserted to negated enables extended pre-charge mode in the 750GX.
2. $\overline{\text{QACK}}$, in a logical low state at the transition of $\overline{\text{QREQ}}$ from asserted to negated, enables the 750GX processor to enter the soft stop (Nap) state for proper JTAG emulator operation.

Table 4-4. Signal Locations

Signal	Ball Location	Signal	Ball Location	Signal	Ball Location	Signal	Ball Location
A0	E20	DH0	W18	DL0	A2	$\overline{\text{AACK}}$	A8
A1	E19	DH1	T17	DL1	A1	$\overline{\text{ABB}}$	Y6
A2	D20	DH2	Y20	DL2	C2	AGND	Y14
A3	C20	DH3	Y19	DL3	E4	$\overline{\text{ARTRY}}$	W7
A4	D19	DH4	W20	DL4	C1	$\overline{\text{BG}}$	W4
A5	C19	DH5	V19	DL5	E2	$\overline{\text{BR}}$	Y3
A6	A20	DH6	U19	DL6	D2	BVSEL	W9
A7	E16	DH7	T16	DL7	E1	$\overline{\text{CHECKSTOP}}$ ($\overline{\text{CKSTP\_OUT}}$)	Y12
A8	B20	DH8	T19	DL8	D1	$\overline{\text{CI}}$	T4
A9	E17	DH9	U20	DL9	F1	CLK_OUT	T5
A10	B18	DH10	V20	DL10	G2	$\overline{\text{CKSTP}}$ ($\overline{\text{CKSTP\_IN}}$)	Y10
A11	A18	DH11	R19	DL11	F2	$\overline{\text{DBB}}$	U7
A12	A17	DH12	N17	DL12	H2	$\overline{\text{DBDIS}}$	A10
A13	A19	DH13	P17	DL13	H4	$\overline{\text{DBG}}$	Y5
A14	A16	DH14	R20	DL14	G1	$\overline{\text{DBWO}}$	A6
A15	B16	DH15	P20	DL15	K2	$\overline{\text{DRTRY}}$	W3
A16	B10	DH16	N20	DL16	J2	$\overline{\text{GBL}}$	W1
A17	B9	DH17	P19	DL17	K1	$\overline{\text{HRESET}}$	Y11
A18	A9	DH18	M20	DL18	J1	$\overline{\text{INT}}$	Y9
A19	B7	DH19	L20	DL19	L2	L1_TSTCLK	Y13
A20	A7	DH20	M19	DL20	M2	L2_TSTCLK	W13
A21	D8	DH21	L19	DL21	L1	$\overline{\text{LSSD\_MODE}}$	U13
A22	A5	DH22	K20	DL22	N2	$\overline{\text{MCP}}$	W12
A23	B6	DH23	J19	DL23	N4	PLL_CFG0	Y18
A24	D7	DH24	K19	DL24	N1	PLL_CFG1	W17
A25	D5	DH25	G20	DL25	P1	PLL_CFG2	Y17
A26	B5	DH26	H20	DL26	P4	PLL_CFG3	U16
A27	B4	DH27	H17	DL27	P2	PLL_CFG4	W14
A28	A4	DH28	H19	DL28	R2	PLL_RNG0	W15
A29	A3	DH29	F19	DL29	R1	PLL_RNG1	U14
A30	B3	DH30	G17	DL30	U2	$\overline{\text{QACK}}$	Y8
A31	E5	DH31	F20	DL31	T1	$\overline{\text{QREQ}}$	U8
						$\overline{\text{RSRV}}$	Y4
						$\overline{\text{SMI}}$	W10
						$\overline{\text{SRESET}}$	Y7
						SYSCLK	W16

Table 4-4. Signal Locations (Continued)

Signal	Ball Location	Signal	Ball Location	Signal	Ball Location	Signal	Ball Location
		AP0	D16	DP0	T20	$\overline{TA}$	A12
		AP1	D13	DP1	N19	TBEN	W8
		AP2	A13	DP2	J20	$\overline{TBST}$	A11
		AP3	B8	DP3	G19	TCK	T2
				DP4	B1	TDI	V2
				DP5	G4	TDO	W5
				DP6	H1	$\overline{TEA}$	W6
				DP7	M1	$\overline{TLBISYNC}$	W11
						TMS	V1
						$\overline{TRST}$	U1
						$\overline{TS}$	B15
						TSIZ0	A14
						TSIZ1	B12
						TSIZ2	B11
						TT0	D14
						TT1	B17
						TT2	B14
						TT3	A15
						TT4	B13
						$\overline{WT}$	U5

Table 4-5. Voltage and Ground Assignments

$A1V_{DD}$	$A2V_{DD}$	OV_{DD}	OV_{DD}	V_{DD}	V_{DD}	GND	GND
Y15	Y16	C4	C7	C10	C11	B2	B19
		C14	C17	E8	E13	C5	C8
		D3	D18	F6	F9	C13	C16
		E10	E11	F12	F15	D10	D11
		G3	G7	J8	J9	E3	E7
		G14	G18	J13	K3	E14	E18
		H5	H16	K8	K11	F10	F11
		K5	K16	K13	K18	G5	G8
		L5	L16	L3	L8	G13	G16
		N5	N16	L11	L13	H3	H8
		P3	P7	L18	M8	H9	H12
		P14	P18	M9	M13	H13	H18
		T10	T11	R6	R9	J12	K4
		U3	U18	R12	R15	K7	K10
		V4	V7	T8	T13	K14	K17
		V14	V17	V10	V11	L4	L7
						L10	L14
						L17	M12
						N3	N8
						N9	N12
						N13	N18
						P5	P8
						P13	P16
						R10	R11
						T3	T7
						T14	T18
						U10	U11
						V5	V8
						V13	V16
						W2	W19

5. System Design Information

This section provides electrical and thermal design recommendations for successful applications on the 750GX.

5.1 Core Voltage Operation

The 750GX supports a single V_{DD} setting for a specific application condition. The AV_{DD} supplies can be set to the same voltage as V_{DD}, and the PLL range (PLL_RNG[0:1]) bits are as defined in *Table 5-1* on page 48.

5.2 Low Voltage Operation at Lower Frequency

Due to the relationship of power to frequency and voltage (power proportional to frequency and a square of voltage), running the processor at an associated lower voltage and lower frequency results in significant power savings. Low voltage application conditions will be defined after characterization is completed.

After the 750GX application condition, within the supported limits, has been selected, the 750GX's dual PLL feature can also be used to provide additional power savings.

5.2.1 Overview

The 750GX design includes two PLLs (PLL0 and PLL1), allowing the processor clock frequency to dynamically change between the PLL frequencies via software control. Use the bits in Hardware Implementation Dependent Register 1 (HID1) to specify:

- The frequency range of each PLL
- The clock multiplier for each PLL
- External or internal control of PLL0
- Which PLL is selected (which is the source of the processor clock at any given time)

At power-on reset, the HID1 register contains zeros for all the non-read-only bits (bits 7 to 31). This configuration corresponds to the selection of PLL0 as the source of the processor clocks and selects the external configuration and range pins to control PLL0. The external configuration and range pin values are accessible to software using HID1 read-only bits 0-6. PLL1 is always controlled by its internal configuration and range bits. The HID1 setting associated with hard reset corresponds to a PLL1 configuration of clock off, and selection of the medium frequency range.

As stated in the hardware specification, $\overline{\text{HRESET}}$ must be asserted during power up long enough for the PLL(s) to lock, and for the internal hardware to be reset. Once this timing is satisfied, $\overline{\text{HRESET}}$ can be negated. The processor now will proceed to execute instructions, clocked by PLL0 as configured via the external pins. The processor clock frequency can be modified from this initial setting in one of two ways. First, as with earlier designs, $\overline{\text{HRESET}}$ can be asserted, and the external configuration pins can be set to a new value. The machine state is lost in this process, and, as always, $\overline{\text{HRESET}}$ must be held asserted while the PLL relocks, and the internal state is reset. Second, the introduction of another PLL provides an alternative means of changing the processor clock frequency, which does not involve the loss of machine state nor a delay for PLL relock.

The following sequence can be used to change processor clock frequency.

Note: Assume PLL0 is currently the source for the processor clock.

1. Configure PLL1 to produce the desired clock frequency by setting HID1[PR1] and HID1[PC1] to the appropriate values.
2. Wait for PLL1 to lock. The lock time is the same for both PLLs (see *Table 3-7, Clock AC Timing Specifications,* on page 18).
3. Set HID1[PS] to '1' to initiate the transition from PLL0 to PLL1 as the source of the processor clocks. From the time the HID1 register is updated to select the new PLL, the transition to the new clock frequency will complete within three bus cycles. After the transition, the HID(PSS) bit indicates which PLL is in use.

   After both PLLs are running and locked, the processor frequency can be toggled with very low latency. For example, when it is time to change back to the PLL0 frequency, there is no need to wait for PLL lock. HID1[PS] can be reset to '0', causing the processor clock source to transition from PLL1 back to PLL0. If PLL0 will not be needed for some time, it can be configured to be off while not in use. This is done by resetting the HID1[PC0] field to '0', and setting HID1[PI0] to '1'. Turning the non-selected PLL off results in a modest power savings, but introduces added latency when changing frequency. If PLL0 is configured to be off, the procedure for switching to PLL0 as the selected PLL involves changing the configuration and range bits, waiting for lock, and then selecting PLL0, as described in the previous paragraph.

5.2.2 Restrictions and Considerations for PLL Configuration

Consider the following when reconfiguring the PLLs:

- The configuration and range bits in HID1 should only be modified for the non-selected PLL, since it will require time to lock before it can be used as the source for the processor clock.
- The HID1[PI0] bit should only be modified when PLL0 is not selected.
- Whenever one of the PLLs is reconfigured, it must not be selected as the active PLL until enough time has elapsed for the PLL to lock.
- At all times, the frequency of the processor clock, as determined by the various configuration settings, must be within the specification range for the current operating conditions.
- Never select a PLL that is in the off configuration.

5.2.2.1 Configuration Restriction on Frequency Transitions

It is considered a programming error to switch from one PLL to the other when both are configured in a half-cycle multiplier mode. For example, with PLL0 configured in 9:2 mode (PC0) and PLL1 configured in 13:2 mode (PC1), changing the select bit (HID1[PS]) is not allowed. In cases where such a pairing of configurations is desired, an intermediate full-cycle configuration must be used between the two half-cycle modes. For example, with PLL0 at 9:2, PLL1, configured at 6:1, is selected. Then PLL0 is reconfigured at 13:2, locked, and selected.

5.2.3 PLL_RNG[0:1] Definitions for Dual PLL Operation

The dual PLLs on the 750GX are configured by the PLL_CFG[0:4] and PLL_RNG[0:1] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and voltage controlled oscillator (VCO) frequency of operation. The 750GX PLL range configuration for dual PLL operation is shown in the following table.

Table 5-1. PLL_RNG[0:1] Definitions for Dual PLL Operation

PLL_RNG[0:1]	PLL Frequency Range
00 (default)	600 MHz–900 MHz
01 (fast)	900 MHz–1.0 GHz
10 (slow)	500 MHz–600 MHz
11 (reserved)	Reserved

Note: PLL_RNG bit settings are valid for a V_{DD} range of 1.4 V–1.55 V and a temperature range of -40°C–105°C.

5.2.4 PLL Configuration

Table 5-2 shows the PLL configuration for the 750GX for nominal frequencies.

Table 5-2. 750GX Microprocessor PLL Configuration

PLL_CFG [0:4]		Processor to Bus Frequency Ratio (PTBFR)	Frequency Range Supported by VCO Having an Example Range of...			
			SYSCLK[1] (MHz)		Core (MHz)	
Binary	Decimal		Minimum ($SYSCLK_{MIN}$)	Maximum ($SYSCLK_{MAX}$)	Minimum ($Core\ Frequency_{MIN}$)	Maximum ($Core\ Frequency_{MAX}$)
00000	0	Off[2]	N/A	N/A	Off	Off
00001	1	Off[2]	N/A	N/A	Off	Off
00010	2	PLL Bypass[3]	N/A	N/A	N/A	N/A
00011	3	PLL Bypass[3]	N/A	N/A	N/A	N/A
00100	4	2×[4]	N/A	N/A	N/A	N/A
00101	5	2.5×[4]	200	200	500	500
00110	6	3×[4]	167	200	500	600
00111	7	3.5×[4]	143	200	500	700
01000	8	4×	125	200	500	800
01001	9	4.5×	111	200	500	900
01010	10	5×	100	200	500	1000
01011	11	5.5×	91	182	500	1000
01100	12	6×	83	166	500	1000

Notes:
1. The SYSCLK frequency equals the core frequency divided by the processor-to-bus frequency ratio (PTBFR).
2. In clock-off mode, no clocking occurs inside the 750GX regardless of the SYSCLK input.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.
   The AC timing specifications given in the document do not apply in PLL-bypass mode.
4. The 2×–3.5× processor-to-bus ratios are currently not supported when miss-under-miss is enabled (HID0(14) = '1').

Table 5-2. 750GX Microprocessor PLL Configuration (Continued)

PLL_CFG [0:4]		Processor to Bus Frequency Ratio (PTBFR)	Frequency Range Supported by VCO Having an Example Range of...			
			SYSCLK[1] (MHz)		Core (MHz)	
Binary	Decimal		Minimum ($SYSCLK_{MIN}$)	Maximum ($SYSCLK_{MAX}$)	Minimum ($Core\ Frequency_{MIN}$)	Maximum ($Core\ Frequency_{MAX}$)
01101	13	6.5×	77	154	500	1000
01110	14	7×	71	143	500	1000
01111	15	7.5×	67	133	500	1000
10000	16	8×	62	125	500	1000
10001	17	8.5×	59	118	500	1000
10010	18	9×	55	111	500	1000
10011	19	9.5×	51	105	500	1000
10100	20	10×	50	100	500	1000
10101	21	11×	45	91	500	1000
10110	22	12×	42	83	500	1000
10111	23	13×	38	77	500	1000
11000	24	14×	36	71	500	1000
11001	25	15×	33	66	500	1000
11010	26	16×	31	63	500	1000
11011	27	17×	29	59	500	1000
11100	28	18×	28	56	500	1000
11101	29	19×	26	53	500	1000
11110	30	20×	25	50	500	1000
11111	31	Off[2]	N/A	N/A	N/A	N/A

Notes:

1. The SYSCLK frequency equals the core frequency divided by the processor-to-bus frequency ratio (PTBFR).
2. In clock-off mode, no clocking occurs inside the 750GX regardless of the SYSCLK input.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.
   The AC timing specifications given in the document do not apply in PLL-bypass mode.
4. The 2×–3.5× processor-to-bus ratios are currently not supported when miss-under-miss is enabled (HID0(14) = '1').

5.3 PLL Power Supply Filtering

The 750GX microprocessor has two separate AV_{DD} signals ($A1V_{DD}$ and $A2V_{DD}$), which provide power to the clock generation PLL.

Most designs are expected to use a single PLL configuration mode throughout the application. These types of designs should use the default PLL (PLL0), filtering its respective supply, $A1V_{DD}$. The $A2V_{DD}$ supply signal should be grounded through a 100 Ω resistor, as shown in *Figure 5-1* on page 51.

For designs planning to optimize power savings through dynamic switching between dual PLL circuits, it is recommended, though not required, that each AV_{DD} have a separate voltage input and filter circuit. This optional circuit is also shown.

To ensure stability of the internal clock, the power supplied to the AV_{DD} input signals should be filtered using a circuit similar to the one shown in *Figure 5-1* on page 51. The circuit should be placed as close as possible to the AV_{DD} pin to ensure it filters out as much noise as possible.

For descriptions of the sample PLL power supply filtering circuits, see *Table 5-3*.

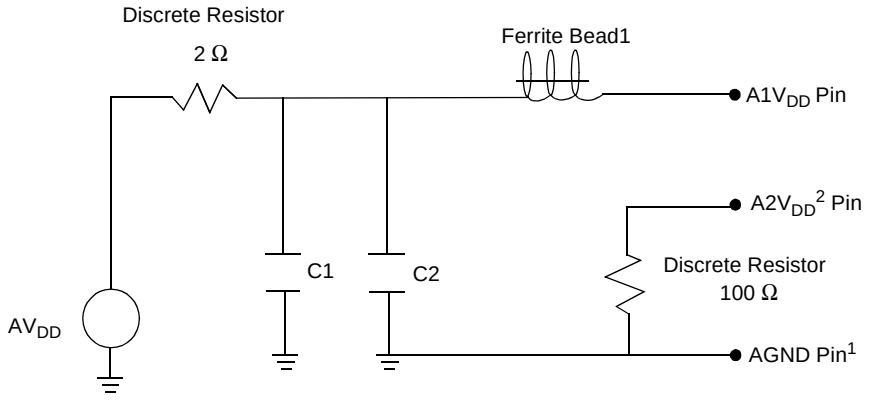
Table 5-3. Sample PLL Power Supply Filtering Circuits

Circuit Description	Number of Filtering Circuits	Ferrite Beads	Circuit Figure	Recommended Circuit Design	Notes
Single PLL circuit configuration that uses the $A1V_{DD}$ and ties the $A2V_{DD}$ pin to GND.	1	1	*Figure 5-1* on page 51	Yes	1, 2
Single PLL circuit configuration that uses both the $A1V_{DD}$ and the $A2V_{DD}$ pins and a single ferrite bead.	1	1	*Figure 5-2* on page 51	Optional	1, 2
Dual PLL configuration that uses a separate circuit for the $A1V_{DD}$ pin and for the $A2V_{DD}$ pin.	2	2	*Figure 5-3* on page 52	Yes	2, 3

Notes:

1. Optional configurations are supported, though not recommended.
2. This circuit design can be used with the dual PLL feature enabled, though optimum power savings may not be realized. For additional information, see *Figure 5-3, Dual PLL Power Supply Filter Circuits,* on page 52.
3. This circuit design can be used with the dual PLL feature enabled to optimize power savings.

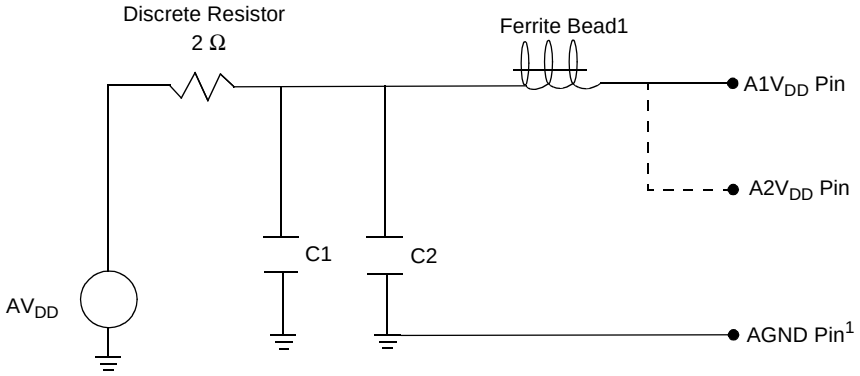
Figure 5-1. Single PLL Power Supply Filter Circuit with $A1V_{DD}$ Pin and $A2V_{DD}$ Pin Tied to GND (Recommended)



Item	Description/Value
Resistor	2 Ω , 100 Ω
C1	0.1 µF Ceramic
C2	10.0 µF Ceramic
Ferrite Bead	30 Ω (typical) - Murata BLM21P300S or similar

Notes:
1. Connected to ground without a filter.
2. Single PLL0 only.

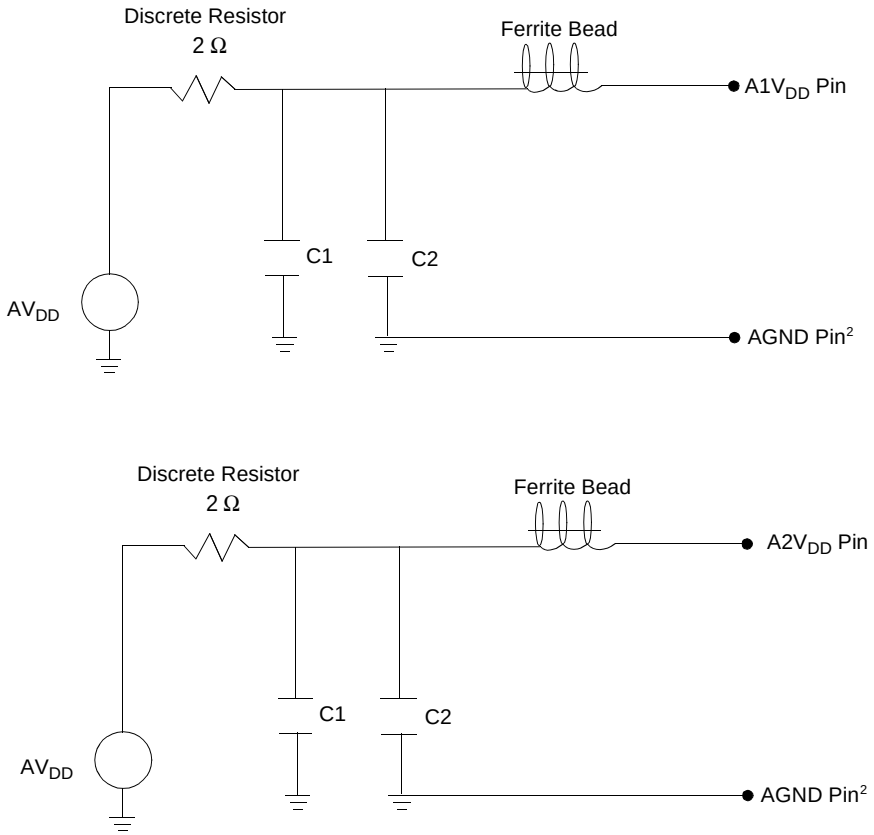
Figure 5-2. PLL Power Supply Filter Circuit with Two AV_{DD} Pins and One Ferrite Bead (Optional)



Item	Description/Value
Resistor	2 Ω
C1	0.1 µF Ceramic
C2	10.0 µF Ceramic
Ferrite Bead	30 Ω (typical) - Murata BLM21P300S or similar

Note:
1. Connected to ground without a filter.

Figure 5-3. Dual PLL Power Supply Filter Circuits (Recommended if Dual-PLL is Enabled)[1]



Item	Description/Value
Resistor	2 Ω
C1	0.1 µF Ceramic
C2	10.0 µF Ceramic
Ferrite Bead	30 Ω (typical) - Murata BLM21P300S or similar

Notes:
1. The dual PLL power supply circuits shown in this figure are recommended for a design that uses the dual PLL feature. For more information about the dual PLL feature, see *Section 5.2, Low Voltage Operation at Lower Frequency,* on page 46.
2. Connected to ground without a filter.

5.4 Decoupling Recommendations

Capacitor decoupling is required for the 750GX. Decoupling capacitors act to reduce high-frequency chip switching noise and provide localized bulk charge storage to reduce major power-surge effects. Guidelines for high-frequency noise decoupling will be provided in a separate application note. Bulk decoupling requires a more complete understanding of the system and system power architecture, which is beyond the scope of this document.

High-frequency decoupling capacitors should be located as close as possible to the processor with low lead inductance to the ground and voltage planes.

Decoupling capacitors are recommended on the back of the card, directly opposite the module. The recommended placement and number of decoupling capacitors, 34 V_{DD}-GND capacitors and 44 OV_{DD}-GND capacitors, are described in *Figure 5-4* on page 54. The recommended decoupling capacitor specifications are provided in *Table 5-4*. The placement and usage described here are guidelines for decoupling capacitors and should be applied for system designs.

Table 5-4. Recommended Decoupling Capacitor Specifications

Item	Description
Decoupling capacitor specifications:	Type X5R or Y5V 10 V minimum 0402 size 40 × 20 mils, nominally 1.0 mm × 0.5 mm ±0.1 mm on both dimensions
	100 nF
Recommended minimum number of decoupling capacitors on the back of the card:	34 V_{DD}-GND capacitors 44 OV_{DD}-GND capacitors

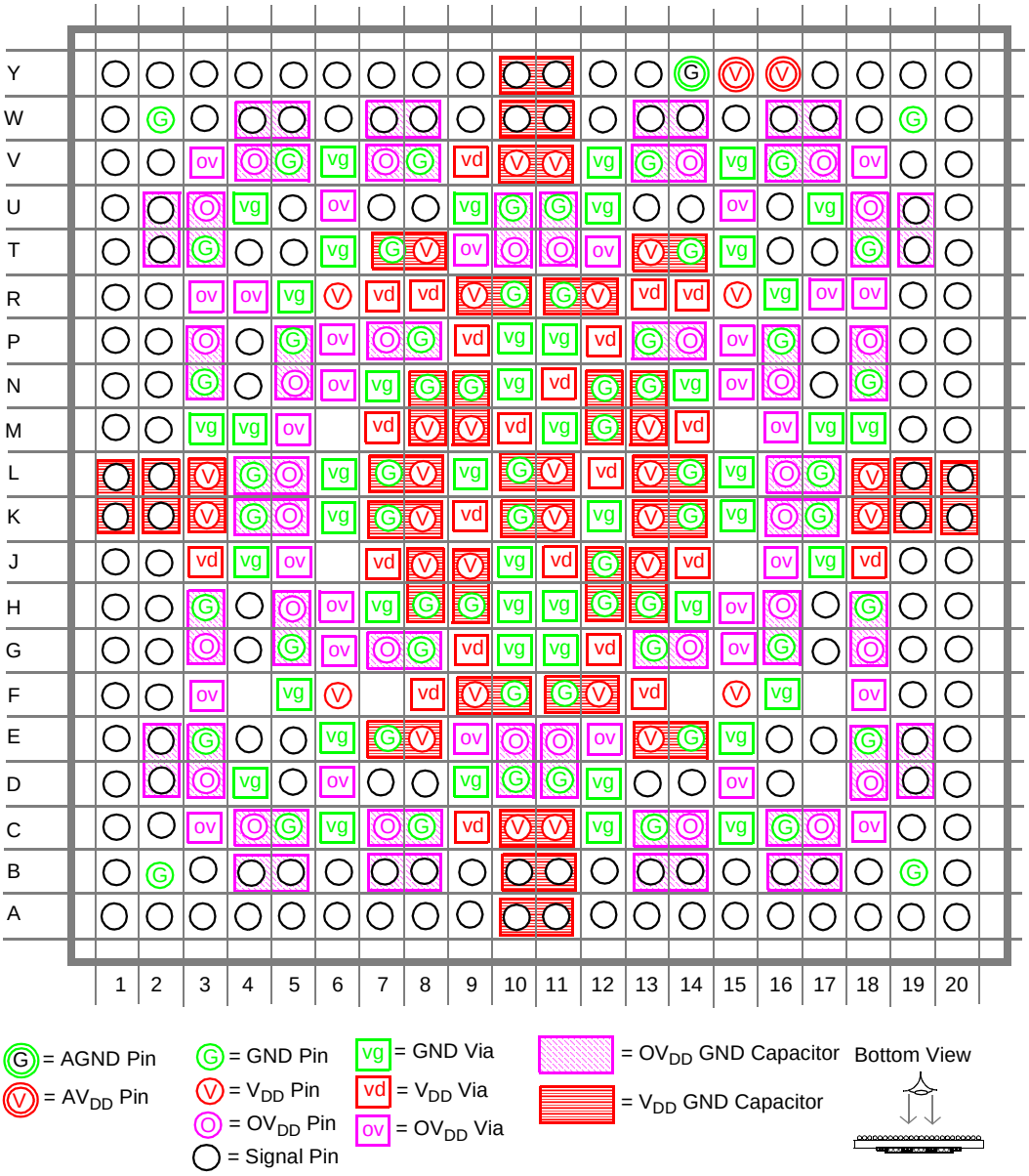
Note: The decoupling capacitor electrodes are located directly opposite their corresponding BGA pins where possible. Also, each electrode for each decoupling capacitor needs to be connected to one or more BGA pins (balls) with a short electrical path. Thus, through-vias adjacent to the decoupling capacitors are recommended.

The card designer can expand on the decoupling capacitor recommendations by doing the following:

- Adding additional decoupling capacitors.
  If using additional decoupling capacitors, verify that these additional capacitors do not reduce the number of card vias or cause the vias to lose proximity to each capacitor electrode.
- Adding additional through-vias or blind-vias.
  Card technologies are available that will reduce the inductance between the decoupling capacitor and the BGA pin (ball). Replacing single vias with multiple vias is certainly approved. Place GND vias close to V_{DD} or OV_{DD} vias to reduce loop inductance.

Figure 5-4 on page 54 shows the mapping of Power, Ground, and Signal pin assignments, and recommended layout of decoupling capacitors under application conditions. In test mode, pins C11 and G8 can be used as Kelvin probes, in which case the pins should be disconnected from card GND and V_{DD}. Capacitors should not be connected to the Kelvin pins during Kelvin probe voltage measurements.

Figure 5-4. Orientation and Layout of the 750GX Decoupling Capacitors



5.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All no-connect (NC) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, AV_{DD}, and GND pins of the 750GX.

5.6 Output Buffer DC Impedance

The 750GX 60x drivers were characterized over various process, voltage, and temperature conditions. To measure driver impedance, an external resistor is connected to the chip pad, either to OV_{DD} or GND. Then the value of such resistor is varied until the pad voltage is $OV_{DD}/2$ (see *Figure 5-5*).

The output impedance is actually the average of two resistances: the resistance of the pull-up and the resistance of pull-down devices. When Data is held high, SW1 is closed (SW2 is open), and R_N is trimmed until Pad = $OV_{DD}/2$; R_N then becomes the resistance of the pull-up devices. When Data is held low, SW2 is closed (SW1 is open), and R_P is trimmed until Pad = $OV_{DD}/2$; R_P then becomes the resistance of the pull-down devices. With a properly designed driver, R_P and R_N are close to each other in value; then driver impedance equals $(R_P + R_N)/2$.

Figure 5-5. Driver Impedance Measurement

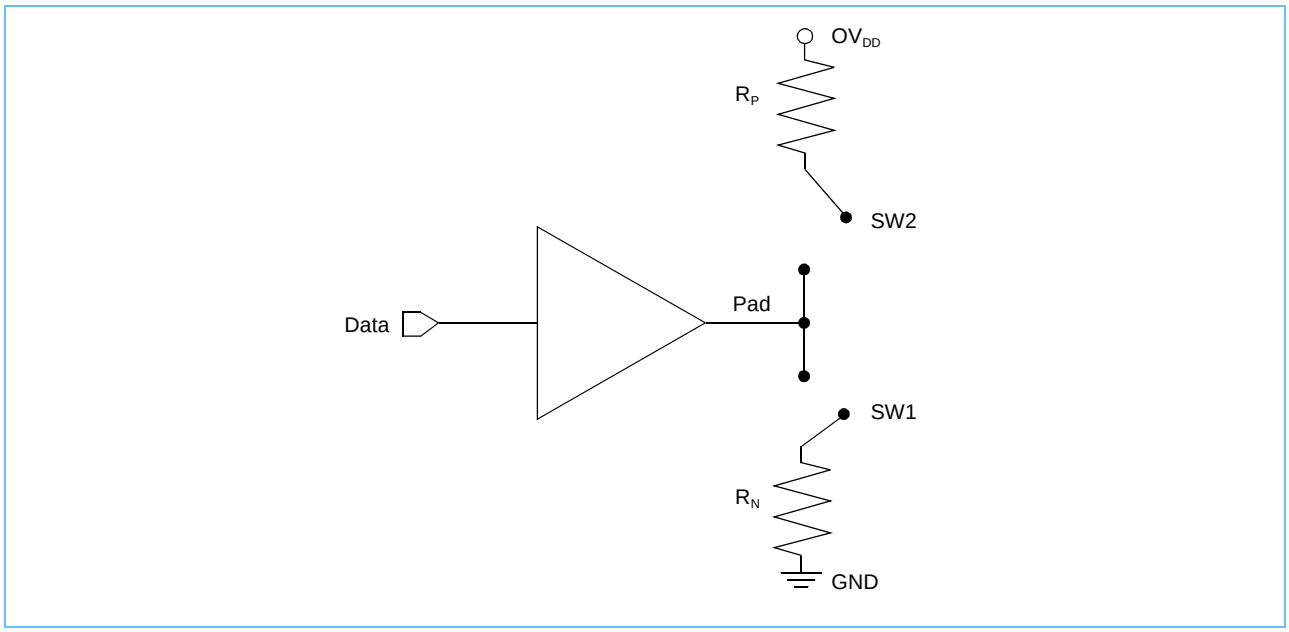


Table 5-5 summarizes the driver impedance characteristics a designer uses to design a typical process.

Table 5-5. Driver Impedance Characteristics

Process	60× Impedance (Ω)	OV_{DD} (V)	Temperature (°C)
Worst	49	1.8	105
Typical	47	1.8	105
Best	43	1.8	85
Worst	47	2.5	105
Typical	45	2.5	105
Best	43	2.5	85
Worst	51	3.3	105
Typical	49	3.3	105
Best	45	3.3	85

5.6.1 Input/Output Usage

Table 5-6, Input/Output Usage, on page 57 provides details on the input/output usage of the IBM PowerPC 750GX RISC Microprocessor signals. The *Usage Group* column refers to the general functional category of the signal.

In the IBM PowerPC 750GX RISC Microprocessor, certain input/output signals have pullups and pulldowns, which may or may not be enabled. In *Table 5-6,* the “Input/Output with Internal Pullup Resistors” column defines which signals have these pullups or pulldowns and their active or inactive state. The “Level Protect” column defines which signals have the designated function added to their Input/Output cell. For more about level protection, see *Section 5.9.1* on page 69.

Caution: This section is based on preliminary information and is subject to change.

Table 5-6. Input/Output Usage

750GX Signal Name	Active Level	Input/ Output	Usage Group	Input/Output with Internal Pullup Resistors	Level Protect	Required External Resistor	Comments	Notes
$A1V_{DD}$	—	—	Power Supply					
$A2V_{DD}$	—	—	Power Supply					
A[0:31]	High	Input/Output	Address Bus		Keeper			1, 3, 4
AACK	Low	Input	Address Termination		Keeper		Must be actively driven	3, 4, 5
$\overline{ABB}$	Low	Input/Output	—		Keeper	5 K Ω	Pullup required to OV_{DD}	3, 4, 5
AGND	—	—	Power Supply					
AP[0:3]	High	Input/Output	—		Keeper			3, 4
$\overline{ARTRY}$	Low	Input/Output	Address Termination		Keeper	5 K Ω	Pullup required to OV_{DD}	3, 4, 5
$\overline{BG}$	Low	Input	Address Arbitration		Keeper		Active driver or pulldown	3, 4, 5
$\overline{BR}$	Low	Output	Address Arbitration		Keeper		Chip actively drives	3, 4, 5
BVSEL	N/A	Input	Mode Select/Control			5 K Ω	Pullup/pulldown, as required	5
$\overline{CHECKSTOP}$	Low	Output	Interrupt/Resets		Keeper	5 K Ω	Pullup required to OV_{DD}	3, 4, 5
$\overline{CI}$	Low	Output	Transfer Attributes		Keeper			1, 3, 4
$\overline{CKSTP\_IN}$	Low	Input	Interrupt/Resets		Keeper		Must be actively driven	3, 4, 5
CLK_OUT	High	Output	—		Keeper			3, 4
$\overline{DBB}$	Low	Input/Output	—		Keeper	5 K Ω	Pullup required to OV_{DD}	3, 4, 5
$\overline{DBDIS}$	Low	Input	Mode Select/Control		Keeper			3, 4, 6
$\overline{DBG}$	Low	Input	Data Arbitration		Keeper		Active driver or tie low	3, 4, 5

Notes:

1. Depends on the system design. The electrical characteristics of the 750GX do not add additional constraints to the system design, so whatever is done with the net will depend on the system requirements.
2. $\overline{HRESET}$, $\overline{SRESET}$, and $\overline{TRST}$ are signals used for RISCWatch to enable proper operation of the debuggers. Logical AND gates should be placed between these signals and the IBM PowerPC 750GX RISC Microprocessor (see *Figure 5-6* on page 61).
3. The 750GX provides protection from meta-stability on inputs through the use of a “keeper” circuit on specific inputs (see *Section 5.9* on page 69 for a more detailed description).
4. If a system design requires a signal level to be maintained while not being actively driven, an external resistor or device must be used (keepers assure no meta-stability of inputs but do not guarantee a level).
5. The 750GX does not require external pullups on address and data lines. Control lines must be treated individually.
6. Mode Select/Control pins require the proper state at $\overline{HRESET}$ to configure the operating mode of the processor (see *Table 5-10, Summary of Mode Select,* on page 70).

Table 5-6. Input/Output Usage (Continued)

750GX Signal Name	Active Level	Input/ Output	Usage Group	Input/Output with Internal Pullup Resistors	Level Protect	Required External Resistor	Comments	Notes
$\overline{\text{DBWO}}$	Low	Input	Mode Select/Control		Keeper			3, 4, 6
DH[0:31]	High	Input/Output	Data Bus		Keeper			1, 3, 4
DL[0:31]	High	Input/Output	Data Bus		Keeper			1, 3, 4
DP[0:7]	High	Input/Output	—					
$\overline{\text{DRTRY}}$	Low	Input	—		Keeper			3, 4, 6
$\overline{\text{GBL}}$	Low	Input/Output	Transfer Attributes		Keeper			1, 3, 4
GND	—	—	Power Supply					
$\overline{\text{HRESET}}$	Low	Input	Interrupt/Resets		Keeper		Active driver	2, 3, 4, 5
$\overline{\text{INT}}$	Low	Input	Interrupt/Resets		Keeper		Active driver or pullup	3, 4, 5
L1_TSTCLK	High	Input	Mode Select/Control	Not enabled		5 K Ω	Pullup/pulldown, as required	5
L2_TSTCLK	High	Input	LSSD	Not enabled		5 K Ω	Pullup required to OV_{DD}	5, 6
$\overline{\text{LSSD\_MODE}}$	Low	Input	LSSD	Not enabled		5 K Ω	Pullup required to OV_{DD}	5
$\overline{\text{MCP}}$	Low	Input	Interrupt/Resets		Keeper		Active driver or pullup	3, 4, 5
OV_{DD}	—	—	Power Supply					
PLL_CFG[0:4]	High	Input	Clock Control		Keeper	As required	Pullup/pulldown, as required	3, 4, 5
PLL_RNG[0:1]	High	Input	—		Keeper	As required	Pullup/pulldown, as required	3, 4, 5
$\overline{\text{QACK}}$	Low	Input	Mode Select/Control		Keeper		Must be actively driven	3, 4, 5, 6
$\overline{\text{QREQ}}$	Low	Output	Status/Control		Keeper		Chip actively drives	3, 4, 5
$\overline{\text{RSRV}}$	Low	Output	—		Keeper		No connect	3, 4, 5

Notes:

1. Depends on the system design. The electrical characteristics of the 750GX do not add additional constraints to the system design, so whatever is done with the net will depend on the system requirements.
2. $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, and $\overline{\text{TRST}}$ are signals used for RISCWatch to enable proper operation of the debuggers. Logical AND gates should be placed between these signals and the IBM PowerPC 750GX RISC Microprocessor (see *Figure 5-6* on page 61).
3. The 750GX provides protection from meta-stability on inputs through the use of a “keeper” circuit on specific inputs (see *Section 5.9* on page 69 for a more detailed description).
4. If a system design requires a signal level to be maintained while not being actively driven, an external resistor or device must be used (keepers assure no meta-stability of inputs but do not guarantee a level).
5. The 750GX does not require external pullups on address and data lines. Control lines must be treated individually.
6. Mode Select/Control pins require the proper state at $\overline{\text{HRESET}}$ to configure the operating mode of the processor (see *Table 5-10, Summary of Mode Select,* on page 70).

Table 5-6. Input/Output Usage (Continued)

750GX Signal Name	Active Level	Input/ Output	Usage Group	Input/Output with Internal Pullup Resistors	Level Protect	Required External Resistor	Comments	Notes
$\overline{\text{SMI}}$	Low	Input	—		Keeper			3, 4
$\overline{\text{SRESET}}$	Low	Input	Interrupt/Resets		Keeper		Active driver or pullup	2, 3, 4, 5
SYSCLK	High	Input	Clock Control		Keeper	No resistor by design	Active driver	3, 4, 5
$\overline{\text{TA}}$	Low	Input	Data Termination		Keeper		Active driver	3, 4, 5
TBEN	High	Input	—					
$\overline{\text{TBST}}$	Low	Input/Output	Transfer Attributes		Keeper			1, 3, 4
TCK	High	Input	JTAG	Not enabled		External pulldown	5 K Ω to GND	5
TDI	High	Input	JTAG	Enabled high	Internal enabled		50 µa @ 2.5 V 25 µa @ 1.8 V (the pullup current for the internal resistor)	5
TDO	High	Output	JTAG		Keeper			3, 4
$\overline{\text{TEA}}$	Low	Input	Data Termination		Keeper		Active driver or pullup	3, 4, 5
$\overline{\text{TLBISYNC}}$	Low	Input	Mode Select/Control		Keeper		Must be actively driven	3, 4, 6
TMS	High	Input	JTAG	Enabled high	Internal enabled		50 µa @ 2.5 V 25 µa @ 1.8 V (the pullup current for the internal resistor)	5

Notes:

1. Depends on the system design. The electrical characteristics of the 750GX do not add additional constraints to the system design, so whatever is done with the net will depend on the system requirements.
2. $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, and $\overline{\text{TRST}}$ are signals used for RISCWatch to enable proper operation of the debuggers. Logical AND gates should be placed between these signals and the IBM PowerPC 750GX RISC Microprocessor (see *Figure 5-6* on page 61).
3. The 750GX provides protection from meta-stability on inputs through the use of a “keeper” circuit on specific inputs (see *Section 5.9* on page 69 for a more detailed description).
4. If a system design requires a signal level to be maintained while not being actively driven, an external resistor or device must be used (keepers assure no meta-stability of inputs but do not guarantee a level).
5. The 750GX does not require external pullups on address and data lines. Control lines must be treated individually.
6. Mode Select/Control pins require the proper state at $\overline{\text{HRESET}}$ to configure the operating mode of the processor (see *Table 5-10, Summary of Mode Select,* on page 70).

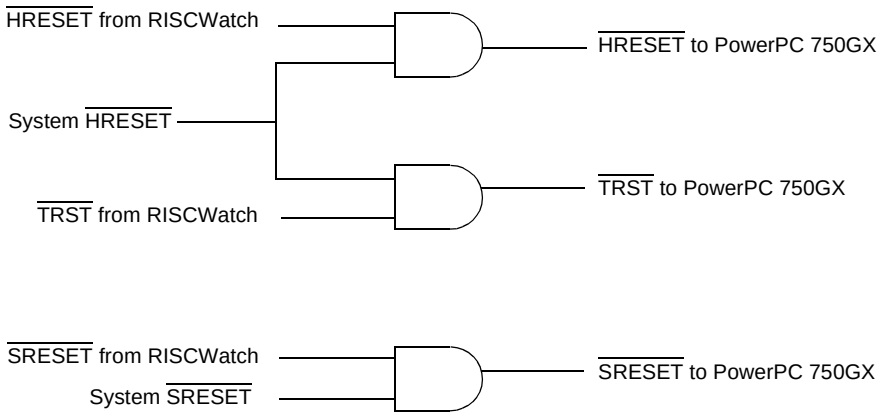
Table 5-6. Input/Output Usage (Continued)

750GX Signal Name	Active Level	Input/ Output	Usage Group	Input/Output with Internal Pullup Resistors	Level Protect	Required External Resistor	Comments
$\overline{\text{TRST}}$	Low	Input	JTAG	Enabled high	Internal enabled		50 µa @ 2.5 V 25 µa @ 1.8 V (the pullup current for th nal resistor)
$\overline{\text{TS}}$	Low	Input/Output	Address Start		Keeper	5 K Ω	Pullup required to OV_{DD}
TSIZ[0:2]	High	Output	Transfer Attributes		Keeper		
TT[0:4]	High	Input/Output	Transfer Attributes		Keeper		
V_{DD}	—	—	Power Supply				
$\overline{\text{WT}}$	Low	Output	Transfer Attributes		Keeper		

Notes:

1. Depends on the system design. The electrical characteristics of the 750GX do not add additional constraints to the system design, so whatever is d depend on the system requirements.
2. $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, and $\overline{\text{TRST}}$ are signals used for RISCWatch to enable proper operation of the debuggers. Logical AND gates should be placed and the IBM PowerPC 750GX RISC Microprocessor (see *Figure 5-6* on page 61).
3. The 750GX provides protection from meta-stability on inputs through the use of a “keeper” circuit on specific inputs (see *Section 5.9* on page 69 for description).
4. If a system design requires a signal level to be maintained while not being actively driven, an external resistor or device must be used (keepers assu inputs but do not guarantee a level).
5. The 750GX does not require external pullups on address and data lines. Control lines must be treated individually.
6. Mode Select/Control pins require the proper state at $\overline{\text{HRESET}}$ to configure the operating mode of the processor (see *Table 5-10, Summary of Mode*

Figure 5-6. IBM RISCWatch JTAG to HRESET, TRST, and SRESET Signal Connector



Note: See notes for *Table 5-6, Input/Output Usage,* on page 57.

5.7 Thermal Management Information

This section provides thermal management information for the CBGA package for air cooled applications. Proper thermal control design is primarily dependent upon the system-level design; that is, the heat sink, air flow, and the thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods: adhesive, spring clip to holes in the printed-circuit board or package, mounting clip, or a screw assembly (see *Figure 5-7, Package Exploded Cross-Sectional View with Several Heat-Sink Options,* on page 62).

Note: This section is based on preliminary information and is subject to change.

Figure 5-7. Package Exploded Cross-Sectional View with Several Heat-Sink Options

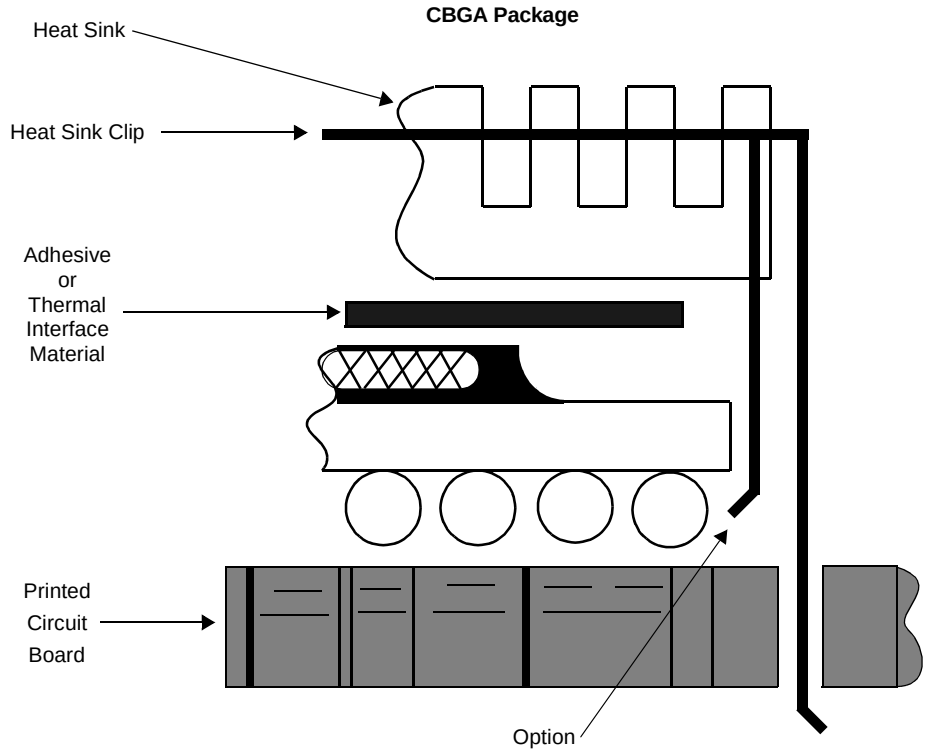


Table 5-7. Maximum Heat-Sink Weight Limit for the CBGA

Force	Maximum	Notes
Maximum dynamic compressive force allowed on the BGA balls	42.9 N	1
Maximum dynamic tensile force allowed on the BGA balls	9.05 N	2
Maximum dynamic compressive force allowed on the chip	22.4 N	3
Maximum mass of module + heat sink when heat sink is not bolted to card	39 g	4
Maximum torque on die (or substrate)	28in-lbs	

1. The maximum instantaneous compressive force distributed across the module surface, and perpendicular to the surface of the board on which it is mounted.
2. The maximum instantaneous tensile force exerted across the module surface, and perpendicular to the surface of the board on which it is mounted.
3. The maximum instantaneous compressive force distributed across the die surface, and perpendicular to the surface of the board on which it is mounted.
4. The maximum combined mass of the module, attached heat sink or spreader, and adhesive material used to secure or support the heat sink or spreader to the module's ceramic surface.

The board designer can choose between several types of heat sinks to place on the 750GX. There are several commercially-available heat sinks for the 750GX provided by the vendors listed in *Table 5-8, 750GX Heat-Sink Vendors,* on page 63.

Table 5-8. 750GX Heat-Sink Vendors

Company Names and Addresses for Heat-Sink Vendors
Chip Coolers, Inc. 333 Strawberry Field Rd. Warwick, RI 02886 (800) 227-0254 http://www.chipcoolers.com
International Electronic Research Corporation (IERC) 413 North Moss Street Burbank, CA 91502 (818) 842-7277 http://www.ctscorp.com/
Aavid Thermalloy 80 Commercial Street Concord, NH 03301 (603) 224-9888 http://www.aavid.com http://www.aavidthermalloy.com
Wakefield Thermal Solutions Inc. 33 Bridge Street Pellham, NH 03076 (603) 635-2800 http://www.wakefield.com

5.7.1 Thermal Assist Unit

IBM recommends that the thermal assist unit (TAU) in these devices be calibrated before use. Calibration methods are discussed in the IBM application note, *Calibrating the Thermal Assist Unit in the IBM25PPC750L Processors*. Although this note was written for the 750L, the calibration methods discussed in this document also apply to the 750GX.

5.7.2 Minimum Heat Sink Requirements

The worst-case power dissipation (P_D) for the 750GX is shown in *Table 3-5, Power Consumption for DD1.1,* on page 17. A conservative thermal management design will provide sufficient cooling to maintain the junction temperature (T_J) of the 750GX below 105°C at maximum P_D and worst-case ambient temperature and airflow conditions.

Many factors affect the 750GX power dissipation, including V_{DD}, T_J, core frequency, process factors, and the code that is running on the processor. In general, P_D increases with increases in T_J, V_{DD}, core frequency, process variables, and the number of instructions executed per second.

For various reasons, a designer may determine that the power dissipation of the 750GX in their application will be less than the maximum value shown in this datasheet. Assuming a lower P_D will result in a thermal management system with less cooling capacity than would be required for the maximum P_D shown in the datasheet. In this case, the designer may decide to determine the actual maximum 750GX P_D in the particular application. Contact your IBM PowerPC field applications engineer for more information.

In addition to the system factors that must be considered in a cooling system analysis, three things should be noted.

First, 750GX P_D rises as T_J increases, so it is most useful to measure P_D while the 750GX junction temperature is at maximum. While not specified or guaranteed, this rise in P_D with T_J is typically less than 1 W per 10°C. So regardless of other factors, the minimum cooling solution must have a maximum temperature rise of no more than 10°C/W. This minimum cooling solution is not generally achievable without a heat sink. A heat sink or heat spreader of some sort must always be used in 750GX applications.

Second, due to process variations, there can be a significant variation in the P_D of individual 750GX devices. In addition, IBM will occasionally supply “downbinned” parts. These are faster parts that are shipped in place of the speed that was ordered. For example, some parts that are marked as 800 MHz may actually run as fast as 933 MHz. These 933 MHz parts will dissipate more power at 800 MHz than the 800 MHz parts. So power dissipation analysis should be conducted using the fastest parts available.

Finally, regardless of methodology, IBM only supports system designs that successfully maintain the maximum junction temperature within the datasheet limits. IBM also supports designs that rely on the maximum P_D values given in this datasheet and supply a cooling solution sufficient to dissipate that amount of power while keeping the maximum junction temperature below the maximum T_J.

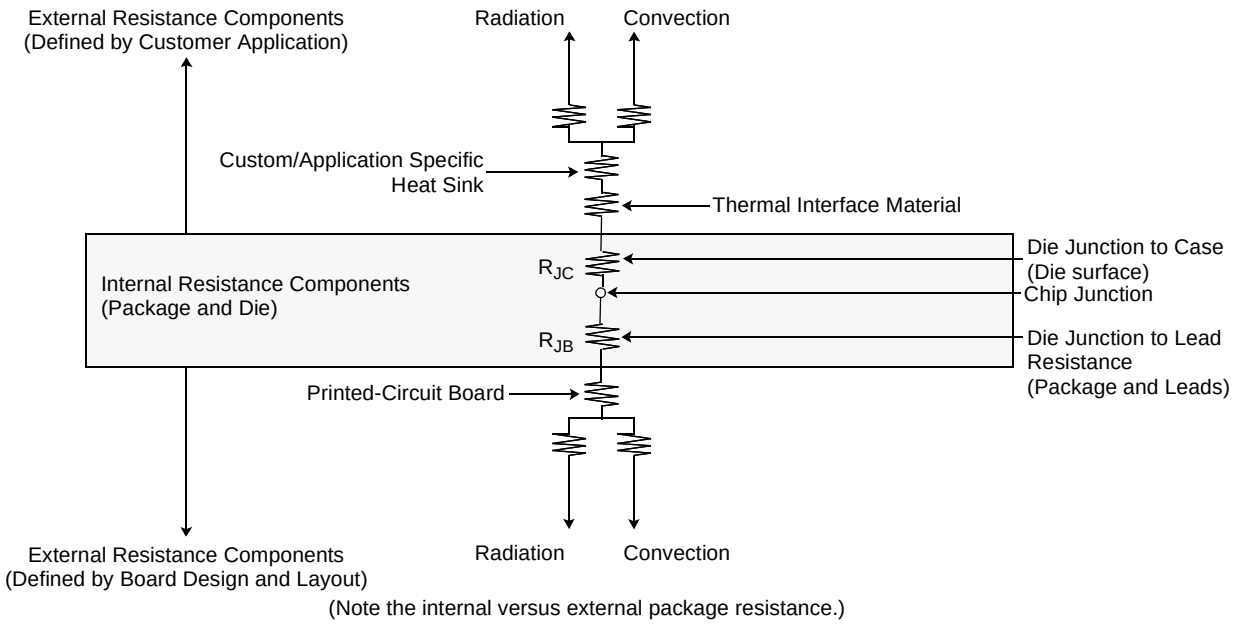
5.7.3 Internal Package Conduction Resistance

For the exposed-die packaging technology, shown in *Table 3-3, Package Thermal Characteristics,* on page 16, the intrinsic conduction thermal resistance paths illustrated in *Figure 5-8* on page 65 are as follows:

- Die junction-to-case thermal resistance (primary thermal path), defined as the thermal resistance from the die junctions to the back (exposed) surface of the die.
- Die junction-to-lead thermal resistance (not normally a significant thermal path), defined as the thermal resistance from the die junctions to the circuit board interface.
- Die junction-to-ambient thermal resistance (largely dependent on customer-supplied heat sink), defined as the sum total of all the thermally conductive components that comprise the end user's application. Ambient is further defined as the air temperature in the immediate vicinity of the thermally conductive components, including the pre-heat contributions of surrounding heat sources.

Figure 5-8 on page 65 is a thermal model, in schematic form, of the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Figure 5-8. C4 Package with Heat Sink Mounted to a Printed-Circuit Board



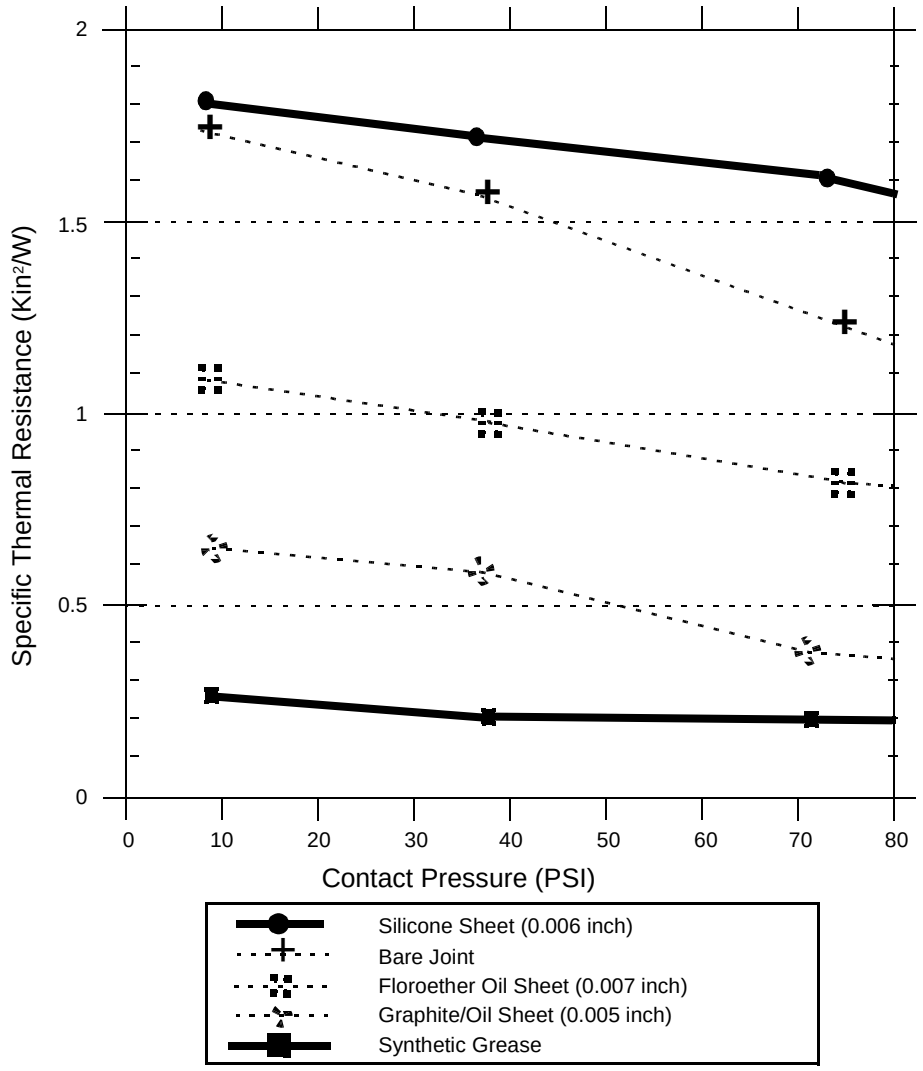
Heat generated on the active side (ball) of the chip is conducted through the silicon, then through the heat-sink attach material (or thermal interface material), and finally to the heat sink; where it is removed by forced-air convection. Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat-sink conduction/convective thermal resistances are the dominant terms.

5.7.4 Adhesives and Thermal Interface Materials

A thermal interface material is required at the package die-surface-to-heat-sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by a spring clip mechanism, *Figure 5-9* on page 66 shows an example of the thermal performance of three thin-sheet thermal-interface materials (silicon, graphite/oil, floroether oil), a bare joint, and a joint with synthetic grease, as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of synthetic grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the synthetic grease joint. Customers are advised to investigate alternative thermal interface materials to ensure the most reliable, efficient, and cost-effective thermal design.

An example of heat-sink attachment to the package by means of a spring clip to holes in the printed-circuit board is illustrated in *Figure 5-7, Package Exploded Cross-Sectional View with Several Heat-Sink Options,* on page 62. Therefore the synthetic grease offers the best thermal performance, considering the low interface pressure. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, and so forth.

Figure 5-9. Thermal Performance of Select Thermal Interface Material



The board designer can choose between several types of thermal interfaces. Heat-sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

Table 5-9. 750GX Thermal Interface and Adhesive Materials Vendors

Company Names and Addresses for Thermal Interfaces and Adhesive Materials Vendors
Dow-Corning Corporation Dow-Corning Electronic Materials P.O. Box 0997 Midland, MI 48686-0997 (989) 496-4000 http://www.dowcorning.com/content/etronics
Chomerics, Inc. 77 Dragon Court Woburn, MA 01888-4850 (781) 935-4850 http://www.chomerics.com
Thermagon, Inc. 4797 Detroit Avenue Cleveland, OH 44102-2216 (216) 939-2300 / (888) 246-9050 http://www.thermagon.com
Loctite Corporation 1001 Trout Brook Crossing Rocky Hill, CT 06067 (860) 571-5100 / (800) 562-8483 http://www.loctite.com
AI Technology 70 Washington Road Princeton, NJ 08550-1097 (609) 799-9388 http://www.aitechnology.com

Section 5.8 provides a heat-sink selection example using one of the commercially available heat sinks.

5.8 Heat-Sink Selection Example

For preliminary heat-sink sizing, the die-junction temperature can be expressed as follows:

$$T_J = T_A + T_R + (\theta_{JC} + \theta_{INT} + \theta_{SA}) \times P_D$$

where:

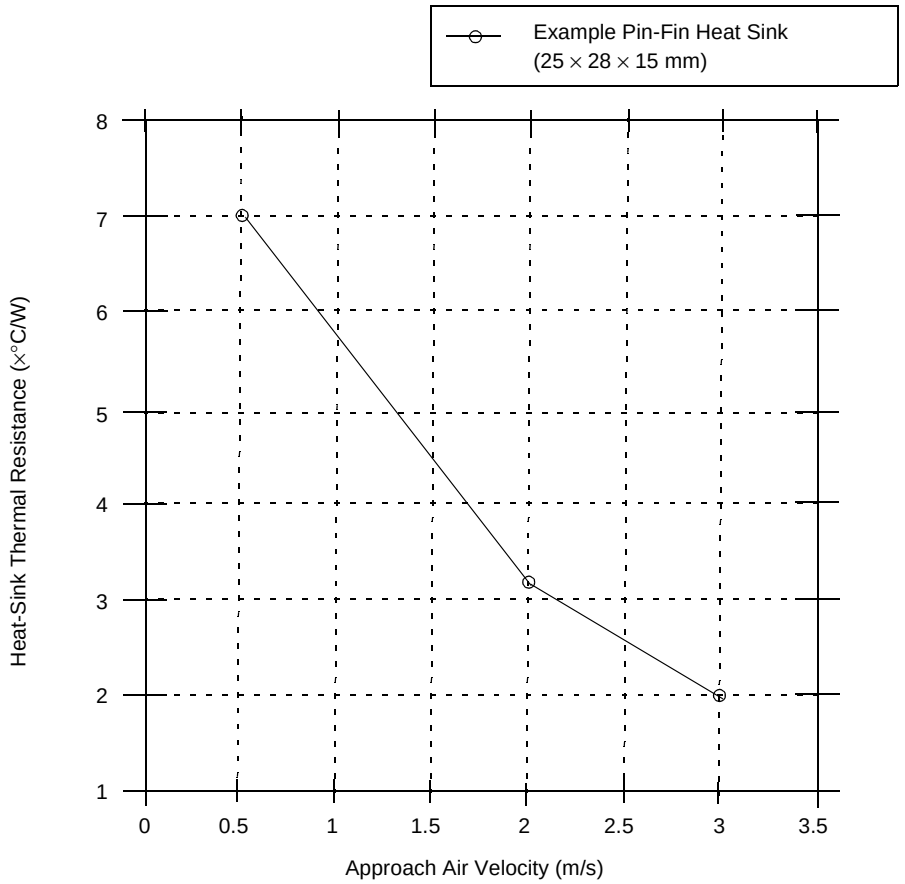
T_J is the die-junction temperature
T_A is the inlet cabinet ambient temperature
T_R is the air temperature rise within the system cabinet
θ_{JC} is the junction-to-case thermal resistance
θ_{INT} is the thermal resistance of the thermal interface material
θ_{SA} is the heat-sink-to-ambient thermal resistance
P_D is the power dissipated by the device

Typical die-junction temperatures (T_J) should be maintained less than the value specified in *Table 3-3, Package Thermal Characteristics,* on page 16. The temperature of the air cooling component greatly depends upon the ambient inlet air temperature and the air temperature rise within the computer cabinet. An electronic cabinet inlet-air temperature (T_A) may range from 30°C to 40°C. The air temperature rise within a cabinet (T_R) may be in the range of 5°C to 10°C. The thermal resistance of the interface material (θ_{INT}) is typically about 1°C/W. Assuming a T_A of 30°C, a T_R of 5°C, a CBGA package θ_{JC} = 0.1, and a power dissipation (P_D) of 10 watts, the following expression for T_J is obtained.

Die-junction temperature: $T_J = 30°C + 5°C + (0.1°C/W + 1.0°C/W + \theta_{SA}) \times 10\ W$

As an example heat sink, the heat-sink-to-ambient thermal resistance (θ_{SA}) versus air flow velocity is shown in *Figure 5-10*.

Figure 5-10. Example of a Pin-Fin Heat-Sink-to-Ambient Thermal Resistance versus Airflow Velocity



Assuming an air velocity of 1.0 m/s, we have an effective θ_{SA} of 5.8°C/W, thus

$T_J = 30°C + 5°C + (0.1°C/W + 1.0°C/W + 5.8°C/W) \times 10\ W,$

resulting in a junction temperature of approximately 104°C, which is within the maximum operating temperature of the component in this example.

Heat sinks offered by companies such as Chip Coolers, IERC, Aavid Thermalloy, and Wakefield Engineering offer different heat-sink-to-ambient thermal resistances, and may or may not need air flow.

Though the junction-to-ambient and the heat-sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final chip-junction operating temperature is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power dissipation, a number of factors affect the final operating die-junction temperature. These factors might include air flow, board population (local heat flux of adjacent components), heat-sink efficiency, heat-sink attach, next-level interconnect technology, system air temperature rise, and so forth.

5.9 Operational and Design Considerations

5.9.1 Level Protection

A level protection feature is included in the IBM PowerPC 750GX RISC Microprocessor. The level protection feature is available in the 1.8 V, 2.5 V, and 3.3 V bus modes. This feature prevents ambiguous floating reference voltages by pulling the respective signal line to the last valid or nearest valid state.

For example, if the input/output voltage level is closer to OV_{DD}, the circuit pulls the I/O level to $OV_{DD.}$ If the I/O level is closer to GND, the I/O level is pulled low. This self-latching circuitry *keeps* the floating inputs defined and avoids meta-stability. In *Table 5-6, Input/Output Usage,* on page 57, these signals are defined as “keeper” in the “Level Protect” column.

The level protect circuitry provides no additional leakage current to the signal I/O; however, some amount of current must be applied to the *keeper* node to overcome the level protection latch. This current is process dependent, but in no case is the current required over 100 µA.

This feature allows the system designer to limit the number of resistors in the design and optimize placement and reduce costs.

Note: Having a *keeper* on the associated signal I/O does not replace a pull-up or pull-down resistor that is needed by a separate device located on the 60x bus. The designer must supply any termination requirements for these separate devices, as defined in their specifications.

5.9.2 64-Bit or 32-Bit Data Bus Mode

The typical operation for the 750GX DD1.X revision level is considered to be in 64-bit data bus mode. Mode setting is determined by the state of the mode signal, TLBISYNC, at the transition of HRESET from its active to inactive state (low to high). If TLBISYNC is *high* when HRESET transitions from active to inactive, 64-bit mode is selected. If TLBISYNC is *low* when HRESET transitions from active to inactive, 32-bit mode is selected.

Special Note: (Reduced pin out mode) To transition from a previous processor with reduced pin out mode, the customer will need to drive TLBISYNC appropriately, leave the DP(0..7) and AP(0..3) pins floating, and disable parity checking with the HID0 bits. The 750GX, like the 750FX, 750CXe, and 750, does not have APE and DPE pins.

5.9.3 I/O Voltage Mode Selection

Selection between 1.8 V, 2.5 V, or 3.3 V I/O modes is accomplished by using the BVSEL and L1_TSTCLK pins:

- If BVSEL = 1 and L1_TSTCLK = 0, then the 3.3 V mode is enabled.
- If BVSEL = 1 and L1_TSTCLK = 1, then the 2.5 V mode is enabled.
- If BVSEL = 0 and L1_TSTCLK = 1, then the 1.8 V mode is enabled.

Note: Do not set BVSEL = 0 and L1_TSTCLK = 0 since it yields an *invalid mode*.

Table 5-10. Summary of Mode Select

Mode	750GX
32-bit mode	Sample $\overline{\text{TLBISYNC}}$ to select High = 64-bit mode Low = 32-bit mode
Data retry mode	Selects DRTRY mode. 0 at HRESET transition No DRTRY mode 1 at HRESET transition DRTRY mode
Factory usage modes	Factory usage modes are selected by sensing the data bus disable ($\overline{\text{DBDIS}}$), data bus write-only (DBWO), and L2_TSTCLK pins at the transition of HRESET from low to high. These pins should be held inactive (high) at the HRESET transition for normal machine operation.
I/O mode selection	3.3 V ±165 mV (BVSEL = 1, L1_TSTCLK = 0) or 2.5 V ±125 mV (BVSEL = 1, L1_TSTCLK = 1) or 1.8 V ±100 mV (BVSEL = 0, L1_TSTCLK = 1)
Standard/extended precharge mode	$\overline{\text{QACK}}$ in a logical high state at the transition of $\overline{\text{HRESET}}$ from asserted to negated enables standard precharge mode, the recommended default. See *Section 5.9.4.1* for details.

5.9.4 $\overline{\text{QACK}}$ Signal Implementation for Selected Features

5.9.4.1 Precharge Duration Selection and Application

An extended precharge feature is available for the signals $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, and $\overline{\text{ARTRY}}$ in situations where the loading and net topology of these signals requires a longer precharge duration for the signals to attain a valid level.

This feature has not been fully tested and should not be necessary in a properly designed system, even at 200 MHz. System designers should assume standard precharge as the default selection, with an option to use extended precharge.

The bus signals, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, and $\overline{\text{ARTRY}}$, require a precharge to the inactive state (bus high) before going to tristate. The precharge duration in standard precharge mode is approximately one half cycle, and should be used for systems with point-to-point topologies. Extended precharge mode increases the precharge duration to one cycle. This increase may be required for bus speeds approaching 200 MHz when bus loading is high.

$\overline{\text{QACK}}$ in a logical high state at the transition of $\overline{\text{HRESET}}$ from asserted to negated enables standard pre-charge mode in the 750GX. $\overline{\text{QACK}}$ in a logical low state at the transition of $\overline{\text{HRESET}}$ from asserted to negated enables extended pre-charge mode in the 750GX.

5.9.4.2 Processor Debug System Enablement when Implementing Precharge Selection

System designers who want to use a processor debug system attached to the 750GX IEEE 1149.1 test access port (TAP) interface (such as the IBM RISCWatch debug system) should provide a method to assert QACK after the transition of HRESET. Debug systems use a “soft stop” feature to stop the processor, allow processor internal states to be read, and then restart of the processor. A soft stop requires the system to be in a quiescent state before the processor can be queried for internal state values. This is accomplished by the assertion of a quiescent request (that is, QREQ is asserted) and subsequent acknowledgement (that is, QACK is asserted). Systems that do not use the power management features; doze, nap, and sleep; and do not require the extended pre-charge feature can drive the QACK pin with an inverted version of HRESET.

Revision Log

Date	Description
January 8, 2003	Initial advance release (version 0.1).
March 29, 2004	First general release (version 1.0).
December 27, 2004	Version 1.1 Added DD2.1 info to *Table 1-1. 750GX Processor Version Register (PVR)* In Section 1.4 Part Number Information, added "C=DD1.2" in the Design Revision Level entry. In Section 1.4 Part Number Information, changed information for 8. In Section 1.4 Part Number Information, added 2 notes.
February 17, 2005	Version SA14-2765-00 Changed document number to SA14-2765-00. Changed notes to Table 3-1 Absolute Maximum Ratings. Changed Table 3-5 Power Consumption for DD1.1. Added new Table 3-6 Power Consumption for DD1.2 Changed Table 3-8 (old 3-7) 60x Bus Input AC Timing Specifications. Changed Table 5-7 Maximum Heat-Sink Weight Limit for the CBGA. Removed “Preliminary“ from document status.
August 8, 2005	Version SA14-2765-01 Changed Section **1.4 Part Number Information**. Changed Table 3-2. Recommended Operating Conditions. Changed Table 3-4. DC Electrical Specifications. Changed Table 3-8. 60x Bus Input AC Timing Specifications. Changed Figure 4-1. Mechanical Dimensions and Bottom Surface Nomenclature of the CBGA Package for DD1.0 to Figure 4-1. Mechanical Dimensions, Standard Package. Changed Figure 4-2. Mechanical Dimensions and Bottom Surface Nomenclature of the CBGA Package for DD1.1 to Figure 4-1. Mechanical Dimensions, ROHS-Compatible Package.
September 2, 2005	Version SA14-2765-02 Removed “Preliminary“ from document headers. Also removed statements about preliminary information from the legal statements. Changed Section **4 Dimensions and Signal assignments by removing second and third paragraphs and Table 4-1 List of Drawings with IBM Package Numbers.** Changed Table 4-1. *Standard and Reduced-Lead Package, Layout, and Assembly Differences.* Changed Figure 4-1. Mechanical Dimensions, Standard Package. Changed Figure 4-1. Mechanical Dimensions, ROHS-Compatible Package.