MP6606

60V, 8-Channel Low-Side Driver with Serial Interface and Fault Indication

DESCRIPTION

The MP6606 is an 8-channel low-side driver IC with a serial interface. The device integrates low-side MOSFET (LS-FET) switches and high-side clamp diodes to drive inductive loads, which makes it well-suited for unipolar stepper motor and solenoid drives.

The MP6606 operates from a supply voltage of up to 60V, and can deliver an output current (I_{OUT}) up to 750mA (depending on PCB design and thermal conditions). The maximum voltage on the motor drive output pins is 60V.

Internal safety features include over-current protection (OCP), under-voltage lockout (UVLO), and thermal shutdown.

The MP6606 is available in a TSSOP-20EP package with an exposed pad.

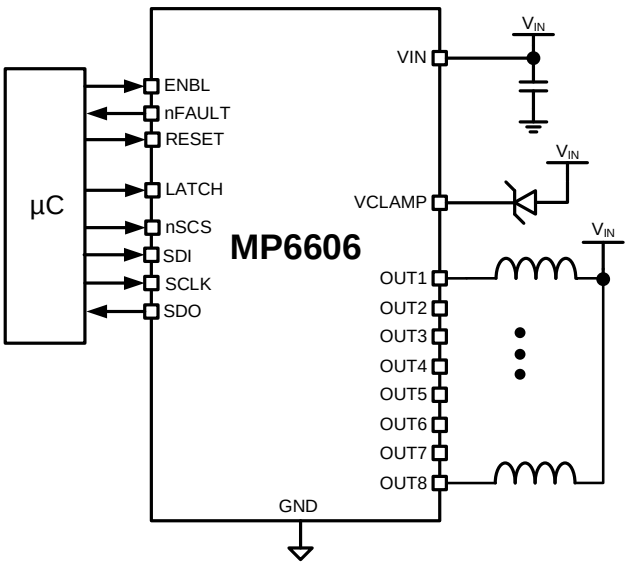
FEATURES

- Wide 4.5V to 60V Input Voltage (V_{IN}) Range
- 60V Maximum Winding Clamp Voltage
- 8 Low-Side MOSFETs (LS-FETs) and Clamp Diodes
- 700mΩ MOSFET On Resistance
- 750mA Maximum Output Current (I_{OUT}) when One LS-FET is On, or 500mA Maximum I_{OUT} when Eight LS-FETs are On
- Over-Current Protection (OCP)
- Thermal Shutdown and Under-Voltage Lockout (UVLO) Protection
- Fault Indication Output
- No Control Power Supply Required
- Simple Logic Interface with Schmitt Triggers
- 3.3V and 5V Compatible Logic Supply
- Available in a Thermally Enhanced TSSOP-20EP Package

APPLICATIONS

- Unipolar Stepper Motors
- Solenoid Drivers

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP6606GF	TSSOP-20EP	*See Below*	2A

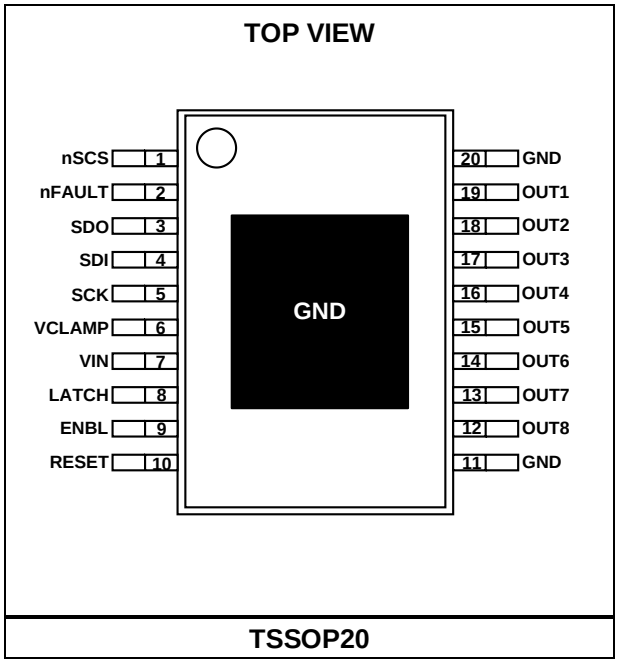
* For Tape & Reel, add suffix -Z (e.g. MP6606GF-Z).

TOP MARKING

MPSYYWW
MP6606
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP6606: part number
LLLLLLLLL: Lot number

PACKAGE REFERENCE



TSSOP20

PIN FUNCTIONS

Pin #	Name	Description
7	VIN	**Input supply voltage.** Decouple the VIN pin to ground with a minimum 100nF ceramic capacitor. Additional bulk capacitance may be required.
11, 20	GND	**Power ground.**
6	VCLAMP	**High side clamp.** Connect the VCLAMP pin to a TVS or Zener diode then connect this pin to VIN to clamp the leakage inductance spike.
4	SDI	**Serial data input.** The SDI pin has an internal pull-down resistor.
5	SCK	**Serial clock input.** The SCK pin has an internal pull-down resistor.
3	SDO	**Serial data output.** The SDO pin is an open-drain output that requires an external pull-up resistor if used.
1	nSCS	**Serial chip selection.** The nSCS pin is an active low serial peripheral interface (SPI) selector. nSCS has an internal pull-down resistor.
8	LATCH	**Latch input.** The LATCH pin has an internal pull-down resistor.
10	RESET	**Device reset input.** Drive the RESET pin active high to initialize the digital logic. RESET has an internal pull-down resistor.
9	ENBL	**Enable input.** Drive the ENBL pin to logic low to disable the outputs; drive ENBL to logic high to enable the outputs. The state of ENBL does not affect the serial interface. ENBL has an internal pull-down resistor.
2	nFAULT	**Fault indication.** The nFAULT pin is an open-drain output that requires an external pull-up resistor if used. nFAULT is driven low if a fault condition occurs.
19	OUT1	**Output terminal 1.**
18	OUT2	**Output terminal 2.**
17	OUT3	**Output terminal 3.**
16	OUT4	**Output terminal 4.**
15	OUT5	**Output terminal 5.**
14	OUT6	**Output terminal 6.**
13	OUT7	**Output terminal 7.**
12	OUT8	**Output terminal 8.**

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) ..... -0.3V to +65V
OUTx voltage (V_{OUTx}) ..... -0.7V to +65V
Clamp voltage (V_{CLAMP}) ..... -0.7V to +65V
All other pins to GND ..... -0.3V to +6.5V
Continuous power dissipation (T_A = 25°C) (2)
.....3.1W
Storage temperature ..... -55°C to +150°C
Junction temperature ..... 150°C
Lead temperature (solder) ..... 260°C

ESD Ratings

Human body model (HBM) ..... ±2kV
Charged device model (CDM) ..... ±2kV

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4.5V to 60V
Output voltage (V_{OUTx}).....0 to 60V
Maximum output current for low-side FETs (I_{LSX})
.....750mA
Maximum output current for high-side diodes (I_{HSX}) .....750mA at duty cycles <20%
Operating junction temp (T_J). ... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSSOP-20EP	40	8 °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can produce an excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{CLAMP} = 36V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		4.5	12 or 24	60	V
Clamp voltage	V_{CLAMP}		V_{IN}		60	V
Quiescent current	I_Q	V_{IN} = 24V, ENBL = 1, with no load		1.2	5	mA
Internal MOSFETs						
Output on resistance	$R_{DS(ON)}$	V_{IN} = 24V, I_{OUT} = 700mA, T_J = 25°C		700	900	mΩ
		V_{IN} = 24V, I_{OUT} = 700mA, T_J = 85°C			1200	mΩ
High-side diode forward voltage	V_F	I_{OUT} = 700mA			1.1	V
Body diode forward voltage	V_{FB}	I_{OUT} = 700mA			1.1	V
Control Logic						
Input logic low threshold	V_{IL}				0.7	V
Input logic high threshold	V_{IH}		2.3			V
Input logic hysteresis	ΔV_{IH}			560		mV
Logic input current	$I_{IN(H)}$	V_{IH} = 5V			20	µA
	$I_{IN(L)}$	V_{IL} = 0.8V			5	µA
nFAULT, SDO Outputs (Open-Drain Outputs)						
Output low voltage	V_{OL}	I_{OUT} = 5mA			0.5	V
Output high leakage current	I_{OH}	V_{OUT} = 3.3V			1	µA
Protection Circuits						
UVLO rising threshold	V_{IN_RISE}			3.2	4	V
Over-current trip level	I_{OCP}		0.9	2.1		A
Over-current deglitch time	t_{OCP}			3.5		µs
Over-current Retry Time	t_{OCR}			2.5		mS
Thermal shutdown (5)	T_{TSD}			168		°C
Thermal shutdown hysteresis (5)	ΔT_{TSD}			30		°C

Note:

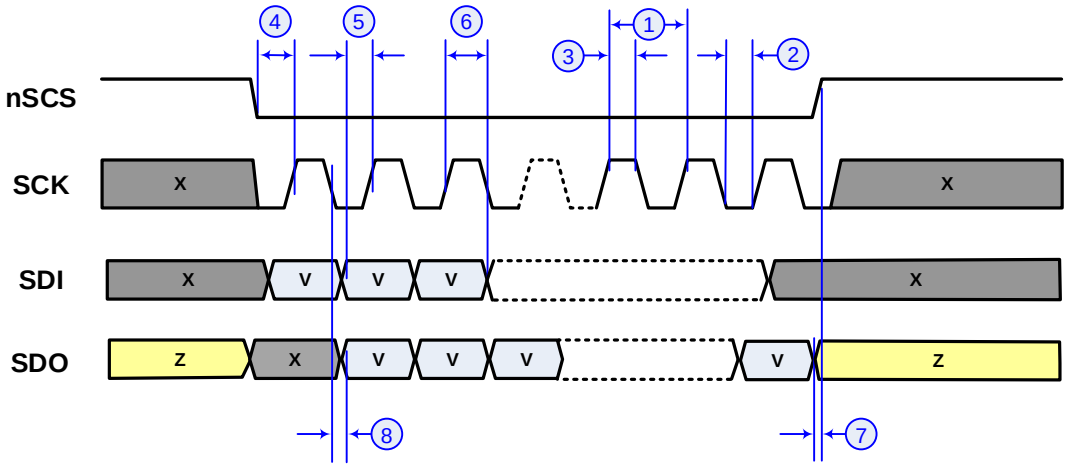
5) Guaranteed by design.

TIMING CHARACTERISTICS (6)

V_{IN} = 24V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
SCK cycle time	t1		100			ns
SCK frequency		This frequency is equal to 1 / t1	0.1		10	MHz
SCK high time	t2		50			ns
SCK low time	t3		50			ns
SCK rising/falling time					50	ns
Set-up time for nSCS low to SCK rising	t4		30			ns
Set-up time for SDI valid to SCK rising	t5		15			ns
Hold time for SCK rising to SDI invalid	t6		10			ns
Disable time for nSCS high to SDO Hi-Z	t7		75		120	ns
Delay time for SCK falling to SDO valid	t8	C_L < 100pF			10	ns
RESET pulse width			100			ns

TIMING DIAGRAM



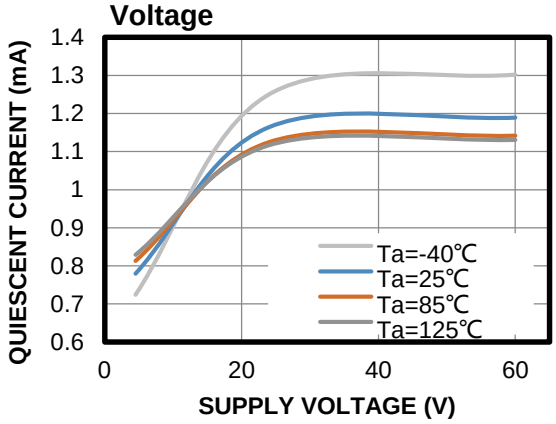
Note:

6) Not subject to production testing. Specified by design.

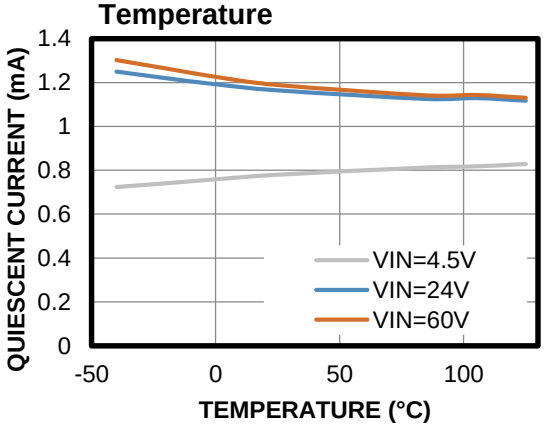
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{CLAMP} = 24V, TVS to VIN, I_{OUT} = 700mA, T_A = 25°C, resistor and inductor load: R = 33Ω, L = 1.5mH/channel, unless otherwise noted.

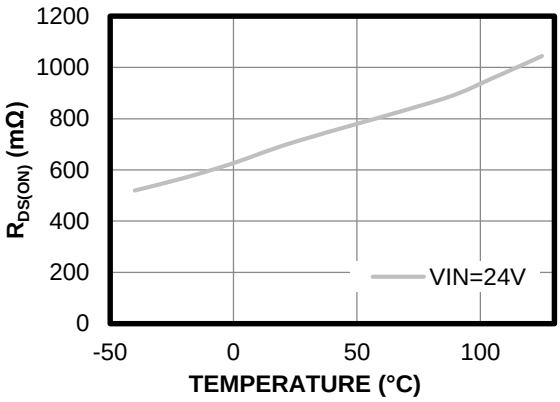
Quiescent Current vs. Supply Voltage



Quiescent Current vs. Temperature



$R_{DS(ON)}$ vs. Temperature

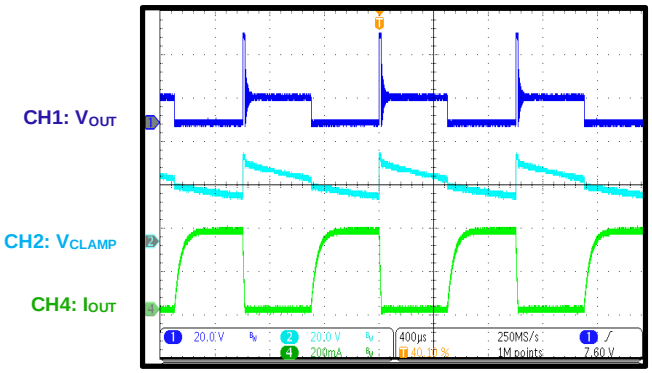


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{CLAMP} = 24V, TVS to VIN, T_A = 25°C, resistor and inductor load: R = 33Ω, L = 1.5mH/channel, unless otherwise noted.

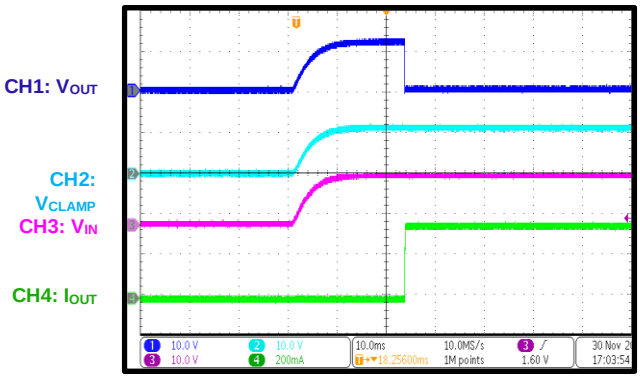
Normal Operation

LATCH connected to nSCS, f_{SW} = 1kHz



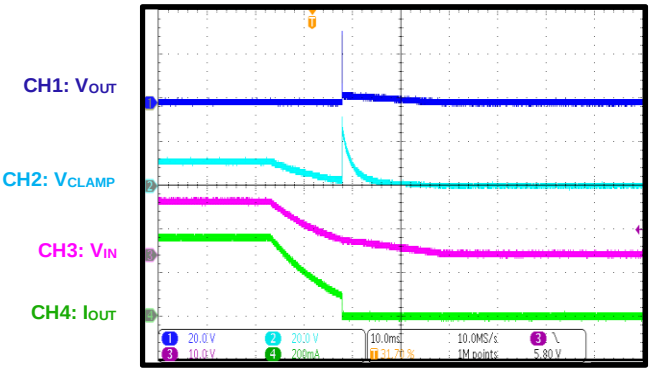
Start-Up through VIN

LATCH connected to nSCS



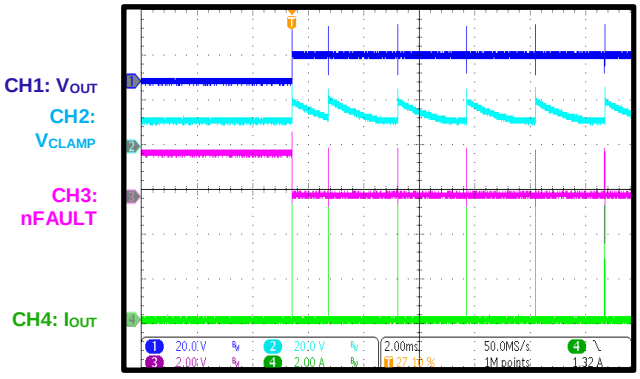
Shutdown through VIN

LATCH connected to nSCS



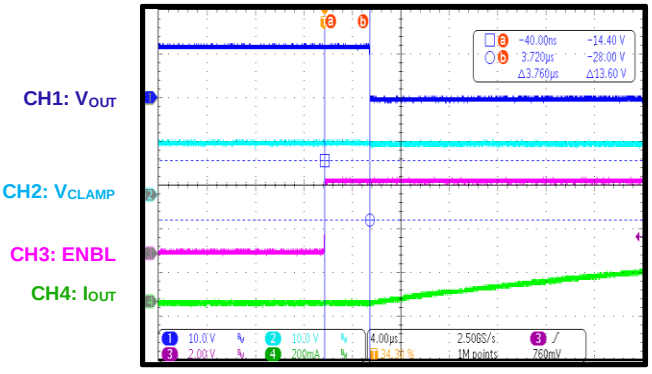
SCP

LATCH connected to nSCS



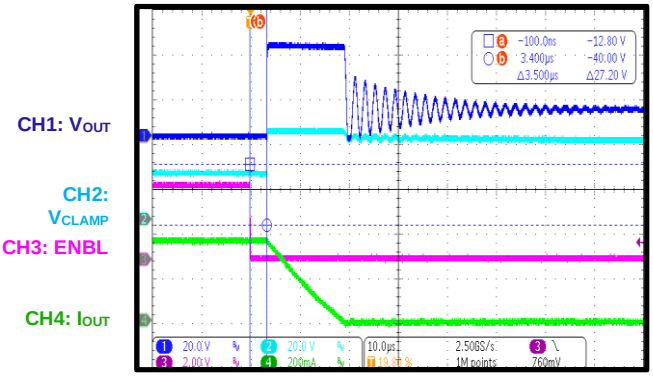
Chip Enabled

LATCH connected to nSCS



Chip Disabled

LATCH connected to nSCS



FUNCTIONAL BLOCK DIAGRAM

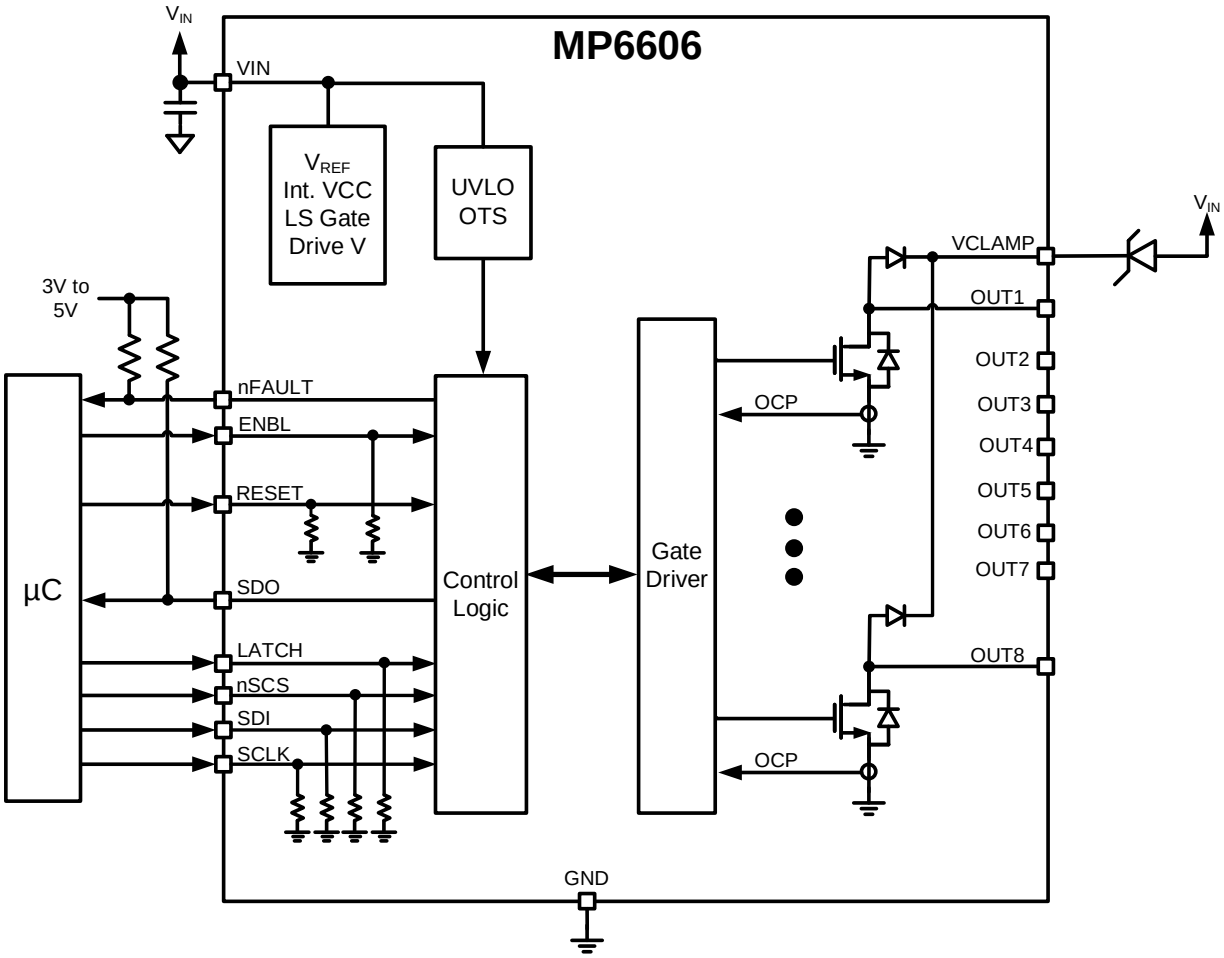


Figure 1: Functional Block Diagram

OPERATION

The MP6606 is an 8-channel low-side driver that integrates eight N-channel power MOSFETs and eight clamp diodes, each of which have a current capability of 750mA. The MP6606 operates over a wide 4.5V to 60V supply voltage range.

The MP6606 is designed to drive inductive loads, including unipolar stepper motors and solenoids.

Unipolar Stepper Operation

A unipolar stepper motor has two windings that are driven with currents that are 90° out of phase. Each winding has a center tap, which is connected to the power source. Current is driven through the winding in a push-pull fashion, which means the sides of the winding are alternately pulled to ground. This reverses the current and the magnetic field.

After a MOSFET turns off due to the inductance of the winding, current continues to flow through the other side of the winding. This current flows from ground through the opposite MOSFET body diode to the power supply.

Leakage Inductance Clamp (VCLAMP)

In a unipolar stepper, the two halves of the winding are not perfectly coupled, which results in leakage inductance. When a MOSFET turns off, the voltage rises up to twice its normal supply for a short period. This leakage inductance spike must be clamped to protect the MOSFETs from over-voltage damage.

When driving a solenoid connected to VIN, when the switch turns off, current must continue to flow until the magnetic field decays. This current goes to the VCLAMP pin.

These currents flow through the internal diodes from each output to a common VCLAMP pin. Generally, VCLAMP is connected to a transient voltage suppressor. This limits the voltage on the output pins to a maximum of 60V, regardless of VIN voltage.

If it is not required for the outputs to exceed the input voltage (V_{IN}) supply, connect VCLAMP to VIN.

The internal diodes can support 750mA of current at a maximum 20% duty cycle.

RESET and ENBL Operation

Driving the RESET pin active high initializes the digital logic. The serial interface and outputs are disabled while RESET is active.

The ENBL pin controls the output drivers. When ENBL is high, the outputs are enabled, and signals on the serial interface are recognized. When ENBL is low, the outputs are disabled, and the serial interface remains operational. ENBL has an internal pull-down resistor.

Logic Input Pins

All other logic inputs use a Schmitt trigger input buffer with a hysteresis. These pins are compatible with a 3.3V or 5V logic.

Fault Reporting

The MP6606 provides an nFAULT pin that reports if a fault condition (such as over-current protection (OCP) or over-temperature protection (OTP)) occurs. nFAULT is an open-drain output that is driven low if a fault condition occurs. If the fault condition is removed, nFAULT is pulled high by an external pull-up resistor.

Over-Current Protection (OCP)

OCP circuitry limits the current through the MOSFETs by disabling the gate driver. If OUTx exceeds the over-current threshold for longer than the over-current deglitch time, all the MOSFETs are disabled, and nFAULT is driven low. The driver automatically re-enables itself after a period of time.

Input Under-Voltage Lockout (UVLO) Protection

If the voltage on the VIN (V_{IN}) pin falls below the under-voltage lockout (UVLO) threshold, all of the circuitry in the device is disabled, and the internal logic is reset. Operation resumes when V_{IN} rises above the UVLO threshold.

Thermal Shutdown

If the die temperature exceeds its safe limits, the outputs are disabled, and nFAULT is driven low. Operation resumes automatically when the die temperature returns to a safe level.

Serial Interface Operation

A serial shift register interface is used to send data to the MP6606 outputs. Data shifts out of the SDO pin at the same time as the serial data is clocked in (see Figure 2). This allows multiple MP6606 devices to be connected in a daisy chain fashion.

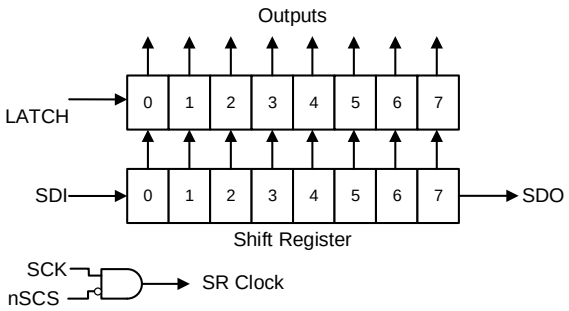


Figure 2: Serial Interface Operation

The outputs do not immediately change as data is shifted in or through the shift register. A rising edge on the LATCH input pin latches the data from the shift register into the outputs.

To write to a single device, 8 bits are clocked in the MSB first, and the previous data is clocked out.

Figure 3 shows how to write to a single device.

To write to two devices connected in a daisy chain, 16 bits are written (see Figure 4).

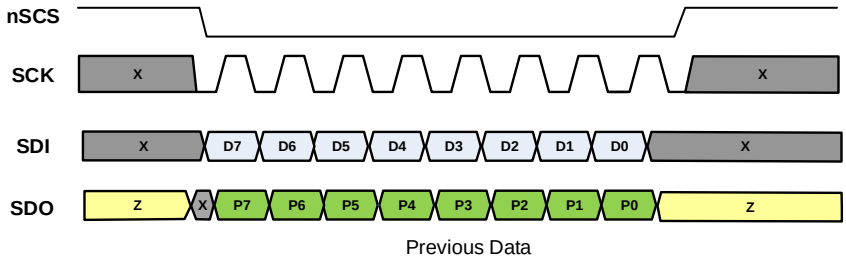


Figure 3: Writing to a Single Device

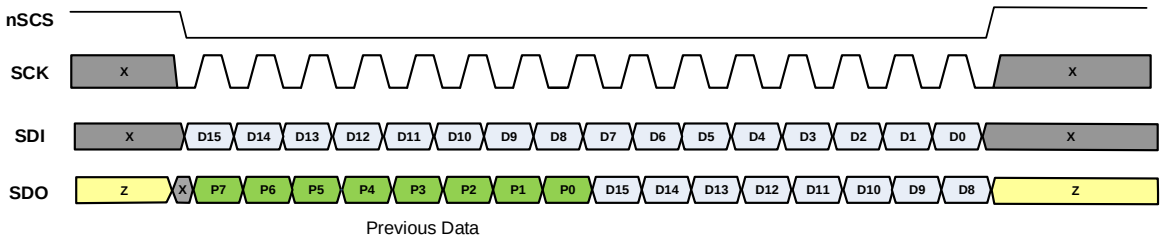


Figure 4: Writing to Two Devices

APPLICATION INFORMATION

Selecting the External Components

The MP6606 requires a 100nF, X7R ceramic bypass capacitor at the VIN pin. In addition, place a larger-value ceramic capacitor (4.7µF at minimum) nearby. Additional capacitance may be recommended. For example, if the device is located far away from the other capacitors located at VIN, it is recommended to place an electrolytic bulk capacitor at the input power supply side.

The VCLAMP pin dissipates the energy in an inductive load when the current is turned off. Depending on the application, VCLAMP can be connected directly to VIN, or to a TVS diode that is also connected to VIN.

Connecting VCLAMP to VIN is equivalent to connecting a diode from each output to VIN. A TVS diode allows the voltage on the output pins to rise above V_{IN} until the TVS diode breaks down. This increased voltage allows the current through the load to decay faster. This is typically recommended for applications with high-speed operation using unipolar stepper motors.

Select the TVS diode's breakdown voltage such that the VCLAMP pin remains below its maximum ratings. Note that TVS breakdown voltage may be higher than expected, as this value is rated for lower currents.

For VIN supply voltages of up to 24V, a 24V TVS diode is recommended. That ensures that the VCLAMP pin voltage stays within its limits.

PCB Layout Guidelines

PCB layout is vital for stable operation. For the best results, follow the guidelines below and refer to Figure 5:

1. Place the bypass capacitors near the IC
2. Place the VCLAMP TVS diode (if used) near the IC.
3. Place thermal vias under the exposed pad to help dissipate heat from the device to a plane either on the inner layer or on the back side of the PCB.

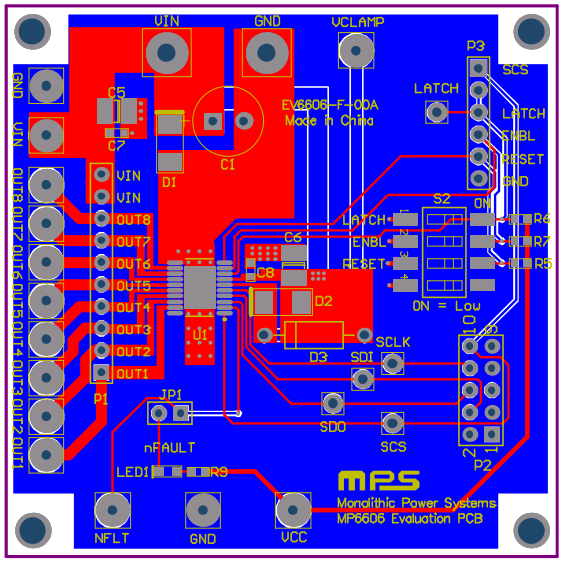


Figure 5: Recommended PCB Layout

TYPICAL APPLICATION CIRCUIT

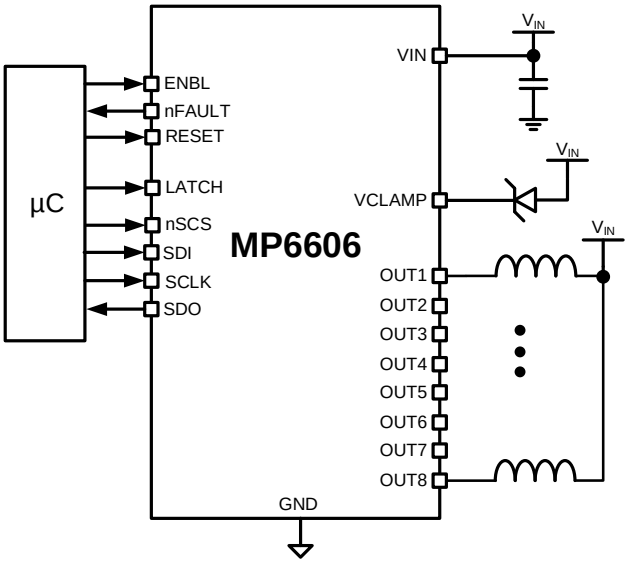
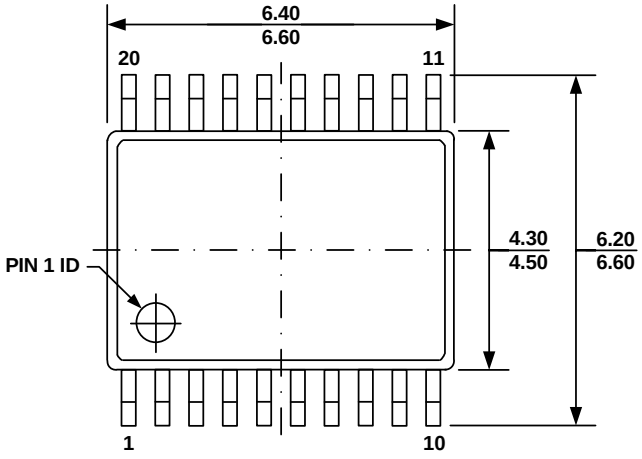


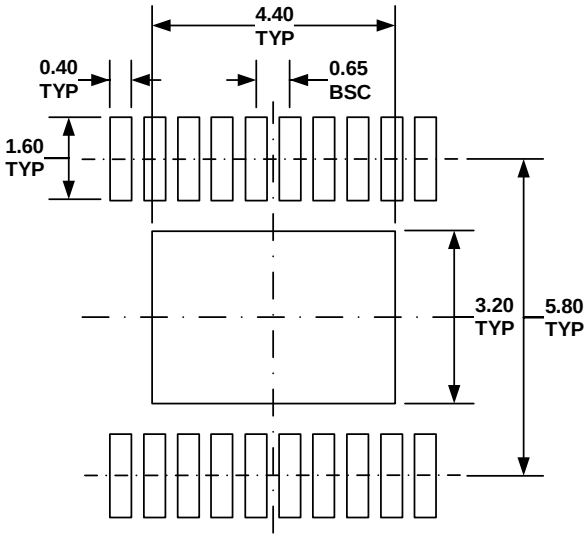
Figure 6: Typical Application Circuit

PACKAGE INFORMATION

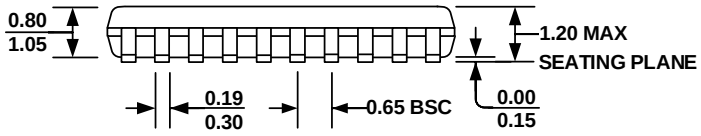
TSSOP-20EP



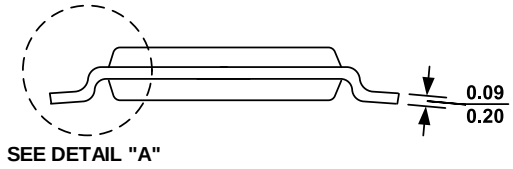
TOP VIEW



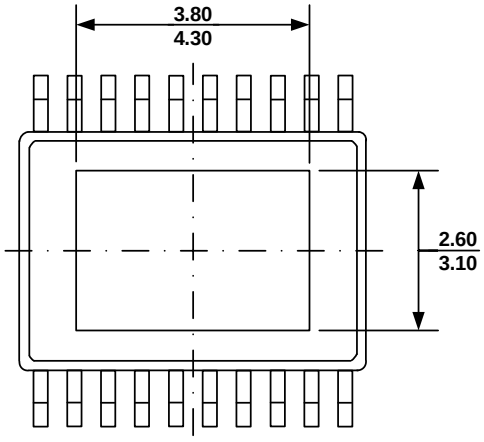
RECOMMENDED LAND PATTERN



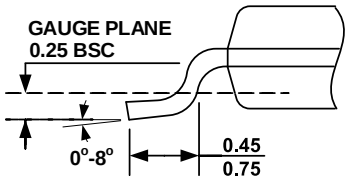
FRONT VIEW



SIDE VIEW



BOTTOM VIEW

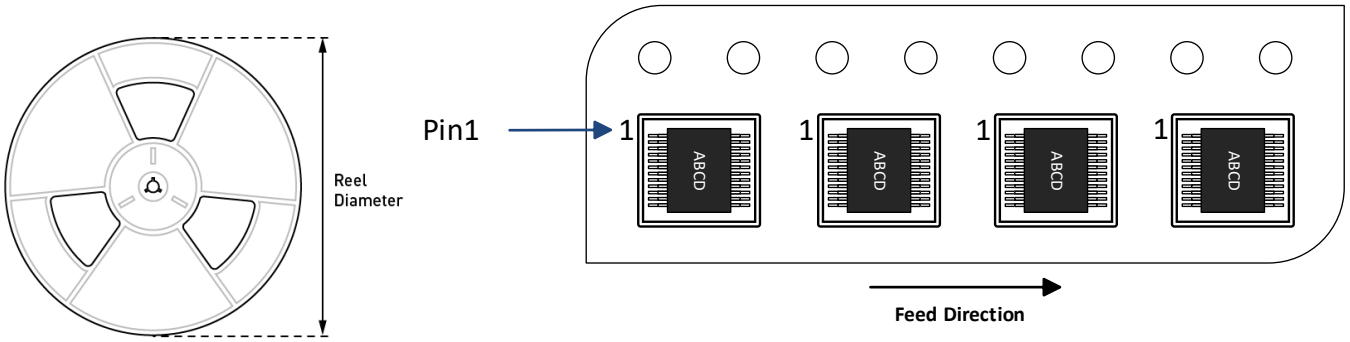


DETAIL “A”

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ACT.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP6606GF-Z	TSSOP-20EP	2500	75	N/A	13in	16mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/11/2022	Initial Release	-