

OptiMOS™-T2 Power-Transistor



Features

- N-channel Logic Level - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

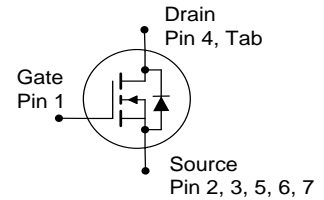
Product Summary

V_{DS}	40	V
$R_{DS(on)}$	1.2	mΩ
I_D	180	A

PG-TO263-7-3



Type	Package	Marking
IPB180N04S4L-01	PG-TO263-7-3	4N04L01



Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_C=25\text{ °C}, V_{GS}=10\text{V}^{1)}$	180	A
		$T_C=100\text{ °C}, V_{GS}=10\text{V}^{2)}$	180	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	720	
Avalanche energy, single pulse	E_{AS}	$I_D=90\text{ A}$	550	mJ
Avalanche current, single pulse	I_{AS}	-	180	A
Gate source voltage	V_{GS}	-	+20/-16	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	188	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C
IEC climatic category; DIN IEC 68-1	-	-	55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics²⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	0.8	K/W
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Electrical characteristics, at $T_j=25\text{ }^\circ\text{C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=140\text{ }\mu\text{A}$	1.2	1.7	2.2	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=40\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$	-	0.06	1	μA
		$V_{DS}=18\text{ V}, V_{GS}=0\text{ V}, T_j=85\text{ }^\circ\text{C}^{2)}$	-	1	20	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=50\text{ A}$	-	1.3	1.6	$\text{m}\Omega$
		$V_{GS}=10\text{ V}, I_D=100\text{ A}$	-	1.0	1.2	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V}, f=1\text{ MHz}$	-	14700	19100	pF
Output capacitance	C_{oss}		-	2400	3120	
Reverse transfer capacitance	C_{rss}		-	120	280	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=20\text{ V}, V_{GS}=10\text{ V}, I_D=180\text{ A}, R_G=3.5\ \Omega$	-	20	-	ns
Rise time	t_r		-	21	-	
Turn-off delay time	$t_{d(off)}$		-	90	-	
Fall time	t_f		-	80	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=32\text{ V}, I_D=180\text{ A}, V_{GS}=0\text{ to }10\text{ V}$	-	42	55	nC
Gate to drain charge	Q_{gd}		-	20	47	
Gate charge total	Q_g		-	188	245	
Gate plateau voltage	$V_{plateau}$		-	2.9	-	V

Reverse Diode

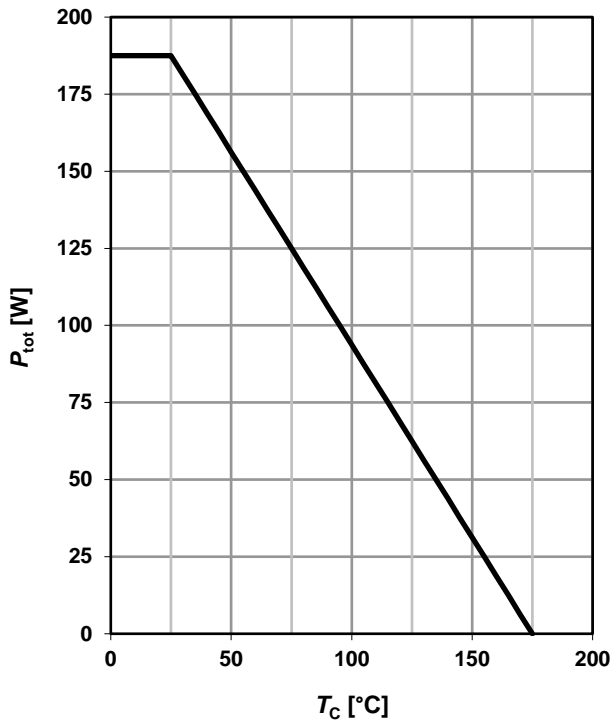
Diode continuous forward current ²⁾	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	180	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	720	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=100\text{ A}, T_J=25\text{ }^\circ\text{C}$	-	0.9	1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=20\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$	-	70	-	ns
Reverse recovery charge ²⁾	Q_{rr}		-	95	-	nC

¹⁾ Current is limited by bondwire; with an $R_{thJC} = 0.8\text{ K/W}$ the chip is able to carry 300 A at 25°C.

²⁾ Defined by design. Not subject to production test.

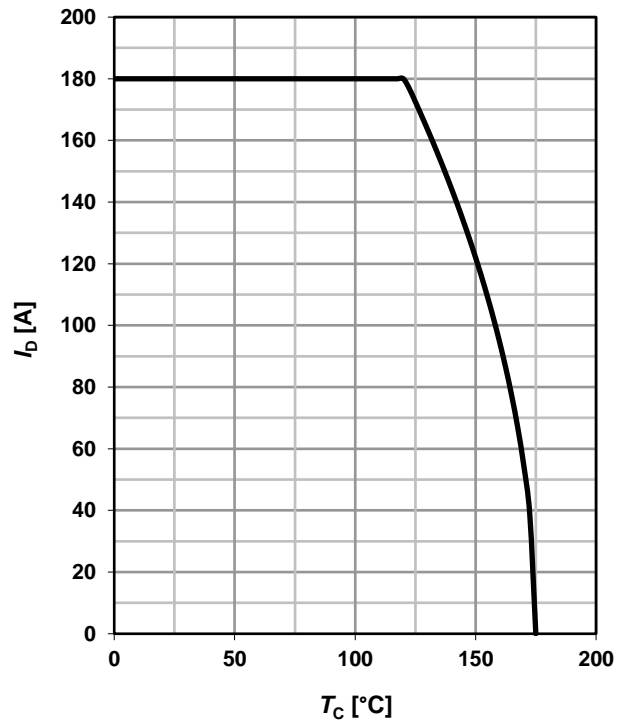
1 Power dissipation

$P_{tot} = f(T_C); V_{GS} \geq 6 \text{ V}$



2 Drain current

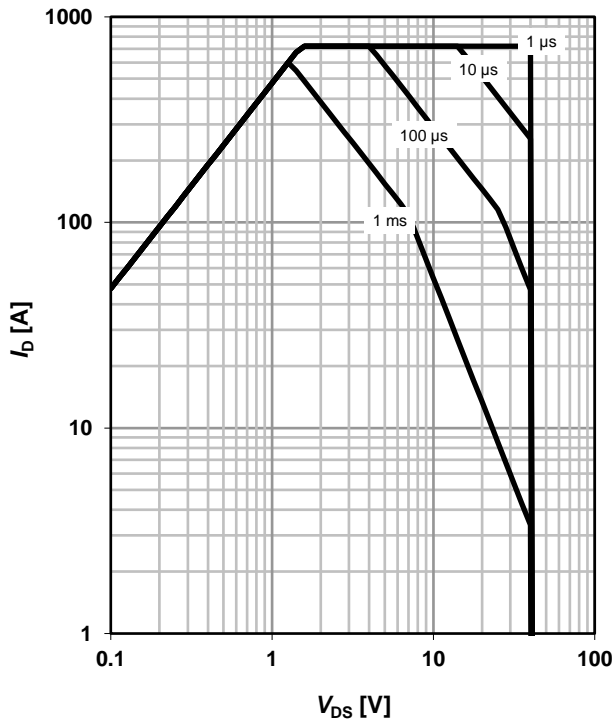
$I_D = f(T_C); V_{GS} \geq 6 \text{ V}$



3 Safe operating area

$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0$

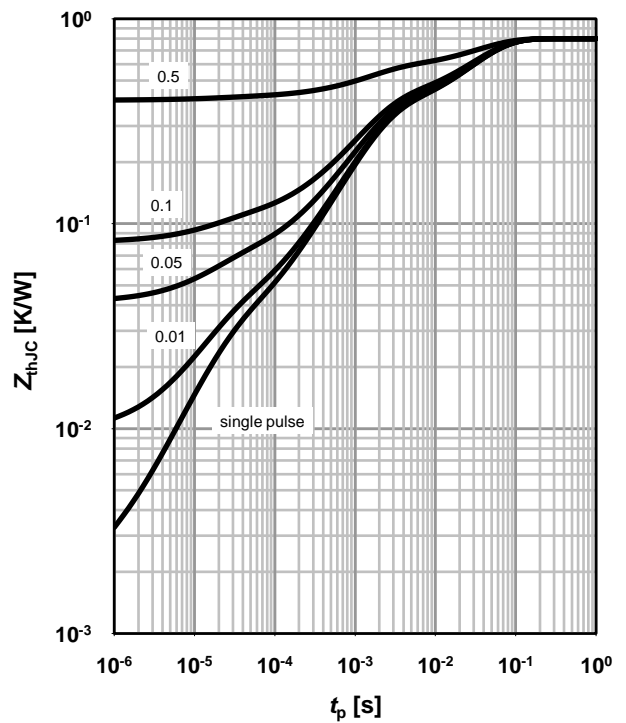
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

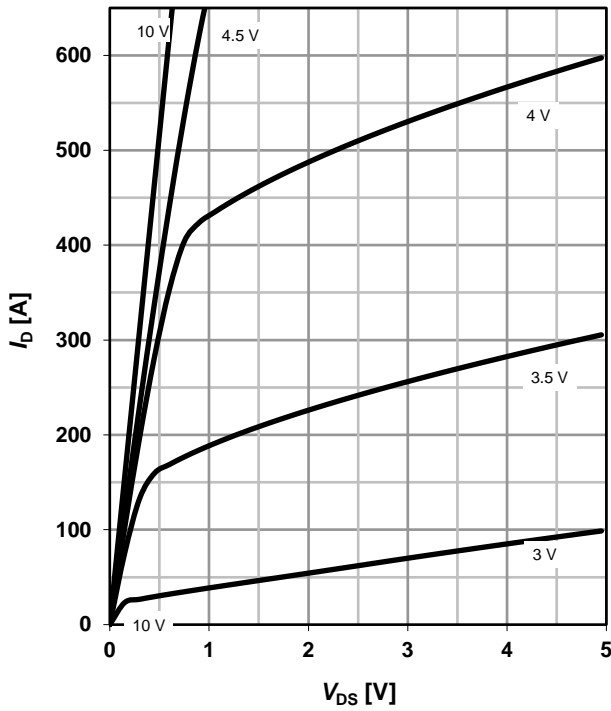
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

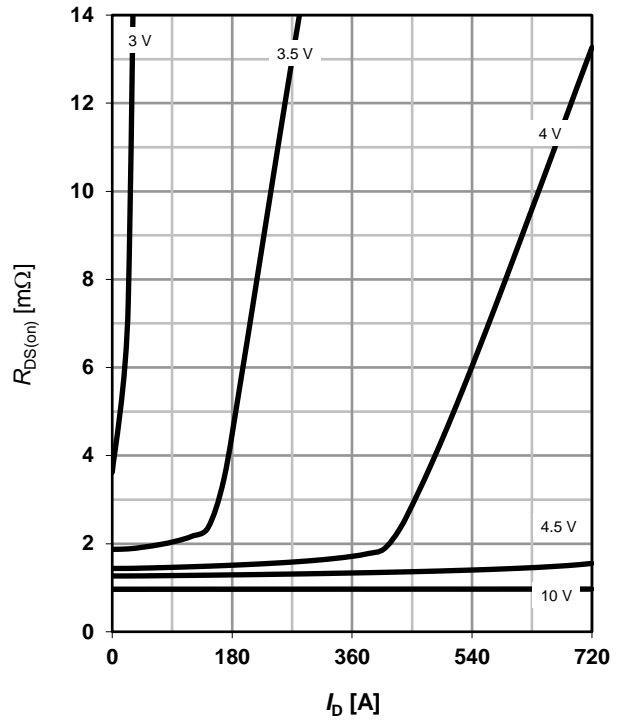
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

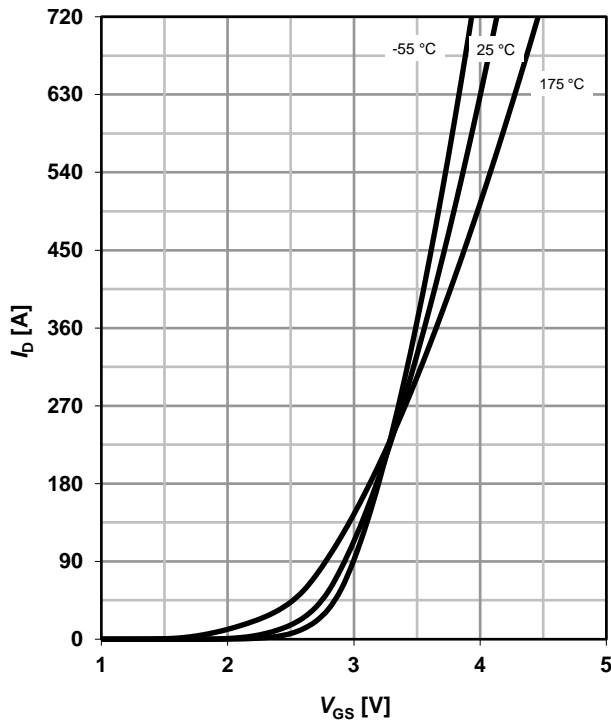
parameter: V_{GS}



7 Typ. transfer characteristics

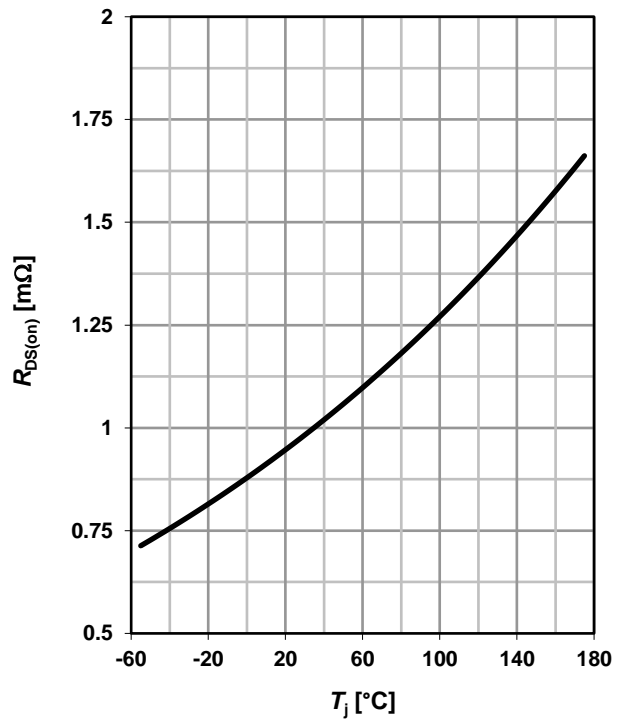
$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

parameter: T_j



8 Typ. drain-source on-state resistance

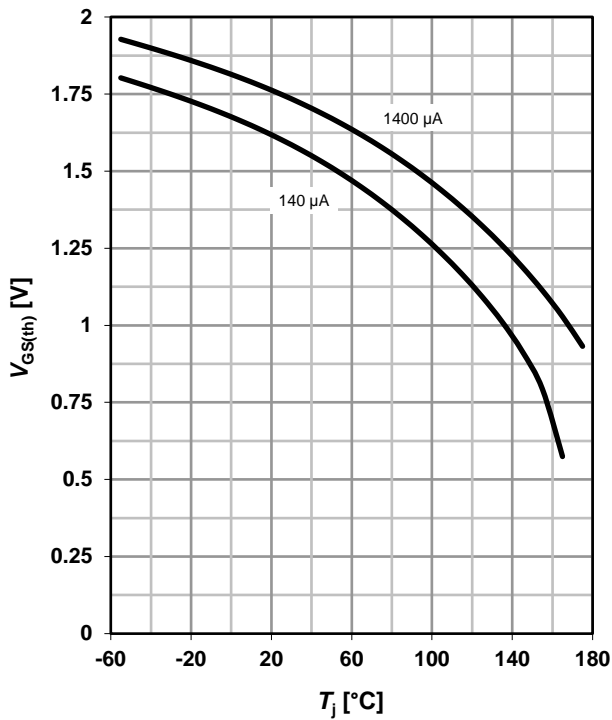
$R_{DS(on)} = f(T_j); I_D = 100\text{ A}; V_{GS} = 10\text{ V}$



9 Typ. gate threshold voltage

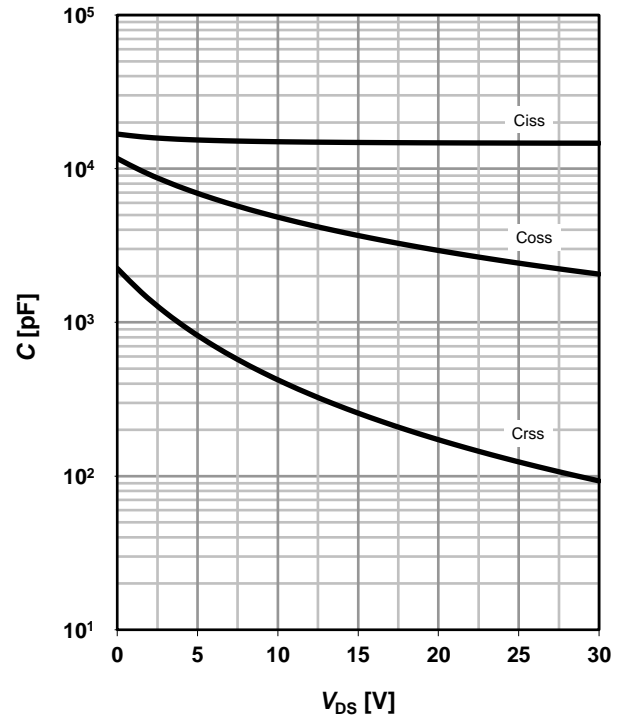
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

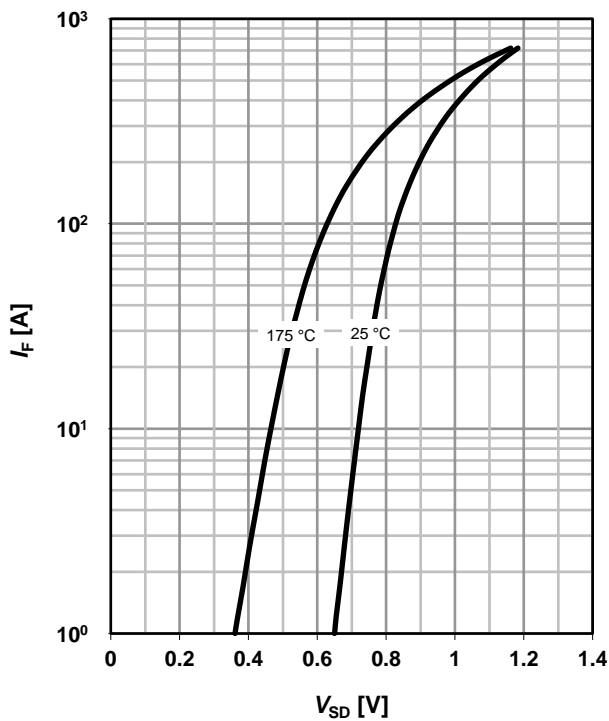
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

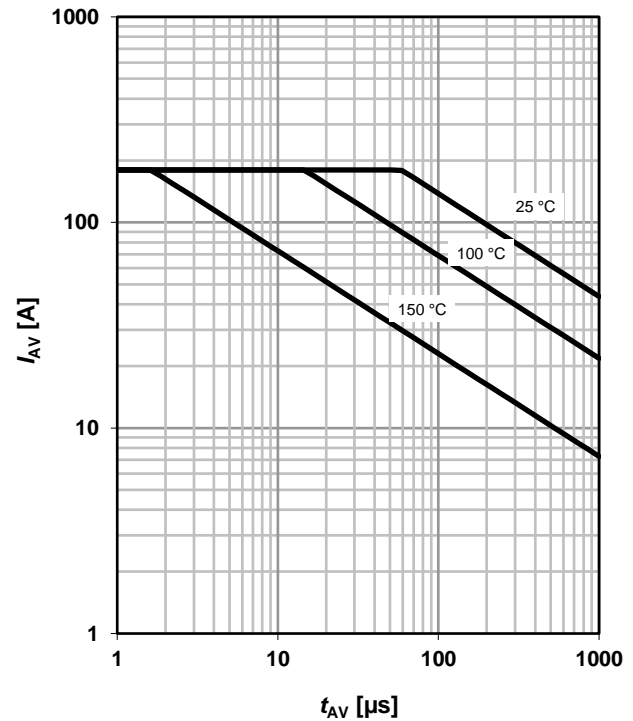
parameter: T_j



12 Typ. avalanche characteristics

$$I_{AS} = f(t_{AV})$$

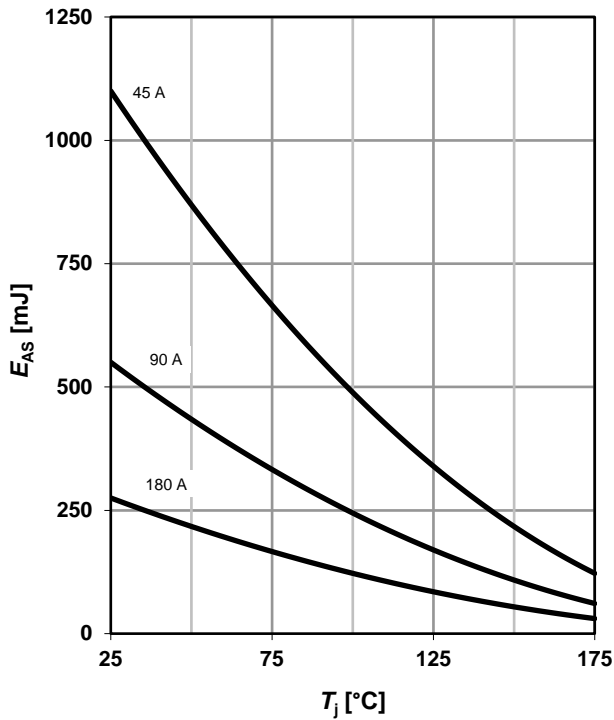
parameter: $T_{j(start)}$



13 Typical avalanche energy

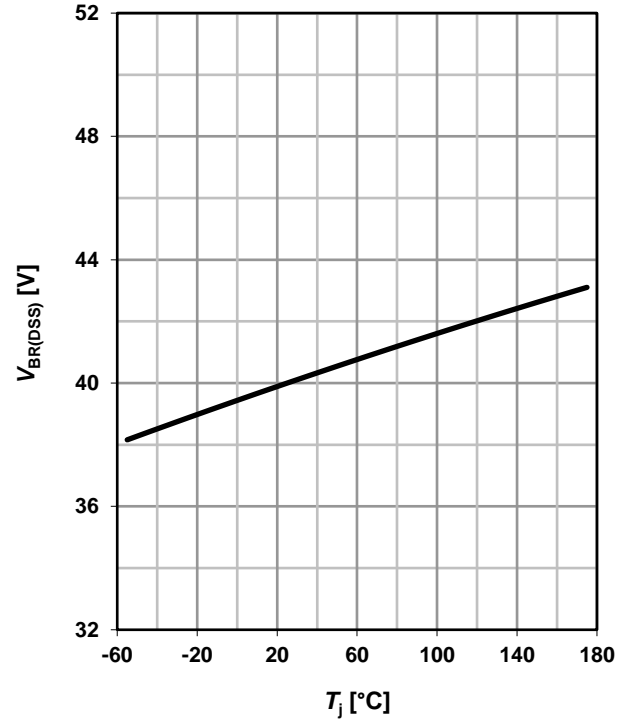
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

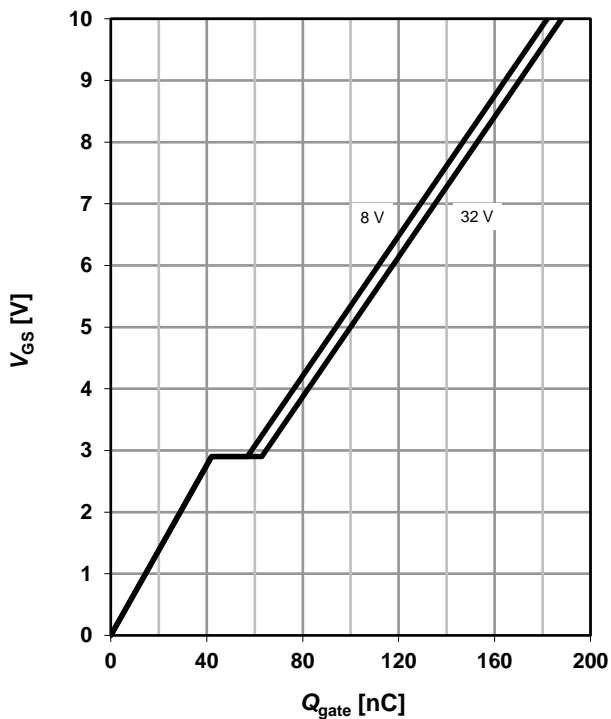
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



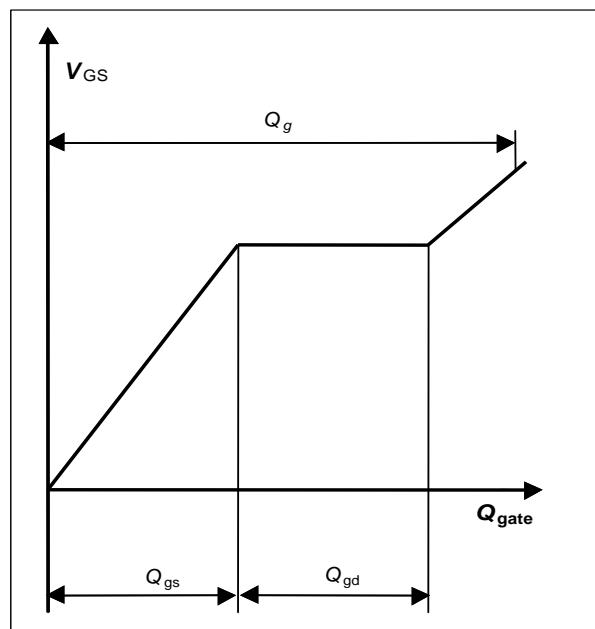
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 180 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



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If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History

Version	Date	Changes
Revision 1.0	03.06.2013	Data Sheet
Revision 1.1	06.08.2019	QGD corrected