HARRIS

HI-DAC85V

12Bit, Low Cost, Monolithic Digital to Analog Converter

June 1989

Features

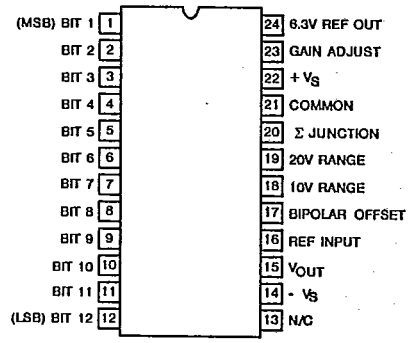
- DAC 85V Alternate Source
- Monolithic Construction
- Fast Settling
- Guaranteed Monotonic
- Wafer Laser Trimmed
- Applications Resistors On-Chip
- On-Board Reference
- Dielectric Isolation (DI) Process
- ±12V Supply Operation

Applications

- High Speed A/D Converters
- Precision Instrumentation
- CRT Display Generation

Pinout

HI1-DAC85V-4 (PLASTIC DIP)
TOP VIEW



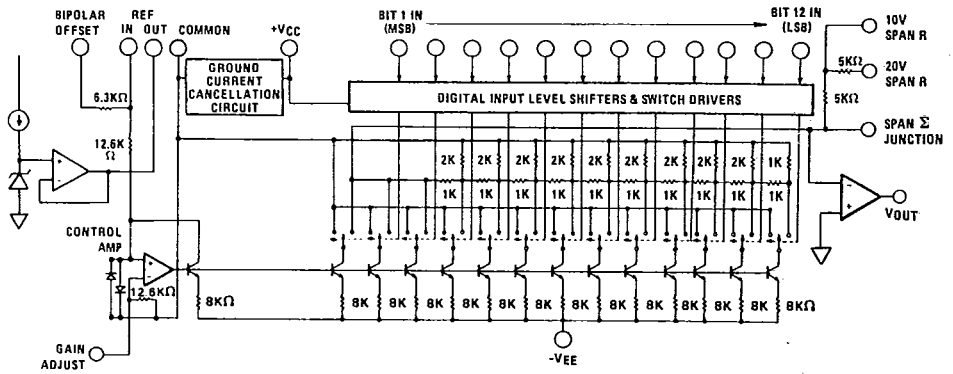
Description

The HI-DAC85V is a monolithic direct replacement for the popular DAC85 and AD DAC85 as well as the HI-5685V. Single chip construction along with several design innovations make the HI-DAC85V the optimum choice for low cost, high reliability applications. Harris' unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching times and minimum glitch. On board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy.

Internally the HI-DAC85V eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

The HI-DAC85V is available as a voltage output device which is guaranteed over the -25°C to +85°C temperature range. It includes a buried zener reference featuring low temperature coefficient as well as an on board operational amplifier. The HI-DAC85V requires only two power supplies and will operate in the range of ± (11.4V to 16.5V).

Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Specifications HI-DAC85V

Absolute Maximum Ratings (Note 1)

Power Supply Inputs $+V_S$ ..... +20V
$-V_S$ ..... -20V
Reference: Input (Pin 16) ..... $+V_S$
Output Drain 2.5mA
Digital Inputs (Bits 1 to 12) ..... -1V to $+V_S$
Max Junction Temperature ..... +175°C
Operating Temperature Range ..... -25°C to +85°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications Unless Otherwise Specified, T_A = +25°C, V_S ±12V to ±15V (Note 5), Pin 16 to Pin 24.

PARAMETER	CONDITIONS	HI-DAC85V-4 MIN	HI-DAC85V-4 TYP	HI-DAC85V-4 MAX	UNITS
RESOLUTION		-	-	12	Bits
DIGITAL INPUT (Note 3)					
Logic Levels	TTL Compatible				
Logic "1"	At +1µA	+2	-	+5.5	Volts
Logic "0"	At -100µA	0	-	+0.8	Volts
ACCURACY (Note 3)					
Integral Linearity Error	At +25°C	-	-	±1/2	LSB
	Full Temperature	-	±1/4	±1/2	LSB
Differential Linearity Error	Full Temperature	-	±1/4	±1/2	LSB
Monotonicity	Full Temperature	Guaranteed			
Gain Error (Notes 2, 4)	Full Temperature: Ceramic DIP	-	±0.1	±0.15	%FSR
	Plastic DIP	-	±0.1	±0.2	%FSR
Offset Error (Note 2)	Full Temperature	-	±0.05	±0.1	%FSR
DRIFT (Note 3)					
Gain		-	-	±20	PPM/°C
Unipolar Offset		-	±1	±3	PPM/°C
Bipolar Offset		-	±5	±10	PPM/°C
CONVERSION SPEED					
Setting Time (Note 3)	to ±0.01% of FSR				
With 10K Feedback	Full Scale Transition all Bits	-	3	-	µs
With 5K Feedback	ON to OFF or OFF to ON	-	1.5	-	µs
For 1 LSB Change		-	1.5	-	µs
Slew Rate		10	15	-	V/µs

Electrical Specifications (Continued) Unless Otherwise Specified, T_A = +25°C, V_S ±12V to ±15V (Note 5), Pin 16 to Pin 24.

PARAMETER	CONDITIONS	HI-DAC85V-4 MIN	HI-DAC85V-4 TYP	HI-DAC85V-4 MAX	UNITS
ANALOG OUTPUT					
Output Ranges		-	±2.5	-	V
		-	±5	-	V
		-	±10	-	V
		-	0 to 5	-	V
		-	0 to 10	-	V
Output current		±5	-	-	mA
Output Resistance		-	0.05	-	Ω
Short Circuit Duration	To Common		Continuous		
INTERNAL REFERENCE					
Output Voltage		6.250	+6.3	6.350	V
Output Impedence		-	1.5	-	Ω
External Current		-	-	+2.5	mA
Tempco of Drift		-	5	-	PPM/°C
POWER SUPPLY SENSITIVITY (Note 3, 5)					
+15V Supply		-	0.001	0.002	%FSR
-15V Supply		-	0.001	0.002	$\%V_S$
POWER SUPPLY REQUIREMENTS (Note 5)					
Voltage Range					
$+V_S$	Full Temperature	+11.4	+15	+16.5	V
$-V_S$	Full Temperature	-11.4	-15	-16.5	V
Current					
$+I_S$	Full Temperature V_S = ±15V	-	+12	+15	mA
$-I_S$	Full Temperature V_S = ±15V	-	-15	-20	mA

NOTES:
1. Absolute maximum ratings are limiting values applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Adjustable to zero using external potentiometers.
3. See definitions.
4. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc.
5. The HI-DAC85V will operate with supply voltages as low as ±11.4V. It is recommended that output voltage range -10V to +10V not be used if the supply voltages are less than ±12.5V.
6. With Gain and Offset errors adjusted to zero at +25°C.

Definitions of Specifications

Digital Inputs

The HI-DAC85V accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

DIGITAL INPUT	ANALOG OUTPUT		
	COMPLEMENTARY STRAIGHT BINARY	COMPLEMENTARY OFFSET BINARY	COMPLEMENTARY TWO'S COMPLEMENT*
MSB...LSB			
000...000	+Full Scale	+Full Scale	-LSB
100...000	Mid Scale-1 LSB	-1 LSB	+Full Scale
111...111	Zero	-Full Scale	Zero
011...111	+1/2 Full Scale	Zero	-Full Scale

* Invert MSB with external inverter to obtain CTC Coding.

Settling Time

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low. In a 12 bit system ±1/2 LSB = ±0.012% of FSR.

Thermal Drift

Thermal drift is based on measurements at +25°C, at high (T_H) and low (T_L) temperatures. Drift calculations are made for the high (T_H-25°C) and low (+25°C-T_L) ranges, and the larger of the two values is given as a specification representing worst case drift.

Gain Drift, Offset Drift, Reference Drift and Total Bipolar Drift are calculated in parts per million per °C as follows:

$$\text{Gain Drift} = \frac{\Delta \text{ FSR}/\Delta^{\circ}\text{C}}{\text{FSR}} \times 10^6$$

$$\text{Offset Drift} = \frac{\Delta \text{ Offset}/\Delta^{\circ}\text{C}}{\text{FSR}} \times 10^6$$

$$\text{Reference Drift} = \frac{\Delta V_{REF}/\Delta^{\circ}\text{C}}{V_{REF}} \times 10^6$$

$$\text{Total Bipolar Drift} = \frac{V_o/\Delta^{\circ}\text{C}}{\text{FSR}} \times 10^6$$

NOTE: FSR = Full Scale Output Voltage -Zero Scale Output Voltage

Δ FSR = FSR (T_H) - FSR (+25°C)
or FSR (+25°C) - FSR (T_L)
V_o = Steady-state response to any input code.

Total Bipolar Drift is the variation of output voltage with temperature, in the bipolar mode of operation. It represents the net effect of drift in Gain, Offset, Linearity and Reference Voltage. Total Bipolar Drift values are calculated, based on measurements as explained above. Gain and Offset need not be calibrated to zero at +25°C. The specified limits for TBD apply for any input code and for any power supply setting within the specified operating range.

Accuracy

LINEARITY ERROR (Short for "Integral Linearity Error." Also, sometimes called "Integral Nonlinearity" and "Nonlinearity".)- The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to end-point linearity for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL LINEARITY ERROR - The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY - The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

TOTAL ERROR - The net output error resulting from all internal effects (primarily non-ideal Gain, Offset, Linearity and Reference Voltage). Supply voltages may be set to any values within the specified operating range. Gain and offset errors must be calibrated to zero at +25°C. Then the specified limits for Total Error apply for any input code and for any temperature within the specified operating range.

Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in $-V_S$, or $+V_S$ supplies. It is specified under DC conditions and expressed as full scale range percent of change divided by power supply percent change.

$$\text{P.S.S.} = \frac{\dfrac{\Delta \text{ Full Scale Range} \times 100}{\text{Full Scale Range (Nominal)}}}{\dfrac{\Delta V_S \times 100}{V_S \text{ (Nominal)}}}$$

Glitch

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale i.e. the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the Product of duration and amplitude.)

Decoupling and Grounding

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in figure 1 should be used. Decoupling capacitors should be connected close to the HI-DAC85V (preferably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

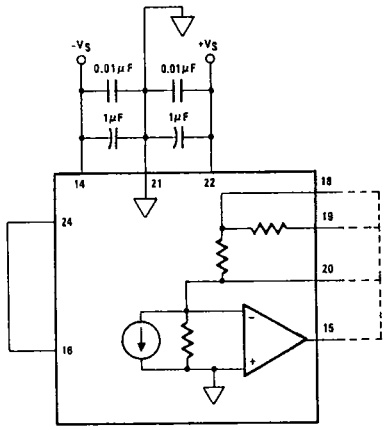


FIGURE 1.

Reference Supply

An internal 6.3 Volt reference is provided on board the HI-DAC85V. The voltage (pin 24) is accurate to ±0.8% and must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-DAC85V. All gain adjustments should be made under constant load conditions.

Output Voltage Ranges

HI-DAC85V

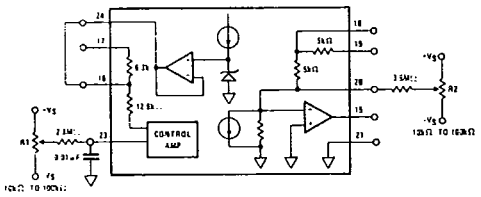


FIGURE 2.

RANGE CONNECTIONS

	RANGE	CONNECT PIN 15	CONNECT PIN 17	CONNECT PIN 19
Unipolar	0 to +5V	18	N.C.	20
	0 to +10V	18	N.C.	N.C.
Bipolar	±2.5V	18	20	20
	±5V	18	20	N.C.
	±10V	19	20	15

Gain and Offset Calibration

UNIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for zero volts out

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for FS-1LSB
- That is:
  - 4.9988 for 0 to +5V range
  - 9.9976 for 0 to +10V range

BIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for Negative FS
- That is:
  - -10V for ±10V range
  - -5V for ±5V range
  - -2.5V for ±2.5 range

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for positive FS-1LSB
- That is:
  - +9.9951V for ±10V range
  - +4.9976V for ±5V range
  - +2.4988V for ±2.5V range

This Bipolar procedure adjusts the output range end points. The maximum error at zero (half scale) will not exceed the Linearity error. See the "Accuracy" specifications.

Die Characteristics

Transistor Count 214
Die Size ..... 108 x 163 mils
Thermal Impedance;
θ_{ja} ..... 79°C/W
θ_{jc} ..... 20°C/W
Tie Substrate to: ..... Ground
Process ..... Bipolar-DI

Ordering Information

Part Number	Temperature Range	Package
HI1-DAC85V-4	-25°C to +85°C	24-Pin Plastic DIP
HI3-DAC85V-4	-25°C to +85°C	24-Pin Plastic DIP
HI3-DAC85V-9	-40°C to +85°C	24-Pin Plastic DIP

NOTES: The HI-DAC85V are now available in plastic DIP packages. The ceramic DIP package will be discontinued in the future and is not recommended for new designs. Below is the ordering information for plastic packages.