HARRIS SEMICONDUCTOR

NOT RECOMMENDED FOR NEW DESIGNS
See HI5810

HI-7153

8-Channel, 10-Bit High Speed Sampling A/D Converter

December 1997

Features

- 5µs Conversion Time
- 8 Channel Input Multiplexer
- 200,000 Channels/Second Throughput Rate
- Over 9 Effective Bits at 20kHz
- No Offset or Gain Adjustments Necessary
- Analog and Reference Inputs Fully Buffered
- On-Chip Track and Hold Amplifier
- µP Compatible Interface
- 2's Complement Data Output
- 150mW Power Consumption
- Only a Single 2.5V Reference Required for a ±2.5V Input Range
- Out-of-Range Flag
- /883 Version Available

Applications

- µP Controlled Data Acquisition Systems
- DSP
  - Avionics
  - Sonar
- Process Control
  - Automotive Transducer Sensing
  - Industrial
- Robotics
- Digital Communications

Description

The HI-7153 is an 8 channel high speed 10 bit A/D converter which uses a Two Step Flash algorithm to achieve through-put rates of 200kHz. The converter features an 8 channel CMOS analog multiplexer with random channel addressing. A unique switched capacitor technique allows a new input voltage to be sampled while a conversion is taking place.

Internal high speed CMOS buffers at both the analog and reference inputs simplifies interface requirements.

A Track and Hold amplifier is included on the chip, consisting of two high speed amplifiers and an internal hold capacitor, reducing external circuitry.

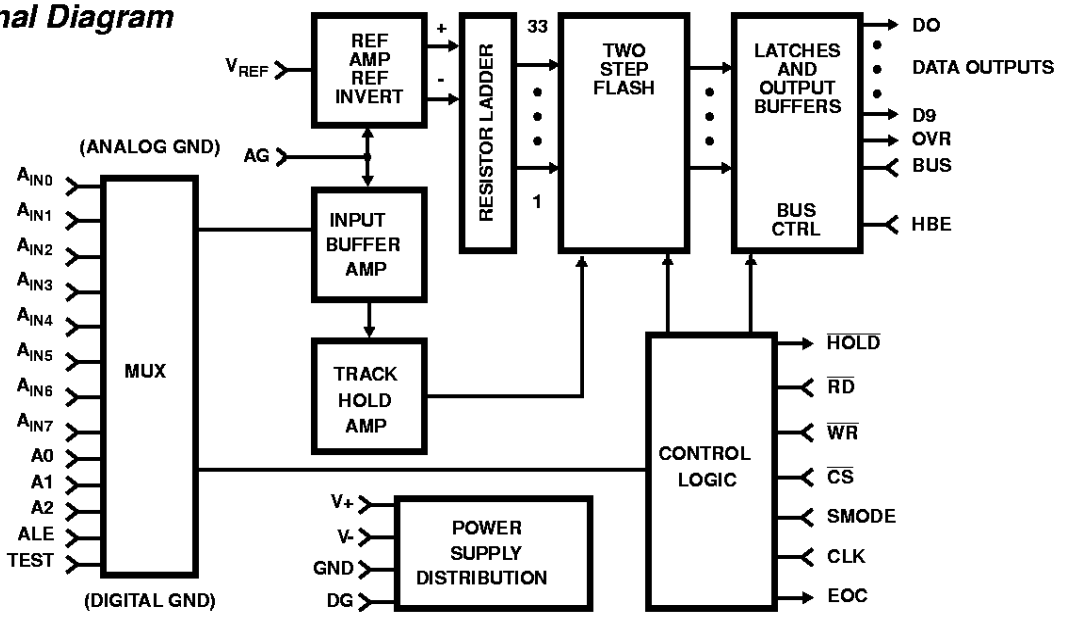
Microprocessor bus interfacing is simplified by the use of standard Chip Select, Read, and Write control signals. The digital three-state outputs are byte organized for bus interface to 8 or 16 bit systems. An Out-of-Range pin, together with the MSB bit, can be used to indicate an under or over-range condition.

The HI-7153 operates with ±5V supplies. Only a single +2.5V reference is required to provide a bipolar input range from -2.5V to +2.5V.

Ordering Information

PART NUMBER	LINEARITY (MAX ILE)	TEMPERATURE RANGE	PACKAGE
HI3-7153J-5	±1.0 LSB	0°C to +70°C	40 Lead Plastic DIP
HI3-7153A-9	±1.0 LSB	-40°C to +85°C	40 Lead Plastic DIP
HI1-7153S-2	±1.0 LSB	-55°C to +125°C	40 Lead Ceramic DIP

Functional Diagram

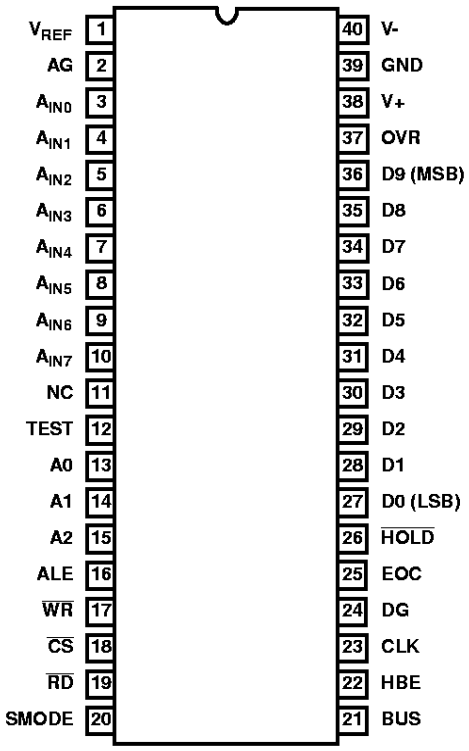


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2787.4**

Pinouts

HI-7153
(CDIP, PDIP)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage
V+ to GND (DG/AG/GND) . . . . . -0.3V < V+ < +5.7V
V- to GND (DG/AG/GND) . . . . . -5.7V < V- < +0.3V
Analog InputPins (Note 1)
(A_{IN0} - A_{IN7}, V_{REF}) . . . . . V- -0.3V < V_{INA} < V+ +0.3V
Digital I/O Pins (Note 1) . . . . . DG -0.3V < $V_{I/O}$ < V+ +0.3V
(D0 - D9, OVR, CLK, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, ALE, SMODE, $\overline{HOLD}$, EOC, HBE, BUS, A0 - A2, TEST)
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C

Thermal Information

Thermal Resistance θ_{JA}
Plastic . . . . . 50°C/W
Operating Temperature Range
HI3-7153X-5 . . . . . 0°C to +70°C
HI3-7153X-9 . . . . . -40°C to +85°C
HI1-7153X-2 . . . . . -55°C to +125°C
Power Dissipation (Note 2) 500mW
Derate above +70°C at 10mW/°C

NOTES:

1. Input voltages may exceed the supply voltage, on input or channel at a time, provided the input current is limited to ±10mA
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = +5V, V- = -5V, V_{REF} = +2.50V, f_{CLK} = 600kHz, $t_R = t_F \leq 25$ns, 50% Duty Cycle. All Typical Values have been Characterized but are Not Tested.

(NOTE 4) PARAMETER	SYMBOL	TEMPERATURE	(NOTE 3) J, A, S GRADE MIN	TYP	MAX	UNITS
ACCURACY						
Resolution (Note 5)	RES	T_A = +25°C	10	-	-	Bits
		$T_{MIN} \leq T_A \leq T_{MAX}$	10	-	-	Bits
Integral Linearity Error	ILE	T_A = +25°C	-	±0.5	±1.0	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±0.75	±1.0	LSB
Differential Linearity Error	DLE	T_A = +25°C	-	±0.5	±1.0	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±0.75	±1.0	LSB
Bipolar Offset Error	V_{OS}	T_A = +25°C	-	±1.0	±2.5	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±1.5	±3.0	LSB
Unadjusted Gain Error	FSE	T_A = +25°C	-	±1.0	±2.5	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±1.5	±3.0	LSB
Channel to Channel Mismatch		T_A = +25°C	-	±0.002	-	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±0.002	-	LSB

NOTES:

1. Input voltages may exceed the supply voltage, one input or channel at a time, provided the input current is limited to 10mA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. See Ordering Information Table.
4. FSR (Full Scale Range) = 2 x V_{REF} (5.00V at V_{REF} = 2.50V). LSB (Least Significant Bit) = FSR/1024 (4.88mV at V_{REF} = 2.50V).
5. Parameter Not tested. Parameter guaranteed by design, simulation, or characterization.
6. T_{MIN} and T_{MAX} limits guaranteed by +25°C test.

Electrical Specifications

T_A = +25°C, V+ = +5V, V- = -5V, V_{REF} = +2.50V, f_{CLK} = 600kHz, t_R = t_F ≤ 25ns, 50% Duty Cycle. All Typical Values have been Characterized but are Not Tested.

(NOTE 1) PARAMETER	SYMBOL	CONDITIONS	+25°C TYP	UNITS
DYNAMIC CHARACTERISTICS				
Signal to Noise Ratio	SNR	f_{IN} = 4.932kHz, ±2.5V	59	dB
		f_{IN} = 14.697kHz, ±2.5V	59	dB
		f_{IN} = 24.462kHz, ±2.5V	58	dB
		f_{IN} = 43.994kHz, ±2.5V	56	dB
Signal to Noise + Distortion	SINAD	f_{IN} = 4.932kHz, ±2.5V	59	dB
		f_{IN} = 14.697kHz, ±2.5V	58	dB
		f_{IN} = 24.462kHz, ±2.5V	55	dB
		f_{IN} = 43.994kHz, ±2.5V	48	dB
Total Harmonic Distortion	THD	f_{IN} = 4.932kHz, ±2.5V	-66	dBc
		f_{IN} = 14.697kHz, ±2.5V	-61	dBc
		f_{IN} = 24.462kHz, ±2.5V	-56	dBc
		f_{IN} = 43.994kHz, ±2.5V	-48	dBc
Spurious-Free Dynamic Range	SFDR	f_{IN} = 4.932kHz, ±2.5V	-76	dB
		f_{IN} = 14.697kHz, ±2.5V	-77	dB
		f_{IN} = 24.462kHz, ±2.5V	-77	dB
		f_{IN} = 43.994kHz, ±2.5V	-74	dB

NOTE:

1. FSR (Full Scale Range) = 2 x V_{REF} (5.00V at V_{REF} = 2.50V). LSB (Least Significant Bit) = FSR/1024 (4.88mV at V_{REF} = 2.50V)

DC Electrical Specifications

T_A = +25°C, V+ = +5V, V- = -5V, V_{REF} = +2.50V, f_{CLK} = 600kHz, t_R = t_F ≤ 25ns, 50% Duty Cycle, Unless Otherwise Specified. All Typical Values have been Characterized but are Not Tested.

(NOTE 1) PARAMETER	SYMBOL	CONDITIONS	+25°C			0°C to +75°C		-40°C to +85°C		-55°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
ANALOG MULTIPLEXER INPUT												
Input Range	VIR		$-V_{REF}$	-	$+V_{REF}$	$-V_{REF}$	$+V_{REF}$	$-V_{REF}$	$+V_{REF}$	$-V_{REF}$	$+V_{REF}$	V
Input Resistance	R_{IN}		-	10	-	-	-	-	-	-	-	MΩ
Input Leakage Current	IBI	A_{IN} = 0V	-	0.01	100	-	100	-	100	-	100	nA
On Channel Input Capacitance	$CA_{IN(ON)}$	A_{IN} = 0V, Note 2	-	10	30	-	30	-	30	-	30	pF
Off Channel Input Capacitance	$CA_{IN(OFF)}$	A_{IN} = 0V, Note 2	-	8	20	-	20	-	20	-	20	pF
MUX On-Resistance	$R_{DS(ON)}$	A_{IN} = ±2.5V, I_{IN} =100µA	-	1.1	2.5	-	2.5	-	2.5	-	2.5	KΩ
Greatest Change in $R_{DS(ON)}$ Between Any Two Channels	$\Delta R_{DS(ON)}$	-2.5V ≤ A_{IN} ≤ +2.5V	-	2.5	-	-	-	-	-	-	-	%

DC Electrical Specifications T_A = +25°C, V+ = +5V, V- = -5V, V_{REF} = +2.50V, f_{CLK} = 600kHz, t_R = t_F ≤ 25ns, 50% Duty Cycle, Unless Otherwise Specified. All Typical Values have been Characterized but are Not Tested. **(Contin-**

(NOTE 1) PARAMETER	SYMBOL	CONDITIONS	+25°C			0°C to +75°C		-40°C to +85°C		-55°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Off-Channel Isolation	OIRR	F_{IN} =100kHz, Note 4	-	-96	-	-	-	-	-	-	-	dB
Channel to Channel Isolation	CCRR	F_{IN} =100kHz, Note 4	-	-83	-	-	-	-	-	-	-	dB
REFERENCE INPUT												
Reference Input Range	VRR	Note 3	2.2	-	2.6	2.2	2.6	2.2	2.6	2.2	2.6	V
Reference Input Bias Current	IBR	V_{REF} = +2.50V	-	0.01	100	-	100	-	100	-	100	nA
Reference Input Capacitance	CV_R	Note 2	-	8	20	-	-	-	-	-	-	pF
LOGIC INPUTS												
Input High Voltage	V_{IH}		2.4	-	-	2.4	-	2.4	-	2.4	-	V
Input Low Voltage	V_{IL}		-	-	0.8	-	0.8	-	0.8	-	0.8	V
Logic Input Current	I_{IL}	V_{IN} = 0V, +5V	-	0.05	1	-	1	-	1	-	1	µA
Input Capacitance	C_{IN}	Note 2	-	7	17	-	-	-	-	-	-	pF
LOGIC OUTPUTS												
Output High Voltage	V_{OH}	I_{OH} = -200µA	2.4	-	-	2.4	-	2.4	-	2.4	-	V
Output Low Voltage	V_{OL}	I_{OL} = 1.6mA	-	-	0.4	-	0.4	-	0.4	-	0.4	V
Output Leakage Current	I_{OL}	$\overline{RD}$ = +5V, V_{OUT} = +5V	-	0.04	1	-	10	-	10	-	10	µA
		$\overline{RD}$ = +5V, V_{OUT} = 0V	-1	-0.01	-	-10	-	-10	-	-10	-	µA
Output Capacitance	C_{OUT}	High-Z State, Note 2	-	7	15	-	-	-	-	-	-	pF
POWER SUPPLY VOLTAGE RANGE												
	V+	Functional Operation Only, Note 3	4.5	5.0	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
	V-		-4.5	-5.0	-5.5	-4.5	-5.5	-4.5	-5.5	-4.5	-5.5	V
POWER SUPPLY REJECTION												
V+, V- Gain Error	ΔFSE	V+ = 5V, V- = -4.75V, -5.25V	-	0.1	0.5	-	0.6	-	0.6	-	0.8	LSB
		V- = -5V, V+ = 4.75V, 5.25V	-	0.1	0.5	-	0.6	-	0.6	-	0.8	LSB
V+, V- Offset Error	ΔVOS	V+ = 5V, V- = -4.75V, -5.25V	-	0.15	0.5	-	0.6	-	0.6	-	0.8	LSB
		V- = -5V, V+ = 4.75V, 5.25V	-	0.15	0.5	-	0.6	-	0.6	-	0.8	LSB

DC Electrical Specifications

T_A = +25°C, V+ = +5V, V- = -5V, V_{REF} = +2.50V, f_{CLK} = 600kHz, $t_R = t_F \leq 25$ns, 50% Duty Cycle, Unless Otherwise Specified. All Typical Values have been Characterized but are Not Tested. **(Contin-**

(NOTE 1) PARAMETER	SYMBOL	CONDITIONS	+25°C			0°C to +75°C		-40°C to +85°C		-55°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
SUPPLY CURRENTS												
V+ Supply Current	I+	V+ = 5V, V- = -5V, V_{IN} = 0V, Digital Outputs Are Unloaded	-	20	30	-	30	-	30	-	30	mA
V- Supply Current	I-		-	-10	-15	-	-15	-	-15	-	-15	mA
GND Current	IGND		-	-8	-	-	-	-	-	-	-	mA
DG Current	IDG		-	-2	-	-	-	-	-	-	-	mA
AG Current	IAG		-	0.02	-	-	-	-	-	-	-	µA

NOTES:

1. FSR (Full Scale Range) = 2 x V_{REF} (5.00V at V_{REF} = 2.50V). LSB (Least Significant Bit) = FSR/1024 (4.88mV at V_{REF} = 2.50V)
2. Parameter Not tested. Parameter guaranteed by design, simulation, or characterization
3. Functionality is guaranteed by negative GAIN ERROR test.
4. Channel Isolation is tested with an input signal of ±2.5Vp-p, 100kHz and the measured pin is loaded with 100Ω to GND

DC Electrical Specifications

T_A = +25°C, V+ = 5V ±10%, V- = -5V, V_{REF} = 2.50V, f_{CLK} = 600kHz, $t_R = t_F \leq 25$ns, 50% Duty Cycle, C_L = 100pF (Including Stray for D0-D9, OVR, $\overline{HOLD}$), Unless Otherwise Specified. All Typical Values have been Characterized but are Not Tested.

(NOTE 4) PARAMETER	SYMBOL	CONDITIONS	+25°C			0°C to +75°C		-40°C to +85°C		-55°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
TIMING CHARACTERISTICS												
Continuous Conversion Time	t_{SPS}	Note 2	-	-	5	-	5	-	5	-	5	µs
		Note 9	60	-	-	60	-	60	-	60	-	µs
		Notes 2, 8	-	-	$3t_{CLK}$	-	$3t_{CLK}$	-	$3t_{CLK}$	-	$3t_{CLK}$	µs
Conversion Time, First Conversion	t_{CONV}	Notes 1, 9	-	-	$4t_{CLK}$ + 0.63	-	$4t_{CLK}$ + 0.75	-	$4t_{CLK}$ + 0.75	-	$4t_{CLK}$ + 0.8	µs
Continuous Throughput	t_{CYC}	Note 2	-	-	$t_{CLK}/3$	-	$t_{CLK}/3$	-	$t_{CLK}/3$	-	$t_{CLK}/3$	CPS
Clock Period	t_{CLK}		-	$1/f_{CLK}$	-	-	-	-	-	-	-	-
Clock Input Duty Cycle	D	Note 9	45	50	55	45	55	45	55	45	55	%
ALE Pulse Width	t_{ALEW}	Note 9	30	15	-	40	-	40	-	50	-	ns
Address Setup Time	t_{AS}	Note 9	40	15	-	80	-	80	-	80	-	ns
Address Hold Time	t_{AH}		0	-16	-	0	-	0	-	0	-	ns
$\overline{WR}$ Pulse Width	t_{WRL}	Notes 1, 3, 9	100	20	$t_{CLK}/2$	100	$t_{CLK}/2$	100	$t_{CLK}/2$	100	$t_{CLK}/2$	ns
$\overline{WR}$ to EOC Low	t_{WREOC}	Notes 1, 9	-	80	130	-	160	-	160	-	160	ns
$\overline{WR}$ to $\overline{HOLD}$ Delay	t_{HOLD}	Notes 1, 9	-	80	150	-	170	-	170	-	170	ns
Clock to $\overline{HOLD}$ Rise Delay	t_{CKHR}	Note 9	150	265	450	140	500	120	500	120	500	ns
Clock to $\overline{HOLD}$ Fall Delay	t_{CKHF}	Notes 2, 9	50	95	200	40	225	40	225	40	225	ns

DC Electrical Specifications

T_A = +25°C, V+ = 5V ±10%, V- = -5V, V_{REF} = 2.50V, f_{CLK} = 600kHz, t_R = t_F ≤ 25ns, 50% Duty Cycle, C_L = 100pF (Including Stray for D0-D9, OVR, $\overline{HOLD}$), Unless Otherwise Specified. All Typical Values have been Characterized but are Not Tested. **(Continued)**

(NOTE 4) PARAMETER	SYMBOL	CONDITIONS	+25°C			0°C to +75°C		-40°C to +85°C		-55°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Clock to EOC High	t_{CKEOC}	Notes 1, 9	-	460	630	-	750	-	750	-	800	ns
$\overline{HOLD}$ to DATA Change	t_{DATA}	Notes 2, 9	100	200	350	90	400	90	400	90	400	ns
$\overline{CS}$ to DATA	t_{CD}	Note 9	-	40	70	-	85	-	85	-	85	ns
HBE to DATA	t_{AD}	Note 9	-	30	50	-	70	-	70	-	70	ns
$\overline{RD}$ LOW to Active	t_{RD}	Notes 6, 9	-	70	100	-	125	-	125	-	125	ns
$\overline{RD}$ HIGH to Inactive	t_{RX}	Notes 7, 9	-	30	60	-	70	-	70	-	70	ns
Output Rise Time	t_R	Notes 5, 9	-	20	40	-	60	-	60	-	60	ns
Output Fall Time	t_F	Notes 5, 9	-	15	30	-	50	-	50	-	50	ns

NOTES:

1. Slow memory mode timing
2. Fast memory or DMA mode of operation, except the first conversion which is equal to t_{CONV}
3. Maximum specification to prevent multiple triggering with $\overline{WR}$
4. All input drive signals are specified with t_R = t_F ≤ 10ns and shall swing from 0.4V to 2.4V for all timing specifications. A signal is considered to change state as it crosses a 1.4V threshold (except t_{RD} and t_{RX})
5. t_R and t_F load is C_L = 100pF (including stray capacitance) to DG and is measured from the 10% - 90% point
6. t_{RD} is the time required for the data output level to change by 10% in response to $\overline{RD}$ crossing a voltage level of 1.4V. High-Z to V_{OH} is measured with R_L = 2.5KΩ and C_L = 100pF (including stray) to DG. High-Z to V_{OL} is measured with R_L = 2.5KΩ to V+ and C_L = 100pF (including stray) to DG
7. t_{RX} is the time required for the data output level to change by 10% in response to $\overline{RD}$ crossing a voltage level of 1.4V. V_{OH} to High-Z is measured with R_L = 2.5KΩ and C_L = 10pF (including stray) to DG. V_{OL} to High-Z is measured with R_L = 2.5KΩ to V+ and C_L = 10pF (including stray) to DG
8. For clock frequencies other than 600kHz
9. Parameter Not Tested. Parameter guaranteed by design, simulation, or characterization