flex

Technical Specification

BMR467 series PoL Regulators Input 7.5 - 14 V, Output up to 120 A / 216 W	28701-BMR 467 Rev E March 2021
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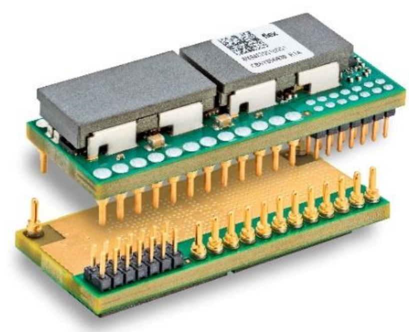
Key Features
- Small Package
  Laydown: 50.8 x 19.05 x 10.4 mm (2.0 x 0.75 x 0.41 in)
  SIP: 50.8 x 8.2 x 19.05 mm (2.0 x 0.32 x 0.75 in)
- Control loop with fast load transient response
- 0.6 V - 1.8 V output voltage range
- High maximum output current, 120 A
- Current sharing up to 4 modules, 480 A
- High efficiency, typ. 93.2% at 12 Vin, 1.8 Vout, half load
- Configuration and monitoring via PMBus
- Phase synchronization & spreading
- Voltage tracking capability
- Margining up/down
- MTBF 10.49 Mh



General Characteristics
- Configuration support via Flex Power Designer
- Monotonic soft-start ramp up
- Reduced external output decoupling capacitance
- Input under-voltage & over-voltage shutdown
- Output over current & over voltage protection
- Over temperature protection
- Remote control & Power Good pins
- Differential sense pins
- Voltage setting via pin-strap or PMBus
- ISO 9001/14001 certified supplier
- Highly automated manufacturing ensures quality

PMBus

Safety Approvals

c UL us   UL EU

Design for Environment

Pb   RoHS compatible

Meets requirements in high-temperature lead-free soldering processes.

Contents

Ordering Information

Product program	Output
BMR 467 $n_1n_2$10/001n_8	0.6-1.8 V, 120 A/216 W

Product number and Packaging

BMR 467 $n_1n_2n_3n_4/n_5n_6n_7n_8$									
Options	n_1	n_2	n_3	n_4	/	n_5	n_6	n_7	n_8
Mounting	o				/				
Mechanical		o			/				
Digital interface			o	o	/				
Configuration file					/	o	o	o	
Packaging					/				o

Options	Description	
n_1	0	Horizontal through hole mounted version (Laydown TH)
	1	Horizontal surface mounted version (Laydown SMD)
	2	Vertical through hole mounted version (Single in Line, SIP)
n_2	0	Open frame
	1	Open frame 5.5mm pin length
n_3 n_4	10	PMBus and pin strap
n_5 n_6 n_7	001	CTRL pin positive logic (active high)
n_8	B	Antistatic tray of 144 products (SIP)
	C	Antistatic tape & reel of 130 products (Laydown TH and SMD)

Example: Product number BMR 467 0010/001C equals a through-hole mounted, open frame, PMBus and analog pin strap, positive RC logic, standard configuration variant, package tape&reel.

General Information

Reliability

The failure rate (λ) and mean time between failures (MTBF= 1/λ) is calculated at max output power and an operating ambient temperature (T_A) of +40°C. Flex Power Modules uses Telcordia SR-332 Issue 2 Method 1 to calculate the mean steady-state failure rate and standard deviation (σ).

Telcordia SR-332 Issue 3 also provides techniques to estimate the upper confidence levels of failure rates based on the mean and standard deviation.

Mean steady-state	Std. deviation, σ
95 nFailures/h	7.6 nFailures/h

MTBF (mean value) for the BMR467 series = 10.49 Mh.
MTBF at 90% confidence level = 9.51 Mh

Compatibility with RoHS requirements

The products are compatible with the relevant clauses and requirements of the RoHS directive 2011/65/EU and have a maximum concentration value of 0.1% by weight in homogeneous materials for lead, mercury, hexavalent chromium, PBB and PBDE and of 0.01% by weight in homogeneous materials for cadmium.

Exemptions in the RoHS directive utilized in Flex Power Modules products are found in the Statement of Compliance document.

Flex Power Modules fulfills and will continuously fulfill all its obligations under regulation (EC) No 1907/2006 concerning the registration, evaluation, authorization and restriction of chemicals (REACH) as they enter into force and is through product materials declarations preparing for the obligations to communicate information on substances in the products.

Quality Statement

The products are designed and manufactured in an industrial environment where quality systems and methods like ISO 9000, Six Sigma, and SPC are intensively in use to boost the continuous improvements strategy. Infant mortality or early failures in the products are screened out and they are subjected to an ATE-based final test. Conservative design rules, design reviews and product qualifications, plus the high competence of an engaged work force, contribute to the high quality of the products.

Warranty

Warranty period and conditions are defined in Flex Power Modules General Terms and Conditions of Sale.

Limitation of Liability

Flex Power Modules does not make any other warranties, expressed or implied including any warranty of merchantability or fitness for a particular purpose (including, but not limited to, use in life support applications, where malfunctions of product can cause injury to a person’s health or life).

Safety Specification

General information

Flex Power Modules DC/DC converters and DC/DC regulators are designed in accordance with the safety standards IEC 60950-1, EN 60950-1 and UL 60950-1 *Safety of Information Technology Equipment*.

IEC/EN/UL 60950-1 contains requirements to prevent injury or damage due to the following hazards:

- Electrical shock
- Energy hazards
- Fire
- Mechanical and heat hazards
- Radiation hazards
- Chemical hazards

On-board DC/DC converters and DC/DC regulators are defined as component power supplies. As components they cannot fully comply with the provisions of any safety requirements without “conditions of acceptability”. Clearance between conductors and between conductive parts of the component power supply and conductors on the board in the final product must meet the applicable safety requirements. Certain conditions of acceptability apply for component power supplies with limited stand-off (see Mechanical Information and Safety Certificate for further information). It is the responsibility of the installer to ensure that the final product housing these components complies with the requirements of all applicable safety standards and regulations for the final product.

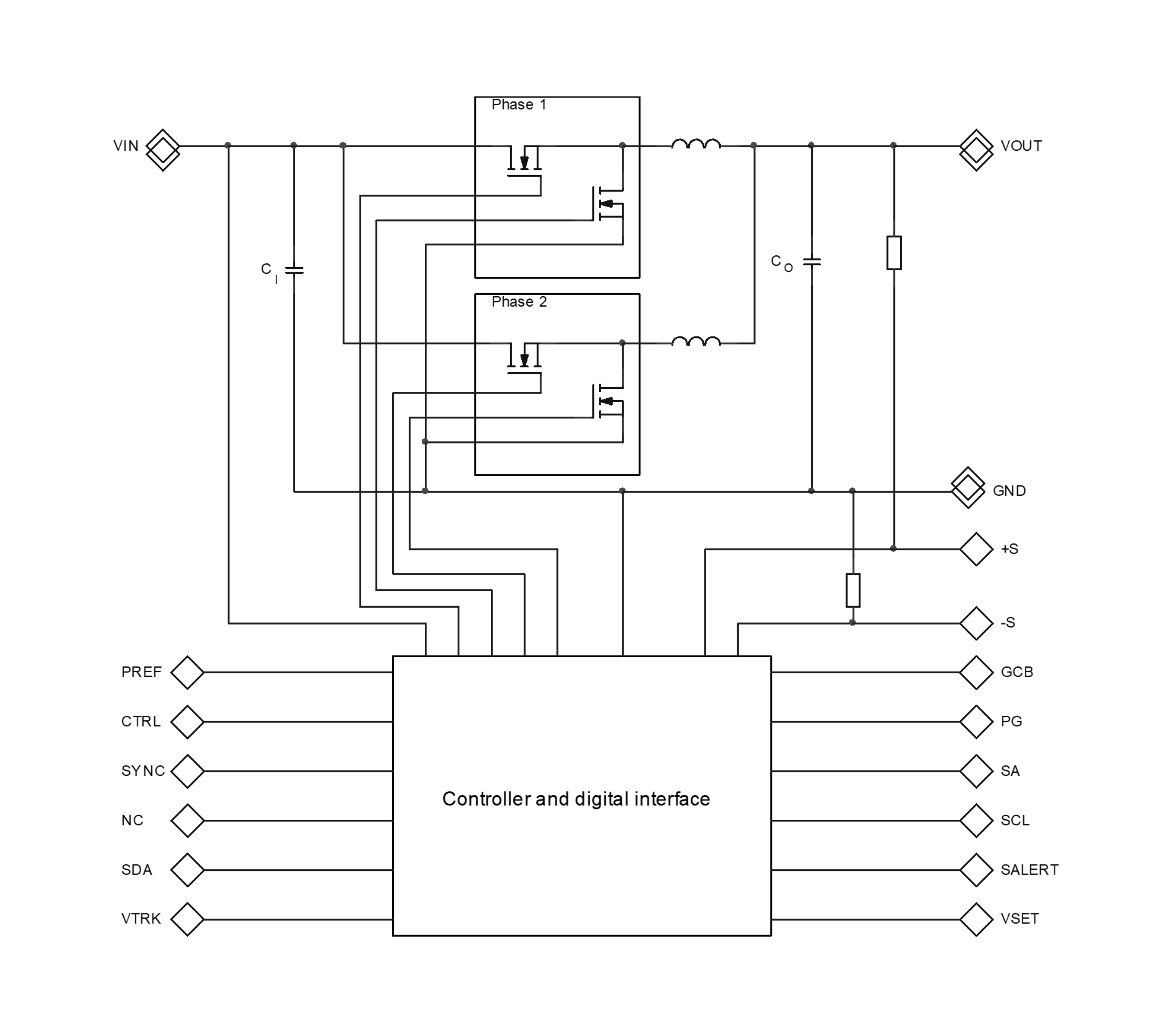
Component power supplies for general use should comply with the requirements in IEC/EN/UL 60950-1 *Safety of Information Technology Equipment.* Product related standards, e.g. IEEE 802.3af *Power over Ethernet*, and ETS-300132-2 *Power interface at the input to telecom equipment, operated by direct current (dc)* are based on IEC/EN/UL 60950-1 with regards to safety.

Flex Power Modules DC/DC converters, Power interface modules and DC/DC regulators are UL 60950-1 recognized and certified in accordance with EN 60950-1. The flammability rating for all construction parts of the products meet requirements for V-0 class material according to IEC 60695-11-10, *Fire hazard testing, test flames* – 50 W horizontal and vertical flame test methods.

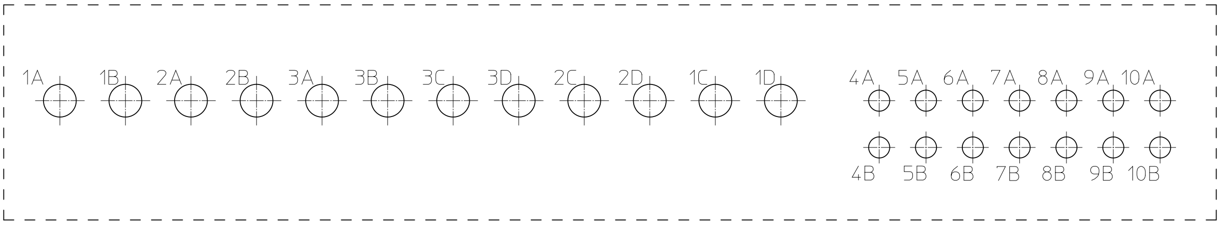
Non - isolated DC/DC regulators

The DC/DC regulator output is SELV if the input source meets the requirements for SELV circuits according to IEC/EN/UL 60950-1.

Internal Circuit Diagram



Pin Descriptions – SIP version

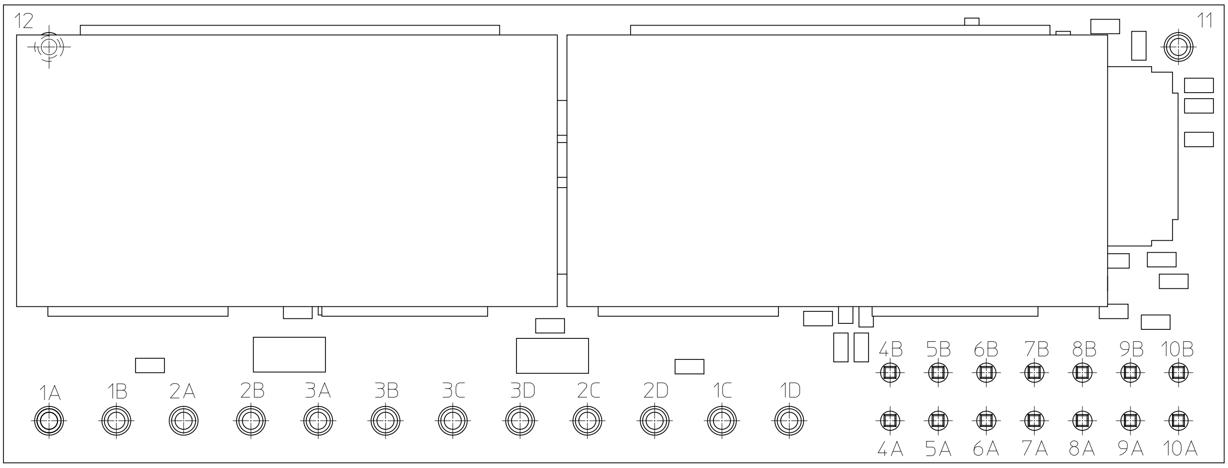


Pin layout, top view.

Pin	Designation	Type	Function
1A, 1B, 1C, 1D	VIN	Power	Input Voltage
2A, 2B, 2C, 2D	GND	Power	Power Ground
3A, 3B, 3C, 3D	VOUT	Power	Output Voltage
4A	+S	I	Positive sense. Connect to output voltage close to the load.
4B	-S	I	Negative sense. Connect to power ground close to the load.
5A	VSET	I	Output voltage pin strap. Used with external resistor to set the nominal output voltage.
5B	VTRK	I	Voltage Tracking input. Allows for tracking of output voltage to an external voltage.
6A	SALERT	O Open-Drain	PMBus Alert. Asserted low when any of the configured protection mechanisms indicate a fault or a warning.
6B	SDA	I/O	PMBus Data. Data signal for PMBus communication. Requires a pull-up resistor even when unused.
7A	SCL	I/O	PMBus Clock. Clock for PMBus communication. Requires a pull-up resistor even when unused.
7B	NC	N/A	Not Connected. See Note 1.
8A	SA	I	PMBus address pin strap. Used with external resistor to assign a unique PMBus address to the product. May be left open if PMBus is not used.
8B	SYNC	I/O	External switching frequency synchronization input or output. May be left open if unused.
9A	PG	O Open-Drain	Power Good output. Asserted high when the product is ready to provide regulated output voltage to the load.
9B	CTRL	I	Remote Control. Can be used to enable/disable the output voltage of the product. May be left open if unused due to internal pull-up.
10A	GCB	I/O	Group Communication Bus. Used for current sharing, and inter-device communication.
10B	PREF	Power	Pin-strap reference. Ground reference for pin-strap resistors.

Note 1. The BMR 467 is pin to pin compatible with the BMR 465 except pin 7B. The pin 7B in BMR 467 is not connected while in BMR 465 it is used to indicate fault in parallel operation. In parallel operation, if desired to be compatible with the BMR 465, Pin 7B of the BMR 467 modules have to be connected together in layout.

Pin Descriptions – Lay Down versions



Pin layout, top view (component placement for illustration only).

Pin	Designation	Type	Function
1A, 1B, 1C, 1D	VIN	Power	Input Voltage
2A, 2B, 2C, 2D	GND	Power	Power Ground
3A, 3B, 3C, 3D	VOUT	Power	Output Voltage
4A	+S	I	Positive sense. Connect to output voltage close to the load.
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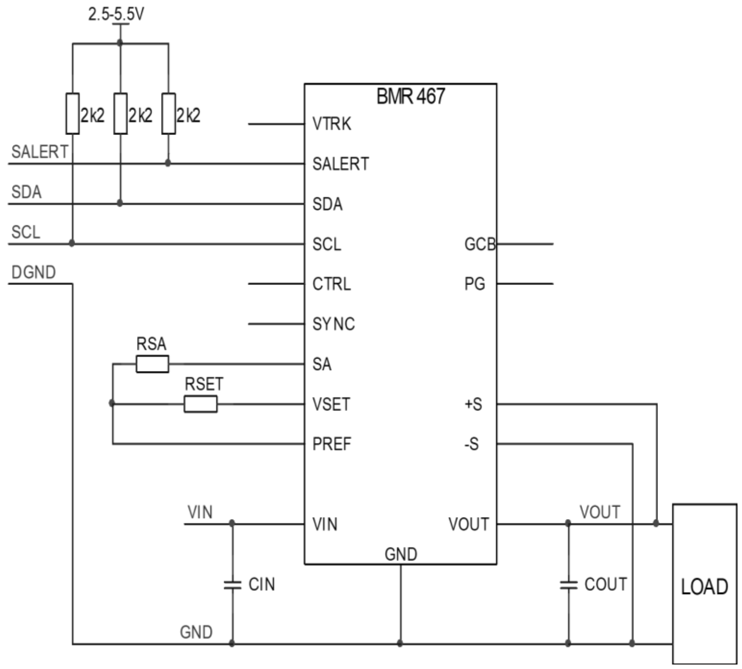
6A	SALERT	O Open-Drain	PMBus Alert. Asserted low when any of the configured protection mechanisms indicate a fault or a warning.
6B	SDA	I/O	PMBus Data. Data signal for PMBus communication. Requires a pull-up resistor even when unused.
7A	SCL	I/O	PMBus Clock. Clock for PMBus communication. Requires a pull-up resistor even when unused.
7B	NC	N/A	Not Connected. See Note 2.
8A	SA	I	PMBus address pin strap. Used with external resistor to assign a unique PMBus address to the product. May be left open if PMBus is not used.
8B	SYNC	I/O	External switching frequency synchronization input or output. May be left open if unused.
9A	PG	O Open-Drain	Power Good output. Asserted high when the product is ready to provide regulated output voltage to the load.
9B	CTRL	I	Remote Control. Can be used to enable/disable the output voltage of the product. May be left open if unused due to internal pull-up.
10A	GCB	I/O	Group Communication Bus. Used for current sharing, and inter-device communication.
10B	PREF	Power	Pin-strap reference. Ground reference for pin-strap resistors.
11, 12	GND	Power	Power Ground. These pins are available only in lay down versions. See Note 2.

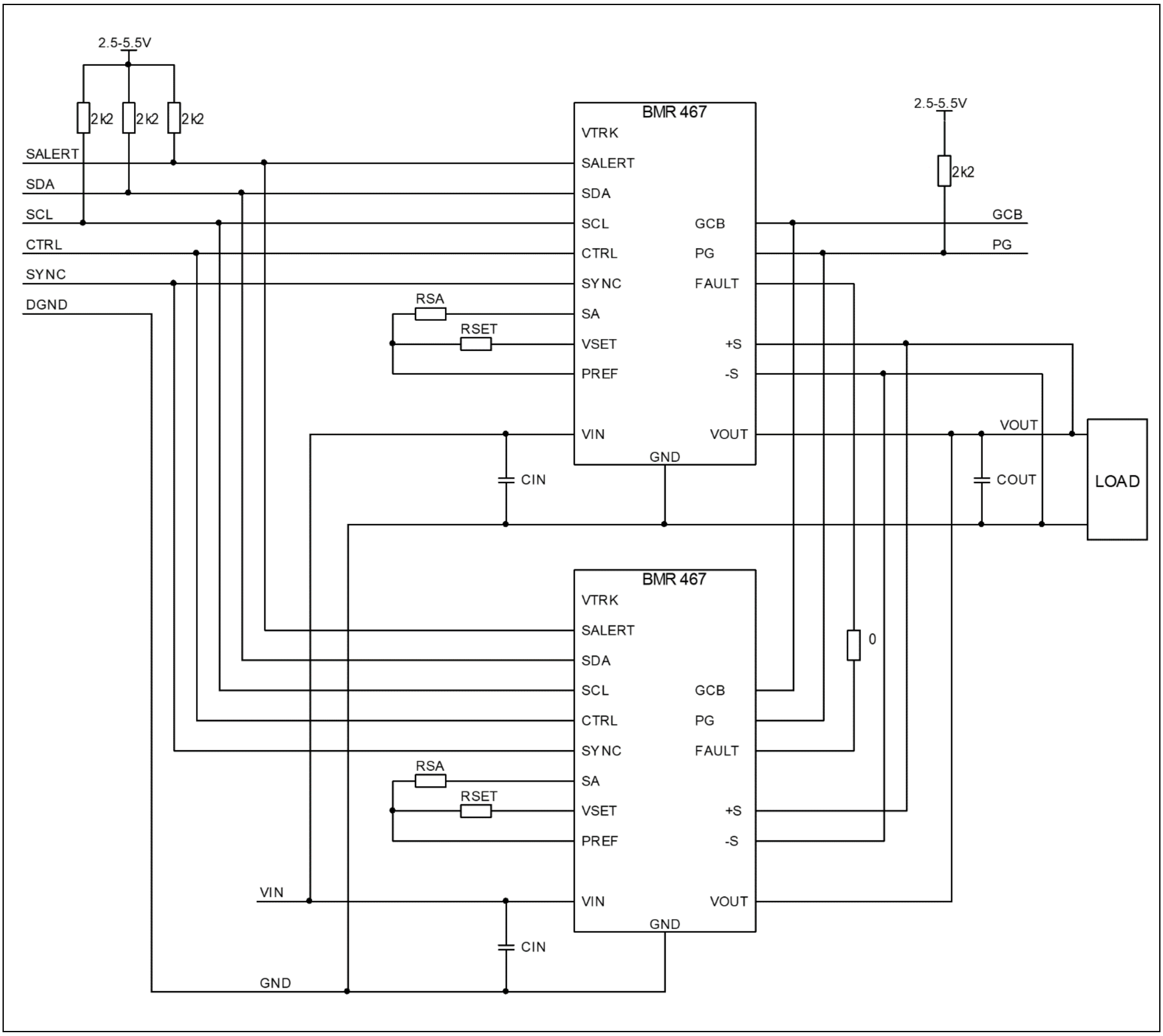
Note 2. The BMR 467 is pin to pin compatible with the BMR 465 except pin 7B. The pin 7B in BMR 467 is not connected while in BMR 465 it is used to indicate fault in parallel operation. In parallel operation, if desired to be compatible with the BMR 465, Pin 7B of the BMR 467 modules have to be connected together in layout. Pins 11 and 12 are not connected in the BMR 465 however they should be connected to the power GND in the BMR 467 case for thermal reasons.

Typical Application Circuit



Standalone operation with PMBus communication.

Typical Application Circuit – Parallel Operation



Parallel operation.

Absolute Maximum Ratings

Characteristics		min	typ	max	Unit
T_{P1}	Operating temperature	-45		125	°C
T_S	Storage temperature (Ambient)	-45		125	°C
V_I	Input voltage (See Operating Information Section for input and output voltage relations)	-0.3		16	V
Signal I/O voltage	CTRL, SA, SALERT, SCL, SDA, VSET, SYNC, PG, GCB	-0.3		6	V
Ground voltage differential	-S, PREF, GND	-0.3		0.3	V
Analog pin voltage	V_O, +S, VTRK	-0.3		6.5	V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the Electrical Specification section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. See technical paper TP023 for details on how data retention time of the Non-Volatile Memory (NVM) of the product is affected by high temperature.

Configuration File

This product is designed with a digital control circuit. The control circuit uses a configuration file which determines the functionality and performance of the product. The Electrical Specification table shows parameter values of functionality and performance with the Standard configuration, unless otherwise specified. The Standard configuration is designed to fit most application needs. Changes in Standard configuration might be required to optimize performance in specific application. Note that current sharing operation requires changed configuration. See application note AN307 for further information.

Common Electrical Specification

This section includes parameter specifications common to all product versions within the product series. Typically these are parameters defined by the digital controller of the products. In the table below PMBus commands for configurable parameters are written in capital letters.

T_{P1} = -40 to +95 °C, V_I = 7.5 to 14 V, unless otherwise specified under Conditions.
Typical values given at: T_{P1} = +25 °C, V_I = 12 V, max I_O, unless otherwise specified under Conditions.
V_O defined by pin-strap. Typical values for PMBus configurable parameters are given for standard (default) configuration.

Characteristics		Conditions	min	typ	max	Unit
f_{SW} = $1/T_{SW}$	Switching Frequency			320		kHz
	Switching Frequency Range, Note 3	PMBus configurable FREQUENCY_SWITCH	200		640	kHz
	Switching Frequency Set-point Accuracy		-5		5	%
	External Sync Pulse Width		150			ns
	Input Clock Frequency Drift Tolerance	External sync	-10		10	%

T_{INIT}	Initialization Time	From V_I > ~2.7 V to ready to be enabled		67	72	ms
T_{ONdel_tot}	Output voltage Total On Delay Time	Enable by input voltage		T_{INIT} + T_{ONdel}		
		Enable by CTRL pin		T_{ONdel}		
T_{ONdel}	Output voltage On Delay Time	Turn on delay duration		5		ms
		Range PMBus configurable TON_DELAY	3		250	ms
		Accuracy (actual delay vs set value)		-0/+2		ms
T_{OFFdel}	Output voltage Off Delay Time	Turn off delay duration, Note 4		0		ms
		Range PMBus configurable TOFF_DELAY	4		250	ms
		Accuracy (actual delay vs set value), Note 5		-0/+2		ms
T_{ONrise} / $T_{OFFfall}$	Output voltage On/Off Ramp Time (0-100%-0 of V_O)	Turn on ramp duration		5		ms
		Turn off ramp duration	Disabled in standard configuration. Turn off immediately upon expiration of Turn off delay.			
		Ramp duration range PMBus configurable TON_RISE/TOFF_FALL	0		100	ms

		Ramp time accuracy for standalone operation (actual ramp time vs set value)		±250		µs
Characteristics		**Conditions**	**min**	**typ**	**max**	**Unit**
Power Good , PG	PG threshold	Rising		90		% V_O
		Falling		85		% V_O
	PG thresholds range	PMBus configurable POWER_GOOD_ON VOUT_UV_FAULT_LIMIT	0		100	% V_O
	PG delay	From V_O reaching target to PG assertion		2		ms
	PG delay range	PMBus configurable POWER_GOOD_DELAY	0		5000	ms

Input Under Voltage Protection, IUVP	IUVP threshold			6.6		V
	IUVP threshold range	PMBus configurable VIN_UV_FAULT_LIMIT	6.6		14	V
	IUVP hysteresis			0.5		V
	IUVP hysteresis range	PMBus configurable VIN_UV_WARN_LIMIT	0		7.4	V
	Set point accuracy		-280		280	mV
	IUVP response delay			100		µs
	Fault response	VIN_UV_FAULT_RESPONSE	Shutdown, automatic restart, 280 ms. Note 6			
Input Over Voltage Protection, IOVP	IOVP threshold			16		V
	IOVP threshold range	PMBus configurable VIN_OV_FAULT_LIMIT	7.1		16	V
	IOVP hysteresis			1		V
	IOVP hysteresis range	PMBus configurable VIN_OV_WARN_LIMIT	0		8.9	V
	Set point accuracy		-280		280	mV
	IOVP response delay			100		µs
	Fault response	VIN_OV_FAULT_RESPONSE	Shutdown, automatic restart, 280 ms. Note 6			
Output Voltage Over/Under Voltage Protection, OVP/UVP	UVP threshold			85		% V_O
	UVP threshold range	PMBus configurable VOUT_UV_FAULT_LIMIT	0		100	% V_O
	OVP threshold			115		% V_O
	OVP threshold range	PMBus configurable VOUT_OV_FAULT_LIMIT	100		115	% V_O
	UVP/OVP response time			10		µs
	Fault response	VOUT_UV_FAULT_RESPONSE VOUT_OV_FAULT_RESPONSE	Shutdown, automatic restart, 280 ms. Note 6			
Over Current Protection, OCP Note 7	OCP threshold	Set value per phase		76		A
	OCP threshold range	PMBus configurable IOUT_AVG_OC_FAULT_LIMIT	0		76	A
	Protection delay	See Note 8		5		T_{SW}
	Fault response	MFR_IOUT_OC_FAULT_RESPONSE	Shutdown, automatic restart, 280 ms. Note 6			
Over Temperature Protection, OTP Position P1 Note 9	OTP threshold			125		°C
	OTP threshold range	PMBus configurable OT_FAULT_LIMIT	-45		125	°C
	OTP hysteresis	PMBus configurable		15		°C
	Fault response	OT_FAULT_RESPONSE	Shutdown, automatic restart, 280 ms. Note 6			

Characteristics		Conditions	min	typ	max	Unit
Monitoring Accuracy	Input voltage READ_VIN		-280		280	mV
	Output voltage READ_VOUT		-1.25	±1	1.25	% V_O
	Output current READ_IOUT, Note 10	T_{P1} = 25 °C, V_O = 1.0 V	-4	±2.5	4	A
		T_{P1} = 0 - 95 °C, V_O = 1.0 V	-7	±5.0	7	A
	Duty cycle READ_DUTY_CYCLE		No tolerance, Read value is the actual value applied by PWM controller.			
	Temperature READ_TEMPERATURE_1	Position P1, T_{P3} = 0 - 95 °C	-10		5	°C

Tracking Input Bias Current	VTRK = 5 V		70	200	µA
Tracking Input Voltage Range	VTRK pin	0		5	V
Tracking Rise-Time	VTRK pin			1	V/ms
Tracking Accuracy	Regulation 100% tracking	-2		2	% V_O

Current difference between products in a current sharing group	Steady state operation	Max 2 x READ_IOUT monitoring accuracy			
Supported number of products in a current sharing group				4	

V_{OL}	Logic output low signal level	SCL, SDA, SYNC, GCB, SALERT, PG Sink/source current = 2 mA			0.5	V
V_{OH}	Logic output high signal level		2.25			V
I_{OL}	Logic output low sink current				2	mA
I_{OH}	Logic output high source current				2	mA
V_{IL}	Logic input low	SCL, SDA, CTRL, SYNC, GCB			0.8	V
V_{IH}	Logic input high		2			V
I_{I_LEAK}	Logic leakage current	SCL, SDA, SYNC, SALERT, PG	-100		100	nA
C_{I_PIN}	Logic pin input capacitance	SCL, SDA, CTRL, SYNC, GCB		12		pF
R_{I_PU}	Logic pin internal pull-up resistance	SCL, SDA, SALERT		No internal pull-up		
		CTRL to +5V		10		kΩ
		GCB to +5V		47		kΩ
f_{SMB}	Supported SMBus Operating frequency		10		400	kHz
T_{BUF}	SMBus Bus free time	STOP bit to START bit	1.3			µs
t_{set}	SMBus SDA setup time from SCL		100			ns
t_{hold}	SMBus SDA hold time from SCL		300			ns
	SMBus START/STOP condition setup/hold time from SCL		600			ns
T_{low}	SCL low period		1.3			µs
T_{high}	SCL high period		0.6			µs

Note 3. There are configuration changes to consider when changing the switching frequency. The switching frequency below 320 kHz is not recommended due to increased ripple current.
Note 4. A default value of 0 ms forces the device to Immediate Off behavior with TOFF_FALL ramp-down setting being ignored.
Note 5. The specified accuracy applies for off delay times larger than 4 ms. When setting 0 ms the actual delay will be 0 ms.
Note 6. Automatic restart ~280 ms after fault if the fault is no longer present. Continuous restart attempts if the fault reappear after restart.
Note 7. The set OCP limit applies per phase. The total OCP limit will be twice the set value. Note that higher OCP threshold than specified may result in damage of the module at OC fault conditions.
Note 8. T_{SW} is the switching period.
Note 9. See section Over Temperature Protection (OTP).
Note 10. Monitoring Accuracy of output current is optimized for V_I = 12 V and V_O = 1.0 V.

Product Electrical Specification

BMR 467 0010, BMR 467 1010
BMR 467 2010, BMR 467 2110

T_{P1} = -40 to +95 °C, V_I = 7.5 to 14 V, unless otherwise specified under Conditions.
Typical values given at: T_{P1} = +25 °C, V_I = 12.0 V, max I_O, unless otherwise specified under Conditions.
V_O defined by pin strap. Standard configuration.
Tested with external C_{IN} = 1000 µF/12 mΩ OS-CON + 24 x 10 µF Ceramic, C_{OUT} = 10 x 470 µF/5 mΩ POS-CAP + 10 x 100 µF Ceramic.
In the test set-up sense lines are connected directly to output pins on a converter and all the output voltage measurements are made on output pins.

Characteristics			Conditions	min	typ	max	Unit
V_I	Input voltage			7.5		14	V
	Input voltage slew rate		Monotonic			6	V/ms

V_O	Output voltage without pin-strap				1.2		V
	Output voltage adjustment range			0.6		1.8	V
	Output voltage adjustment including PMBus margining			0.54		1.98	V
	Output voltage set-point resolution				±0.025		% V_O
	Output voltage accuracy, Note 11		Including line, load, temp	-1		1	% V_O
	Internal resistance +S/-S to VOUT/GND				47		Ω
	+S bias current			-100	20	100	µA
	-S bias current				20		µA
	Line regulation	I_O = max I_O	V_O = 0.6 V		1		mV
			V_O = 1.0 V		1		
			V_O = 1.8 V		1		
	Load regulation	I_O = 0 - 100%	V_O = 0.6 V		1		mV
			V_O = 1.0 V		1		
			V_O = 1.8 V		1		
V_{Oac}	Output ripple & noise (up to 20 MHz bandwidth)		V_O = 0.6 V		4.5		mVp-p
			V_O = 1.0 V		5.0		
			V_O = 1.8 V		7.0		

I_O	Output current			0		120	A
I_{lim}	Current limit threshold			130	145	150	A
I_{sc}	Short circuit current		RMS, hiccup mode, V_O = 1.0 V, 1.5 mΩ short		12.5		A

η	Efficiency	50% of max I_O	V_O = 0.6 V		86.5		%
			V_O = 1.0 V		90.5		
			V_O = 1.8 V		93.2		
		I_O = max I_O	V_O = 0.6 V		83.5		%
			V_O = 1.0 V		88.6		
			V_O = 1.8 V		91.9		
P_d	Power dissipation at max I_O		V_O = 0.6 V		14.2	18.0	W
			V_O = 1.0 V		15.5	19.5	
			V_O = 1.8 V		19.0	23.5	
P_{li}	Input idling power	I_O = 0	V_O = 0.6 V		2.0		W
			V_O = 1.0 V		2.5		
			V_O = 1.8 V		3.5		
P_{CTRL}	Input standby power		Turned off with CTRL-pin		0.44		W
C_I	Internal input capacitance		V_I = 0 V		279		µF
C_O	Internal output capacitance		V_O = 0 V		700		µF

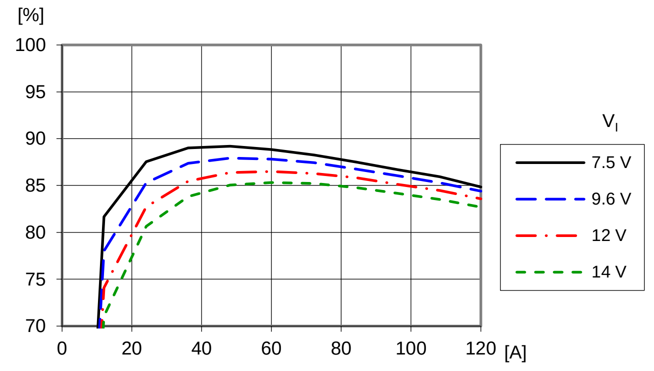
Note 11. For V_O < 1.0 V accuracy is +/-10 mV.

Typical Output Characteristics, V_O = 0.6 V

Standard configuration unless otherwise specified, T_{P1}=+25 °C

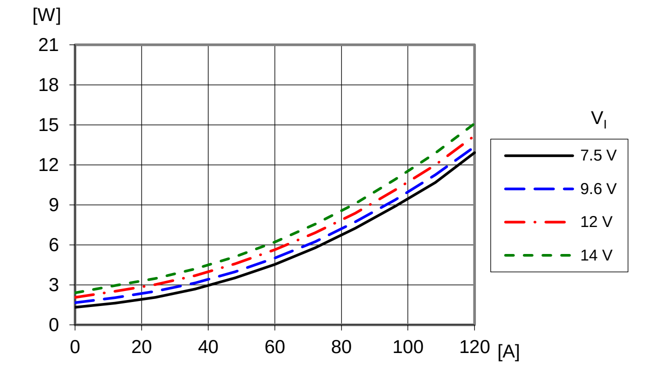
BMR 467 0010, BMR 467 1010
BMR 467 2010, BMR 467 2110

Efficiency



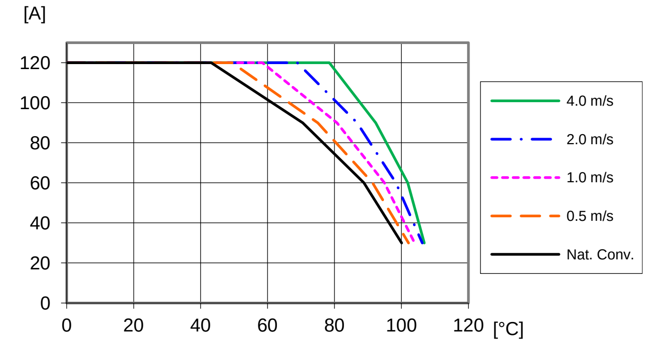
Efficiency vs. load current and input voltage.

Power Dissipation



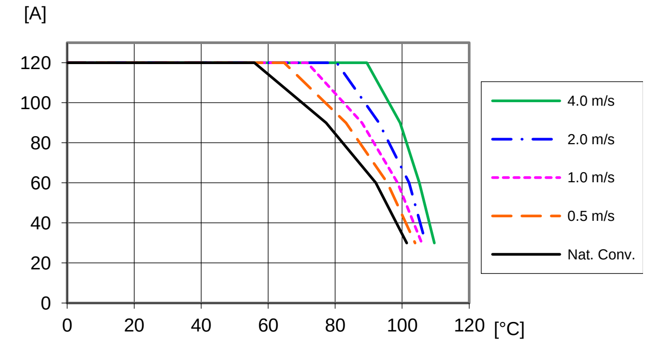
Dissipated power vs. load current and input voltage.

Output Current Derating for SIP version



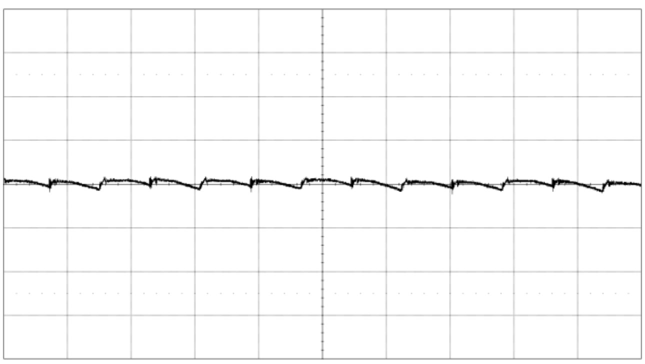
Available load current vs. ambient air temperature and airflow at V_I = 12 V.

Output Current Derating for Lay Down versions



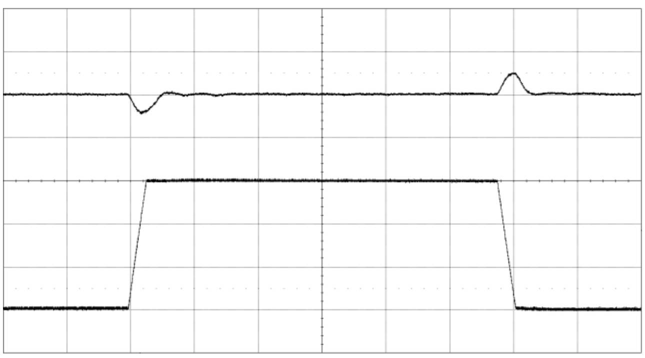
Available load current vs. ambient air temperature and airflow at V_I = 12 V.

Output Ripple and Noise



Fundamental output voltage ripple at V_I = 12 V, I_O = max I_O,
C_{OUT} = 10 x 470 µF/5 mΩ + 10 x 100 µF.
Scale: 10 mV/div, 2 µs/div, 20 MHz bandwidth.
See section Output Ripple and Noise.

Transient Response



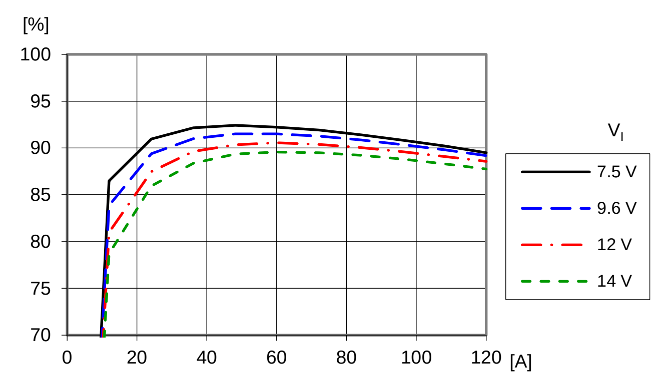
Output voltage response to load current step change (30–90–30 A) at
V_I = 12 V, C_{OUT} = 10 x 470 µF/5 mΩ + 10 x 100 µF, di/dt = 2 A/µs,
ASCR Gain = 300 and ASCR Residual = 90.
Scale from top: 50 mV/div, 20 A/div, 100 µs/div.
Note: Sense pins are connected to load.

Typical Output Characteristics, V_O = 1.0 V

Standard configuration unless otherwise specified, T_{P1}=+25 °C

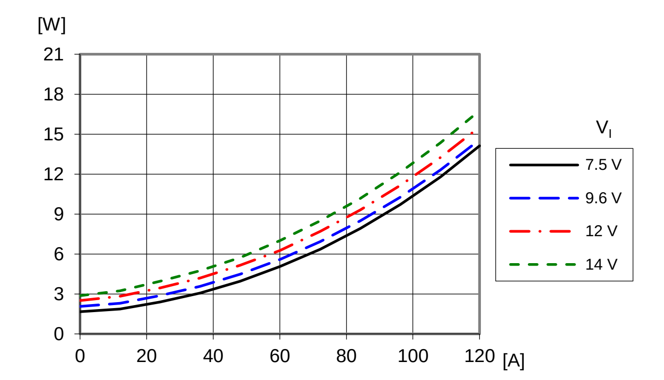
BMR 467 0010, BMR 467 1010
BMR 467 2010, BMR 467 2110

Efficiency



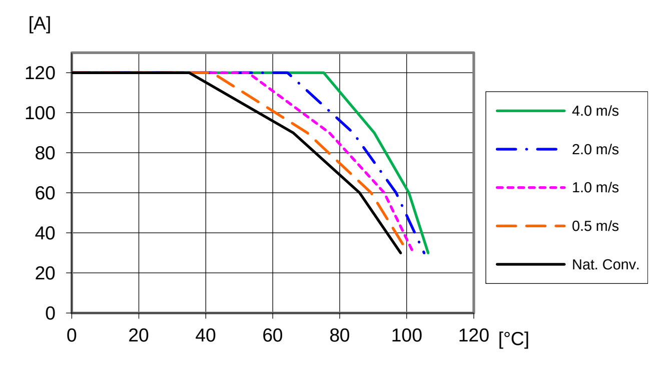
Efficiency vs. load current and input voltage.

Power Dissipation



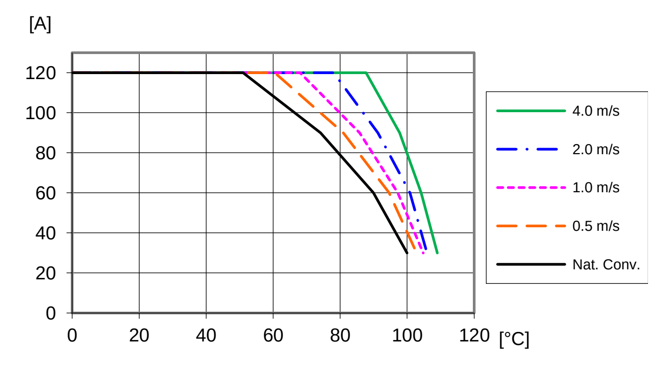
Dissipated power vs. load current and input voltage.

Output Current Derating for SIP version



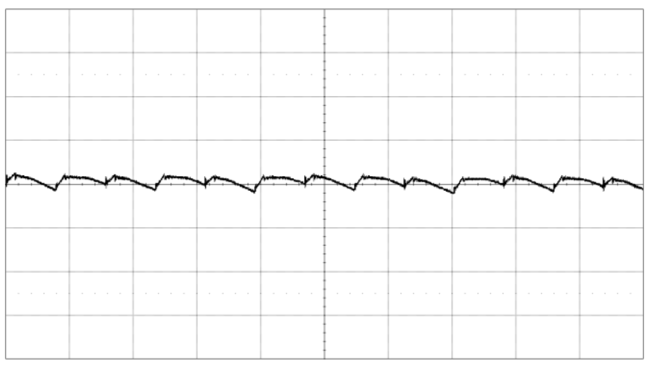
Available load current vs. ambient air temperature and airflow at V_I = 12 V.

Output Current Derating for Lay Down versions



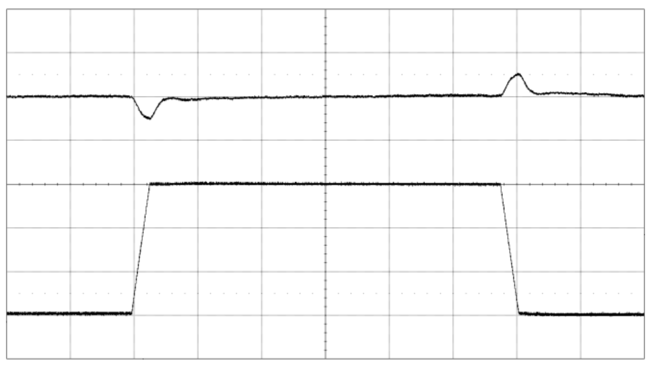
Available load current vs. ambient air temperature and airflow at V_I = 12 V.

Output Ripple and Noise



Fundamental output voltage ripple at V_I = 12 V, I_O = max I_O,
C_{OUT} = 10 x 470 µF/5 mΩ + 10 x 100 µF.
Scale: 10 mV/div, 2 µs/div, 20 MHz bandwidth.
See section Output Ripple and Noise.

Transient Response



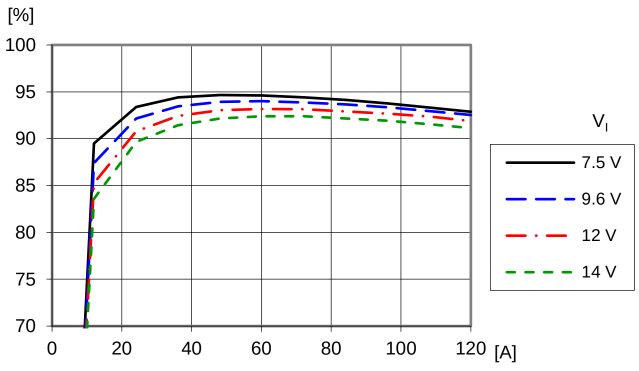
Output voltage response to load current step change (30–90–30 A) at
V_I = 12 V, C_{OUT} = 10 x 470 µF/5 mΩ + 10 x 100 µF, di/dt = 2 A/µs,
ASCR Gain = 300 and ASCR Residual = 90.
Scale from top: 50 mV/div, 20 A/div, 100 µs/div.
Note: Sense pins are connected to load.

Typical Output Characteristics, V_O = 1.8 V

Standard configuration unless otherwise specified, T_{P1}=+25 °C

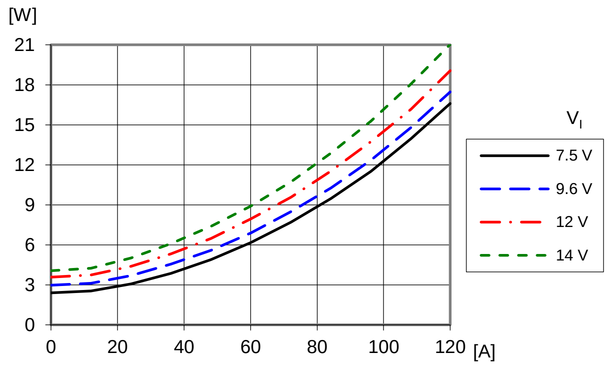
BMR 467 0010, BMR 467 1010
BMR 467 2010, BMR 467 2110

Efficiency



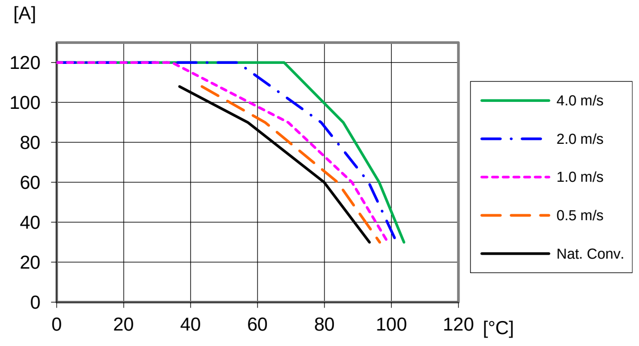
Efficiency vs. load current and input voltage.

Power Dissipation



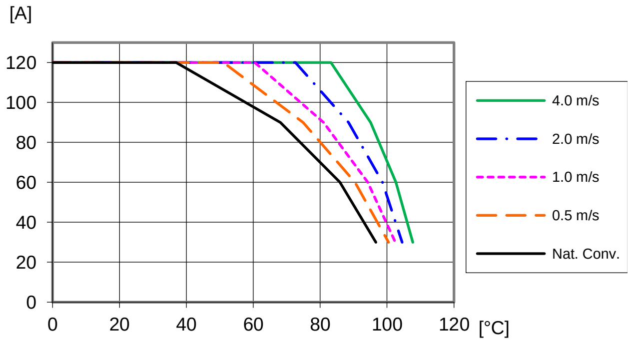
Dissipated power vs. load current and input voltage.

Output Current Derating for SIP version



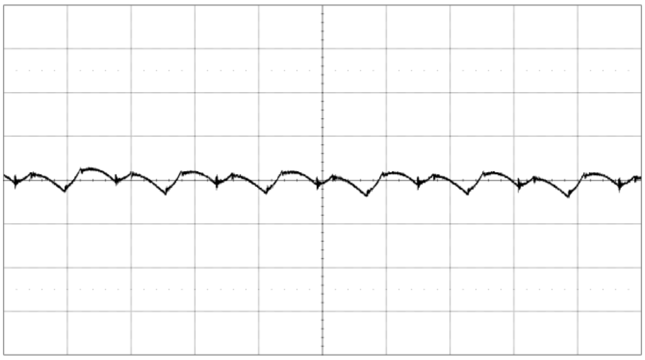
Available load current vs. ambient air temperature and airflow at V_I = 12 V.

Output Current Derating for Lay Down versions



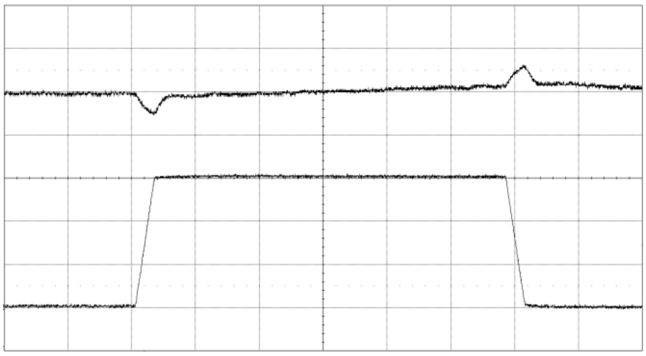
Available load current vs. ambient air temperature and airflow at V_I = 12 V.

Output Ripple and Noise



Fundamental output voltage ripple at V_I = 12 V, I_O = max I_O,
C_{OUT} = 10 x 470 µF/5 mΩ + 10 x 100 µF.
Scale: 10 mV/div, 2 µs/div, 20 MHz bandwidth.
See section Output Ripple and Noise.

Transient Response

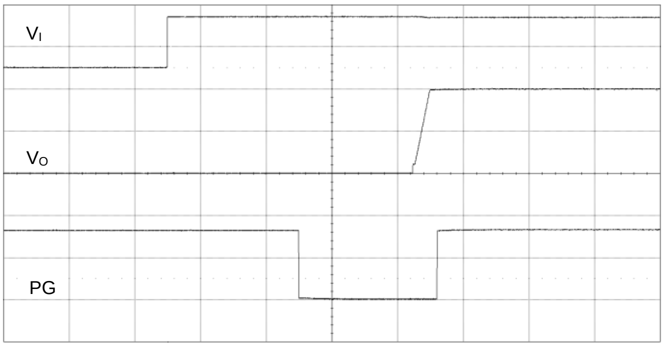


Output voltage response to load current step change (30–90–30 A) at
V_I = 12 V, C_{OUT} = 10 x 470 µF/5 mΩ + 10 x 100 µF, di/dt = 2 A/µs,
ASCR Gain = 300 and ASCR Residual = 90.
Scale from top: 50 mV/div, 20 A/div, 100 µs/div.
Note: Sense pins are connected to load.

Typical On/Off Characteristics
Standard configuration, T_{P1} = +25 °C, V_O = 1.0 V

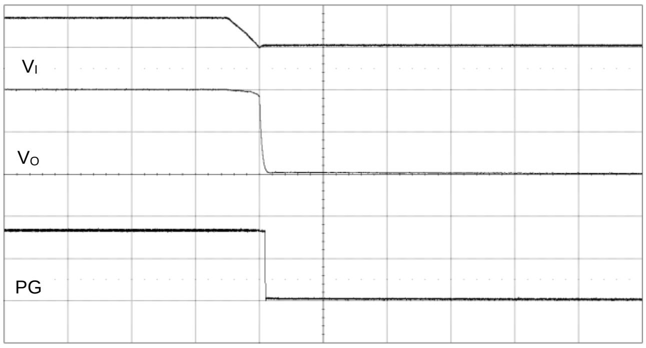
BMR 467 0010, BMR 467 1010
BMR 467 2010, BMR 467 2110

Enable by input voltage – PG Open-Drain (default)



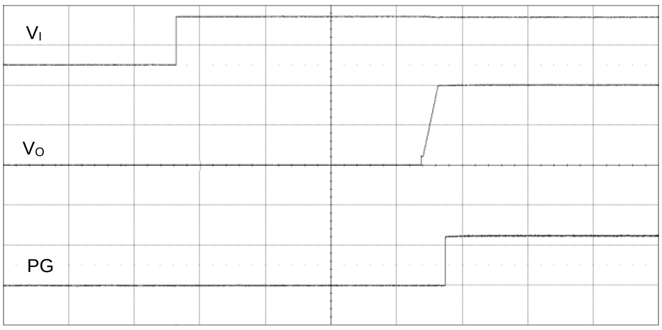
Output enabled by applying V_I. V_I = 12 V, I_O = max I_O.
TON_DELAY = TON_RISE = 5 ms, POWER_GOOD_DELAY = 2 ms.
USER_CONFIG = 0x1480 (default). PG pulled up to external voltage.
Note: PG being high before Vin applied can be avoided by pulling up PG to Vout.
Scale from top: 10, 0.5, 2 V/div, 20 ms/div.

Disable by input voltage – PG Open-Drain (default)



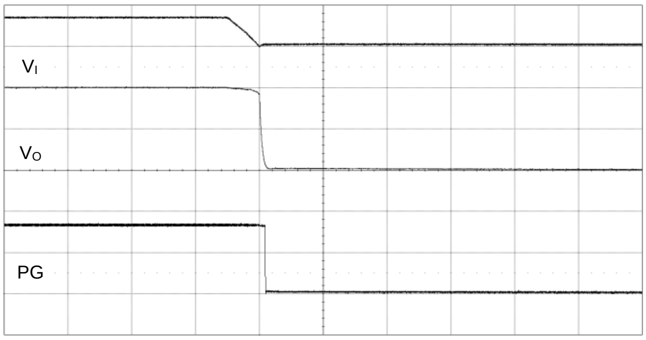
Output disabled by removing V_I. V_I = 12 V, I_O = max I_O.
Scale from top: 10, 0.5, 2 V/div, 1 ms/div.

Enable by input voltage – PG Push-Pull



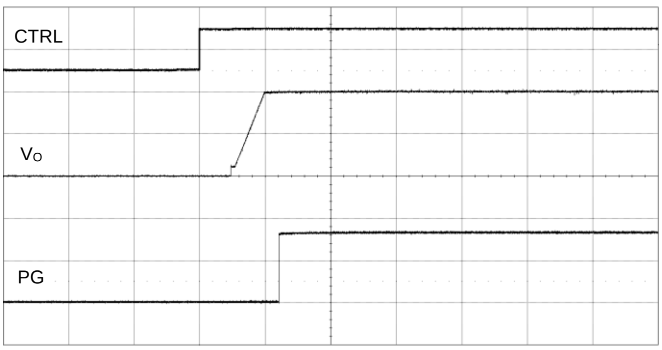
Output enabled by applying V_I. V_I = 12 V, I_O = max I_O.
TON_DELAY = TON_RISE = 5 ms, POWER_GOOD_DELAY = 2 ms.
USER_CONFIG = 0x1484 (PG push-pull).
Scale from top: 10, 0.5, 2 V/div, 20 ms/div.

Disable by input voltage – PG Push-Pull



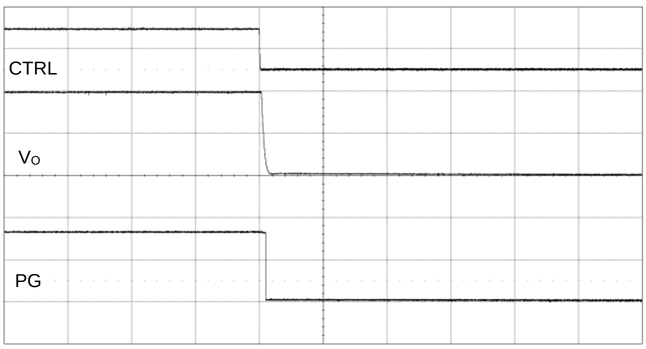
Output disabled by removing V_I. V_I = 12 V, I_O = max I_O.
Scale from top: 10, 0.5, 2 V/div, 1 ms/div.

Enable by CTRL pin



Output enabled by CTRL pin. V_I = 12 V, I_O = max I_O.
TON_DELAY = TON_RISE = 5 ms, POWER_GOOD_DELAY = 2 ms.
Scale from top: 5, 0.5, 2 V/div, 10 ms/div.

Disable by CTRL pin



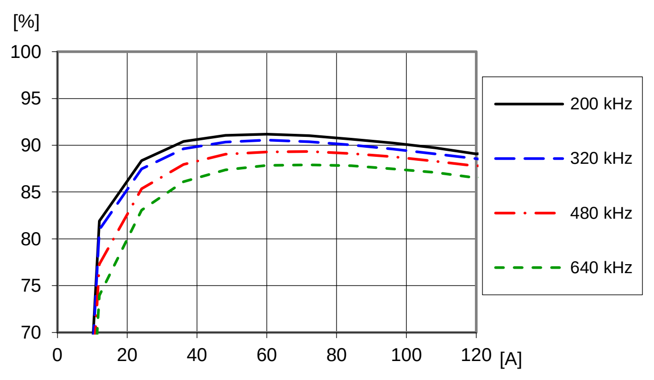
Output disabled by CTRL pin. V_I = 12 V, I_O = max I_O.
Scale from top: 5, 0.5, 2 V/div, 1 ms/div.

Typical Charactersitics

Standard configuration unless otherwise specified, T_{P1}=+25 °C

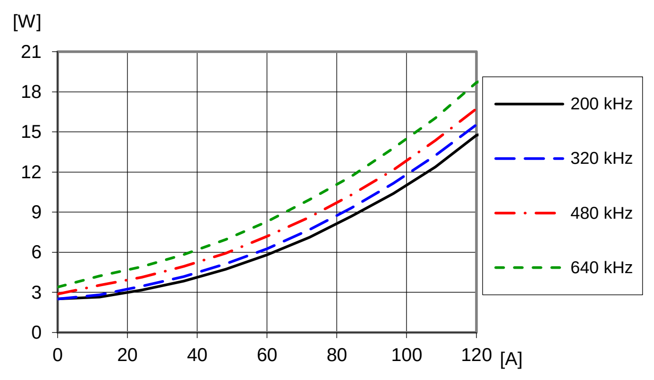
BMR 467 0010, BMR 467 1010
BMR 467 2010, BMR 467 2110

Efficiency vs. Output Current and Switching Frequency



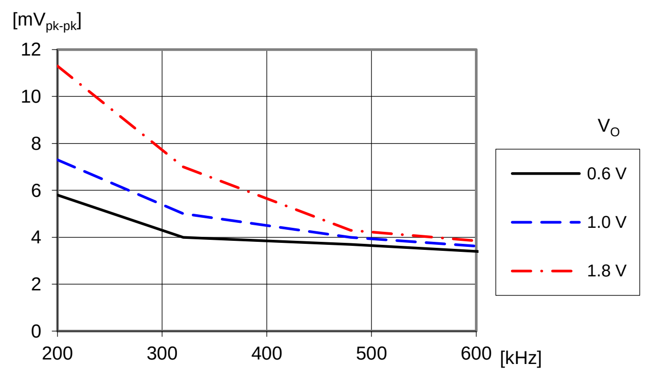
Efficiency vs. load current and switching frequency at
V_I = 12 V, V_O = 1.0 V, C_O = 10 x 470 µF/5 mΩ + 10 x 100 µF.
Frequency changed by PMBus command FREQUENCY_SWITCH.

Power Dissipation vs. Output Current and Switching Frequency



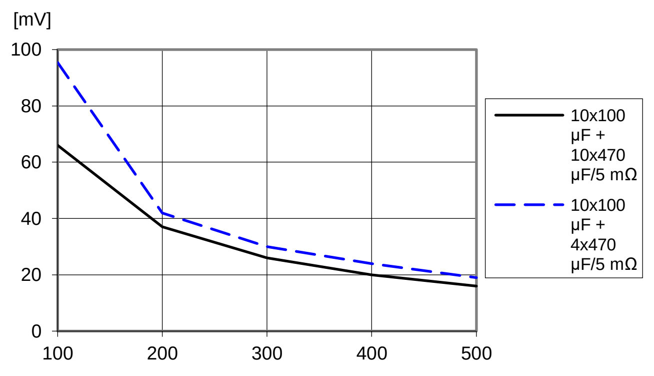
Dissipated power vs. load current and switching frequency at
V_I = 12 V, V_O = 1.0 V, C_O = 10 x 470 µF/5 mΩ + 10 x 100 µF.
Frequency changed by PMBus command FREQUENCY_SWITCH.

Output Ripple vs. Switching Frequency



Output voltage ripple V_{pk-pk} vs. switching frequency at
V_I = 12 V, I_O = max I_O, C_O = 10 x 470 µF/5 mΩ + 10 x 100 µF.
Frequency changed by PMBus command FREQUENCY_SWITCH.

Load Transient vs. ASCR Gain and External Output Capacitance

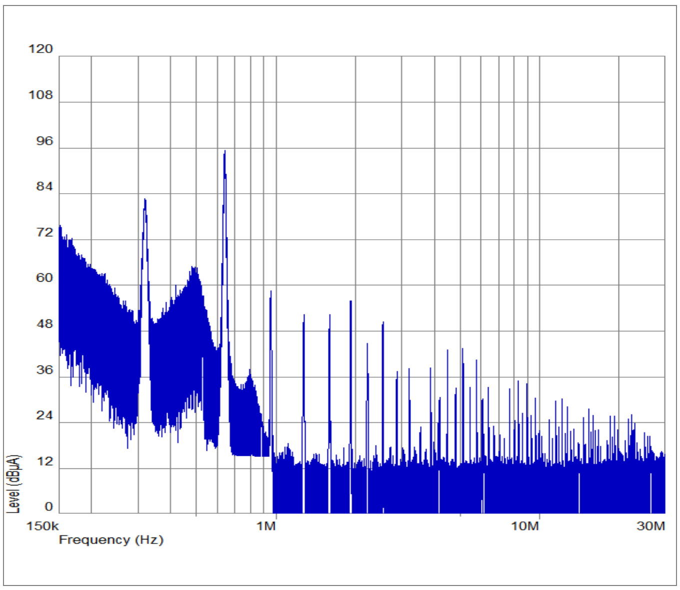


Load transient peak voltage deviation vs. ASCR gain and external capacitance. Step (30–90–30 A).
V_I = 12 V, V_O = 1.0 V, f_{sw} = 320 kHz, ASCR residual =90, di/dt = 2 A/µs.
ASCR gain changed by PMBus command ASCR_CONFIG.

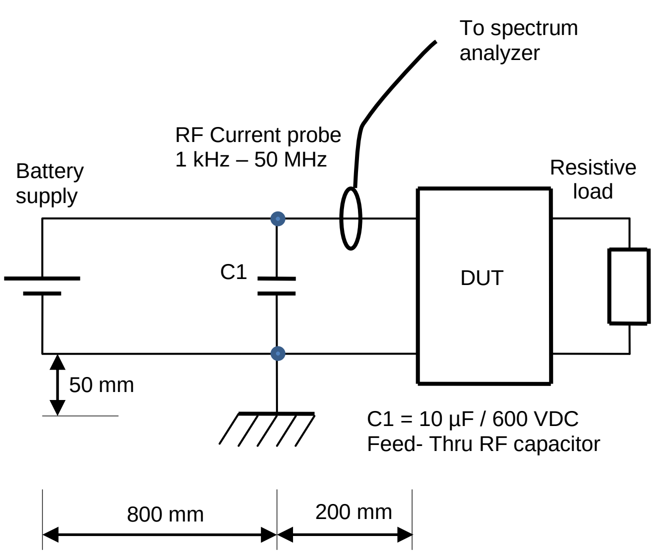
EMC Specification

Conducted EMI is measured according to the test set-up below. The typical fundamental switching frequency is 320 kHz.

Conducted EMI Input terminal value (typical for standard configuration). V_I = 12 V, V_O = 1.0 V, I_O = 120 A.



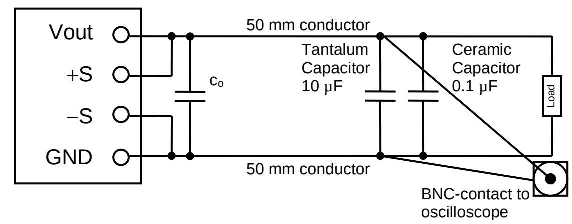
EMI without filter



Test set-up conducted emission, power lead.
DUT = Product mounted on a 182 cm² test board with the external capacitances C_{IN} = 1000 µF/12 mΩ + 24 x 10 µF and C_{OUT} = 10 x 470 µF/5 mΩ + 10 x 100 µF.

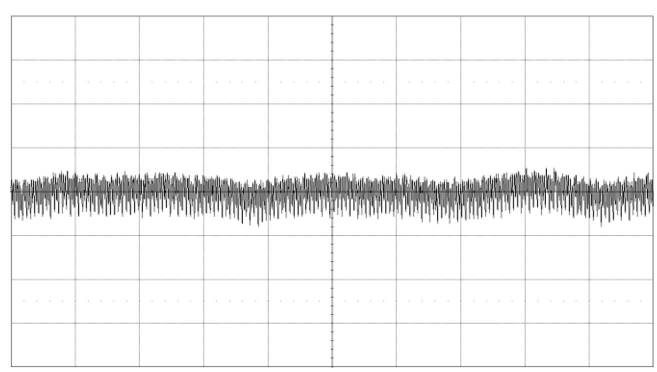
Output Ripple and Noise

Output ripple and noise are measured according to figure below. A 50 mm conductor works as a small inductor forming together with the two capacitances a damped filter.



Output ripple and noise test set-up.

The digital compensation of the product is designed to automatically provide stability, accurate line and load regulation and good transient performance for a wide range of operating conditions (switching frequency, input voltage, output voltage, output capacitance). Inherent from the implementation and normal to the product there will be some low frequency ripple at the output, in addition to the fundamental switching frequency output ripple. The total output ripple and noise is maintained at a low level.



V_I = 12 V, V_O = 1.0 V, I_O = 120 A, C_{OUT} = 10 x 470 µF/5 mΩ + 10 x 100 µF, 5 mV/div, 50 µs/div

Example of low frequency ripple at the output.

PMBus Interface

Power Management Overview

This product incorporates a wide range of configurable power management features that are simple to implement with a minimum of external components. Additionally, the product includes protection features that continuously safeguard the load from damage due to unexpected system faults.

The product's standard configuration is suitable for a wide range of operation in terms of input voltage, output voltage and load. The configuration is stored in an internal Non-Volatile Memory (NVM). All power management functions can be reconfigured using the PMBus interface.

Throughout this document, different PMBus commands are referenced. A detailed description of each command is provided in the appendix at the end of this specification.

The Flex Power Designer software suite can be used to configure and monitor this product via the PMBus interface. For more information please contact your local Flexsales representative.

SMBus Interface

The product can be used with any standard two-wire I²C or SMBus host device. See Electrical Specification for allowed clock frequency range. In addition, the product is compatible with PMBus version 1.2 and includes an SALERT line to help mitigate limitations related to continuous fault monitoring. The PMBus signals SCL, SDA and SALERT require passive pull-up resistors as stated in the SMBus Specification. Pull-up resistors values should be selected to guarantee the rise time according to equation below:

$$\tau = R_P C_p \le 1\,\mu s$$

where R_p is the pull-up resistor value and C_p is the bus loading. The maximum allowed bus load is 400 pF. The pull-up resistor should be tied to an external supply voltage in range from 2.5 to 5.5 V, which should be present prior to or during power-up. If the proper power supply is not available, voltage dividers may be applied. Note that in this case, the resistance in the equation above corresponds to parallel connection of the resistors forming the voltage divider.
See application note AN304 for details on interfacing the product with a microcontroller.

PMBus Addressing

The PMBus address is configured with a resistor connected between the SA pin and the PREF pin, as shown in the Typical Application Circuit. Recommended resistor values are shown in the table below. 1% tolerance resistors are required.

R_{SA} [kΩ]	Address
0 (short)	0x26
10	0x19
11	0x1A
12.1	0x1B
13.3	0x1C
14.7	0x1D
16.2	0x1E
17.8	0x1F
19.6	0x20
21.5	0x21
23.7	0x22
26.1	0x23
28.7	0x24
31.6	0x25
34.8	0x26
38.3	0x27

R_{SA} [kΩ]	Address
42.2	0x28
46.4	0x29
51.1	0x2A
56.2	0x2B
61.9	0x2C
68.1	0x2D
75	0x2E
82.5	0x2F
90.9	0x30
100	0x31
110	0x32
121	0x33
133	0x34
147	0x35
162	0x36
178	0x37
Infinite (open)	0x28

Reserved Addresses

Addresses listed in the table below are reserved or assigned according to the SMBus specification and may not be usable. Refer to the SMBus specification for further information.

Address	Comment
0x00	General Call Address / START byte
0x01	CBUS address
0x02	Address reserved for different bus format
0x03 - 0x07	Reserved for future use
0x08	SMBus Host
0x09 - 0x0B	Assigned for Smart Battery
0x0C	SMBus Alert Response Address
0x28	Reserved for ACCESS.bus host
0x2C - 0x2D	Reserved by previous versions of the SMBus specification
0x37	Reserved for ACCESS.bus default address
0x40 - 0x44	Reserved by previous versions of the SMBus specification
0x48 - 0x4B	Unrestricted addresses
0x61	SMBus Device Default Address
0x78 - 0x7B	10-bit slave addressing
0x7C - 0x7F	Reserved for future use

Monitoring via PMBus

It is possible to continuously monitor a wide variety of parameters through the PMBus interface. These include, but are not limited to, the parameters listed in the table below.

Parameter	PMBus Command
Input voltage	READ_VIN
Output voltage	READ_VOUT
Total output current	READ_IOUT
Output current of each phase	READ_IOUT0 READ_IOUT1
Controller temperature (T_{P1})	READ_TEMPERATURE_1
Switching frequency	READ_FREQUENCY
Duty cycle	READ_DUTY_CYCLE

Monitoring Faults

Fault conditions can be monitored using the SALERT pin, which will be asserted low when any number of pre-configured fault or warning conditions occurs. The SALERT pin will be held low until faults and/or warnings are cleared by the CLEAR_FAULTS command, or until the output voltage has been re-enabled.
It is possible to mask which fault conditions should not assert the SALERT pin by the command MFR_SMBALERT_MASK.

In response to the SALERT signal, the user may read a number of status commands to find out what fault or warning condition occurred, see table below.

Fault & Warning Status	PMBus Command
Overview, Power Good	STATUS_WORD STATUS_BYTE
Output voltage level	STATUS_VOUT
Output current level	STATUS_IOUT
Input voltage level	STATUS_INPUT
Temperature level	STATUS_TEMPERATURE
PMBus communication	STATUS_CML
Miscellaneous	STATUS_MFR_SPECIFIC

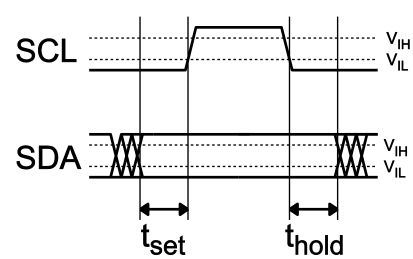
Snapshot Parameter Capture

This product offers a special feature that enables the user to capture parametric data during normal operation by a single PMBus command. The following parameters are stored:

- Input voltage
- Output voltage
- Output current
- Controller temperature
- Switching frequency
- Duty cycle
- Status and fault information

When a fault occurs the Snapshot functionality will automatically store this parametric data to NVM. The data can then later be read back using the SNAPSHOT command to provide valuable information for analysis. It is possible to select which faults will trigger a store to NVM by the PMBus command SNAPSHOT_FAULT_MASK.
See application note AN320 for details on using the Snapshot feature.

PMBus/I²C Timing



Setup and hold times timing diagram.

The setup time, t_{set}, is the time data, SDA, must be stable before the rising edge of the clock signal, SCL. The hold time t_{hold}, is the time data, SDA, must be stable after the falling edge of the clock signal, SCL. If these times are violated incorrect data may be captured or meta-stability may occur and the bus communication may fail. All standard SMBus protocols must be followed, including clock stretching. Refer to the SMBus specification, for SMBus electrical and timing requirements.

This product supports the BUSY flag in the status commands to indicate product being too busy for SMBus response. A bus-free time delay according to this specification must occur between every SMBus transmission (between every stop & start condition).
The product supports PEC (Packet Error Checking) according to the SMBus specification.

When sending subsequent commands to the same module, it is recommended to insert additional delays according to the table below.

After sending PMBus Command	Required delay before additional command
STORE_USER_ALL	100 ms
STORE_DEFAULT_ALL	
RESTORE_USER_ALL	100 ms
RESTORE_DEFAULT_ALL	
VOUT_MAX	10 ms
Any other command	2 ms after reading 10 ms after writing

Non-Volatile Memory (NVM)

The product incorporates two Non-Volatile Memory areas for storage of the PMBus command values; the Default NVM and the User NVM.
The Default NVM is pre-loaded with Flexfactory default values. The Default NVM is write-protected and can be used to restore the Flexfactory default values through the command RESTORE_DEFAULT_ALL.
The User NVM is pre-loaded with Flexfactory default values. The User NVM is writable and open for customization. The values in NVM are loaded during initialization according to section Initialization Procedure, whereafter commands can be changed through the PMBus Interface. The STORE_USER_ALL command will store the changed parameters to the User NVM.

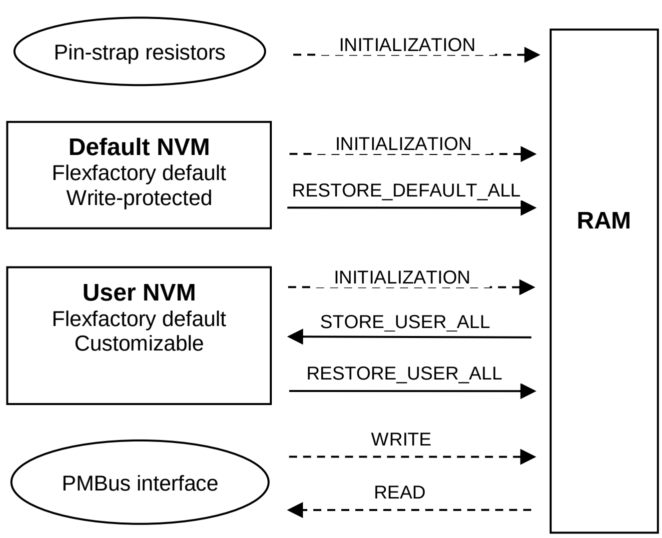


Illustration of memory areas of the product.

Command Protection

The user may write-protect specific PMBus commands in the User NVM by using the command UNPROTECT.

Initialization Procedure

The product follows an internal initialization procedure after power is applied to the VIN pins:

1. Self-test and memory check.
2. The address pin-strap resistors are measured and the associated PMBus address is defined.
3. The output voltage pin-strap resistor is measured and the associated output voltage level will be loaded to operational RAM of PMBus command VOUT_COMMAND.
4. Flexfactory default values stored in default NVM memory are loaded to operational RAM. This overwrites any previously loaded values.
5. Values stored in the User NVM are loaded into operational RAM memory. This overwrites any previously loaded values (e.g. VOUT_COMMAND by pin-strap).
6. Check for external clock signal at the SYNC pin and lock internal clock to the external clock if used.

Once this procedure is completed and the Initialization Time has passed (see Electrical Specification), the output voltage is ready to be enabled using the CTRL pin. The product is also ready to accept commands via the PMBus interface, which in case of writes will overwrite any values loaded during the initialization procedure.

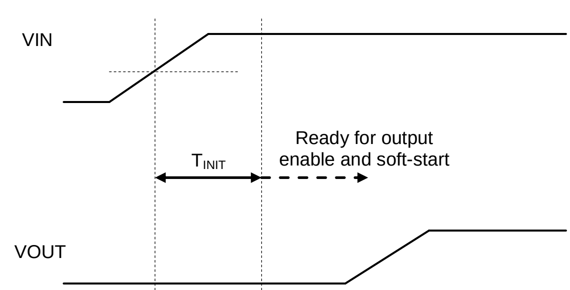


Illustration Initialization time.

Operating Information

Input Voltage

The input voltage range 7.5 - 14 V makes the product easy to use in intermediate bus applications when powered by a non-regulated bus converter or a regulated bus converter.

Input Under Voltage Protection (IUVP)

The product monitors the input voltage and will turn-on and turn-off at configured thresholds (see Electrical Specification). The turn-on input voltage threshold is set higher than the corresponding turn-off threshold. Hence, there is a hysteresis between turn-on and turn-off input voltage levels. Once the input voltage falls below the turn-off threshold, the device can respond in several ways as follows:

1. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus command CLEAR_FAULTS or the output voltage is re-enabled.
2. Immediate shutdown of output voltage while the input voltage is below the turn-on threshold. Operation resumes automatically and the output is enabled when the input voltage has risen above the turn-on threshold.

The default response is option 2. The IUVP function can be reconfigured using the PMBus commands VIN_UV_FAULT_LIMIT (turn-off threshold), VIN_UV_WARN_LIMIT (turn-on threshold) and VIN_UV_FAULT_RESPONSE.

For products configured to operate in current sharing mode, response option 1 will always be used, regardless of VIN_UV_FAULT_RESPONSE command settings.

Input Over Voltage Protection (IOVP)

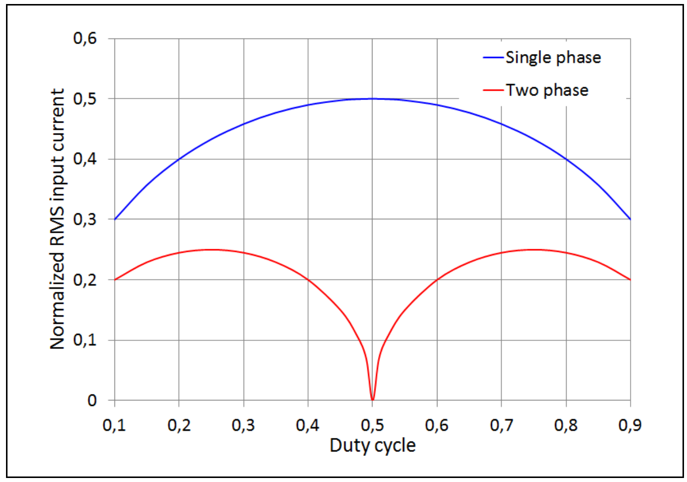
The product monitors the input voltage continuously and will respond as configured when the input voltage rises above the configured threshold level (see Electrical Specification). Refer to section “Input Under Voltage Protection” for functionality, response configuration options and default setting.
The IOVP function can be reconfigured using the PMBus commands VIN_OV_FAULT_LIMIT (turn-off threshold), VIN_OV_WARN_LIMIT (turn-on threshold) and VIN_OV_FAULT_RESPONSE.

Input and Output Impedance

The impedance of both the input source and the load will interact with the impedance of the product. It is important that the input source has low characteristic impedance. If the input voltage source contains significant inductance, the addition of a capacitor with low ESR at the input of the product will ensure stable operation.

External Input Capacitors

The product is a two-phase converter which gives lower input ripple than a single phase design, see picture below. Thus, ripple-current-rating requirements for the input capacitors are lower relatively to a single phase converter.



The input ripple RMS current in a two-phase buck converter can be estimated to

$$I_{inputRMS} = I_{load}\sqrt{D(0.5-D)} \qquad \text{(valid for } D < 0.5\text{)}$$

Where I_{load} is the output load current and D is the duty cycle. The maximum load ripple current becomes $I_{load}/4$. The ripple current is divided into three parts, i.e., currents in the input source, external input capacitor and internal input capacitor. How the current is divided depends on the impedance of the input source, ESR and capacitance values in the capacitors.

For most applications non-tantalum capacitors are preferred due to the robustness of such capacitors to accommodate high inrush currents of systems being powered from very low impedance sources. It is recommended to use a combination of ceramic capacitors and low-ESR electrolytic/polymer bulk capacitors. The low ESR of ceramic capacitors effectively limits the input ripple voltage level, while the bulk capacitance minimizes deviations in the input voltage at large load transients.

If several products are connected in a phase spreading setup the amount of input ripple current, and capacitance per product, can be reduced. The amount of input ripple current for such setup can be estimated using the Flex Power Designer software and capacitor selection can be made based on this number.

Ceramic input capacitors must be placed close to the input pins of a converter and with low impedance connections to the VIN and GND pins in order to be effective. See application note AN323 for further guidelines on how to choose and apply input capacitors.

External Output Capacitors

The output capacitor requirement depends on two considerations; output ripple voltage and load transient response. To achieve low ripple voltage, the output capacitor bank must have a low ESR value, which is achieved with ceramic output capacitors. A low ESR value is critical also for a small output voltage deviation during load transients. Designs with smaller load transients can use fewer capacitors and designs with more dynamic load content will require more load capacitors to minimize output voltage deviation. Improved transient response can also be achieved by adjusting the settings of the control loop of the product. Adding output capacitance decreases loop band-width.

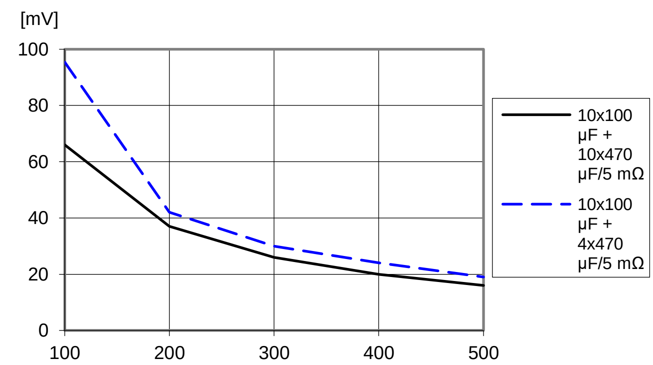
It is recommended to place low ESR ceramic and low ESR electrolytic/polymer capacitors as close to the load as possible, using several capacitors in parallel to lower the effective ESR. It is important to use low resistance and low inductance PCB layouts in order for capacitance to be effective.

Optimization of output filter together with load step simulations can be made using the Flex Power Designer software. See application note AN321 for further guidelines on how to choose and apply output capacitors.

Control Loop

The products use a fully digital control loop that achieves precise control of the entire power conversion process, resulting in a very flexible device that is also very easy to use. The control loop utilizes oversampling of the output voltage compared to the switching frequency, and a dual edge modulation PWM, to minimize the delay in the control loop. The actual duty cycle is updated after each sample within each switching cycle, achieving a smaller total output voltage variation with less output capacitance than traditional PWM controllers, thus saving cost and board space.

Control may be set more or less aggressive by adjusting a gain factor, set by the PMBus command ASCR_CONFIG. Increasing the gain factor will reduce the voltage deviation at load transients, at the expense of somewhat increased ripple on the output. Too high gain can also cause increase in jitter and instability. Stability analysis can be made using the Flex Power Designer software. Below graph exemplifies the effect of the gain factor on the voltage deviation during a load transient. The typical range of the gain factor is 100 - 600.



Load step 30-90-30 A, di/dt = 2 A/μs.
V_I = 12 V, V_O = 1.0 V, f_{sw} = 320 kHz, Residual factor = 90.
Gain factor changed by PMBus command ASCR_CONFIG.

Voltage deviation vs. control loop gain setting and output capacitance.

The user may also adjust the residual factor, set by the ASCR_CONFIG command, to improve the recovery time after a load transient. The typical usable range of the residual factor is 70 - 120. A higher value than 127 may damage the device and must not be used. Note that the gain factor will also affect the recovery time.

By default the product is configured with a moderate gain factor to provide a trade-off between load transient performance and output ripple for a wide range of operating conditions. For a specific application the gain factor can be increased to improve load transient response.

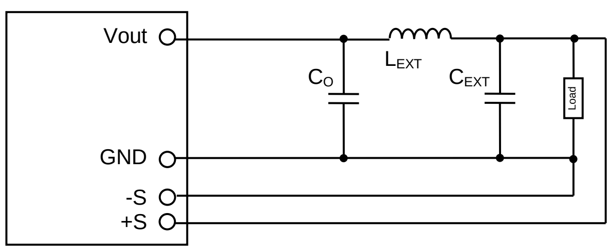
Optimization of control loop settings and output filter, together with load step simulations, can be made using the Flex Power Designer software.

Remote Sense

The product has remote sense to compensate the voltage drops between the output and the point of load. The sense traces should be laid out as a differential pair and preferably be shielded by the PCB ground layer to reduce noise susceptibility.

Generally the module is designed for an external capacitive decoupling near the module, see Section “External Output Capacitors” for further information. The Flex Power Designer software can be used to simulate the condition and help to place the correct decoupling and configure the module for optimal performance.

In case of parasitic or deliberate inductance in the output power train, it can influence the stability of the regulator. The placement of the sense point is then critical. For example, assume the external output filter includes an inductor (forming a PI filter) according to the picture below. If C_o = 2 x 470 µF/5 mΩ POS-CAP + 2 x 100 µF ceramic and C_{EXT} = 8 x 470 µF/5 mΩ POS-CAP + 8 x 100 µF ceramic, 30 nH will be the maximum value of the PI filter inductance (L_{EXT}) to guaranty stability of the system. In that case, gain factor of the control loop must be reduced to 100 at cost of higher voltage deviation in case of a load transient. As mention above, the Flex Power Designer tool can be used to simulate the condition, stabilize the control loop, and help to place the output filter.



External output filter with inductor (PI filter).

Enabling Output Voltage

The following options are available to enable and disable this device:

1. Output voltage is enabled through the CTRL pin.
2. Output voltage is enabled using the PMBus command OPERATION.

The CTRL pin can be used with active high (positive) logic or active low (negative) logic.

The CTRL pin polarity can be reconfigured using the PMBus command ON_OFF_CONFIG.

The CTRL pin has an internal 10 kΩ pull-up resistor to 5 V. The external device must have a sufficient sink current ability to be able pull CTRL pin voltage down below logic low threshold level (see Electrical Characteristics). When the CTRL pin is left open, the voltage on the CTRL pin is pulled up to 5 V.

If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to enabling the output voltage.

Output Voltage Adjust using Pin-strap Resistor

Using an external pin-strap resistor, R_{SET}, the output voltage can be set to several predefined levels shown in the table below. Only the voltage levels specified in the table can be set by R_{SET}. The resistor should be applied between the VSET pin and the PREF pin as shown in the Typical Application Circuit. Maximum 1% tolerance resistors are required.

R_{SET} [kΩ]	V_{OUT} [V]
0 (short)	1.00
10	0.60
11	0.65
12.1	0.70
13.3	0.75
14.7	0.80
16.2	0.85
17.8	0.90
19.6	0.95
21.5	1.00
23.7	1.05

R_{SET} [kΩ]	V_{OUT} [V]
26.1	1.10
28.7	1.15
31.6	1.20
34.8	1.25
38.3	1.30
42.2	1.40
46.4	1.50
51.1	1.60
56.2	1.70
61.9	1.80
Infinite (open)	1.20

R_{SET} also sets the maximum output voltage; see section Output Voltage Range Limitation. The resistor is sensed only during the initialization procedure after application of input voltage. Changing the resistor value during normal operation will not change the output voltage. See Ordering Information for output voltage range.

Output Voltage Adjust using PMBus

The output voltage set by pin-strap can be overridden up to a certain level (see section Output Voltage Range Limitation) by using the PMBus command VOUT_COMMAND. See Electrical Specification for adjustment range. Make sure a new VOUT_COMMAND is not sent 15 ms prior to enabling the output, until after power good (PG) is asserted.

Voltage Margining Up/Down

Using the PMBus interface it is possible to adjust the output voltage to one of two predefined levels above or below the nominal voltage setting in order to determine whether the load device is capable of operating outside its specified supply voltage range. This provides a convenient method for dynamically testing the operation of the load circuit outside its typical operating range. This functionality can also be used to test of supply voltage supervisors. Margin limits of the nominal output voltage ±5% are default, but the margin limits can be reconfigured using the PMBus commands VOUT_MARGIN_LOW and VOUT_MARGIN_HIGH. Margining is activated by the command OPERATION and can be used regardless of the output voltage being enabled by the CTRL pin or by the PMBus.

Output Voltage Trim

The actual output voltage can be trimmed to optimize performance of a specific load by setting a non-zero value for PMBus command VOUT_TRIM. The value of VOUT_TRIM is summed with the nominal output voltage set by VOUT_COMMAND, allowing for multiple products to be commanded to a common nominal value, but with slight adjustments per load.

Output Voltage Range Limitation

The output voltage range that is possible to set by configuration or by the PMBus interface is hardware limited by the pin-strap resistor R_{SET}. The maximum output voltage is set to 115% of the output value defined by R_{SET}. This protects the application circuit from an over voltage due to an accidental PMBus command.
The limitation applies to the actual regulated output voltage rather than to the configured value. Thus, it is possible to write and read back a VOUT_COMMAND value higher than the limit, but the actual output voltage will be limited.
The output voltage limit can be reconfigured to a *lower* than 115% of Vout value by writing the PMBus command VOUT_MAX.

Output Over Voltage Protection (OVP)

The product includes over voltage limiting circuitry for protection of the load. The default OVP limit is 15% above the nominal output voltage. The product can be configured to respond in different ways to the output voltage exceeding the OVP limit:

1. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus command CLEAR_FAULTS or the output voltage is re-enabled.
2. Immediate shutdown of output voltage followed by continuous restart attempts of the output voltage with a preset interval (“hiccup” mode).

The default response is option 2. The OVP limit and fault response can be reconfigured using the PMBus commands VOUT_OV_FAULT_LIMIT, VOUT_OV_FAULT_RESPONSE and OVUV_CONFIG.

For products configured to operate in current sharing mode, response option 1 will always be used, regardless of this command configuration.

Output Under Voltage Protection (UVP)

The product includes output under voltage limiting circuitry for protection of the load. The default UVP limit is 15% below the nominal output voltage. Refer to section Output Over Voltage Protection for response configuration options and default setting.
The UVP limit and fault response can be reconfigured using the PMBus commands VOUT_UV_FAULT_LIMIT and VOUT_UV_FAULT_RESPONSE.

Power Good

The power good pin (PG) indicates when the product is ready to provide regulated output voltage to the load. During ramp-up and during a fault condition, PG is held low. By default, PG is asserted high after the output has ramped to a voltage above 90% of the nominal voltage, and deasserted if the output voltage falls below 85% of the nominal voltage. These thresholds may be changed using the PMBus commands POWER_GOOD_ON and VOUT_UV_FAULT_LIMIT.

The time between when the POWER_GOOD_ON threshold is reached and when the PG pin is actually asserted is set by the PMBus command POWER_GOOD_DELAY. See Electrical Specification for default value and range.

By default the PG pin is configured as an open drain output but it is also possible to set the output in push-pull mode by the command USER_CONFIG.

The PG output is not defined during ramp up of the input voltage due to the initialization of the product.

Over Current Protection (OCP)

The product includes robust current limiting circuitry for protection at continuous overload. After ramp-up is complete the product can detect an output overload/short condition. The following OCP response options are available:

1. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus command CLEAR_FAULTS or the output voltage is re-enabled.
2. Immediate shutdown of output voltage followed by continuous restart attempts of the output voltage with a preset interval (“hiccup” mode).

The default response from an over current fault is option 2. Note that delayed shutdown is not supported. The load distribution should be designed for the current set by the current limit threashold. The OCP limit and response can be reconfigured using the PMBus commands IOUT_AVG_OC_FAULT_LIMIT and MFR_IOUT_OC_FAULT_RESPONSE.

For products operated in current sharing mode, response option 1 will always be used, regardless of configuration.

Under Current Protection (UCP)

The product includes robust current limiting circuitry for protection at continuous reversed current, due to a synchronous rectifier ability to sink current. Refer to section Over Current Protection for response configuration options and default setting. The UCP limit and response can be reconfigured using the PMBus commands IOUT_AVG_UC_FAULT_LIMIT and MFR_IOUT_UC_FAULT_RESPONSE.

Switching Frequency

The default switching frequency is chosen as the best tradeoff between efficiency, thermal performance, output ripple and load transient performance. The switching frequency can be re-configured in a certain range using the PMBus command FREQUENCY_SWITCH. Refer to Electrical Specification for default switching frequency and range.

Changing the switching frequency will affect efficiency, power dissipation, load transient response (control loop characteristics) and output ripple. Control loop settings may need to be adjusted.

The default switching frequency will optimize efficiency while an increase of frequency will improve ripple and load response at the cost of lower efficiency.

Note that since the product has two phases the effective switching frequency will be twice the configured.

Synchronization

One or more products may be synchronized with an external clock to eliminate beat frequencies reflected back to the input supply rail. Eliminating the slow beat frequencies (usually <10 kHz) relaxes the filtering requirements. Synchronization can also be utilized for phase spreading, described in section Phase Spreading.
The products can be synchronized with an external oscillator or one product can be configured with the SYNC pin as a SYNC output, working as a source of synchronization signal for other products connected to the same synchronization line. The SYNC pin of products being synchronized must be configured as SYNC Input. Default configuration is using the internal clock, independently of signal at the SYNC pin.
Synchronization is configured using PMBus command MFR_USER_CONFIG.
See application note AN309 for further information.

Phase Spreading

When multiple products share a common DC input supply, spreading of the switching clock phase between the products can be utilized. This dramatically reduces input capacitance requirements and power losses, since the peak current drawn from the input supply is effectively spread out over the whole switch period. This requires that the products are synchronized using the SYNC pin.

The phase offset is measured from the rising edge of the applied external clock to the rising edge of the PWM pulse as illustrated below.

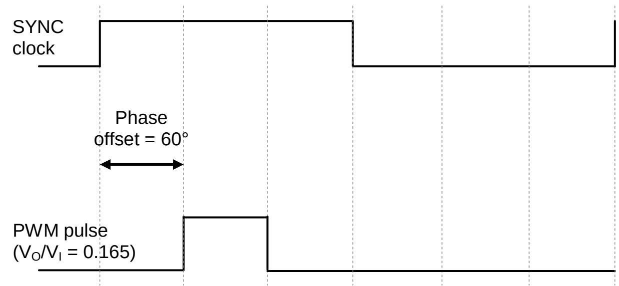


Illustration of phase offset.

The phase offset is configured using the PMBus command INTERLEAVE and is defined as:

$$Phase\_offset(°) = 360° \times \frac{Interleave\_order}{Number\_in\_group}$$

Interleave_order is in the range 0-15. *Number_in_group* is in the range 0-15 where a value of 0 means 16. The set resolution for the phase offset is 360° / 16 = 22.5°.

By default *Number_in_group = 0 and Interleave_order* = Four LSB's of set PMBus address (see section PMBus Addressing).

Optimized phase spreading for several modules is easily set up using Flex Power Designer software. See application note AN309 for further information.

Soft-start and Soft-stop

The soft-start and soft-stop control functionality allows the output voltage to ramp-up and ramp-down with defined timing with respect to the control of the output. This can be used to control inrush current and manage supply sequencing of multiple controllers.
The rise time is the time taken for the output to ramp to its target voltage, while the fall time is the time taken for the output to ramp down from its regulation voltage to 0 V. The on delay time sets a delay from when the output is enabled until the output voltage starts to ramp up. The off delay time sets a delay from when the output is disabled until the output voltage starts to ramp down.

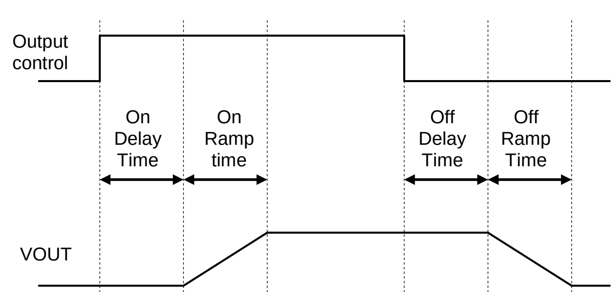


Illustration of soft-start and soft-stop.

By default soft-stop is disabled and the regulation of output voltage stops immediately when the output is disabled. Soft-stop can be enabled through the PMBus command ON_OFF_CONFIG. The delay and ramp times can be reconfigured using the PMBus commands TON_DELAY, TON_RISE, TOFF_DELAY and TOFF_FALL.

Output Voltage Sequencing

A group of products may be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs and ASICs that require one supply to reach its operating voltage prior to another.

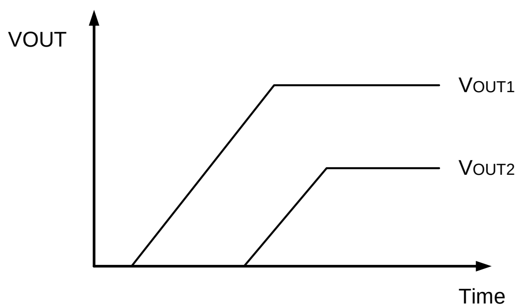


Illustration of output voltage sequencing.

Different types of multi-product sequencing are supported:

1. Time based sequencing. Configuring the start delay and rise time of each module through the PMBus interface and by connecting the CTRL pin of each product to a common enable signal.

2. Event based sequencing. Routing the PG pin signal of one module to the CTRL pin of the next module in the sequence.

3. GCB based sequencing. Power Good triggered sequencing with the sequence order defined by configuration. Configured through the PMBus interface and uses the GCB bus, see section Group Communication Bus.

These sequencing options are easily configured using the Flex Power Designer software. See application note AN310 for further information.

Pre-Bias Startup Capability

Pre-bias startup often occurs in complex digital systems when current from another power source is fed back through a dual-supply logic component, such as FPGAs or ASICs. There could also be still charged output capacitors when starting up shortly after turn-off.
The product incorporates synchronous rectifiers, but will not sink current during startup, or turn off, or whenever a fault shuts down the product in a pre-bias condition.

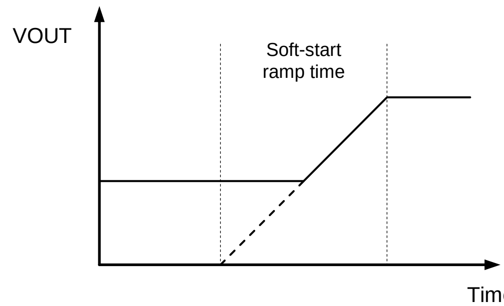


Illustration of pre-bias startup.

Voltage Tracking

The product integrates a lossless tracking scheme that allows its output to track a voltage that is applied to the VTRK pin with no external components required. During ramp-up, the output voltage follows the VTRK voltage until the preset output voltage level is met. The product offers two modes of tracking as follows:

1. Coincident. This mode configures the product to ramp its output voltage at the same rate as the voltage applied to the VTRK pin.

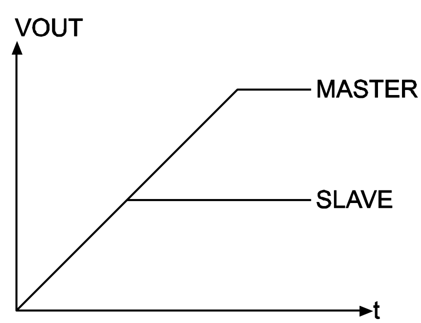


Illustration of coincident voltage tracking.

2. Ratiometric. In this mode the product ramps its output voltage at a rate that is a percentage of the voltage applied to the VTRK pin. Ratiometric tracking is achieved by configuring the product for coincident tracking and adding an external resistive voltage divider.

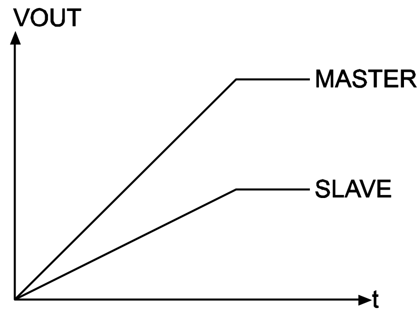


Illustration of ratiometric voltage tracking.

The master device in a tracking group is defined as the device that has the highest target output voltage within the group. This master device will control the ramp rate of all tracking devices and is not configured for tracking mode. Any device configured in tracking mode will ignore its soft-start/stop settings and take on the turn-on/turn-off characteristics of the voltage present at the VTRK pin.

All of the CTRL pins in the tracking group must be connected and driven by a single logic source. Tracking is configured using the PMBus command TRACK_CONFIG.

Tracking configurations are easily set up using Flex Power Designer software.
See application note AN310 for further details and limitations of the tracking functionality.

Group Communication Bus (GCB)

The Group Communication Bus, GCB, is used to communicate between products. This dedicated single wire bus provides the communication channel between devices for features such as sequencing, fault spreading and current sharing. The GCB solves the PMBus data rate limitation. The GCB pin on all devices in an application should be connected together. A pull-up resistor is required on the common GCB in order to guarantee the rise time as according to equation below:

$$\tau = R_{GCB} C_{GCB} \leq 1 \mu s$$

where RGCB is the pull up resistor value and CGCB is the bus loading. The pull-up resistor should be tied to an external supply voltage in range from 2.5 V to 5.5 V, which should be present prior to or during power-up.
Note: GCB bus requires an “always on” source, therefore, a 47 kΩ internal pull-up resistor is connected to 5.0 V.

The GCB is an internal bus, such that it is only connected across the modules and not the PMBus system host. GCB addresses are assigned on a rail level, i.e. modules within the same current sharing group share the same GCB address. Addressing rails across the GCB is done with a 5 bit GCB ID, yielding a theoretical total of 32 rails that can be shared with a single GCB bus.

By default the GCB ID is set to the five LSB’s of set PMBus address (see section PMBus Addressing).

Limitations apply when using this product on the same GCB bus as other Flex Power Modules POL products operated in parallel. Please contact your sales representative for detailed information.

Parallel Operation (Current Sharing)

Paralleling multiple products can be used to increase the output current capability of a single power rail. By connecting the GCB and SYNC pins of each device and configuring the devices as a current sharing rail, the units will share the current equally, enabling up to 100% utilization of the current capability for each device in the current sharing rail. The product uses a low-bandwidth, first-order digital current sharing by aligning the output voltage of the slave devices to deliver the same current as the master device. Artificial droop resistance is added to the output voltage path to control the slope of the load line curve, calibrating out the physical parasitic mismatches due to power train components and PWB layout. Up to 4 devices can be configured in a given current sharing group.

Note that continuous restarts after a fault (“hiccup mode”) are not supported for parallel operation.

Parallel operation is easily configured using Flex Power Designer software. See application note AN307 for further information.

Broadcast Control

The product can be configured to broadcast output voltage enable or setting of output voltage level over the GCB bus to other devices in the group. If configured to do so, a device receiving a PMBus OPERATION command or VOUT_COMMAND command will broadcast the same command over the GCB bus, and other devices on the GCB bus will respond to the same commands, if configured to do so. Broadcast control is configured using the PMBus command GCB_GROUP.

Fault spreading

The product can be configured to broadcast a fault event over the GCB bus to the other devices in the group. When a non-destructive fault occurs and the device is configured to shut down on a fault, the device will shut down and broadcast the fault event over the GCB bus. The other devices on the GCB bus will shut down together if configured to do so, and will attempt to re-start in their prescribed order if configured to do so. Fault spreading is configured using the PMBus command GCB_GROUP or LEGACY_FAULT_GROUP.
See application note AN308 for further information.

Thermal Consideration

General

The product is designed to operate in different thermal environments and sufficient cooling must be provided to ensure reliable operation. Cooling is achieved mainly by conduction, from the pins to the host board, and convection, which is dependent on the airflow across the product. Increased airflow enhances the cooling of the product.

The Output Current Derating graph found in the Output section for each model provides the available output current versus ambient air temperature and air velocity at specified V_I.

The product is tested on a 254 x 254 mm, 35 µm (1 oz) test board mounted vertically in a wind tunnel with a cross-section of 608 x 203 mm. The test board has 16 layers.

Note that the cooling via power pins does not only have to handle the power loss from the module. A low resistance between module and target device is of major importance to reduce additional power loss.

See Design Note 019 for further information.

Definition of Product Operating Temperature

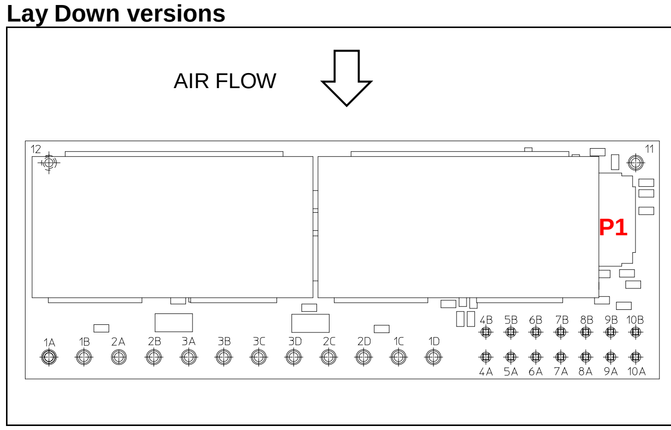
The temperature at position P1 should not exceed the maximum temperatures in the table below. The number of measurement points may vary with different thermal design and topology. Temperature above specified maximum measured at the specified position is not allowed and may cause permanent damage.

Note that the maximum value is the maximum operating temperature and that the provided Electrical Specification data is guaranteed up to T_{P1} = +95 °C.

Position	Description	Max Temperature
P1	N1, Control circuit Reference point	T_{P1} = 115 °C for Lay Down T_{P1} = 120 °C for SIP

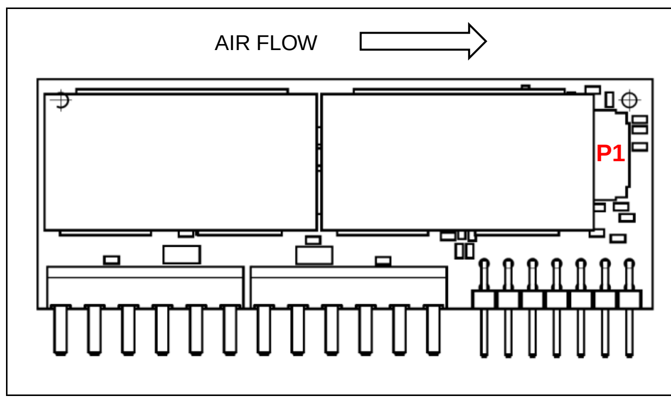
P1 is not the hot spot (the position with the highest temperature) in all cases. However securing that P1 is below its maximum temperature is securing that all other components are below their maximum limits. Note that the temperature at P1 can be monitored via the PMBus interface (see section Monitoring via PMBus).

Lay Down versions



Temperature positions and air flow direction (top view).

SIP version



Temperature positions and air flow direction (side view).

Note that the same PCB is used for both Lay Down and SIP versions. Thus, the position indicated in the pictures applies to both versions.

Definition of Reference Temperature T_{P1}

The temperature at position P1 has been used as a reference temperature for the Electrical Specification data provided.

Thermal Model

The thermal models described below can be used to estimate the temperature at position P1, based on ambient and board temperatures. The equations can be used to make a first rough estimate of the conditions required to keep the position P1 temperature below specified maximum.

For Lay Down version:

$$T_{P1} = \frac{P_d + \left(\frac{T_A}{R_A} + \frac{T_{BRD}}{R_{BRD}}\right)}{\frac{1}{R_A} + \frac{1}{R_{BRD}}},$$

$$R_A = \frac{30.6}{v} \quad (^\circ\mathrm{C/W}) \quad \& \quad R_{BRD} = 0.75\ ^\circ\mathrm{C/W}$$

For SIP version:

$$T_{P1} = \frac{P_d + \left(\frac{T_A}{R_A} + \frac{T_{BRD}}{R_{BRD}}\right)}{\frac{1}{R_A} + \frac{1}{R_{BRD}}},$$

$$R_A = 24.3\, v^{-0.74} \quad (^\circ\mathrm{C/W}) \quad \& \quad R_{BRD} = 1.7\ ^\circ\mathrm{C/W}$$

T_{P1} = Temperature at position P1 (°C),
P_d = Power dissipation of module (W),
T_A = Ambient temperature (°C),
v = Airflow (m/s),
T_{BRD} = Board temperature (°C) (close to module GND pads).

It should be noted that the models are optimized for loads higher than 50% of max I_O.

Over Temperature Protection (OTP)

The products are protected from thermal overload by an internal over temperature shutdown function in the controller N1, located in position P1.

The temperature T_{P1} is continuously monitored and when a temperature rises above the configured fault threshold level the product will respond as configured. The product can respond in several ways as follows:

1. Immediate and definite shutdown of output voltage until the fault is cleared by PMBus command CLEAR_FAULTS or the output voltage is re-enabled.
2. Immediate shutdown of output voltage while the temperature is above the warning threshold. Operation resumes automatically and the output is enabled when the temperature has fallen below the warning threshold, i.e. there is a hysteresis defined by the difference between the fault threshold and the warning threshold.

Default response is option 2. The default OTP thresholds and hysteresis are specified in Electrical Characteristics.

The OTP limit, hysteresis and response for temperature in position P1 is configured using the PMBus commands OT_FAULT_LIMIT, OT_WARN_LIMIT and OT_FAULT_RESPONSE.

For products operated in current sharing mode, response option 1 will always be used, regardless of configuration.

PCB Layout Consideration

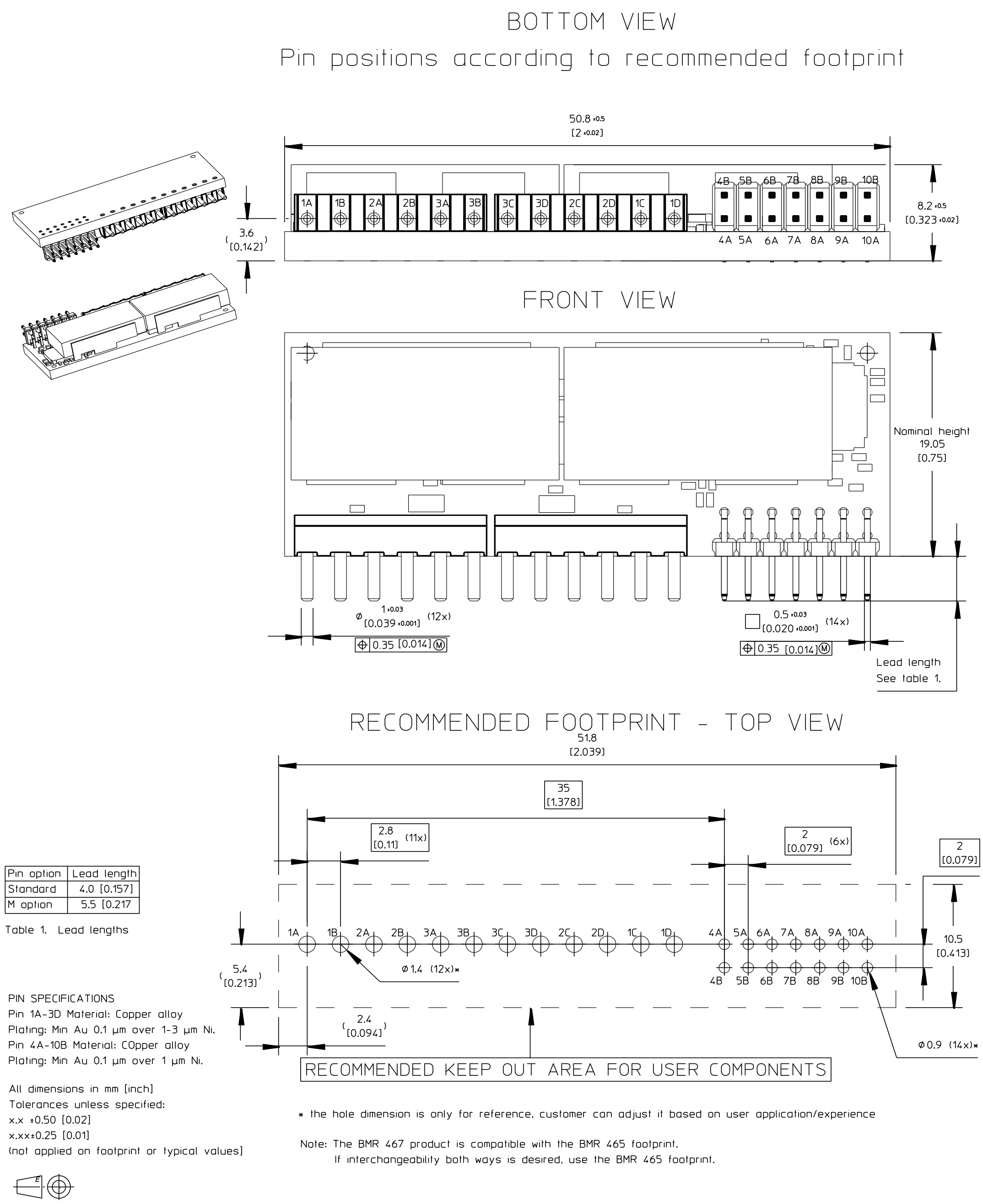
The radiated EMI performance of the product will depend on the PCB layout and ground layer design. If a ground layer is used, it should be connected to the output of the product and the equipment ground or chassis.
A ground layer will increase the stray capacitance in the PCB and improve the high frequency EMC performance.

Further layout recommendations are listed below.

- The pin strap resistors, R_{SET}, and R_{SA} should be placed as close to the product as possible to minimize loops that may pick up noise. Avoid capacitive load on these signals as it may result in false pin strap reading.
- Avoid current carrying planes under the pin strap resistors and the PMBus signals.
- The capacitors C_{IN} should be placed as close to the input pins as possible and with low impedance connections, e.g. using via stitching around capacitors' terminals. See AN323 for more details.
- The capacitors C_{OUT} should in general be placed close to the load. However typically you would like to place larger ceramic output capacitors close to the module output in order to handle the output ripple current. See AN321 for more details. Low impedance connections must be used, e.g. via stitching around capacitors' terminals.
- Care should be taken in the routing of the connections from the point of load to the S+ and S- terminals. These sensing connections should be routed as a differential pair, preferably between ground planes which are not carrying high currents. The routing should avoid areas of high electric or magnetic fields. In case of current sharing (parallel) operation each module must sense at the same points. Avoid sensing close to the module.
- If possible use planes on several layers to carry V_I, V_O and GND. There should be a large number of vias close to the VIN, VOUT and GND pads in order to lower input and output impedances and improve heat spreading between the product and the host board. Minimum total copper thickness of VOUT and GND layers respectively has to be 140 µm (4 oz) in order to distribute maximum current without unacceptable losses.

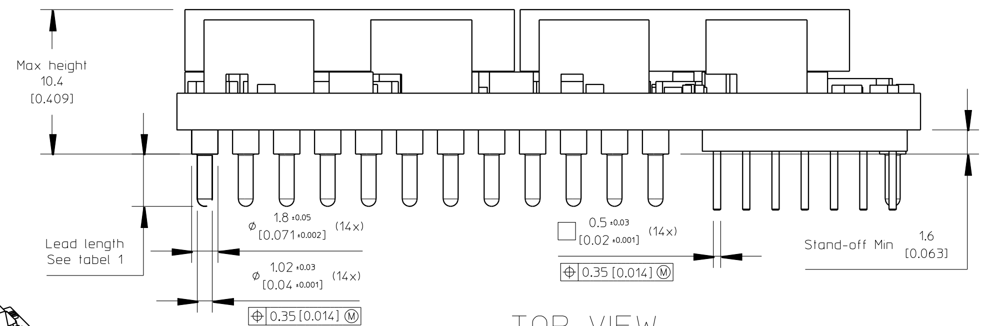
See the User Guide of the product's reference board for an example layout where the recommendations above are

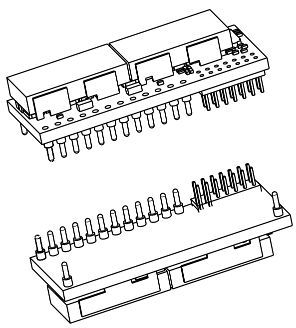
Mechanical Information - Hole Mount, SIP version



All component placements – whether shown as physical components or symbolical outline – are for reference only and are subject to change throughout the product's life cycle, unless explicitly described and dimensioned in this drawing.

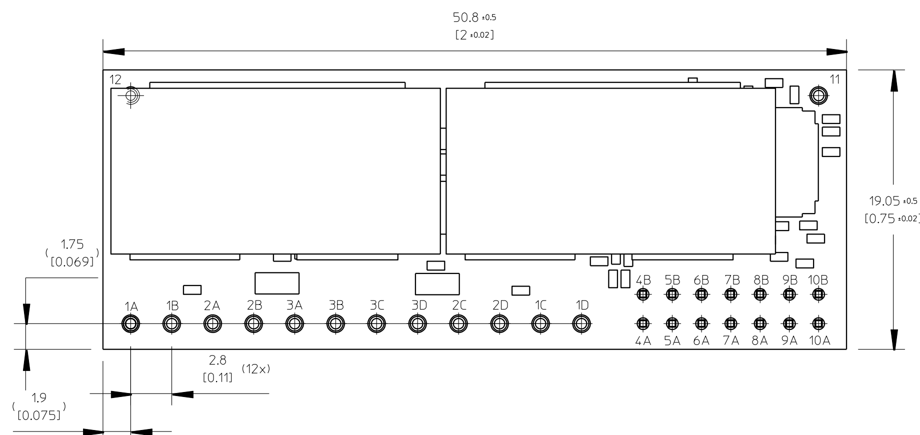
Mechanical Information - Hole Mount, Open frame version



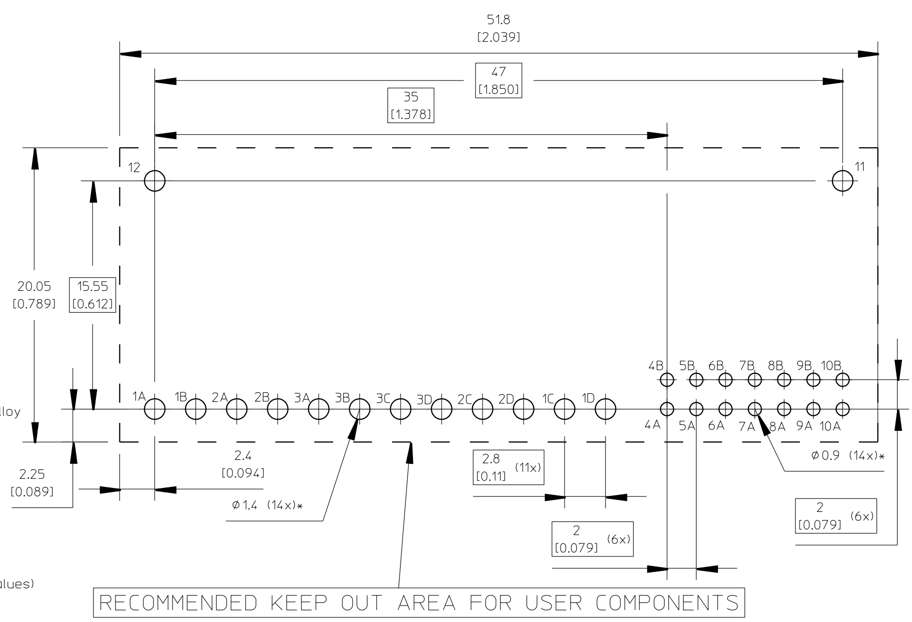


TOP VIEW

Pin positions according to recommended footprint



RECOMMENDED FOOTPRINT - TOP VIEW



Pin option	Lead length
Standard	3.56 [0.14]
M option	5.5 [0.217]

Table 1. Lead lengths

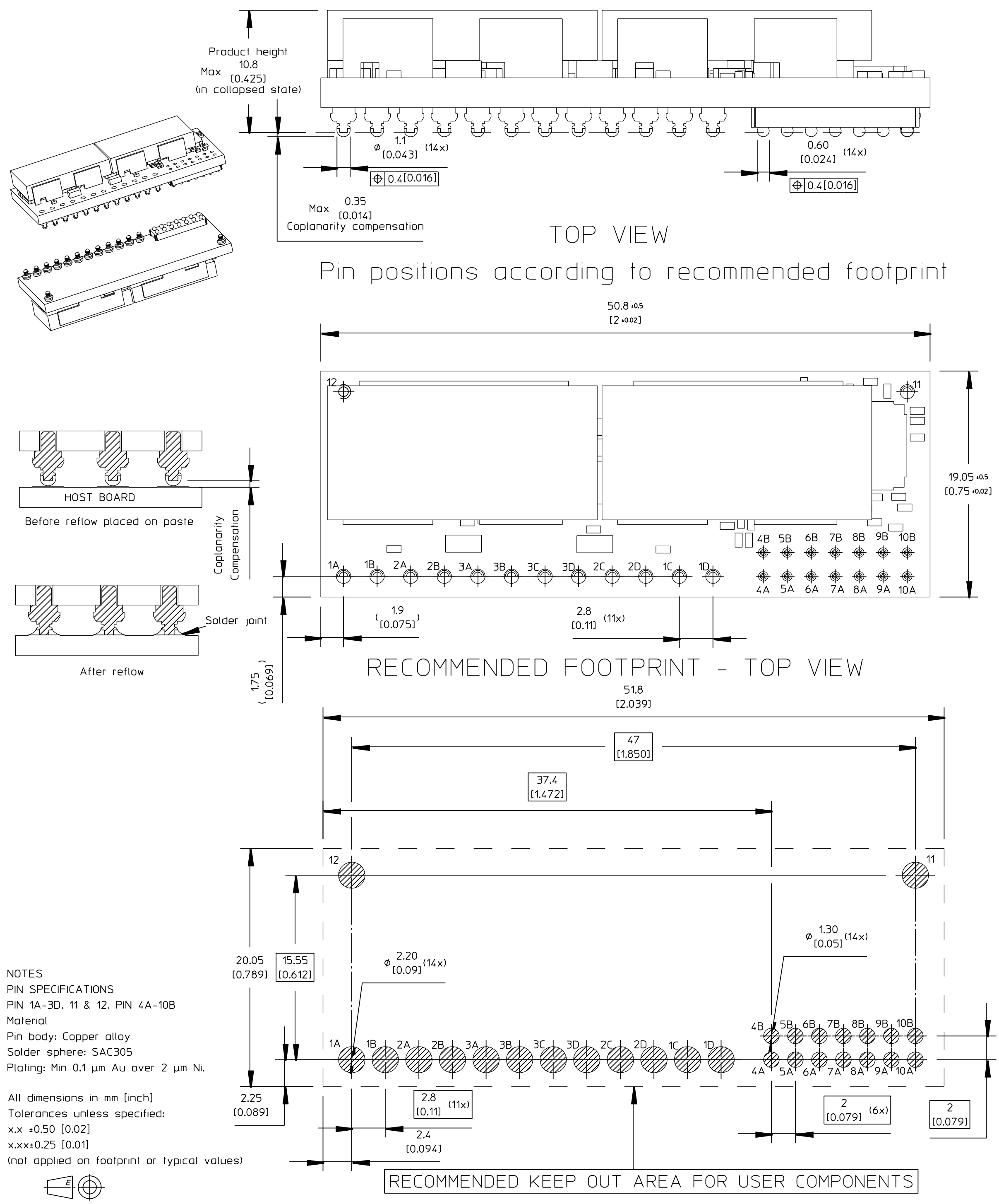
PIN SPECIFICATONSS
PIN 1A-3D, 11 & 12 Material: Copper alloy
Plating:Min 0.1 µm Au over 1-3 µm Ni
PIN 4a-10B Material: Copper alloy
Plating: Min 0.1 µm Au over 1 µm Ni

All dimensions in mm [inch]
Tolerances unless specified:
x.x ±0.50 [0.02]
x.xx±0.25 [0.01]
(not applied on footprint or typical values)

* The hole dimension is only for reference, customer can adjust it based on user application/experience

All component placements – whether shown as physical components or symbolical outline – are for reference only and are subject to change throughout the product's life cycle, unless explicitly described and dimensioned in this drawing.

Mechanical Information – Surface mount, Open frame version



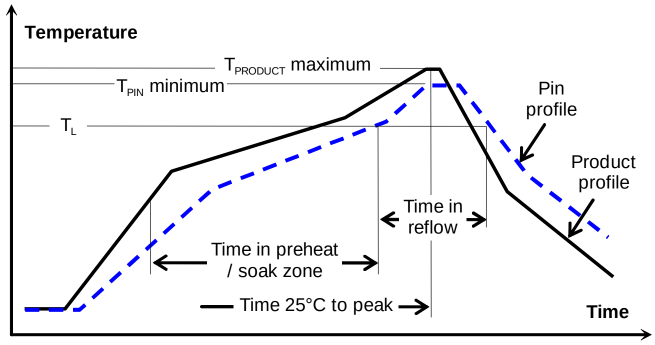
Soldering Information – Surface Mounting and Hole Mount through Pin in Paste Assembly

The surface mount product is intended for forced convection or vapor phase reflow soldering in SnPb or Pb-free processes.

The reflow profile should be optimised to avoid excessive heating of the product. It is recommended to have a sufficiently extended preheat time to ensure an even temperature across the host PWB and it is also recommended to minimize the time in reflow.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board, since cleaning residues may affect long time reliability and isolation voltage.

General reflow process specifications		SnPb eutectic	Pb-free
Average ramp-up ($T_{PRODUCT}$)		3°C/s max	3°C/s max
Typical solder melting (liquidus) temperature	T_L	183°C	221°C
Minimum reflow time above T_L		60 s	60 s
Minimum pin temperature	T_{PIN}	210°C	235°C
Peak product temperature	$T_{PRODUCT}$	225°C	260°C
Average ramp-down ($T_{PRODUCT}$)		6°C/s max	6°C/s max
Maximum time 25°C to peak		6 minutes	8 minutes



Minimum Pin Temperature Recommendations

Pin number 3C is chosen as reference location for the minimum pin temperature recommendation since this will likely be the coolest solder joint during the reflow process.

SnPb solder processes

For SnPb solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature, (T_L, 183°C for Sn63Pb37) for more than 60 seconds and a peak temperature of 220°C is recommended to ensure a reliable solder joint.

For dry packed products only: depending on the type of solder paste and flux system used on the host board, up to a recommended maximum temperature of 245°C could be used, if the products are kept in a controlled environment (dry pack handling and storage) prior to assembly.

Lead-free (Pb-free) solder processes

For Pb-free solder processes, a pin temperature (T_{PIN}) in excess of the solder melting temperature (T_L, 217 to 221°C for SnAgCu solder alloys) for more than 60 seconds and a peak temperature of 245°C on all solder joints is recommended to ensure a reliable solder joint.

Maximum Product Temperature Requirements

Top of the product PWB near pin 10A is chosen as reference location for the maximum (peak) allowed product temperature ($T_{PRODUCT}$) since this will likely be the warmest part of the product during the reflow process.

SnPb solder processes

For SnPb solder processes, the product is qualified for MSL 1 according to IPC/JEDEC standard J-STD-020C.

During reflow $T_{PRODUCT}$ must not exceed 225 °C at any time.

Pb-free solder processes

For Pb-free solder processes, the product is qualified for MSL 3 according to IPC/JEDEC standard J-STD-020C.

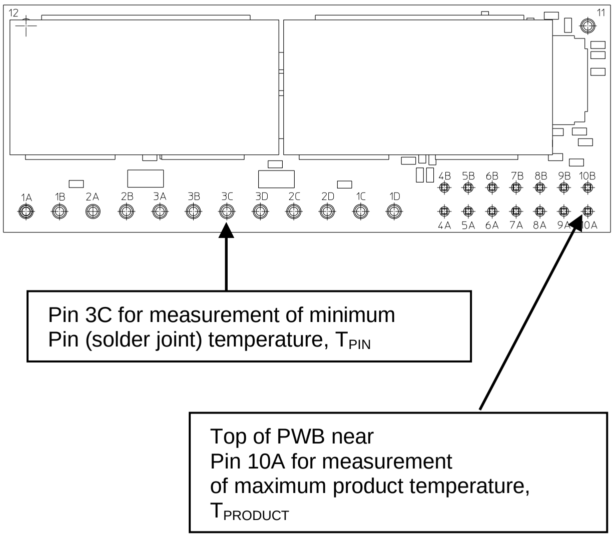
During reflow $T_{PRODUCT}$ must not exceed 260 °C at any time.

Dry Pack Information

Products intended for Pb-free reflow soldering processes are delivered in standard moisture barrier bags according to IPC/JEDEC standard J-STD-033 (Handling, packing, shipping and use of moisture/reflow sensitivity surface mount devices).

Using products in high temperature Pb-free soldering processes requires dry pack storage and handling. In case the products have been stored in an uncontrolled environment and no longer can be considered dry, the modules must be baked according to J-STD-033.

Thermocoupler Attachment



Soldering Information - Hole Mounting

The hole mounted product is intended for plated through hole mounting by wave or manual soldering. The pin temperature is specified to maximum to 270°C for maximum 10 seconds.

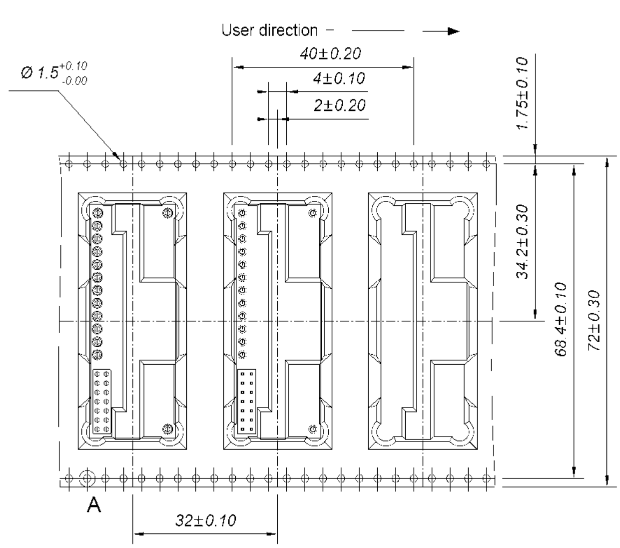
A maximum preheat rate of 4°C/s and maximum preheat temperature of 150°C is suggested. When soldering by hand, care should be taken to avoid direct contact between the hot soldering iron tip and the pins for more than a few seconds in order to prevent overheating.

A no-clean flux is recommended to avoid entrapment of cleaning fluids in cavities inside the product or between the product and the host board. The cleaning residues may affect long time reliability and isolation voltage.

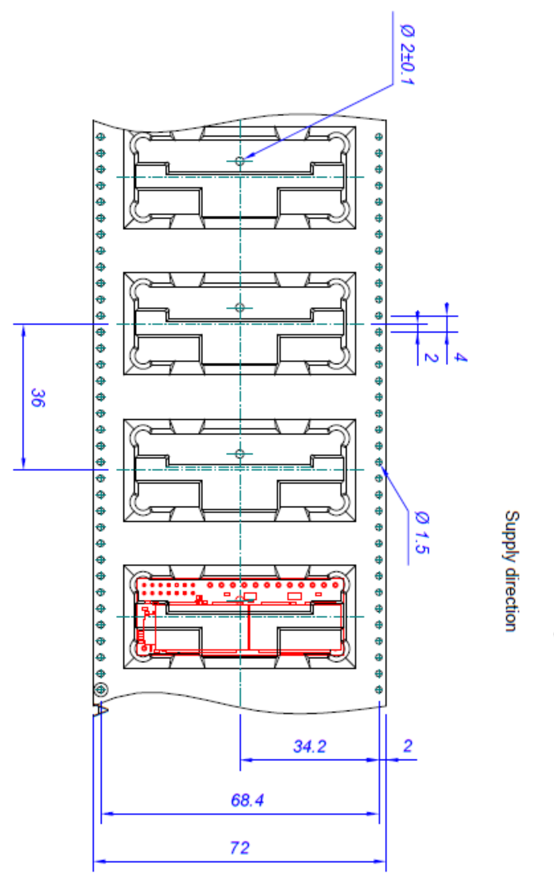
Delivery Package Information

The products are delivered in antistatic trays (SIP variant) and in antistatic carrier tape (laydown variant, EIA 481 standard). All versions are delivered in dry-pack.

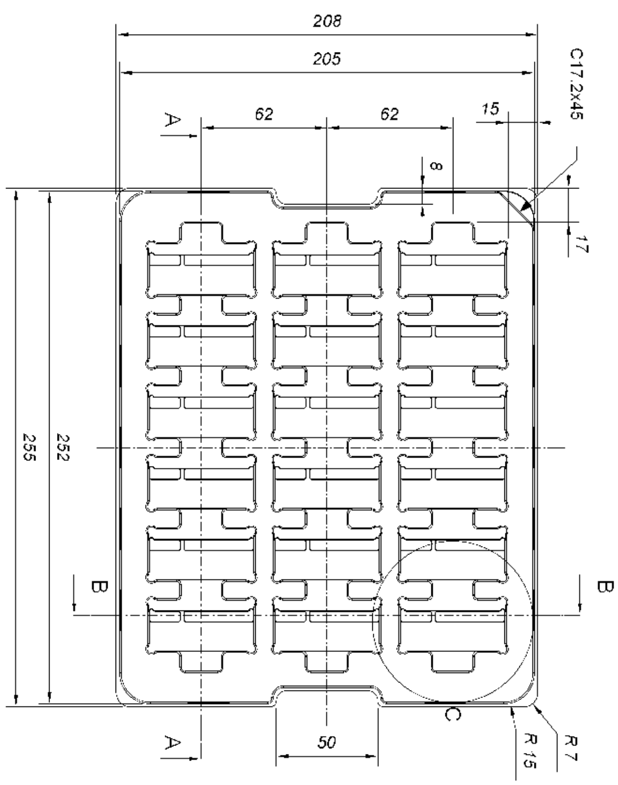
Carrier Tape Specifications - Pin length 3.56mm	
Material	Antistatic PS
Surface resistance	10^5 < Ohm/square < 10^{10}
Bakeability	The tape is not bakeable
Tape width, W	72 mm [2.83 inch]
Pocket pitch, P_1	32 mm [1.26 inch]
Pocket depth, K_0	15.16 mm [0.597 inch]
Reel diameter	330 mm [13 inch]
Reel capacity	130 products /reel
Reel weight	350 g empty [3340 g full reel]
Box capacity	260 products (2 reels/box)



Carrier Tape Specifications - Pin length 5.5mm	
Material	Transparent PET
Surface resistance	10^5 < Ohm/square < 10^{10}
Bakeability	The tape is not bakeable
Tape width, W	72 mm [2.83 inch]
Pocket pitch, P_1	36 mm [1.42 inch]
Pocket depth, K_0	16.7 mm [0.657 inch]
Reel diameter	330 mm [13 inch]
Reel capacity	80 products /reel
Reel weight	350 g empty [2300 g full reel]
Box capacity	160 products (2 reels/box)



Tray Specifications	
Material	ESD PS
Surface resistance	10 < Ohm/square < 10^5
Bakeability	The trays are not bakeable
Tray thickness	16.5 mm [0.650 inch]
Box capacity	144 products (8 full trays/box)
Tray weight	60 g empty [474 g full tray]



Product Qualification Specification

Characteristics			
External visual inspection	IPC-A-610		
Change of temperature (Temperature cycling)	IEC 60068-2-14 Na	Temperature range Number of cycles Dwell/transfer time	-40 to 100°C 1000 15 min/0-1 min
Cold (in operation)	IEC 60068-2-1 Ad	Temperature T_A Duration	-45°C 72 h
Damp heat	IEC 60068-2-67 Cy	Temperature Humidity Duration	85°C 85 % RH 1000 hours
Dry heat	IEC 60068-2-2 Bd	Temperature Duration	125°C 1000 h
Electrostatic discharge susceptibility	IEC 61340-3-1, JESD 22-A114 IEC 61340-3-2, JESD 22-A115	Human body model (HBM) Machine Model (MM)	Class 2, 2000 V Class 3, 200 V
Immersion in cleaning solvents	IEC 60068-2-45 XA, method 2	Water Glycol ether Isopropyl alcohol	55°C 35°C 35°C
Mechanical shock	IEC 60068-2-27 Ea	Peak acceleration Duration	100 g 6 ms
Moisture reflow sensitivity [1]	J-STD-020C	Level 1 (SnPb-eutectic) Level 3 (Pb Free)	225°C 260°C
Operational life test	MIL-STD-202G, method 108A	Duration	1000 h
Resistance to soldering heat [2]	IEC 60068-2-20 Tb, method 1A	Solder temperature Duration	270°C 10-13 s
Robustness of terminations	IEC 60068-2-21 Test Ua1 IEC 60068-2-21 Test Ue1	Through hole mount products Surface mount products	All leads All leads
Solderability	IEC 60068-2-58 test Td [1] IEC 60068-2-20 test Ta [2]	Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free Preconditioning Temperature, SnPb Eutectic Temperature, Pb-free	150°C dry bake 16 h 215°C 235°C Steam ageing 235°C 245°C
Vibration, broad band random	IEC 60068-2-64 Fh, method 1	Frequency Spectral density Duration	10 to 500 Hz 0.07 g^2/Hz 10 min in each direction

Notes
[1] Only for products intended for reflow soldering (surface mount products)
[2] Only for products intended for wave soldering (plated through hole products)

Appendix - PMBus Commands

This appendix contains a detailed reference of the PMBus commands supported by the product.

Data Formats

The products make use of a few standardized numerical formats, along with custom data formats. A detailed walkthrough of the above formats is provided in AN304, as well as in sections 7 and 8 of the PMBus Specification Part II. The custom data formats vary depending on the command, and are detailed in the command description.

Standard Commands

The functionality of commands with code 0x00 to 0xCF is usually based on the corresponding command specification provided in the PMBus Standard Specification Part II (see Power System Management Bus Protocol Documents below). However there might be different interpretations of the PMBus Standard Specification or only parts of the Standard Specification applied, thus the detailed command description below should always be consulted.

Forum Websites

The System Management Interface Forum (SMIF)
http://www.powersig.org/
The System Management Interface Forum (SMIF) supports the rapid advancement of an efficient and compatible technology base that promotes power management and systems technology implementations. The SMIF provides a membership path for any company or individual to be active participants in any or all of the various working groups established by the implementer forums.

Power Management Bus Implementers Forum
(PMBUS-IF)
http://pmbus.org/
The PMBus-IF supports the advancement and early adoption of the PMBus protocol for power management. This website offers recent PMBus specification documents, PMBus articles, as well as upcoming PMBus presentations and seminars, PMBus Document Review Board (DRB) meeting notes, and other PMBus related news.

PMBus – Power System Management Bus Protocol Documents

These specification documents may be obtained from the PMBus-IF website described above. These are required reading for complete understanding of the PMBus implementation. This appendix will not re-address all of the details contained within the two PMBus Specification documents.

Specification Part I – General Requirements Transport and Electrical Interface
Includes the general requirements, defines the transport and electrical interface and timing requirements of hard wired signals.

Specification Part II – Command Language
Describes the operation of commands, data formats, fault management and defines the command language used with the PMBus.

SMBus – System Management Bus Documents

System Management Bus Specification, Version 2.0, August 3, 2000
This specification specifies the version of the SMBus on which Revision 1.2 of the PMBus Specification is based. This specification is freely available from the System Management Interface Forum Web site at:
http://www.smbus.org/specs/

PMBus Command Summary and Factory Default Values of Standard Configuration

The factory default values provided in the table below are valid for the Standard configuration. Factory default values for other configurations can be found using the Ericsson Power Designer tool.

Code	Name	Data Format	Factory Default Value Standard Configuration BMR 467 0X10/001 R1	
0x01	OPERATION	R/W Byte	0x80	
0x02	ON_OFF_CONFIG	R/W Byte	0x17	
0x03	CLEAR_FAULTS	Send Byte		
0x11	STORE_DEFAULT_ALL	Send Byte		
0x12	RESTORE_DEFAULT_ALL	Send Byte		
0x15	STORE_USER_ALL	Send Byte		
0x16	RESTORE_USER_ALL	Send Byte		
0x20	VOUT_MODE	Read Byte	0x13	
0x21	VOUT_COMMAND	R/W Word	1 x Vout by pin-strap	
0x22	VOUT_TRIM	R/W Word	0x0000	0.0 V
0x23	VOUT_CAL_OFFSET	R/W Word	Unit Specific	
0x24	VOUT_MAX	R/W Word	1.15 x Vout by pin-strap	
0x25	VOUT_MARGIN_HIGH	R/W Word	1.05 x Vout by pin-strap	
0x26	VOUT_MARGIN_LOW	R/W Word	0.95 x Vout by pin-strap	
0x27	VOUT_TRANSITION_RATE	R/W Word	0xBA00	1.0 V/ms
0x28	VOUT_DROOP	R/W Word	0x0000	0.0 mV/A
0x33	FREQUENCY_SWITCH	R/W Word	0xFA80	320.0 kHz
0x37	INTERLEAVE	R/W Word		
0x40	VOUT_OV_FAULT_LIMIT	R/W Word	1.15 x Vout by pin-strap	
0x41	VOUT_OV_FAULT_RESPONSE	R/W Byte	0xBF	
0x44	VOUT_UV_FAULT_LIMIT	R/W Word	0.85 x Vout by pin-strap	
0x45	VOUT_UV_FAULT_RESPONSE	R/W Byte	0xBF	
0x46	IOUT_OC_FAULT_LIMIT	R/W Word	0xEAB8	87.0 A
0x4B	IOUT_UC_FAULT_LIMIT	R/W Word	0xE4E0	-50.0 A
0x4F	OT_FAULT_LIMIT	R/W Word	0xEBE8	125.0 °C
0x50	OT_FAULT_RESPONSE	R/W Byte	0xBF	
0x51	OT_WARN_LIMIT	R/W Word	0xEB70	110.0 °C
0x52	UT_WARN_LIMIT	R/W Word	0xE4E0	-50.0 °C
0x53	UT_FAULT_LIMIT	R/W Word	0xE490	-55.0 °C
0x54	UT_FAULT_RESPONSE	R/W Byte	0xBF	
0x55	VIN_OV_FAULT_LIMIT	R/W Word	0xDA00	16.0 V
0x56	VIN_OV_FAULT_RESPONSE	R/W Byte	0xBF	
0x57	VIN_OV_WARN_LIMIT	R/W Word	0xD3C0	15.0 V
0x58	VIN_UV_WARN_LIMIT	R/W Word	0xCB8D	7.1 V
0x59	VIN_UV_FAULT_LIMIT	R/W Word	0xCB4D	6.6 V
0x5A	VIN_UV_FAULT_RESPONSE	R/W Byte	0xBF	
0x5E	POWER_GOOD_ON	R/W Word	0.9 x Vout by pin-strap	
0x60	TON_DELAY	R/W Word	0xCA80	5.0 ms
0x61	TON_RISE	R/W Word	0xCA80	5.0 ms
0x64	TOFF_DELAY	R/W Word	0x0000	0.0 ms
0x65	TOFF_FALL	R/W Word	0xCA80	5.0 ms
0x78	STATUS_BYTE	Read Byte		
0x79	STATUS_WORD	Read Word		
0x7A	STATUS_VOUT	Read Byte		
0x7B	STATUS_IOUT	Read Byte		
0x7C	STATUS_INPUT	Read Byte		
0x7D	STATUS_TEMPERATURE	Read Byte		
0x7E	STATUS_CML	Read Byte		
0x80	STATUS_MFR_SPECIFIC	Read Byte		
0x88	READ_VIN	Read Word		
0x8B	READ_VOUT	Read Word		
0x8C	READ_IOUT	Read Word		
0x8D	READ_TEMPERATURE_1	Read Word		
0x8E	READ_TEMPERATURE_2	Read Word		
0x8F	READ_TEMPERATURE_3	Read Word		

Code	Name	Data Format	Factory Default Value Standard Configuration BMR 467 0X10/001 R1	
0x94	READ_DUTY_CYCLE	Read Word		
0x95	READ_FREQUENCY	Read Word		
0x98	PMBUS_REVISION	Read Byte		
0x99	MFR_ID	R/W Block (22)	Unit Specific	
0x9A	MFR_MODEL	R/W Block (14)	Unit Specific	
0x9B	MFR_REVISION	R/W Block (24)	Unit Specific	
0x9C	MFR_LOCATION	R/W Block (7)	Unit Specific	
0x9D	MFR_DATE	R/W Block (10)	Unit Specific	
0x9E	MFR_SERIAL	R/W Block (13)	Unit Specific	
0xAD	IC_DEVICE_ID	Read Block (4)		
0xAE	IC_DEVICE_REV	Read Block (4)		
0xB0	USER_DATA_00	R/W Block (23)	Unit Specific	
0xB1	USER_DATA_01	R/W Block (8)	Unit Specific	
0xBF	DEADTIME_MAX	R/W Word	0x3838	56 ns, 56 ns
0xCA	IOUT0_CAL_GAIN	R/W Word	Unit Specific	
0xCB	IOUT1_CAL_GAIN	R/W Word	Unit Specific	
0xCC	IOUT0_CAL_OFFSET	R/W Word	Unit Specific	
0xCD	IOUT1_CAL_OFFSET	R/W Word	Unit Specific	
0xCE	MIN_VOUT_REG	R/W Word	0xF258	150.0 mV
0xD0	ISENSE_CONFIG	R/W Word	0x3205	
0xD1	USER_CONFIG	R/W Word	0x1480	
0xD3	GCB_CONFIG	R/W Word		
0xD4	POWER_GOOD_DELAY	R/W Word	0xC200	2.0 ms
0xD5	MULTI_PHASE_RAMP_GAIN	R/W Byte	0x03	
0xD6	INDUCTOR	R/W Word	0xA2B9	0.2 µH
0xD7	SNAPSHOT_FAULT_MASK	R/W Word	0x0100	
0xD8	OVUV_CONFIG	R/W Byte	0x0F	
0xD9	XTEMP_SCALE	R/W Word	0xBA00	
0xDA	XTEMP_OFFSET	R/W Word	0x0000	0.0 °C
0xDB	MFR_SMBALERT_MASK	R/W Block (7)	0x11000000000000	
0xDC	TEMPCO_CONFIG	R/W Byte	0x26	38 x 100ppm/°C
0xDD	DEADTIME	R/W Word	0x1010	16 ns, 16 ns
0xDE	DEADTIME_CONFIG	R/W Word	0x8888	8 x 2ns, 8 x 2ns
0xDF	ASCR_CONFIG	R/W Block (4)	0x015A012C	
0xE0	SEQUENCE	R/W Word	0x0000	
0xE1	TRACK_CONFIG	R/W Byte	0x00	
0xE2	GCB_GROUP	R/W Block (4)	0x00000000	
0xE3	READ_IOUT1	Read Word		
0xE4	DEVICE_ID	Read Block (16)		
0xE5	MFR_IOUT_OC_FAULT_RESPONSE	R/W Byte	0xBF	
0xE6	MFR_IOUT_UC_FAULT_RESPONSE	R/W Byte	0xBF	
0xE7	IOUT_AVG_OC_FAULT_LIMIT	R/W Word	0xEA60	76.0 A
0xE8	IOUT_AVG_UC_FAULT_LIMIT	R/W Word	0xDC40	-30.0 A
0xE9	MFR_USER_CONFIG	R/W Word	0x0000	
0xEA	SNAPSHOT	Read Block (32)		
0xEB	BLANK_PARAMS	Read Block (16)		
0xF0	LEGACY_FAULT_GROUP	R/W Block (4)	0x00000000	
0xF2	READ_IOUT0	Read Word		
0xF3	SNAPSHOT_CONTROL	R/W Byte	0x00	
0xF5	MFR_VMON_OV_FAULT_LIMIT	R/W Word	0xD203	8.0 V
0xF6	MFR_VMON_UV_FAULT_LIMIT	R/W Word	0xCB06	6.0 V
0xF8	VMON_OV_FAULT_RESPONSE	R/W Byte	0x00	
0xF9	VMON_UV_FAULT_RESPONSE	R/W Byte	0xBF	
0xFA	SECURITY_LEVEL	Read Byte		
0xFB	PRIVATE_PASSWORD	R/W Block (9)	Unit Specific	
0xFC	PUBLIC_PASSWORD	R/W Block (4)	Unit Specific	
0xFD	UNPROTECT	R/W Block (32)	Unit Specific	

PMBus Command Details

OPERATION (0x01)
Transfer Type: R/W Byte
Description: Controls enable and margin operations.

Bit	Function	Description	Value	Function	Description
7:6	Enable	Make the device enable or disable if PMBus Enable has been activated in ON_OFF_CONFIG.	00	Immediate Off	Disable Immediately without controlled ramp-down.
			01	Soft Off	Disable "Softly" by controlled ramp-down defined by TOFF_FALL.
			10	Enable	Enable device to the chosen voltage level.
5:4	Margin	Select between margin high/low states or nominal output.	00	Nominal	Operate at nominal output voltage.
			01	Margin Low	Operate at voltage set by command VOUT_MARGIN_LOW.
			10	Margin High	Operate at voltage set by command VOUT_MARGIN_HIGH.
3:2	Act on Fault	Controls whether the device during margining will ignore or handle overvoltage/undervoltage warnings and faults and respond as programmed by the fault response commands.	01	Ignore Faults	Ignore Faults when in a margined state.
			10	Act on Faults	Act on Faults when in a margined state.

ON_OFF_CONFIG (0x02)
Transfer Type: R/W Byte
Description: Configures how the device is controlled by the CTRL pin and the PMBus.

Bit	Function	Description	Value	Function	Description
4	Powerup Operation		1	CTRL pin or PMBus	Device does not power up until commanded by the CTRL pin or OPERATION command.
3	PMBus Enable Mode	Controls how the device responds to the PMBus command OPERATION.	0	Ignore PMBus command	Ignores the on/off portion of the OPERATION command.
			1	Use PMBus command	Device requires on by OPERATION command to enable the output voltage.
2	Enable Pin Mode	Controls how the device responds to the CTRL pin.	0	Ignore CTRL pin	Device ignores the CTRL pin.
			1	Use CTRL pin	Device requires the CTRL pin to be asserted to enable the output voltage.
1	Enable Pin Polarity	Polarity of the CTRL pin.	0	Active Low	CTRL pin will cause device to enable when driven low.
			1	Active High	CTRL pin will cause device to enable when driven high.
0	Disable Action	CTRL pin action when commanding the output to turn off.	0	Soft Off	Use the configured turn off delay and fall time.
			1	Immediate Off	Turn off the output and stop transferring energy to the output as fast as possible. The device's product literature shall specify whether or not the device sinks current to decrease the output voltage fall time.

CLEAR_FAULTS (0x03)
Transfer Type: Send Byte
Description: Clears all fault status bits

STORE_DEFAULT_ALL (0x11)
Transfer Type: Send Byte
Description: Commands the device to store its configuration into the Default Store. By default this command is protected to prevent a change of Ericsson factory values in Default NVM.

RESTORE_DEFAULT_ALL (0x12)
Transfer Type: Send Byte
Description: Commands the device to restore its configuration from the Default Store.

STORE_USER_ALL (0x15)
Transfer Type: Send Byte
Description: Stores, at the USER level, all PMBus values that were changed since the last restore command. To add to the USER store, perform a RESTORE_USER_ALL, write commands to be added, then STORE_USER_ALL. Wait 20 ms after a STORE_USER_ALL command before issuing another PMBus command.

RESTORE_USER_ALL (0x16)
Transfer Type: Send Byte
Description: Restores PMBus settings that were stored using STORE_USER_ALL. This command is automatically performed at power up. The values restored will overwrite the values previously loaded by the RESTORE_DEFAULT_ALL command. The security level is changed to Level 1 following this command. Wait 20 ms after a RESTORE_USER_ALL command before issuing another PMBus command.

VOUT_MODE (0x20)
Transfer Type: Read Byte
Description: Controls how future VOUT-related commands parameters will be interpreted.

Bit	Function	Description	Format
4:0		Five bit two's complement EXPONENT for the MANTISSA delivered as the data bytes for VOUT_COMMAND in VOUT_LINEAR Mode.	Integer Signed

Bit	Function	Description	Value	Function	Description
7:5		Selection of mode for representation of output voltage parameters.	000	Linear	Linear Mode Format.
			001	VID	VID Mode.
			010	Direct	Direct Mode.

VOUT_COMMAND (0x21)
Transfer Type: R/W Word
Description: Sets the nominal value of the output voltage.

Bit	Description	Format	Unit
15:0	Sets the nominal value of the output voltage.	Vout Mode Unsigned	V

VOUT_TRIM (0x22)
Transfer Type: R/W Word
Description: Configures a fixed offset to be applied to the output voltage when enabled.

Bit	Description	Format	Unit
15:0	Sets VOUT trim value. The range is limited to +/-150 mV.	Vout Mode Signed	V

VOUT_CAL_OFFSET (0x23)
Transfer Type: R/W Word
Description: Configures a fixed offset to be applied to the output voltage when enabled.

Bit	Description	Format	Unit

Bit	Description	Format	Unit
15:0	Sets VOUT calibration offset(same function as VOUT_TRIM).	Vout Mode Signed	V

VOUT_MAX (0x24)
Transfer Type: R/W Word
Description: Configures the maximum allowed output voltage.

Bit	Description	Format	Unit
15:0	If the device is commanded to a Vout value higher than this level, the output voltage will be clamped to this level. The max VOUT_MAX setting is 115% of the VSET pin-strap setting.	Vout Mode Unsigned	V

VOUT_MARGIN_HIGH (0x25)
Transfer Type: R/W Word
Description: Configures the target for margin-up commands.

Bit	Description	Format	Unit
15:0	Sets the output voltage value during a margin high.	Vout Mode Unsigned	V

VOUT_MARGIN_LOW (0x26)
Transfer Type: R/W Word
Description: Configures the target for margin-down commands.

Bit	Description	Format	Unit
15:0	Sets the output voltage value during a margin low.	Vout Mode Unsigned	V

VOUT_TRANSITION_RATE (0x27)
Transfer Type: R/W Word
Description: Sets the transition rate when changing output voltage.

Bit	Description	Format	Unit
15:0	Configures the transition time for margining and on-the-fly VOUT_COMMAND changes.	Linear	V/ms

VOUT_DROOP (0x28)
Transfer Type: R/W Word
Description: Configures a droop of output voltage.

Bit	Description	Format	Unit
15:0	Sets the effective load line (V/I slope) for the rail in which the device is used. When the device is part of a current sharing rail, this value must be non-zero and the same for all devices in the rail.	Linear	mV/A

FREQUENCY_SWITCH (0x33)
Transfer Type: R/W Word
Description: Controls the switching frequency.

Bit	Description	Format	Unit
15:0	Sets the switching frequency in 1 kHz steps. The specified range is 200 - 640 kHz.	Linear	kHz

INTERLEAVE (0x37)
Transfer Type: R/W Word
Description: Configures the phase offset with respect to a common SYNC clock.

Bit	Function	Description	Format
7:4	Number of Rails	Value 0-15. Sets the number of rails in the group. A value of 0 is interpreted as 16.	Integer Unsigned
3:0	Rail Position	Value 0-15. Sets position of the device's rail within the group.	Integer Unsigned

VOUT_OV_FAULT_LIMIT (0x40)
Transfer Type: R/W Word
Description: Sets the VOUT overvoltage fault threshold.

Bit	Description	Format	Unit
15:0	Sets the VOUT overvoltage fault threshold.	Vout Mode Unsigned	V

VOUT_OV_FAULT_RESPONSE (0x41)
Transfer Type: R/W Byte
Description: Sets the VOUT OV fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	10	Disable and Retry	Disable the output without delay and retry according to the setting in bits [5:3].
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Do Not Retry	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time	Retry delay time = (Value +1) * 35 ms. Sets the time between retries in 35 ms increments. Range is 35 ms to 280 ms.	000	35 ms	
			001	70 ms	
			010	105 ms	
			011	140 ms	
			100	175 ms	
			101	210 ms	
			110	245 ms	
			111	280 ms	

VOUT_UV_FAULT_LIMIT (0x44)
Transfer Type: R/W Word
Description: Sets the VOUT under-voltage fault threshold. This threshold is also used for deasserting PG (Power Good).

Bit	Description	Format	Unit
15:0	Sets the VOUT under-voltage fault threshold	Vout Mode Unsigned	V

VOUT_UV_FAULT_RESPONSE (0x45)
Transfer Type: R/W Byte
Description: Sets the VOUT UV LIMIT Response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	10	Disable and Retry	Disable the output without delay and retry according to the setting in bits [5:3].
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Do Not Retry	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.

Bit	Function	Description	Value	Function	Description
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time	Retry delay time = (Value +1) * 35 ms. Sets the time between retries in 35 ms increments. Range is 35 ms to 280 ms.	000	35 ms	
			001	70 ms	
			010	105 ms	
			011	140 ms	
			100	175 ms	
			101	210 ms	
			110	245 ms	
			111	280 ms	

IOUT_OC_FAULT_LIMIT (0x46)
Transfer Type: R/W Word
Description: Sets the output over-current peak limit.

Bit	Description	Format	Unit
15:0	Sets the IOUT overcurrent peak fault threshold for each phase, i.e. either phase can trigger an overcurrent fault. Thus, the effective fault threshold will be twice the value of this command.	Linear	A

IOUT_UC_FAULT_LIMIT (0x4B)
Transfer Type: R/W Word
Description: Sets the output under-current peak limit.

Bit	Description	Format	Unit
15:0	Sets the IOUT undercurrent peak fault threshold for each phase, i.e. either phase can trigger an undercurrent fault. Thus, the effective fault threshold will be twice the value of this command.	Linear	A

OT_FAULT_LIMIT (0x4F)
Transfer Type: R/W Word
Description: Sets the over-temperature fault limit.

Bit	Description	Format	Unit
15:0	Sets the over-temperature fault threshold.	Linear	°C

OT_FAULT_RESPONSE (0x50)
Transfer Type: R/W Byte
Description: Sets the over-temperature fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	10	Disable and Retry	Disable the output without delay and retry according to the setting in bits [5:3].
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Do Not Retry	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.

Bit	Function	Description	Value	Function	Description
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time	Retry delay time = (Value +1) * 35 ms. Sets the time between retries in 35 ms increments. Range is 35 ms to 280 ms.	000	35 ms	
			001	70 ms	
			010	105 ms	
			011	140 ms	
			100	175 ms	
			101	210 ms	
			110	245 ms	
			111	280 ms	

OT_WARN_LIMIT (0x51)
Transfer Type: R/W Word
Description: Sets the over-temperature warning limit.

Bit	Description	Format	Unit
15:0	Sets the over-temperature warning threshold.	Linear	°C

UT_WARN_LIMIT (0x52)
Transfer Type: R/W Word
Description: Sets the under-temperature warning limit.

Bit	Description	Format	Unit
15:0	Sets the undertemperature warning threshold.	Linear	°C

UT_FAULT_LIMIT (0x53)
Transfer Type: R/W Word
Description: Sets the under-temperature fault limit.

Bit	Description	Format	Unit
15:0	Sets the undertemperature fault threshold.	Linear	°C

UT_FAULT_RESPONSE (0x54)
Transfer Type: R/W Byte
Description: Sets the under-temperature fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	10	Disable and Retry	Disable the output without delay and retry according to the setting in bits [5:3].
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Do Not Retry	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time	Retry delay time = (Value +1) * 35 ms. Sets the time between retries	000	35 ms	
			001	70 ms	

Bit	Function	Description	Value	Function	Description
		in 35 ms increments. Range is 35 ms to 280 ms.	010	105 ms	
			011	140 ms	
			100	175 ms	
			101	210 ms	
			110	245 ms	
			111	280 ms	

VIN_OV_FAULT_LIMIT (0x55)
Transfer Type: R/W Word
Description: Sets the input over-voltage fault limit.

Bit	Description	Format	Unit
15:0	Sets the VIN overvoltage fault threshold.	Linear	V

VIN_OV_FAULT_RESPONSE (0x56)
Transfer Type: R/W Byte
Description: Sets the input over-voltage fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	10	Disable and Retry	Disable the output without delay and retry according to the setting in bits [5:3].
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Do Not Retry	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time	Retry delay time = (Value +1) * 35 ms. Sets the time between retries in 35 ms increments. Range is 35 ms to 280 ms.	000	35 ms	
			001	70 ms	
			010	105 ms	
			011	140 ms	
			100	175 ms	
			101	210 ms	
			110	245 ms	
			111	280 ms	

VIN_OV_WARN_LIMIT (0x57)
Transfer Type: R/W Word
Description: Sets the input over-voltage warning limit.

Bit	Description	Format	Unit
15:0	Sets the VIN overvoltage warning threshold.	Linear	V

VIN_UV_WARN_LIMIT (0x58)
Transfer Type: R/W Word
Description: Sets the input under-voltage warning limit.

Bit	Description	Format	Unit
15:0	Sets the VIN undervoltage warning threshold.	Linear	V

VIN_UV_FAULT_LIMIT (0x59)
Transfer Type: R/W Word
Description: Sets the input under-voltage fault limit.

Bit	Description	Format	Unit
15:0	Sets the VIN undervoltage fault threshold.	Linear	V

VIN_UV_FAULT_RESPONSE (0x5A)
Transfer Type: R/W Byte
Description: Sets the input under-voltage fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	10	Disable and Retry	Disable the output without delay and retry according to the setting in bits [5:3].
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Do Not Retry	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time	Retry delay time = (Value +1) * 35 ms. Sets the time between retries in 35 ms increments. Range is 35 ms to 280 ms.	000	35 ms	
			001	70 ms	
			010	105 ms	
			011	140 ms	
			100	175 ms	
			101	210 ms	
			110	245 ms	
			111	280 ms	

POWER_GOOD_ON (0x5E)
Transfer Type: R/W Word
Description: Sets the output voltage threshold for asserting PG (Power Good).

Bit	Description	Format	Unit
15:0	Sets the output voltage threshold for asserting PG (Power Good).	Vout Mode Unsigned	V

TON_DELAY (0x60)
Transfer Type: R/W Word
Description: Sets the turn-on delay time

Bit	Description	Format	Unit
15:0	Sets the delay time from ENABLE to start of the rise of the output voltage. The time can range from 3 ms up to 250 ms. For a current sharing group this range is valid if PMBus enable or CTRL pin enable is used. To guarantee operation with the slowest of input ramps in a self-enabled scenario, a minimum TON_DELAY of 30 ms is recommended.	Linear	ms

TON_RISE (0x61)
Transfer Type: R/W Word
Description: Sets the turn-on ramp-up time.

Bit	Description	Format	Unit

Bit	Description	Format	Unit
15:0	Sets the rise time of VOUT after ENABLE and On Delay. The time can range from 0 ms to 100 ms.	Linear	ms

TOFF_DELAY (0x64)
Transfer Type: R/W Word
Description: Sets the turn-off delay.

Bit	Description	Format	Unit
15:0	Sets the delay time from DISABLE to start of the fall of the output voltage. Normally the time can range from 4 ms up to 250 ms. A value of 0 ms can be set to guarantee a fast shut-off, but this will force the device to Immediate Off behaviour, even if soft-off, i.e. ramp-down, is configured (in ON_OFF_CONFIG).	Linear	ms

TOFF_FALL (0x65)
Transfer Type: R/W Word
Description: Sets the turn-off ramp-down time.

Bit	Description	Format	Unit
15:0	Sets the fall time for VOUT after DISABLE and Off Delay. The time can range from 0 ms to 100 ms.	Linear	ms

STATUS_BYTE (0x78)
Transfer Type: Read Byte
Description: Returns a brief fault/warning status byte.

Bit	Function	Description	Value	Description
7	Busy	A fault was declared because the device was busy and unable to respond.	0	No fault
			1	Fault
6	Off	This bit is asserted if the unit is not providing power to the output due to not being enabled, i.e. not set when output shuts-down due to a fault.	0	No fault
			1	Fault
5	Vout Overvoltage Fault	An output overvoltage fault has occurred.	0	No fault
			1	Fault
4	Iout Overcurrent Fault	An output overcurrent fault has occurred.	0	No fault
			1	Fault
3	Vin Undervoltage Fault	An input undervoltage fault has occurred.	0	No fault
			1	Fault
2	Temperature	A temperature fault or warning has occurred.	0	No fault
			1	Fault
1	Communication/Logic	A communications, memory or logic fault has occurred.	0	No fault
			1	Fault

STATUS_WORD (0x79)
Transfer Type: Read Word
Description: Returns an extended fault/warning status byte.

Bit	Function	Description	Value	Description
15	Vout	An output voltage fault or warning has occurred.	0	No fault
			1	Fault
14	Iout	An output current fault or warning has occurred.	0	No Fault.
			1	Fault.
13	Input	An input voltage, input current, or input power fault or warning has occurred.	0	No Fault.
			1	Fault.
12	Mfr	A manufacturer specific fault or warning has occurred.	0	No Fault.
			1	Fault.
11	Power-Good	The Power-Good signal, if present, is negated.	0	No Fault.
			1	Fault.
9	Other	A bit in STATUS_VOUT, STATUS_IOUT, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_CML or STATUS_MFR_SPECIFIC is set.	0	No Fault.
			1	Fault.
7	Busy	A fault was declared because the device was busy	0	No Fault.

Bit	Function	Description	Value	Description
		and unable to respond.	1	Fault.
6	Off	This bit is asserted if the unit is not providing power to the output due to not being enabled, i.e. not set when output shuts-down due to a fault.	0	No Fault.
			1	Fault.
5	Vout Overvoltage Fault	An output overvoltage fault has occurred.	0	No Fault.
			1	Fault.
4	Iout Overcurrent Fault	An output overcurrent fault has occurred.	0	No Fault.
			1	Fault.
3	Vin Undervoltage Fault	An input undervoltage fault has occurred.	0	No Fault.
			1	Fault.
2	Temperature	A temperature fault or warning has occurred.	0	No Fault.
			1	Fault.
1	Communication/Logic	A communications, memory or logic fault has occurred.	0	No fault.
			1	Fault.

STATUS_VOUT (0x7A)
Transfer Type: Read Byte
Description: Returns Vout-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Vout Overvoltage Fault	Vout Overvoltage Fault.	0	No Fault.
			1	Fault.
4	Vout Undervoltage Fault	Vout Undervoltage Fault.	0	No Fault.
			1	Fault.

STATUS_IOUT (0x7B)
Transfer Type: Read Byte
Description: Returns Iout-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Iout Overcurrent Fault	Iout Overcurrent Fault.	0	No Fault.
			1	Fault.
4	Iout Undercurrent Fault	Iout Undercurrent Fault.	0	No Fault.
			1	Fault.

STATUS_INPUT (0x7C)
Transfer Type: Read Byte
Description: Returns VIN/IIN-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Vin Overvoltage Fault	Vin Overvoltage Fault.	0	No Fault.
			1	Fault.
6	Vin Overvoltage Warning	VIN Overvoltage Warning.	0	No Warning.
			1	Warning.
5	Vin Undervoltage Warning	Vin Undervoltage Warning.	0	No Warning.
			1	Warning.
4	Vin Undervoltage Fault	Vin Undervoltage Fault.	0	No Fault.
			1	Fault.

STATUS_TEMPERATURE (0x7D)
Transfer Type: Read Byte
Description: Returns the temperature-related fault/warning status bits

Bit	Function	Description	Value	Description
7	Overtemperature Fault	Overtemperature Fault.	0	No Fault.
			1	Fault.
6	Overtemperature Warning	Overtemperature Warning.	0	No Warning.
			1	Warning.
5	Undertemperature Warning	Undertemperature Warning.	0	No Warning.
			1	Warning.

Bit	Function	Description	Value	Description
4	Undertemperature Fault	Undertemperature Fault.	0	No Fault.
			1	Fault.
3	Internal Temp Sensor Fault	A warning or fault occurred from the internal temperature sensor.	0	No Fault.
			1	Fault.
2	External Temp Sensor 0 Fault	A warning or fault occurred from the external temperature sensor 0 (not used).	0	No Fault.
			1	Fault.
1	External Temp Sensor 1 Fault	A warning or fault occurred from the external temperature sensor 1 (not used).	0	No Fault.
			1	Fault.

STATUS_CML (0x7E)
Transfer Type: Read Byte
Description: Returns Communication/Logic/Memory-related fault/warning status bits.

Bit	Function	Description	Value	Description
7	Invalid Or Unsupported Command Received	Invalid Or Unsupported Command Received.	0	No Invalid Command Received.
			1	Invalid Command Received.
6	Invalid Or Unsupported Data Received	Invalid Or Unsupported Data Received.	0	No Invalid Data Received.
			1	Invalid Data Received.
5	Packet Error Check Failed	Packet Error Check (PEC) Failed.	0	No Failure.
			1	Failure.
3	CRC Fault	A CRC fault was detected.	0	No Fault.
			1	Fault.
2	CPU Fault	A CPU fault was detected.	0	No Fault.
			1	Fault.
1	Other Communication Fault	A PMBus command tried to write to a read-only or protected command, or a communication fault other than the ones listed in this table has occurred.	0	No Fault.
			1	Fault.

STATUS_MFR_SPECIFIC (0x80)
Transfer Type: Read Byte
Description: Returns manufacturer specific status information.

Bit	Function	Description	Value	Description
7	Multi phase init error	A phase or phases of a multi-phase current sharing group did not initialize.	0	No Fault.
			1	Fault.
6	GCB fault	An error occurred in GCB communication	0	No Fault.
			1	Fault.
5	VMON UV warning	VMON under voltage warning. The warning limit is 110% of the configured VMON UV fault limit.	0	No Fault.
			1	Fault.
4	VMON OV warning	VMON over voltage warning. The warning limit is 95% of the configured VMON OV fault limit.	0	No Fault.
			1	Fault.
3	Clock Fail/Loss of sync	External Switching Period Fault (TSW); indicates loss of external SYNC clock.	0	No Fault.
			1	Fault.
2	Group fault	A rail in the fault group has failed.	0	No Fault.
			1	Fault.
1	VMON UV fault	VMON under voltage fault	0	No Fault.
			1	Fault.
0	VMON OV fault	VMON over voltage fault.	0	No Fault.
			1	Fault.

READ_VIN (0x88)
Transfer Type: Read Word
Description: Returns the measured input voltage.

Bit	Description	Format	Unit
15:0	Returns the input voltage reading.	Linear	V

READ_VOUT (0x8B)
Transfer Type: Read Word
Description: Returns the measured output voltage.

Bit	Description	Format	Unit
15:0	Returns the measured output voltage.	Vout Mode Unsigned	V

READ_IOUT (0x8C)
Transfer Type: Read Word
Description: Returns the measured output current.

Bit	Description	Format	Unit
15:0	Returns the output current reading. The device will NACK this command when not enabled and not in the USER_CONFIG monitor mode.	Linear	A

READ_TEMPERATURE_1 (0x8D)
Transfer Type: Read Word
Description: Returns the measured temperature (internal).

Bit	Description	Format	Unit
15:0	Returns the measured temperature of internal sensor.	Linear	°C

READ_TEMPERATURE_2 (0x8E)
Transfer Type: Read Word
Description: Returns the measured temperature of external sensor 0 (not used).

Bit	Description	Format	Unit
15:0	Returns the measured temperature of external sensor 0 (not used).	Linear	°C

READ_TEMPERATURE_3 (0x8F)
Transfer Type: Read Word
Description: Returns the measured temperature of external sensor 1 (not used).

Bit	Description	Format	Unit
15:0	Returns the measured temperature of external sensor 1 (not used).	Linear	°C

READ_DUTY_CYCLE (0x94)
Transfer Type: Read Word
Description: Returns the measured duty cycle in percent.

Bit	Description	Format	Unit
15:0	Returns the target duty cycle during the ENABLE state. The device will NACK this command when not enabled and not in the USER_CONFIG monitor mode.	Linear	%

READ_FREQUENCY (0x95)
Transfer Type: Read Word
Description: Returns the measured switching frequency.

Bit	Description	Format	Unit
15:0	Returns the measured operating switch frequency.	Linear	kHz

PMBUS_REVISION (0x98)
Transfer Type: Read Byte
Description: Returns the PMBus revision number for this device.

Bit	Function	Description	Value	Function	Description
7:4	Part I Revision	Part I Revision.	0000	1.0	Part I Revision 1.0.
			0001	1.1	Part I Revision 1.1.
			0010	1.2	Part I Revision 1.2.

Bit	Function	Description	Value	Function	Description
3:0	Part II Revision	Part II Revision.	0000	1.0	Part II Revision 1.0.
			0001	1.1	Part II Revision 1.1.
			0010	1.2	Part II Revision 1.2.

MFR_ID (0x99)
Transfer Type: R/W Block (22 bytes)
Description: Sets the manufacturer ID String.

Bit	Description	Format
175:0	Maximum of 22 characters.	ASCII

MFR_MODEL (0x9A)
Transfer Type: R/W Block (14 bytes)
Description: Sets the manufacturer model string.

Bit	Description	Format
111:0	Maximum of 14 characters.	ASCII

MFR_REVISION (0x9B)
Transfer Type: R/W Block (24 bytes)
Description: Sets the manufacturer revision string.

Bit	Description	Format
191:0	Maximum of 24 characters.	ASCII

MFR_LOCATION (0x9C)
Transfer Type: R/W Block (7 bytes)
Description: Sets the manufacturer location string.

Bit	Description	Format
55:0	Maximum of 7 characters.	ASCII

MFR_DATE (0x9D)
Transfer Type: R/W Block (10 bytes)
Description: Sets the manufacturer date at YYMMDD.

Bit	Description	Format
79:0	Maximum of 10 characters.	ASCII

MFR_SERIAL (0x9E)
Transfer Type: R/W Block (13 bytes)
Description: Sets the manufacturer serial string.

Bit	Description	Format
103:0	Maximum of 13 characters.	ASCII

IC_DEVICE_ID (0xAD)
Transfer Type: Read Block (4 bytes)
Description: Reports identification information (not used)

Bit	Description	Format
31:0	Reports identification information (not used)	Byte Array

IC_DEVICE_REV (0xAE)
Transfer Type: Read Block (4 bytes)
Description: Reports revision information (not used)

Bit	Description	Format
31:0	Reports revision information (not used)	Byte Array

USER_DATA_00 (0xB0)
Transfer Type: R/W Block (23 bytes)
Description: Sets a user defined data string.

Bit	Description	Format
183:0	Maximum of 23 characters.	ASCII

USER_DATA_01 (0xB1)
Transfer Type: R/W Block (8 bytes)
Description: Sets a user defined data string. This is a fixed length command with dedicated 8 bytes. If the string is shorter than 8 characters the program will fill with zero data up to 8 bytes.

Bit	Description	Format
63:0	Maximum of 8 characters.	ASCII fixed length

DEADTIME_MAX (0xBF)
Transfer Type: R/W Word
Description: Sets the maximum deadtime value for the adaptive deadtime algorithm.

Bit	Function	Description	Format	Unit
14:8	Deadtime max	Value 0 to 60 ns. Maximum allowed H-L (high-side to low-side) deadtime.	Integer Signed	ns
6:0	Deadtime max	Value 0 to 60 ns. Maximum allowed L-H (low-side to high-side) deadtime.	Integer Signed	ns

IOUT0_CAL_GAIN (0xCA)
Transfer Type: R/W Word
Description: Sets the current sense resistance for phase 0.

Bit	Description	Format	Unit
15:0	Sets the effective impedance for phase 0 current sensing at +25°C.	Linear	mΩ

IOUT1_CAL_GAIN (0xCB)
Transfer Type: R/W Word
Description: Sets the current sense resistance for phase 1.

Bit	Description	Format	Unit
15:0	Sets the effective impedance for phase 1 current sensing at +25°C.	Linear	mΩ

IOUT0_CAL_OFFSET (0xCC)
Transfer Type: R/W Word
Description: Sets the current-sense offset for phase 0.

Bit	Description	Format	Unit
15:0	Sets an offset to phase 0 IOUT readings. Use to compensate for delayed measurements of current ramp.	Linear	A

IOUT1_CAL_OFFSET (0xCD)
Transfer Type: R/W Word
Description: Sets the current-sense offset for phase 1.

Bit	Description	Format	Unit
15:0	Sets an offset to phase 1 IOUT readings. Use to compensate for delayed measurements of current ramp.	Linear	A

MIN_VOUT_REG (0xCE)
Transfer Type: R/W Word
Description: Minimum regulation voltage.

Bit	Description	Format	Unit
15:0	Sets the minimum output voltage that the device will attempt to regulate to during start-up and shut-down ramps.	Linear	mV

ISENSE_CONFIG (0xD0)
Transfer Type: R/W Word
Description: Configures the current sense circuitry.

Bit	Function	Description	Value	Function	Description
15:11	Current Sense Blanking Delay	Sets the current sense blanking time (i.e. the time after switch transition before current measurement starts) in increments of 32ns.	00000	0 ns	
			00001	32 ns	
			00010	64 ns	
			00011	96 ns	
			00100	128 ns	
			00101	160 ns	
			00110	192 ns	
			00111	224 ns	
			01000	256 ns	
			01001	288 ns	
			01010	320 ns	
			01011	352 ns	
			01100	384 ns	
			01101	416 ns	
			01110	448 ns	
			01111	480 ns	
			10000	512 ns	
			10001	544 ns	
			10010	576 ns	
			10011	608 ns	
			10100	640 ns	
			10101	672 ns	
			10110	704 ns	
			10111	736 ns	
			11000	768 ns	
			11001	800 ns	
			11010	832 ns	
10:8	Current Sense Fault Count	Sets the number of consecutive over-current (OC) or under-current (UC) events required for a fault. An event can occur once during each switching cycle. For example, if 5 is selected, an OC or UC event must occur for 5 consecutive switching cycles, resulting in a delay of at least 5 switching periods.	000	1	
			001	3	
			010	5	
			011	7	
			100	9	
			101	11	
			110	13	
			111	15	
3:2	Current Sense Control	Selection of DCR current sensing method across inductor.	01	DCR Down Slope	Measurements at down slope of ripple current.
			10	DCR Up Slope	Measurements at up slope of ripple current.
1:0	Current Sense Range	Sets the range of the current sense ADC.	00	Low range ±25 mV	
			01	Mid range ±35 mV	
			10	High range ±50 mV	

USER_CONFIG (0xD1)
Transfer Type: R/W Word
Description: Sets misc. device configurations.

Bit	Function	Description	Format

Bit	Function	Description	Format
15:11	Minimum Duty Cycle	Value 0-31. Sets the minimum duty cycle to 2 x (value + 1) / 512 x Tsw when enabled by Bit 7 (Tsw = switching period).	Integer Unsigned

Bit	Function	Description	Value	Function	Description
10	Power device drive	Enable or disable power device drive.	1		Power device drive is enabled.
			0		Power device drive is disabled.
7	Min. Duty Cycle Control	Enable or disable minimum duty cycle.	1		Minimum Duty Cycle Enabled.
			0		Minimum Duty Cycle Disabled.
2	PG Pin Output Control	PG Pin Output Control.	0	Open-Drain	PG is open-drain
			1	Push-Pull	PG is push-pull
1	Ext. Temp Sense	Enable or disable external temperature sensor (not used). When enabled it will be used for temp compensation of read current.	1		External temperature sensor enabled.
			0		External temperature sensor disabled.
0	Ext. Temp Sense for Faults	Selects external temperature sensor to determine temperature faults (not used).	1		Select external temperature sensor.
			0		Do not select external temperature sensor (internal sensor is used).

GCB_CONFIG (0xD3)
Transfer Type: R/W Word
Description: Configures the Group Communication Bus addressing and current sharing.

Bit	Function	Description	Format
12:8	GCB/Rail ID	Value 0-31. Sets the rail's GCB ID for current sharing, sequencing and fault spreading. All devices within a current sharing group must be assigned the same GCB ID.	Integer Unsigned

Bit	Function	Description	Value	Function	Description
15:13	Phase ID	Value 0-3. Sets a device's position within a current sharing group (-1).	00	Position 1	
			01	Position 2	
			10	Position 3	
			11	Position 4	
3:0	Phases in rail	Value 1, 3, 5 or 7. Identifies the number of phases on the same rail.	001	2 phases	
			011	4 phases	
			101	6 phases	
			111	8 phases	

POWER_GOOD_DELAY (0xD4)
Transfer Type: R/W Word
Description: Sets the Power-Good delay time.

Bit	Description	Format	Unit
15:0	Sets the delay applied between the output exceeding the PG threshold (POWER_GOOD_ON) and asserting the PG pin. The delay time can range from 0 ms up to 5000 ms. Inside the device, the set value will be rounded to closest integer value.	Linear	ms

MULTI_PHASE_RAMP_GAIN (0xD5)
Transfer Type: R/W Byte
Description: This command value indirectly determines the output voltage rise time for current sharing rails. Typical gain values range from 1 to 5. Lower gain values produce longer ramp times. This ramp mode is automatically selected when the product is configured for current sharing. When in current sharing ramp mode, the normal high bandwidth turn-on ramp is disabled, resulting in a lower loop bandwidth during start-up ramps. Large load current transitions during multi-phase ramp-ups will cause output voltage discontinuities. Once Power Good has been asserted, the normal high bandwidth control loop is enabled and the product operates normally. When in a current sharing setup, Soft Off ramps are not allowed (TOFF_FALL is ignored).

Bit	Description	Format
7:0	Current sharing ramp-up gain value.	Integer Unsigned

INDUCTOR (0xD6)
Transfer Type: R/W Word
Description: Informs the device of circuit's inductor value.

Bit	Description	Format	Unit
15:0	This is used in adaptive algorithm calculations relating to the inductor ripple current. Range is 0-100 µH.	Linear	µH

SNAPSHOT_FAULT_MASK (0xD7)
Transfer Type: R/W Word
Description: Masking for which faults will trigger a snapshot NVM write.

Bit	Function	Description	Value	Description
13	Group fault	Block fault from when a rail in your fault group has faulted.	1	Trigger blocked
			0	Trigger enabled
12	Phase fault	Block fault from when a phase in your rail has faulted.	1	Trigger blocked
			0	Trigger enabled
11	CPU fault	Block general purpose CPU fault.	1	Trigger blocked
			0	Trigger enabled
10	CRC fault	Block memory CRC fault	1	Trigger blocked
			0	Trigger enabled
9	VMON UV fault	Block VMON under voltage fault	1	Trigger blocked
			0	Trigger enabled
8	VMON OV fault	Block VMON over voltage fault	1	Trigger blocked
			0	Trigger enabled
7	Iout UC fault	Block output under current fault	1	Trigger blocked
			0	Trigger enabled
6	Iout OC fault	Block output over current fault	1	Trigger blocked
			0	Trigger enabled
5	Vin UV fault	Block input under voltage fault	1	Trigger blocked
			0	Trigger enabled
4	Vin OV fault	Block input over voltage fault	1	Trigger blocked
			0	Trigger enabled
3	UT fault	Block under temperature fault	1	Trigger blocked
			0	Trigger enabled
2	OT fault	Block over temperature fault	1	Trigger blocked
			0	Trigger enabled
1	Vout UV fault	Block output under voltage fault	1	Trigger blocked
			0	Trigger enabled
0	Vout OV fault	Block output over voltage fault	1	Trigger blocked
			0	Trigger enabled

OVUV_CONFIG (0xD8)
Transfer Type: R/W Byte
Description: Sets output OV/UV control features.

Bit	Function	Description	Format
3:0	No Of Limit Violations	Value 0-15. Value + 1 consecutive OV or UV violations to initiate a fault response.	Integer Unsigned

Bit	Function	Description	Value	Description
7	OV Fault Control (Crowbar)	Control of low-side power switch after an Over Voltage fault.	0	An OV fault does not enable the low-side power device.
			1	An OV fault enables the low-side power device.

XTEMP_SCALE (0xD9)
Transfer Type: R/W Word
Description: Scale for external temp sensor (not used).

Bit	Description	Format
15:0	The constant is applied to the equation READ_TEMPERATURE_2/3 = ExternalTemperature / XTEMP_SCALE + XTEMP_OFFSET to produce the read value via the PMBus command READ_TEMPERATURE_2/3.	Linear

XTEMP_OFFSET (0xDA)
Transfer Type: R/W Word
Description: Offset for external temp sensor (not used).

Bit	Description	Format	Unit
15:0	The constant is applied to the equation READ_TEMPERATURE_2/3 = ExternalTemperature / XTEMP_SCALE + XTEMP_OFFSET to produce the read value via the PMBus command READ_TEMPERATURE_2/3.	Linear	°C

MFR_SMBALERT_MASK (0xDB)
Transfer Type: R/W Block (7 bytes)
Description: Masking of which warning or fault indications that will trigger an assertion of the SALERT signal output. Each byte corresponds to masking of one status command according to: Byte 0: Mask of STATUS_VOUT [7:0] Byte 1: Mask of STATUS_IOUT [7:0] Byte 2: Mask of STATUS_INPUT [7:0] Byte 3: Mask of STATUS_TEMPERATURE [7:0] Byte 4: Mask of STATUS_CML [7:0] Byte 5: Mask of STATUS_OTHER[7:0] Byte 6: Mask of STATUS_MFR_SPECIFIC [7:0]

Bit	Function	Description	Value	Description
55	Multi phase init error	A phase or phases of a multi-phase current sharing group did not initialize.	1	Trigger blocked
			0	Trigger enabled
54	GCB fault	An error occurred in GCB communication	1	Trigger blocked
			0	Trigger enabled
53	VMON UV warning	VMON under voltage warning. The warning limit is 110% of the configured VMON UV fault limit.	1	Trigger blocked
			0	Trigger enabled
52	VMON OV warning	VMON over voltage warning. The warning limit is 95% of the configured VMON OV fault limit.	1	Trigger blocked
			0	Trigger enabled
51	Clock Fail/Loss of sync	External Switching Period Fault (TSW); indicates loss of external SYNC clock.	1	Trigger blocked
			0	Trigger enabled
50	Rail fault in group	One of the rails in your group faulted	1	Trigger blocked
			0	Trigger enabled
49	VMON UV fault	VMON under voltage fault	1	Trigger blocked
			0	Trigger enabled
48	VMON OV fault	VMON over voltage fault	1	Trigger blocked
			0	Trigger enabled
39	Invalid Or Unsupported Command Received	Invalid Or Unsupported Command Received.	1	Trigger blocked
			0	Trigger enabled
38	Invalid Or Unsupported Data Received	Invalid Or Unsupported Data Received.	1	Trigger blocked
			0	Trigger enabled
37	Packet Error Check Failed	Packet Error Check Failed.	1	Trigger blocked
			0	Trigger enabled
33	Other Communication Fault	A PMBus command tried to write to a read-only or protected command, or a communication fault other than the ones listed in this table has occurred.	1	Trigger blocked
			0	Trigger enabled
31	Overtemperature Fault	Overtemperature Fault.	1	Trigger blocked
			0	Trigger enabled
30	Overtemperature Warning	Overtemperature Warning.	1	Trigger blocked
			0	Trigger enabled
29	Undertemperature Warning	Undertemperature Warning.	1	Trigger blocked
			0	Trigger enabled
28	Undertemperature Fault	Undertemperature Fault.	1	Trigger blocked
			0	Trigger enabled
27	Internal Temp Sensor Fault	A warning or fault occurred from the internal temperature sensor.	1	Trigger blocked
			0	Trigger enabled
26	External Temp Sensor 0 Fault	A warning or fault occurred from the external temperature sensor 0.	1	Trigger blocked
			0	Trigger enabled
25	External Temp	A warning or fault occurred from the external	1	Trigger blocked

Bit	Function	Description	Value	Description
	Sensor 1 Fault	temperature sensor 1.	0	Trigger enabled
23	Vin Overvoltage Fault	Vin Overvoltage Fault.	1	Trigger blocked
			0	Trigger enabled
22	Vin Overvoltage Warning	VIN Overvoltage Warning.	1	Trigger blocked
			0	Trigger enabled
21	Vin Undervoltage Warning	Vin Undervoltage Warning.	1	Trigger blocked
			0	Trigger enabled
20	Vin Undervoltage Fault	Vin Undervoltage Fault.	1	Trigger blocked
			0	Trigger enabled
15	Iout Overcurrent Fault	Iout Overcurrent Fault.	1	Trigger blocked
			0	Trigger enabled
12	Iout Undercurrent Fault	Iout Undercurrent Fault.	1	Trigger blocked
			0	Trigger enabled
11	Iout fault on Phase 0	Iout fault on Phase 0	1	Trigger blocked
			0	Trigger enabled
10	Iout fault on Phase 1	Iout fault on Phase 1	1	Trigger blocked
			0	Trigger enabled
7	Vout Overvoltage Fault	Vout Overvoltage Fault.	1	Trigger blocked
			0	Trigger enabled
4	Vout Undervoltage Fault	Vout Undervoltage Fault.	1	Trigger blocked
			0	Trigger enabled

TEMPCO_CONFIG (0xDC)
Transfer Type: R/W Byte
Description: Temp correction factor for measured output current.

Bit	Function	Description	Format	Unit
6:0	Isense Temperature Correction	Configures the correction factor TC for output current sense. When using external temperature sensors, the coefficient applies to both temperature sensors. RSEN (DCR) = IOUT_CAL_GAIN x (1 + TC x 10^-4 x (T - 25)) where RSEN = resistance of sense element.	Integer Unsigned	x 100ppm/°C

Bit	Function	Description	Value	Function	Description
7	Temperature correction source	Selects the temperature sensor source for current sense temp correction. (To use the external temp sensor it must be enabled in USER_CONFIG).	0	Internal temp sensor	Selects the internal temperature sensor.
			1	External temp sensor	Selects the external temperature sensors.

DEADTIME (0xDD)
Transfer Type: R/W Word
Description: Configures power switch dead times.

Bit	Function	Description	Format	Unit
15:8	Deadtime H-L	Value -10 to 60 ns. Controls the high-side to low-side deadtime value. Positive values imply a non-overlap of the FET drive on-times. Negative values imply an overlap of the FET drive on-times. The default value of the maximum deadtime for the adaptive deadtime algorithm is 60ns. Writing a value to this command immediately before writing the DEADTIME_CONFIG command will set a new maximum for the adaptive deadtime algorithm. The device will operate at the deadtime values written to this command when adaptive deadtime is disabled.	Integer Signed	ns
7:0	Deadtime L-H	Value -10 to 60 ns. Controls the low-side to high-side deadtime value. Positive values imply a non-overlap of the FET drive on-times. Negative values imply an overlap of the FET drive on-times. Writing a value to this command immediately before writing the DEADTIME_CONFIG command will set a new maximum for the adaptive deadtime algorithm. The device will operate at the deadtime values written to this command when adaptive deadtime is disabled.	Integer Signed	ns

DEADTIME_CONFIG (0xDE)
Transfer Type: R/W Word
Description: Configures the deadtime optimization mode.

Bit	Function	Description	Format	Unit
14:8	Min Deadtime H-L	Value -5 to 28 ns. Limits the minimum allowed H-to-L deadtime for adaptive algorithm to value x 2 ns (signed).	Integer Signed	x 2ns
6:0	Min. L-H Deadtime	Value -5 to 28 ns. Limits the minimum allowed L-to-H deadtime for adaptive algorithm to value x 2ns (signed).	Integer Signed	x 2ns

Bit	Function	Description	Value	Function	Description
15	H-L Deadtime Mode	Selects adaptive or fixed H-to-L dead time.	0	Adaptive	Adaptive H-to-L deadtime control.
			1	Freeze	Freeze the H-to-L deadtime.
7	L-H Deadtime Mode	Selects adaptive or fixed L-to-H dead time.	0	Adaptive	Adaptive L-to-H deadtime control.
			1	Freeze	Freeze the L-to-H deadtime.

ASCR_CONFIG (0xDF)
Transfer Type: R/W Block (4 bytes)
Description: Control loop settings

Bit	Function	Description	Format
23:16	ASCR Residual	Residual factor	Integer Unsigned
15:0	ASCR Gain	Gain factor	Integer Unsigned

Bit	Function	Description	Value	Description
24	ASCR Enable	Enable or disable the ASCR function.	1	ASCR enabled
			0	ASCR disabled

SEQUENCE (0xE0)
Transfer Type: R/W Word
Description: The device will enable its output when its CTRL or OPERATION enable state, as defined by ON_OFF_CONFIG, is set and the prequel device has issued a Power-Good event on the GCB bus. The device will disable its output (using the programmed delay values) when the sequel device has issued a Power-Down event on the GCB bus. The data field is a two-byte value. The most-significant byte contains the 5-bit Rail GCB ID of the prequel device. The least-significant byte contains the 5-bit Rail GCB ID of the sequel device. The most significant bit of each byte contains the enable of the prequel or sequel mode.

Bit	Function	Description	Format
12:8	Prequel Rail GCB ID	Value 0-31. Set to the Rail GCB ID of the rail that should precede this device's rail in a sequence order.	Integer Unsigned
4:0	Sequel Rail GCB ID	Value 0-31. Set to the Rail GCB ID of the rail that should follow this device's rail in a sequence order.	Integer Unsigned

Bit	Function	Description	Value	Description
15	Prequel Enable	Prequel Enable/Disable.	0	Disable, no prequel preceding this rail.
			1	Enable, prequel to this rail is defined by bits 12:8.
7	Sequel Enable	Sequel Enable/Disable.	0	Disable, no sequel following this rail.
			1	Enable, sequel to this rail is defined by bits 4:0.

TRACK_CONFIG (0xE1)
Transfer Type: R/W Byte
Description: Configures the voltage tracking modes of the device

Bit	Function	Description	Value	Function	Description
7	Enable Voltage Tracking	Enables voltage tracking.	0		Tracking is disabled.
			1		Tracking is enabled.
2	Upper Tracking Ratio	Controls upper tracking ratio.	0	Output Tracks 100% Of VTRK	Output tracks 100% of VTRK.
			1	Output Tracks 50% Of VTRK	Output tracks 50% of VTRK.
1	Upper Track Limit	Controls upper track limit.	0	Limited By Target Voltage	Output is limited by target voltage.
			1	Limited By VTRK	Output is limited by VTRK pin.

GCB_GROUP (0xE2)
Transfer Type: R/W Block (4 bytes)
Description: Rails (output voltages) are assigned group numbers in order to share specific behaviours. The GCB_GROUP configures fault spreading group ID and enable, broadcast OPERATION group ID and enable, and broadcast VOUT_COMMAND group ID and enable. Note that GCB Groups are separate and unique from GCB Phases. Current sharing rails need to be in the same DDC Group in order to respond to broadcast VOUT_COMMAND and OPERATION commands. Power fail event responses are automatically spread in current sharing rails when they are configured using GCB_CONFIG, regardless of their setting in GCB_GROUP.

Bit	Function	Description	Format
20:16	Broadcast VOUT_COMMAND Group ID	Group ID (0-31) sent as data for broadcast VOUT_COMMAND command events.	Integer Unsigned
12:8	Broadcast OPERATION Group ID	Group ID (0-31) sent as data for broadcast OPERATION command events.	Integer Unsigned
4:0	Fault Spreading Group ID	Group ID (0-31) sent as data for broadcast power fail events.	Integer Unsigned

Bit	Function	Description	Value	Function	Description
21	Broadcast VOUT_COMMAND Response	Controls how the device should respond to a received broadcast VOUT_COMMAND command event.	0	Ignore events	Ignores broadcast VOUT_COMMAND command events.
			1	Respond to events	Respond to broadcast VOUT_COMMAND command events with same Broadcast VOUT_COMMAND Group ID.
13	Broadcast OPERATION Response	Controls how the device should respond to a received broadcast OPERATION command event.	0	Ignore events	Ignores broadcast OPERATION command events.
			1	Respond to events	Respond to broadcast OPERATION command events with same Broadcast Enable Group ID.
5	Fault Spreading Response	Controls how the device should respond to a received broadcast power fail event.	0	Sequenced Shutdown	Responds to power fail events with same Power Fail Group ID with sequenced shutdown.
			1	Immediate Shutdown	Responds to power fail events with same Power Fail Group ID by shutting down immediately.

READ_IOUT1 (0xE3)
Transfer Type: Read Word
Description: Returns the measured output current of phase 1.

Bit	Description	Format	Unit
15:0	Returns the output current reading of phase 1.	Linear	A

DEVICE_ID (0xE4)
Transfer Type: Read Block (16 bytes)
Description: Returns the 16-byte (character) device identifier string.

Bit	Description	Format
127:0	Returns the 16-byte (character) device identifier string.	ASCII

MFR_IOUT_OC_FAULT_RESPONSE (0xE5)
Transfer Type: R/W Byte
Description: Configures the output overcurrent fault response. The command format is the same as the PMBus standard responses for voltage and temperature faults except that it sets the overcurrent status bit.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	10	Disable and Retry	Disable the output without delay and retry according to the setting in bits [5:3].
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Do Not Retry	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time	Retry delay time = (Value +1) * 35 ms. Sets the time between retries in 35 ms increments. Range is 35 ms to 280 ms.	000	35 ms	
			001	70 ms	
			010	105 ms	
			011	140 ms	
			100	175 ms	
			101	210 ms	
			110	245 ms	
			111	280 ms	

MFR_IOUT_UC_FAULT_RESPONSE (0xE6)
Transfer Type: R/W Byte
Description: Configures the output undercurrent fault response. The command format is the same as the PMBus standard responses for voltage and temperature faults except that it sets the undercurrent status bit.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	10	Disable and Retry	Disable the output without delay and retry according to the setting in bits [5:3].
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Do Not Retry	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time	Retry delay time = (Value +1) * 35	000	35 ms	

Bit	Function	Description	Value	Function	Description
		ms. Sets the time between retries in 35 ms increments. Range is 35 ms to 280 ms.	001	70 ms	
			010	105 ms	
			011	140 ms	
			100	175 ms	
			101	210 ms	
			110	245 ms	
			111	280 ms	

IOUT_AVG_OC_FAULT_LIMIT (0xE7)
Transfer Type: R/W Word
Description: Sets the IOUT average overcurrent fault threshold for each phase. For down-slope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the 1-D interval). For up-slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the D interval). This feature shares the OC fault bit operation (in STATUS_IOUT) and OC fault response with IOUT_OC_FAULT_LIMIT.

Bit	Description	Format	Unit
15:0	Sets the IOUT average overcurrent fault threshold for each phase. Thus, the effective fault threshold will be twice the value of this command.	Linear	A

IOUT_AVG_UC_FAULT_LIMIT (0xE8)
Transfer Type: R/W Word
Description: Sets the IOUT average undercurrent fault threshold for each phase. For down-slope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the 1-D interval). For up-slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the Current Sense Blanking time (which occurs at the beginning of the D interval). This feature shares the UC fault bit operation (in STATUS_IOUT) and UC fault response with IOUT_UC_FAULT_LIMIT.

Bit	Description	Format	Unit
15:0	Sets the IOUT average undercurrent fault threshold for each phase. Thus, the effective fault threshold will be twice the value of this command.	Linear	A

MFR_USER_CONFIG (0xE9)
Transfer Type: R/W Word
Description: This command is used to set options for output voltage sensing, maximum output voltage override, SMBus timeout, and GCB and SYNC output configurations.

Bit	Function	Description	Value	Function	Description
6	GCB Output Control	Configures how the GCB pin is used.	0	Open drain	GCB output is open-drain.
			1	Push-pull	GCB output is push-pull.
4	SMBus Timeout Enable	Enables or disables SMBus time-outs.	0		SMBus time-outs enabled.
			1		SMBus time-outs disabled.
2:1	Sync IO Control	Configures how the SYNC pin is used	00	SYNC pin not used	The internal clock is used for regulator's switching.
			01	SYNC pin as output	The internal clock is output on the SYNC pin, while also being used for regulator's switching.
			10	SYNC pin as input	An external clock on the SYNC pin is used for regulator's switching.

SNAPSHOT (0xEA)
Transfer Type: Read Block (32 bytes)
Description: The SNAPSHOT command is a 32-byte read-back of parametric and status values. It allows monitoring and status data to be stored to NVM either during a fault condition or via SNAPSHOT_CONTROL command. Snapshot is continuously updated in RAM (also when the output is disabled) and can be read using the SNAPSHOT command. When a fault occurs, and that fault is not masked off by the SNAPSHOT_MASK command, the update of snapshot in RAM is stopped and the latest snapshot in RAM is stored to NVM. That snapshot data can then be read back by reading SNAPSHOT command, also after input voltage has been cycled. By checking the Flash Memory Status bits [183:176] in SNAPSHOT one can tell whether snapshot data is from NVM (due to a fault) or not. [183:176] = 0 means data is from NVM (and the continuous update in RAM is stopped), while [183:176] = 255 means the continuous update of snapshot in RAM is ongoing.

Bit	Function	Description	Format
231:216	Load Current of phase 1	Load current of phase 1.	Linear
215:200	Load Current of phase 0	Load current of phase 0.	Linear
199:184	External Temperature2	External temperature2.	Linear
183:176	NVM status	Value 0: Snapshot data is from NVM and the continuous update in RAM is stopped (snapshot disabled) Value 255: Continuous update of snapshot in RAM is ongoing (snapshot enabled)	Integer Unsigned
175:168	Manufacturer Specific Status Byte	Manufacturer specific status byte.	Integer Unsigned
167:160	Status CML	Status CML.	Integer Unsigned
159:152	Status Temperature	Status temperature.	Integer Unsigned
151:144	Status Vin	Status Vin.	Integer Unsigned
143:136	Status Iout	Status iout.	Integer Unsigned
135:128	Status Vout	Status vout.	Integer Unsigned
127:112	Switching Frequency	Switching frequency.	Linear
111:96	External Temperature1	External Temperature1	Linear
95:80	Internal Temperature	Internal temperature.	Linear
79:64	Duty Cycle	Duty cycle.	Linear
63:48	Peak Current	Peal current.	Linear
47:32	Load Current	Load current.	Linear
31:16	Output Voltage	Output voltage.	Vout Mode Unsigned
15:0	Input Voltage	Input voltage.	Linear

BLANK_PARAMS (0xEB)
Transfer Type: Read Block (16 bytes)
Description: Returns a 16-byte string which indicates which parameter values were either retrieved by the last RESTORE operation or have been written since that time. Reading BLANK_PARAMS immediately after a restore operation allows the user to determine which parameters are stored in that store. A one indicates the parameter is not present in the store and has not been written since the RESTORE operation.

Bit	Description	Format
127:0		Byte Array

LEGACY_FAULT_GROUP (0xF0)
Transfer Type: R/W Block (4 bytes)
Description: This command allows the product to fault spread with other BMR products with different definition of the GCB_GROUP command. The command sets which rail GCB IDs should be listened to for fault spreading information. The data sent is a 4-byte, 32-bit, bit vector where every bit represents a rail's GCB ID. A bit set to 1 indicates a device GCB ID to which the configured device will respond upon receiving a fault spreading event. In this vector, bit 0 of byte 0 corresponds to the rail with GCB ID 0. Following through, Bit 7 of byte 3 corresponds to the rail with GCB ID 31. NOTE: The rail's own GCB ID should not be set within the LEGACY_FAULT_GROUP command for that device/rail. All products in a current share rail must shutdown for the rail to report a shutdown. If fault spread mode is enabled in USER_CONFIG, the device will immediately shut down if one of its GCB_GROUP members fail. The rail will attempt its configured restart only after all devices/rails within the GCB_GROUP have cleared their faults. If fault spread mode is disabled in USER_CONFIG, the device will perform a sequenced shutdown as defined by the SEQUENCE command setting. The rails/devices in a sequencing set only attempt their configured restart after all faults have cleared within the GCB_GROUP. If fault spread mode is disabled and sequencing is also disabled, the device will ignore faults from other devices and stay enabled.

Bit	Description	Format
31:0		Byte Array

READ_IOUT0 (0xF2)
Transfer Type: Read Word
Description: Returns the measured output current of phase 0.

Bit	Description	Format	Unit
15:0	Returns the output current reading of phase 0.	Linear	A

SNAPSHOT_CONTROL (0xF3)
Transfer Type: R/W Byte
Description: Used to erase snapshot data in NVM or copy snapshot data between RAM and NVM. Note: It is advised that these operations be performed while the output voltage is disabled.

Bit	Description	Value	Function	Description
7:0	Used to perform memory operations of snapshot data. Note: It is advised that this operation be performed while the output voltage is disabled.	0x01	Copy NVM to RAM	Causes the current SNAPSHOT values in NVM to be copied to RAM.
		0x02	Store RAM to NVM.	Causes the values to be stored in set location in NVM memory.
		0x03	Erase in NVM	Erase the snapshot data from NVM.

MFR_VMON_OV_FAULT_LIMIT (0xF5)
Transfer Type: R/W Word
Description: Sets the VMON overvoltage fault threshold. The VMON input is used to measure the supply voltage of drivers of power switches. The VMON overvoltage warn limit is automatically set to 95% of this fault value.

Bit	Description	Format	Unit
15:0	Sets the VMON overvoltage fault threshold.	Linear	V

MFR_VMON_UV_FAULT_LIMIT (0xF6)
Transfer Type: R/W Word
Description: Sets the VMON undervoltage fault threshold. The VMON input is used to measure the supply voltage of drivers of power switches. The VMON undervoltage warn limit is automatically set to 110% of this fault value.

Bit	Description	Format	Unit
15:0	Sets the VMON undervoltage fault threshold.	Linear	V

VMON_OV_FAULT_RESPONSE (0xF8)
Transfer Type: R/W Byte
Description: Sets the VMON overvoltage fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	00	Ignore Fault	Ignore Fault.
			10	Disable and Retry	Disable the output without delay and retry according to the setting in bits [5:3].
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Do Not Retry	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time	Retry delay time = (Value +1) * 35 ms. Sets the time between retries in 35 ms increments. Range is 35	000	35 ms	
			001	70 ms	
			010	105 ms	

Bit	Function	Description	Value	Function	Description
		ms to 280 ms.	011	140 ms	
			100	175 ms	
			101	210 ms	
			110	245 ms	
			111	280 ms	

VMON_UV_FAULT_RESPONSE (0xF9)
Transfer Type: R/W Byte
Description: Sets the VMON undervoltage fault response.

Bit	Function	Description	Value	Function	Description
7:6	Response	Describes the device interruption operation. For all modes set by bits [7:6], the device pulls SALERT low and sets the related fault bit in the status registers.	00	Ignore Fault	Ignore Fault.
			10	Disable and Retry	Disable the output without delay and retry according to the setting in bits [5:3].
5:3	Retry Setting	The device attempts to restart the number of times set by these bits.	000	Do Not Retry	A zero value for the Retry Setting means that the unit does not attempt to restart. The output remains disabled until the fault is cleared.
			111	Retry Continuously	The PMBus device attempts to restart continuously, without limitation, until output is DISABLED, bias power is removed, or another fault condition causes the output to shut down.
2:0	Retry Time	Retry delay time = (Value +1) * 35 ms. Sets the time between retries in 35 ms increments. Range is 35 ms to 280 ms.	000	35 ms	
			001	70 ms	
			010	105 ms	
			011	140 ms	
			100	175 ms	
			101	210 ms	
			110	245 ms	
			111	280 ms	

SECURITY_LEVEL (0xFA)
Transfer Type: Read Byte
Description: Returns the current security level. The device provides write protection for individual commands. Each bit in the UNPROTECT parameter controls whether its corresponding command is writable (commands are always readable). If a command is not writable, a password must be entered in order to change its parameter (i.e., to enable writes to that command). There are two types of passwords, public and private. The public password provides a simple lock-and-key protection against accidental changes to the device. It would typically be sent to the device in the application prior to making changes. Private passwords allow commands marked as non-writable in the UNPROTECT parameter to be changed. Private passwords are intended for protecting Default-installed configurations and would not typically be used in the application. Each store (USER and DEFAULT) can have its own UNPROTECT string and private password. If a command is marked as non-writable in the DEFAULT UNPROTECT parameter (its corresponding bit is cleared), the private password in the DEFAULT Store must be sent in order to change that command. If a command is writable according to the Default UNPROTECT parameter, it may still be marked as non-writable in the User Store UNPROTECT parameter. In this case, the User private password can be sent to make the command writable.

Bit	Description	Value	Function	Description
7:0	The device provides write protection for individual commands.	0x03	Level 3	Security Level 3 – Module Vendor.
		0x02	Level 2	Security Level 2 – User.
		0x01	Level 1	Security Level 1 – Public.
		0x00	Level 0	Security Level 0 - Unprotected.

PRIVATE_PASSWORD (0xFB)
Transfer Type: R/W Block (9 bytes)
Description: Sets the private password string for the USER_STORE. Password strings have the same format as the MFR_ID parameters.

Bit	Description	Format
71:0	Sets the private password string for the USER_STORE.	ASCII

PUBLIC_PASSWORD (0xFC)
Transfer Type: R/W Block (4 bytes)
Description: Sends a password to the device.

Bit	Description	Format
31:0	Sets the public password string.	ASCII

UNPROTECT (0xFD)
Transfer Type: R/W Block (32 bytes)
Description: Sets a 256-bit (32-byte) parameter which identifies which commands are to be protected against write-access at lower security levels. Each bit in this parameter corresponds to a command according to the command's code. The command with a code of 00h (PAGE) is protected by the least-significant bit of the least-significant byte, followed by the command with a code of 01h and so forth. Note that all possible commands have a corresponding bit regardless of whether they are protectable or supported by the device. Clearing a command's UNPROTECT bit indicates that write-access to that command is only allowed if the device's security level has been raised to an appropriate level. The UNPROTECT bits in the DEFAULT store require a security level 3 or greater to be writeable. The UNPROTECT bits in the USER store require a security level of 2 or higher.

Bit	Description	Format
255:0		Byte Array