IH5116
16-Channel Fault Protected CMOS Analog Multiplexer

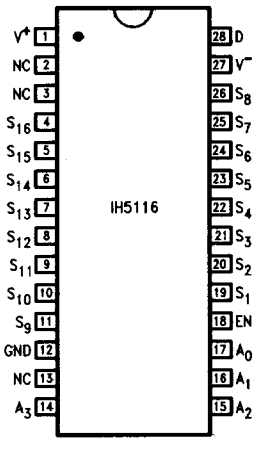
GENERAL DESCRIPTION

The IH5116 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the HI546 and similar devices, but adding fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ±25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc. Cross talk onto "good" channels is also prevented.

A binary 4-bit address code together with the ENable input allows selection of any channel or none at all. These 5 inputs are all TTL compatible for easy logic interface. The ENable input also facilitates MUX expansion and cascading.

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH5116MJI	−55°C to +125°C	28 pin CERDIP
IH5116CJI	0°C to +70°C	28 pin CERDIP
IH5116CPI	0°C to +70°C	28 pin Plastic DIP



TOP VIEW

V+ COMMON TO SUBTRATE

Figure 1: Pin Configuration (Outline dwg JI, PI)

FEATURES

- **All Channels OFF When Power OFF, for Analog Signals Up to ±25V**
- **Power Supply Quiescent Current Less Than 1mA**
- **±13V Analog Signal Range**
- **No SCR Latchup**
- **Break-Before-Make Switching**
- **TTL and CMOS Compatible Strobe Control**
- **Pin Compatible With HI546**
- **Any Channel Turns OFF If Input Exceeds Supply Rails By Up to ±25V**
- **TTL and CMOS Compatible Binary Address and ENable Inputs**

TRUTH TABLE

A_3	A_2	A_1	A_0	EN	On Switch
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Logic "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 2.4V$

Logic "0" = $V_{AL} \leq 0.8V$

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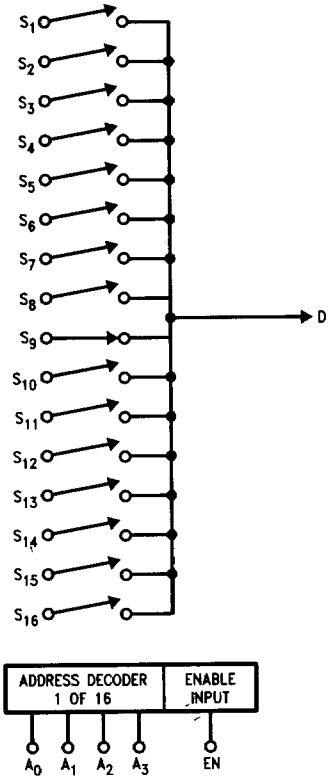
NOTE: All typical values have been characterized but are not tested.



4 LINE BINARY ADDRESS INPUTS
(0001) AND EN = 5V
ABOVE EXAMPLE SHOWS CHANNELS 9
TURNED ON.

Figure 2: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

IH5116

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V to +15V
V_S or V_D to V^+ ..... +25V to −40V
V_S or V_D to V^- ..... −25V to +40V
V^+ to Ground 20V
V^- to Ground ..... −20V
Current (Any Terminal) 20mA
Operating Temperature
C Suffix ..... 0°C to +70°C
M Suffix ..... −55°C to +125°C
Storage Temperature ..... −65 to +150°C
Storage Temperature
C Suffix ..... −65°C to +125°C
M Suffix ..... −65°C to +150°C

Lead Temperature (Soldering, 10 Sec.) ..... 300°C
Power Dissipation*
28-Pin CERDIP Package** ..... 1200 mW
28-Pin Plastic Package*** ..... 625 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 16 mW/°C above 75°C

***Derate 8.3 mW/°C above 75°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS ($V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.)

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions		Typ 25°C	Max Limits M Suffix −55°C	M Suffix 25°C	M Suffix 125°C	C Suffix 0°C	C Suffix 25°C	C Suffix 70°C	Units
SWITCH												
$R_{DS(on)}$	S to D	16	$V_D = 10V$, $I_S = -100\mu A$	Sequence each switch on	900	1200	1200	1800	1500	1500	2000	Ω
		16	$V_D = -10V$ $I_S = -100\mu A$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$	900	1200	1200	1800	1500	1500	2000	
$\Delta R_{DS(on)}$			$\Delta R_{DS(on)} = \frac{R_{DS(on)max} - R_{DS(on)min}}{R_{DS(on)avg.}}$ $V_S = \pm 10V$		5							%
$I_{S(off)}$	S	16	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0.8V$	±0.02		±0.5	±50		±1.0	±50	nA
		16	$V_S = -10V$, $V_D = 10V$		±0.02		±0.5	±50		±1.0	±50	
$I_{D(off)}$	D	1	$V_D = 10V$, $V_S = -10V$		±0.05		±1.0	±100		±2.0	±100	
		1	$V_D = -10V$, $V_S = 10V$		±0.05		±1.0	±100		±2.0	±100	
$I_{D(on)}$	D	16	$V_{S(All)} = V_D = 10V$	Sequence each switch on	±0.1		±2.0	±100		±4.0	±100	
		16	$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$	±0.1		±2.0	±100		±4.0	±100	
FAULT												
I_S with Power OFF	S	16	$V_{SUPP} = 0V$, $V_{IN} = \pm 25V$, $V_{EN} = V_O = 0V$, $A_0, A_1, A_2 = 0V$ or 5V		±1.0		±2.0			±5.0		μA
$I_{S(off)}$ with Overvoltage	S	16	$V_{IN} = \pm 25V$, $V_0 = \pm 10V$		±1.0		±2.0			±5.0		
INPUT												
$I_{EN(on)}$ $I_{A(on)}$ or $I_{EN(off)}$ $I_{A(off)}$	A_0, A_1, A_2, A_3 or EN	4	$V_A = 0V$		0.01		−10	−30		−10	−30	μA
		4	$V_A = 15V$		0.01		10	30		10	30	

NOTE: All typical values have been characterized but are not tested.

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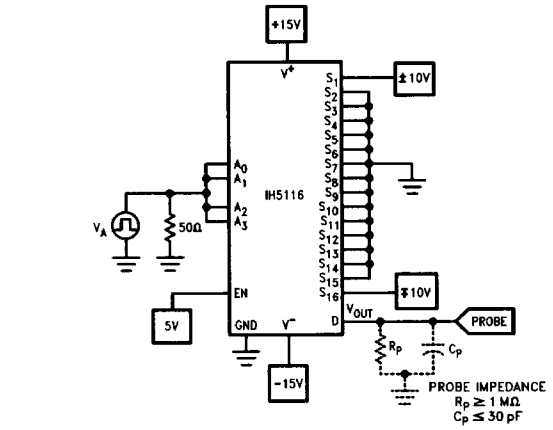
ELECTRICAL CHARACTERISTICS

($V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.) (Continued)

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions		Typ 25°C	Max Limits M Suffix −55°C	M Suffix 25°C	M Suffix 125°C	C Suffix 0°C	C Suffix 25°C	C Suffix 70°C	Units
DYNAMIC												
$t_{transition}$	D		See Figure 3		0.3		1					μs
t_{open}	D		See Figure 4		0.2							
$t_{on(EN)}$	D		See Figure 5		0.6		1.5					
$t_{off(EN)}$	D				0.4		1					
t_{on}-t_{off} Break-Before-Make Delay Settling Time	D		$V_{EN} = +5V$, A_0, A_1, A_2 Strobed $V_{IN} = \pm 10V$, See Figure 6		25							ns
"OFF" Isolation	D		$V_{EN} = 0V$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3VRMS$, $f = 500kHz$		60							dB
$C_{s(off)}$	S		$V_S = 0V$	$V_{EN} = 0V$, $f = 140kHz$ to 1 MHz	5							pF
$C_{D(off)}$	D		$V_D = 0V$		25							
$C_{DS(off)}$	D to S		$V_S = 0V$, $V_D = 0V$		1							
SUPPLY												
Supply Current	+	I^+	1	All $V_A = 0V/5V$ $V_{EN} = 5V$	0.5		0.6			1.0		mA
	−	I^-	1		0.02		0.6			1.0		

NOTE: All typical values have been characterized but are not tested.



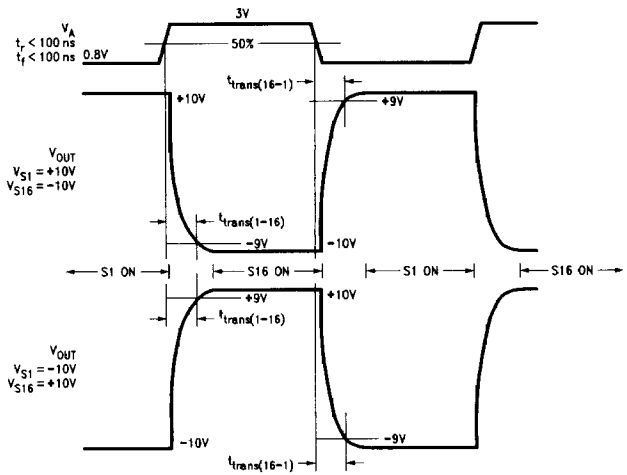
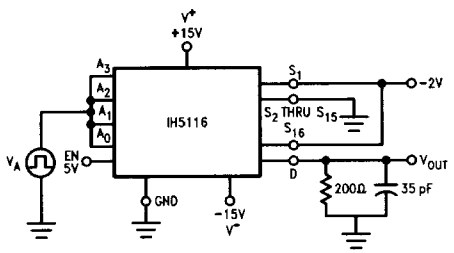


Figure 3: $t_{transition}$ Switching Test Circuit and Waveforms



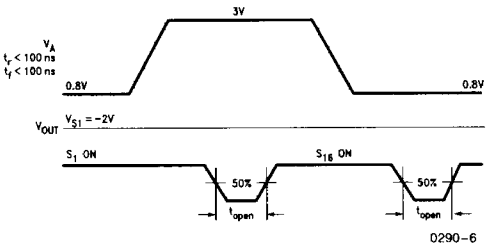


Figure 4: t_{open} (Break-Before-Make) Switching Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

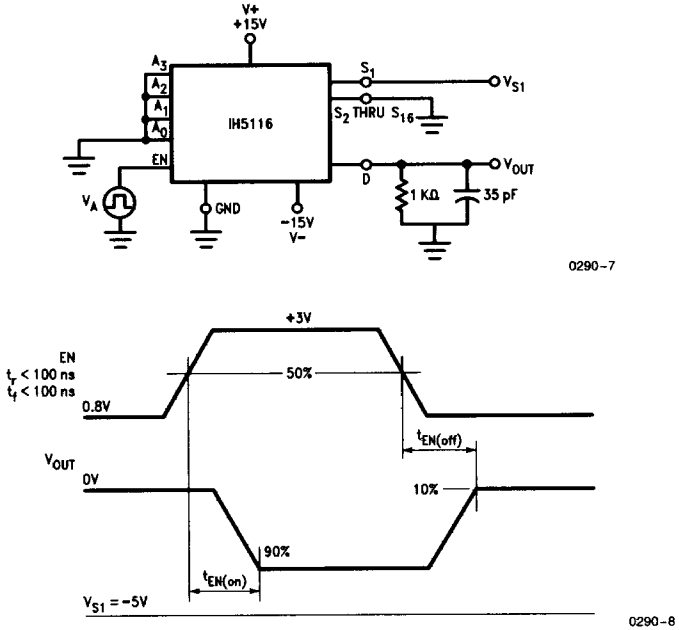


Figure 5: ENABLE t_{on} and t_{off} Switching Test Circuit and Waveforms

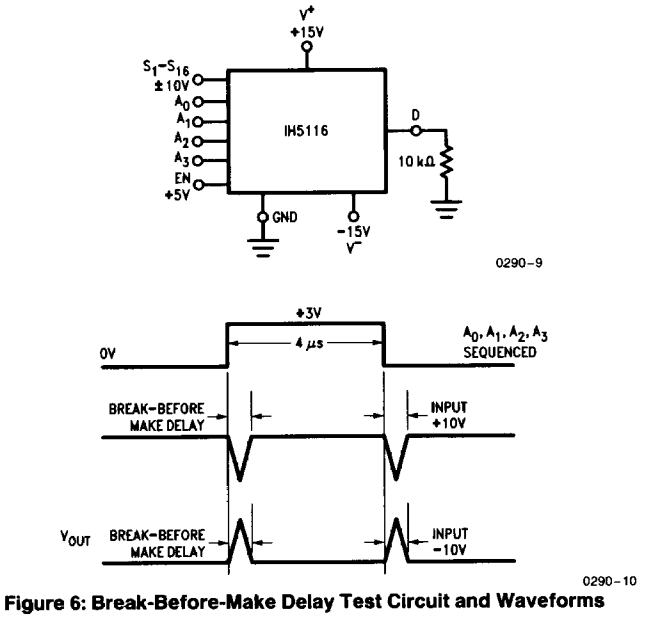


Figure 6: Break-Before-Make Delay Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

The IH5116, like all Harris multiplexers, contains a set of CMOS switches that form the channels, and driver and decoder circuitry to control which channel turns ON, if any. In addition, the IH5116 contains an internal regulator which provides a fully TTL compatible ENable input that is identical in operation to the Address inputs. This does away with the special conditions that many multiplexer enable inputs require for proper logic swings. The identical circuit conditions of the ENable and Address lines also helps ensure the extension of break-before-make switching to wider multiplexer systems (see applications section).

Another, and more important difference lies in the switching channel. Previous devices have used parallel n- and p-channel MOSFET switches. While this scheme yields reasonably good ON resistance characteristics and allows the switching of rail-to-rail input signals, it also has a number of drawbacks. The sources and drains of the switch transistors will conduct to the substrate if the input goes outside the supply rails, and even careful use of diodes cannot avoid channel-to-output and channel-to-channel coupling in cases of input overrange. The IH5116 uses a novel series arrangement of the p- and n-channel switches (Figure 7) combined with a dielectrically isolated process to eliminate these problems.

Within the normal analog signal range, the inherent variation of switch ON resistance will balance out almost as well as the customary parallel configuration, but as the analog signal approaches either supply rail, even for an ON channel, either the p- or the n-channel will become a source follower, disconnecting the channel (Figure 8). Thus protection is provided for any input or output channel against overvoltage, even in the absence of multiplexer supply voltages. This applies up to the breakdown voltage of the respective switches. Figure 9 shows a more detailed schematic of the channel switches, including the back-gate driver devices which ensure optimum channel ON resistances and breakdown voltage under the various conditions.

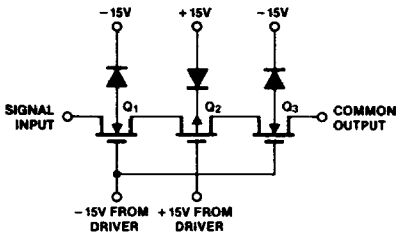
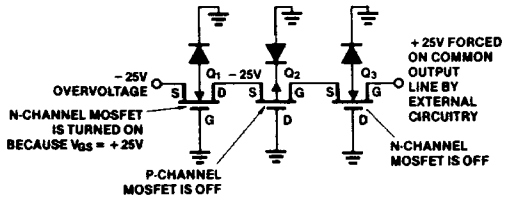
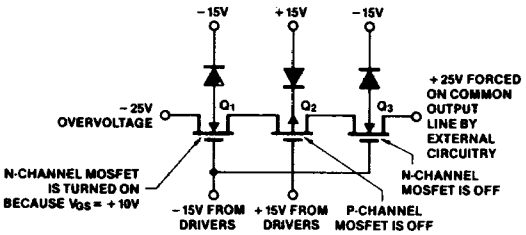


Figure 7: Series Connection of Channel Switches

Under some circumstances, if the logic inputs are present but the multiplexer supplies are not, the circuit will use the logic inputs as a sort of phantom supply; this could result in an output up to that logic level. To prevent this from occurring, simply ensure that the ENable pin is LOW any time the multiplexer supply voltages are missing (Figure 10).



(a) OVERVOLTAGE WITH MUX POWER OFF



(b) OVERVOLTAGE WITH MUX POWER ON

Figure 8: Overvoltage Protection

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NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION (Continued)

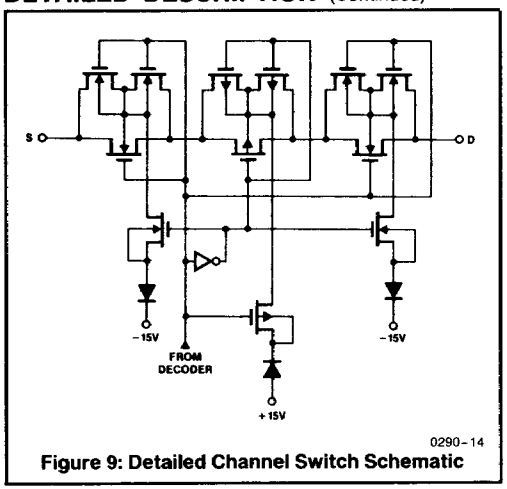


Figure 9: Detailed Channel Switch Schematic

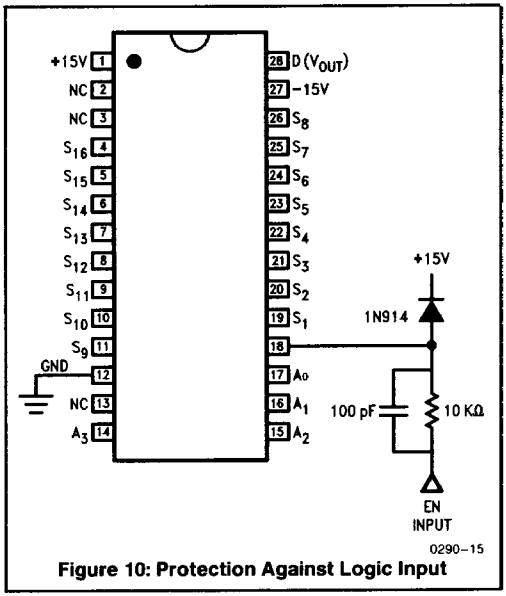


Figure 10: Protection Against Logic Input

MAXIMUM SIGNAL HANDLING CAPABILITY

The IH5116 is designed to handle signals in the ±10V range, with a typical $R_{DS(on)}$ of 900Ω; it can successfully handle signals up to ±12V, however, $R_{DS(on)}$ will increase to about 1.8kΩ. Beyond ±12V the device approaches an open circuit, and thus ±12V is about the practical limit, see Figure 11.

Figure 12 shows the input/output characteristics of an ON channel, illustrating the inherent limiting action of the series switch connection (see Detailed Description), while Figure 13 gives the ON resistance variation with temperature.

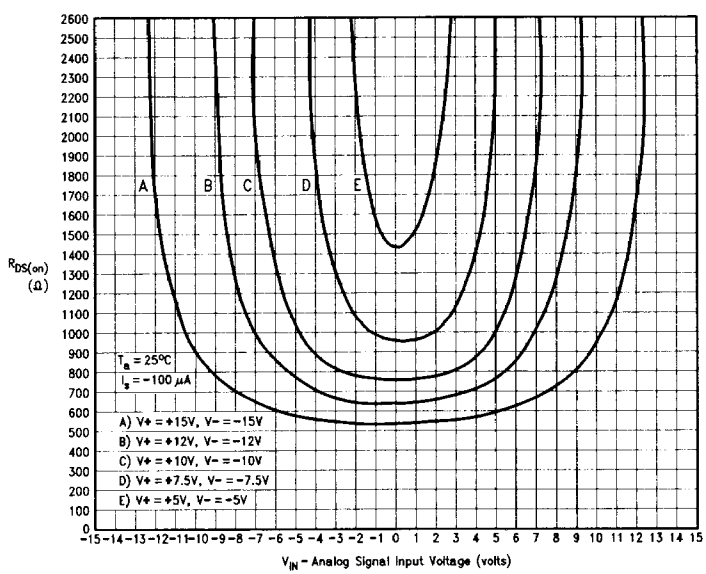
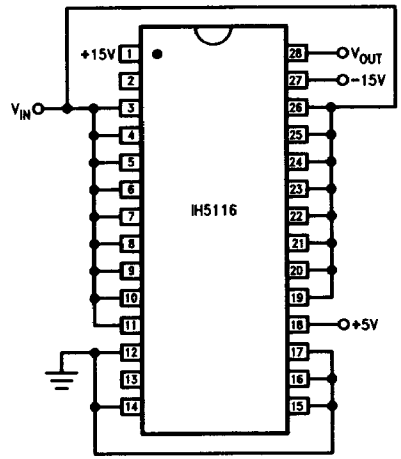


Figure 11: $R_{DS(on)}$ vs Analog Signal Voltage

NOTE: All typical values have been characterized but are not tested.



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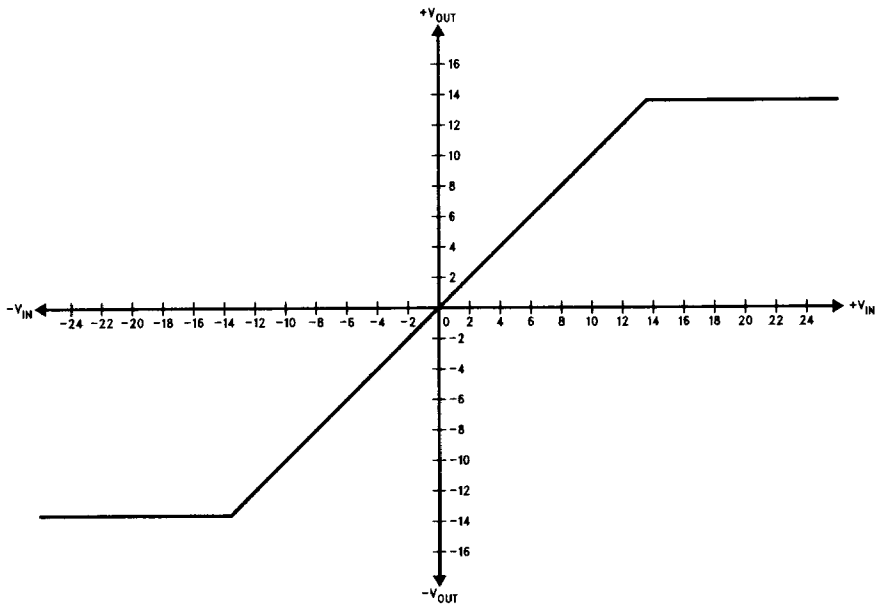

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Figure 12: MUX Output Voltage vs Input Voltage (Channel 1 Shown; All Channels Similar)

NOTE: All typical values have been characterized but are not tested.

IH5116 APPLICATIONS

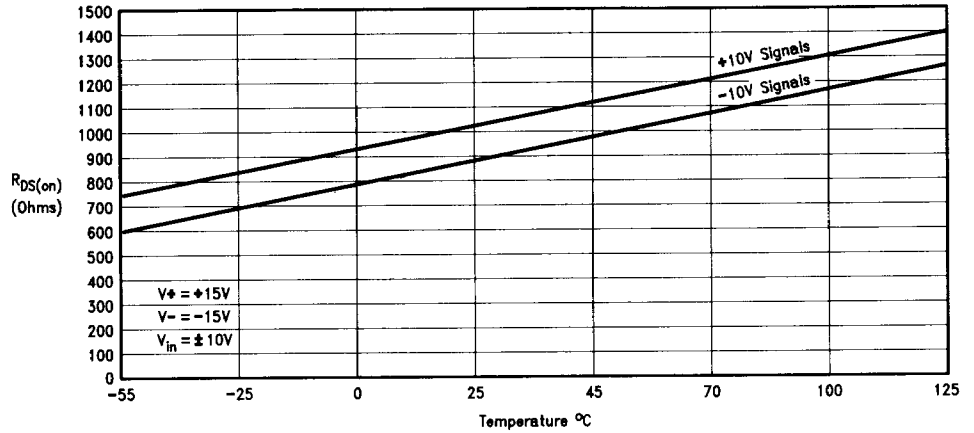
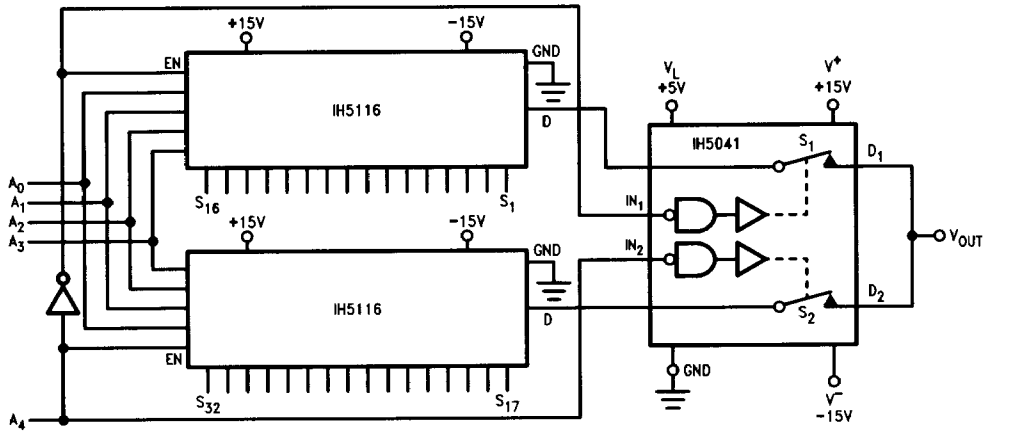


Figure 13: Typical $R_{DS(ON)}$ Variation with Temperature

NOTE: All typical values have been characterized but are not tested.

IH5116 APPLICATIONS (Continued)



TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 15: 1 of 32 Channel Multiplexer Using 2 IH5116's and an IH5041 for Submultiplexing

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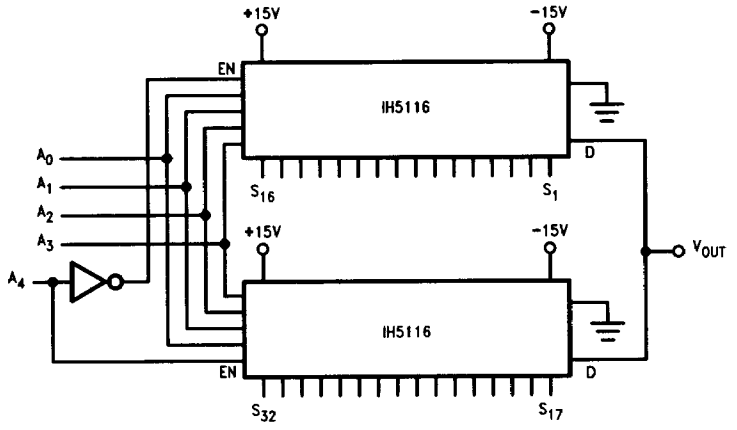
NOTE: All typical values have been characterized but are not tested.

IH5116 APPLICATIONS (Continued)



TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 16: 1 of 32 Channel Multiplexer Using 2 IH5116's

NOTE: All typical values have been characterized but are not tested.

IH5116 APPLICATIONS (Continued)

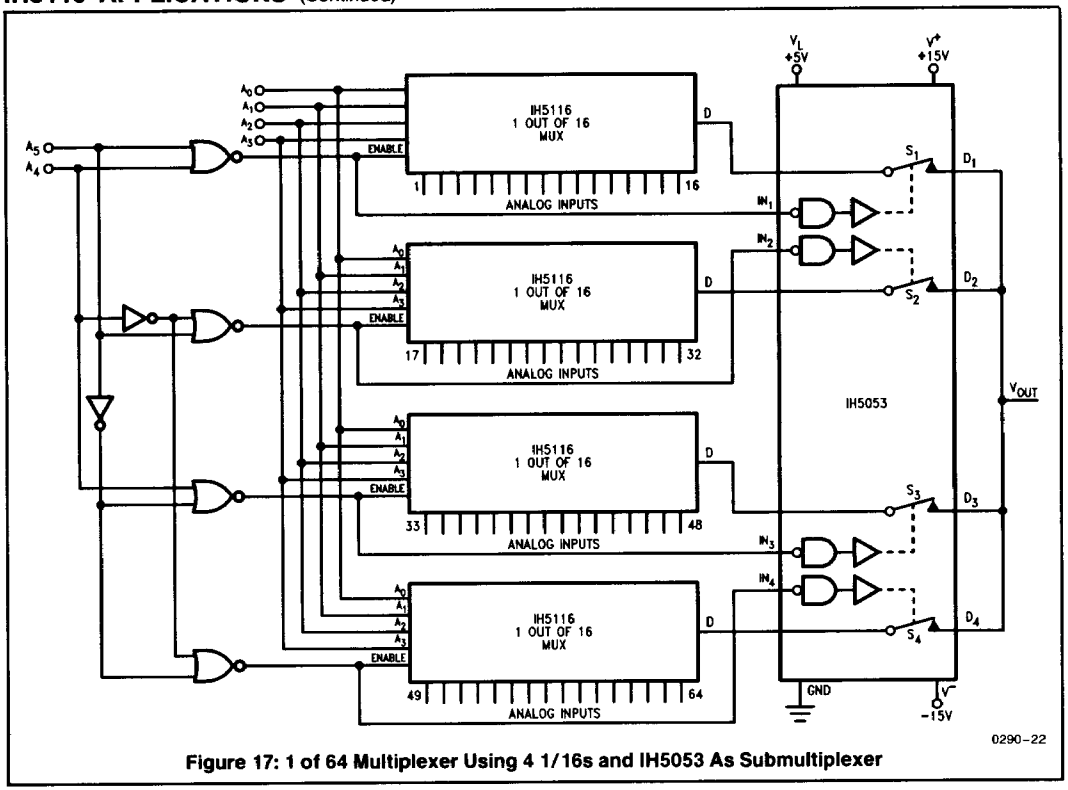


Figure 17: 1 of 64 Multiplexer Using 4 1/16s and IH5053 As Submultiplexer

General note on expandability of IH5116

Figures 15, 16, and 17 show how the IH5116 can be expanded.

Figure 15 shows a 1 of 32 multiplexer, using 2 IH5116s.

Figure 16 shows the 1 of 32 MUX of Figure 15, with a second tier of submultiplexing added to further reduce leakage and output capacitance. The IH5041 has typical ON resistances of 50Ω (max. is 75Ω) so it only increases thruput channel resistance from the 900Ω of Figure 15 to about 950Ω for Figure 16.

Figure 17 shows a 1 of 64 MUX using 2 tier MUXing (similar to Figure 16). The V_{OUT} point will see 15 OFF channels and 1 ON channel at any one time, so that the typical leakages will be about 0.05 nA. Throughput channel resistance will be in the 950Ω range.

USING THE IH5116 WITH SUPPLIES OTHER THAN ±15V

The IH5116 will operate successfully with supply voltages from ±5V to ±15V, however, $r_{DS(on)}$ increases as supply voltage decreases, as shown in Figure 11. Leakage currents, on the other hand, decrease with a lowering of supply voltage, and therefore the error term product of $r_{DS(on)}$ and leadkage current remains reasonably constant. $r_{DS(on)}$ also decreases as signal levels decrease. For high system accuracy [acceptable levels of $r_{DS(on)}$] the maximum input signal should be 3V less than the supply voltages. The logic levels remain TTL compatible.

APPLICATION NOTES

Further information may be found in:

A003 "Understanding and Applying the Analog Switch"

A006 "A New CMOS Analog Gate Technology"

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing"

R009 "Reduce CMOS Multiplexer Troubles Through Proper Device Selection"

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NOTE: All typical values have been characterized but are not tested.