

# EPC2306 – Enhancement Mode Power Transistor

$V_{DS}$ , 100 V

$R_{DS(on)}$ , 3.8 mΩ max

**PRELIMINARY**



RoHS



Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low  $R_{DS(on)}$  while its lateral device structure and majority carrier diode provide exceptionally low  $Q_G$  and zero  $Q_{RR}$ . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

## Application Notes:

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions:  
EPC GaN Talk  
Support Forum



**EPC2306**

Package size: 3 x 5 mm

Maximum Ratings			
PARAMETER		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	
$I_D$	Continuous ( $T_A = 25^\circ\text{C}$ )	48	A
	Pulsed ( $25^\circ\text{C}$ , $T_{PULSE} = 300 \mu\text{s}$ )	197	
$V_{GS}$	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
$T_J$	Operating Temperature	-40 to 150	°C
$T_{STG}$	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Case TOP)	0.5	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board (Case BOTTOM)	3.0	
$R_{\theta JA\_JEDEC}$	Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB)	54	
$R_{\theta JA\_EVB}$	Thermal Resistance, Junction-to-Ambient (using EPC90145 EVB)	23	

Static Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}$ , $I_D = [\text{TBD}]$	100			V
$I_{DSS}$	Drain-Source Leakage	$V_{GS} = 0\text{ V}$ , $V_{DS} = 80\text{ V}$		0.5		μA
$I_{GSS}$	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$		0.005	1.9	mA
	Gate-to-Source Forward Leakage <sup>#</sup>	$V_{GS} = 5\text{ V}$ , $T_J = 125^\circ\text{C}$		0.2	4.2	
	Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$		0.005		
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 7\text{ mA}$	0.8	1.3	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}$ , $I_D = 25\text{ A}$		3.0	3.8	mΩ
$V_{SD}$	Source-Drain Forward Voltage <sup>#</sup>	$I_S = 0.5\text{ A}$ , $V_{GS} = 0\text{ V}$		1.6		V

<sup>#</sup> Defined by design. Not subject to production test.

## Applications

- AC-DC chargers, SMPS, adaptors, power supplies
- High Frequency DC-DC Conversion up to 80 V input (Buck, Boost, Buck-Boost and LLC)
- 24 V–60 V Motor Drives
- High Power Density DC-DC modules from 40 V– 60 V to 5 V–12 V
- Synchronous Rectification
- Solar MPPT

## Benefits

- Higher Efficiency – Lower conduction and switching losses, zero reverse recovery losses
- Ultra Small Footprint – Higher power density

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC2306>

Dynamic Characteristics <sup>#</sup> (T <sub>J</sub> = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V		1667	2366	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			3.6		
C <sub>OSS</sub>	Output Capacitance			482	559	
C <sub>OSS(ER)</sub>	Effective Output Capacitance, Energy Related (Note 1)	V <sub>DS</sub> = 0 to 50 V, V <sub>GS</sub> = 0 V		593		
C <sub>OSS(TR)</sub>	Effective Output Capacitance, Time Related (Note 2)			767		
R <sub>G</sub>	Gate Resistance			0.4		Ω
Q <sub>G</sub>	Total Gate Charge	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 5 V, I <sub>D</sub> = 25 A		11.6	16.3	nC
Q <sub>GS</sub>	Gate to Source Charge	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 25 A		4.1		
Q <sub>GD</sub>	Gate-to-Drain Charge			0.8		
Q <sub>G(TH)</sub>	Gate Charge at Threshold			3		
Q <sub>OSS</sub>	Output Charge	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V		38	47	
Q <sub>RR</sub>	Source-Drain Recovery Charge			0		

All measurements were done with substrate shorted to source.

# Defined by design. Not subject to production test.

Note 1: C<sub>OSS(ER)</sub> is a fixed capacitance that gives the same stored energy as C<sub>OSS</sub> while V<sub>DS</sub> is rising from 0 to 50% BV<sub>DSS</sub>.

Note 2: C<sub>OSS(TR)</sub> is a fixed capacitance that gives the same charging time as C<sub>OSS</sub> while V<sub>DS</sub> is rising from 0 to 50% BV<sub>DSS</sub>.

Figure 1: Typical Output Characteristics at 25°C

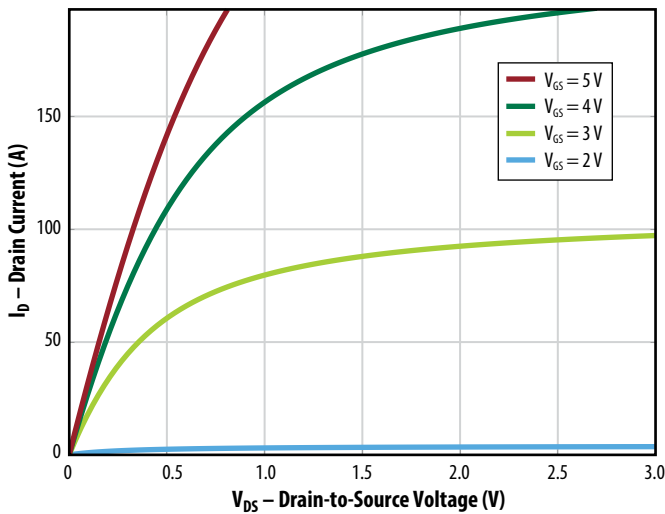


Figure 2: Typical Transfer Characteristics

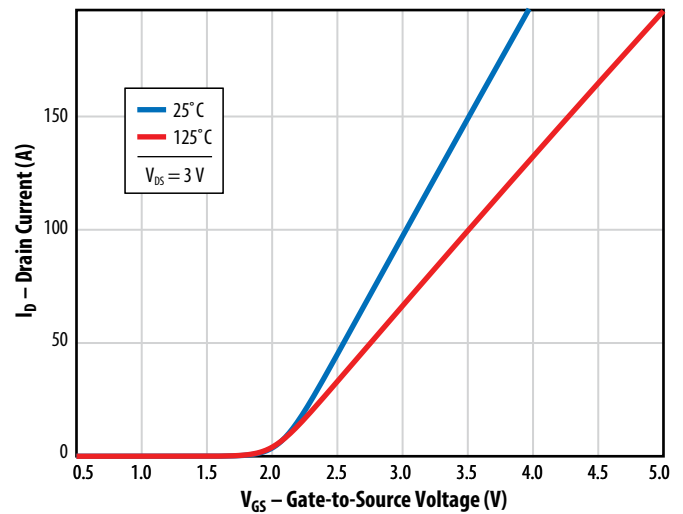


Figure 3: Typical R<sub>DS(on)</sub> vs. V<sub>GS</sub> for Various Drain Currents

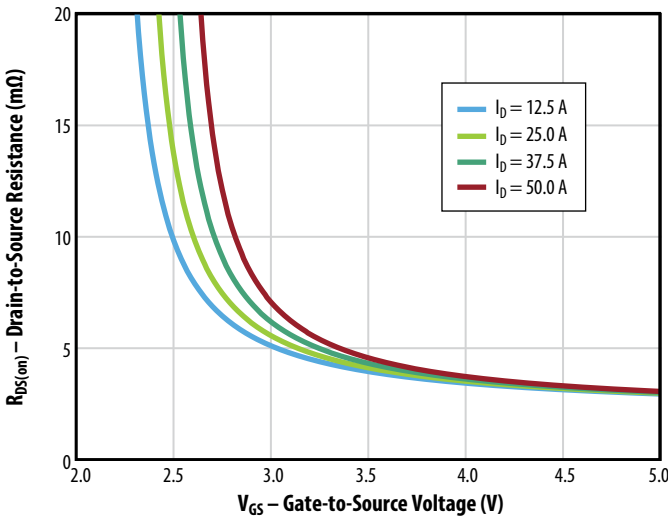


Figure 4: Typical R<sub>DS(on)</sub> vs. V<sub>GS</sub> for Various Temperatures

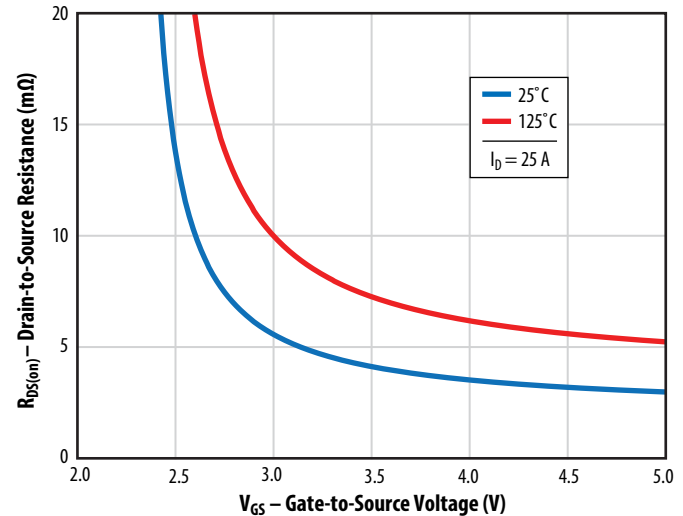


Figure 5a: Typical Capacitance (Linear Scale)

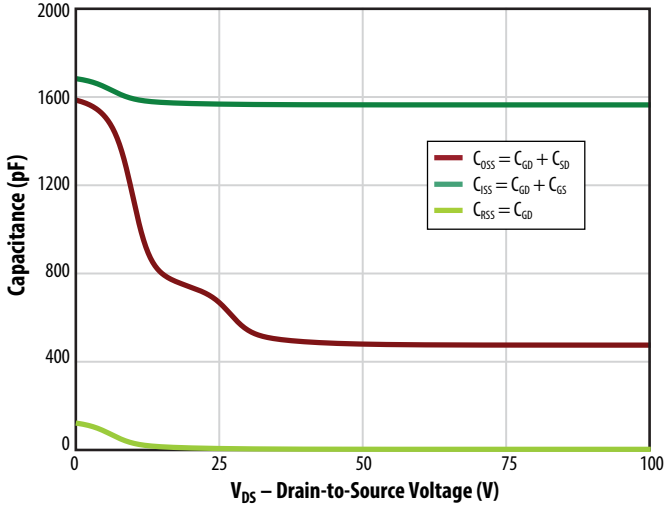


Figure 5b: Typical Capacitance (Log Scale)

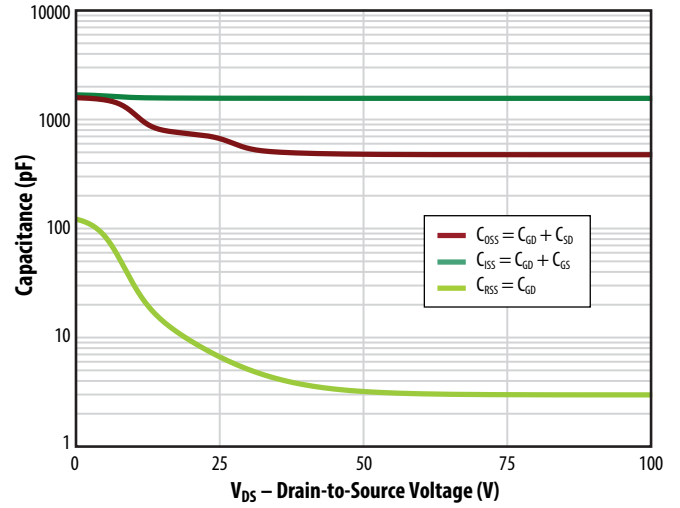


Figure 6: Typical Output Charge and C\_oss Stored Energy

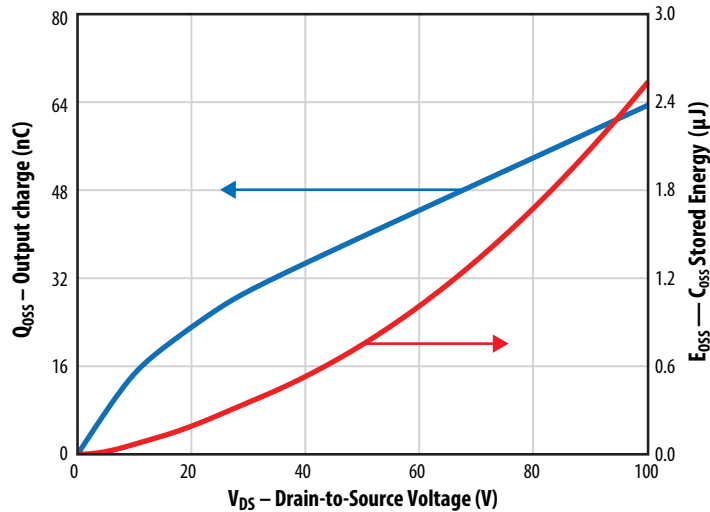


Figure 7: Typical Gate Charge

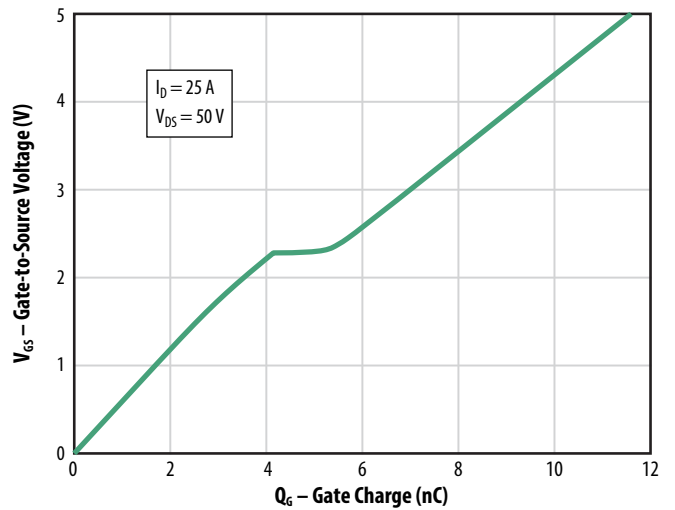
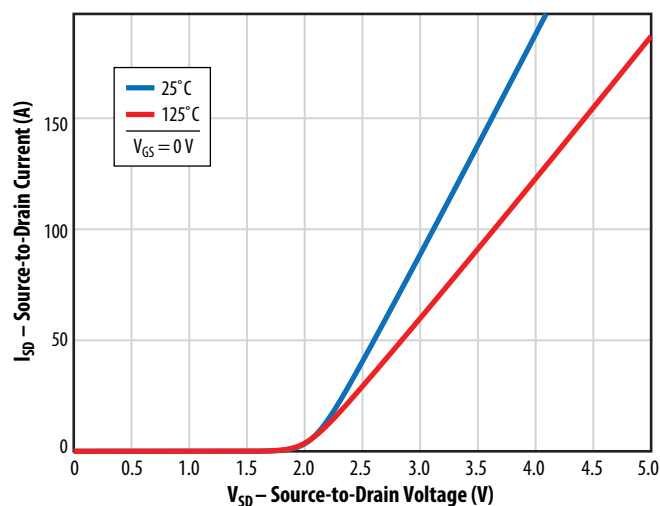


Figure 8: Typical Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage.  
EPC recommends 0 V for OFF.

Figure 9: Typical Normalized On-State Resistance vs. Temp.

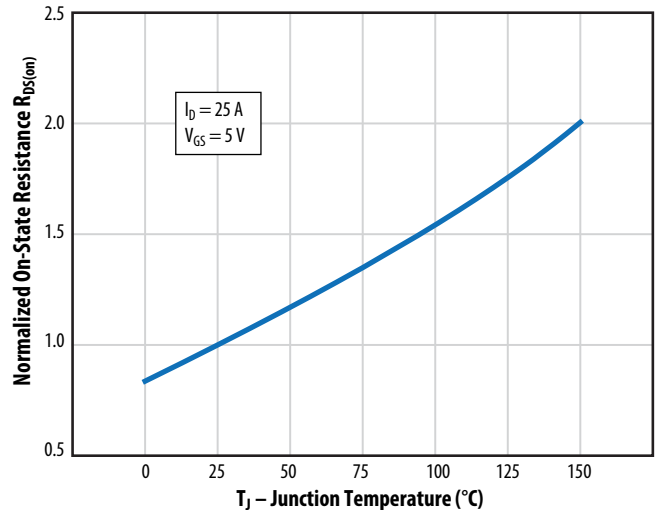


Figure 10: Typical Normalized Threshold Voltage vs. Temp.

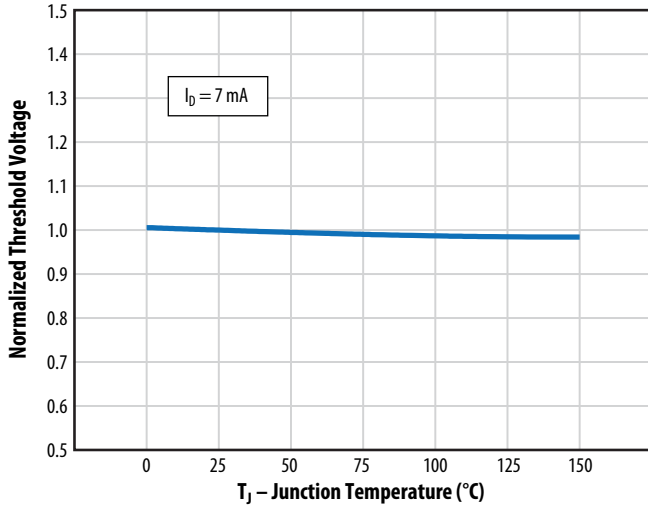


Figure 11: Safe Operating Area

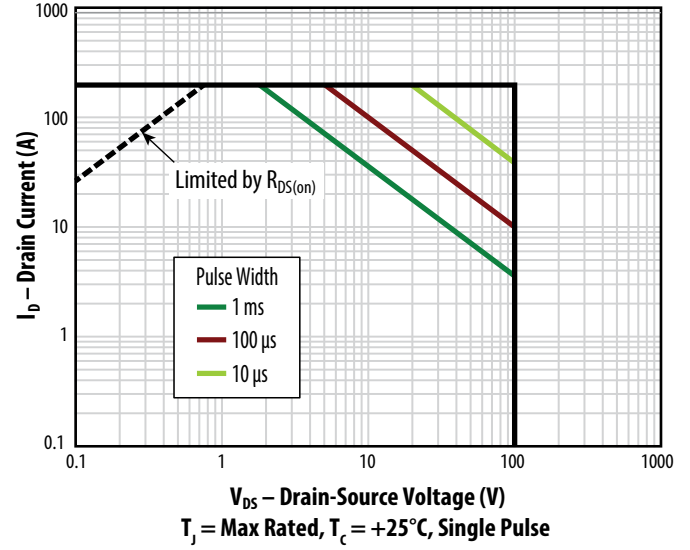
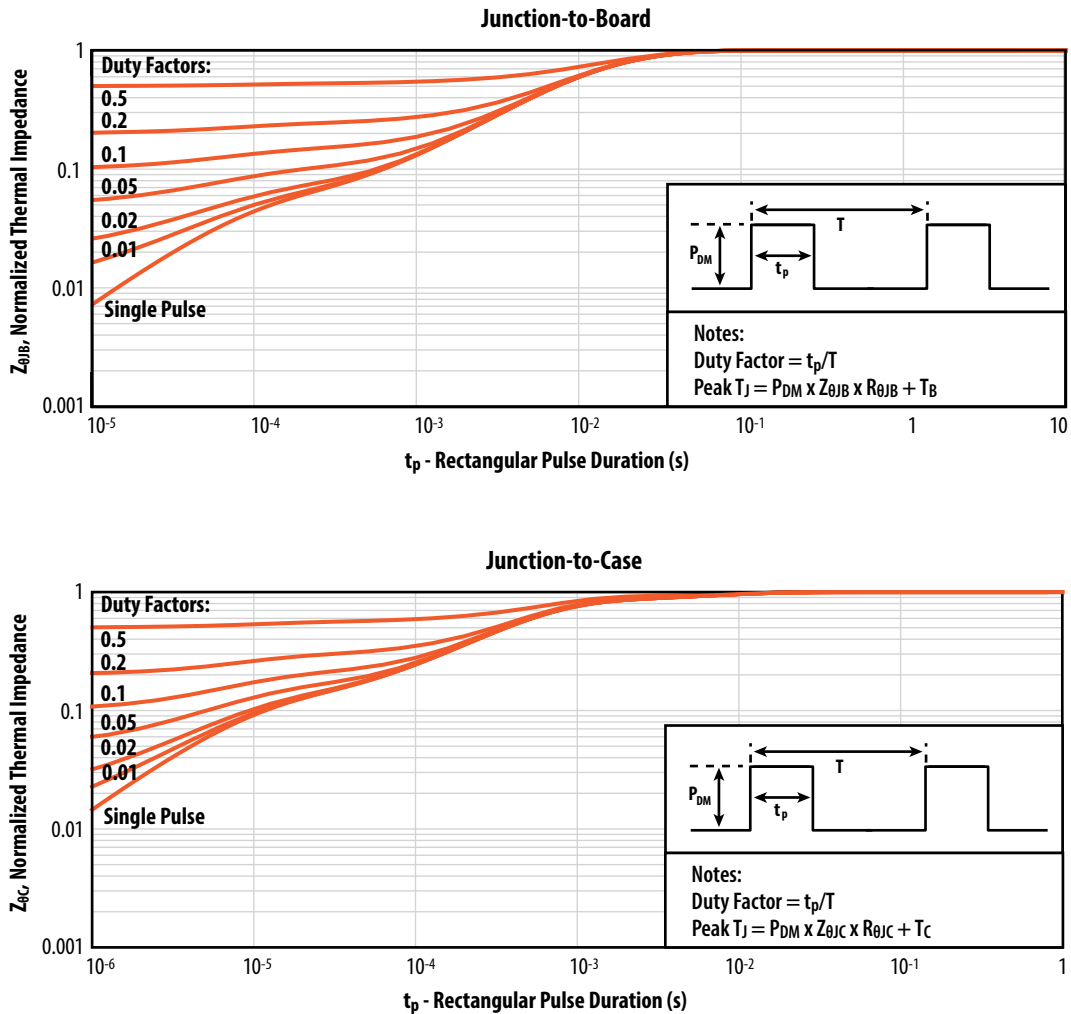
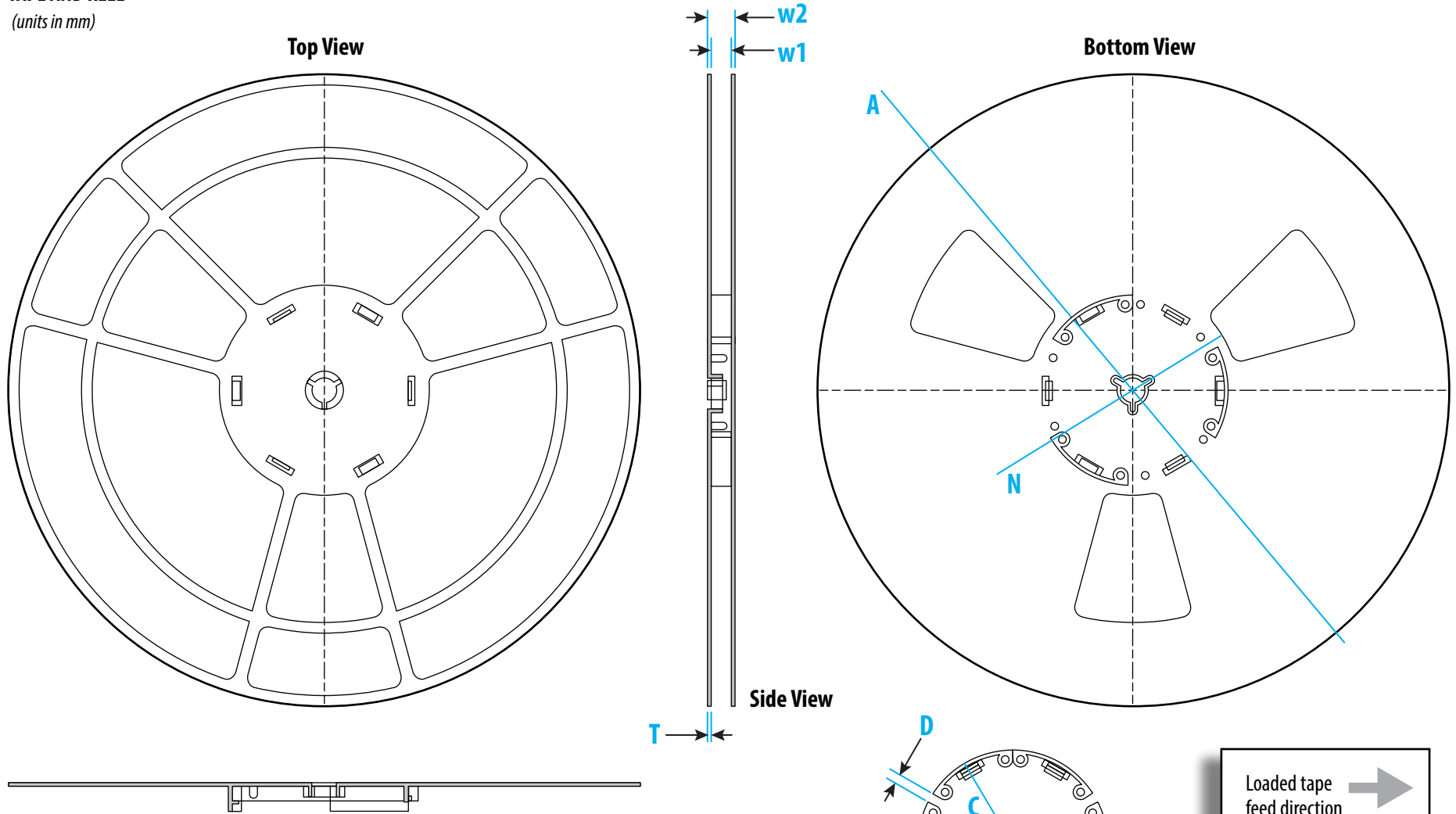


Figure 12: Transient Thermal Response Curves

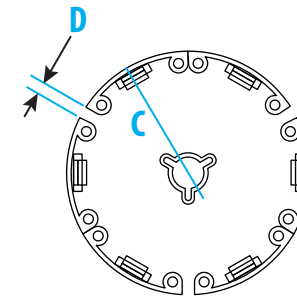


**TAPE AND REEL**

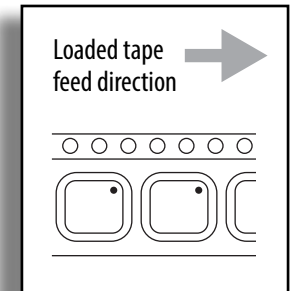
(units in mm)

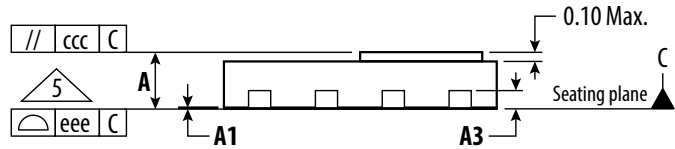
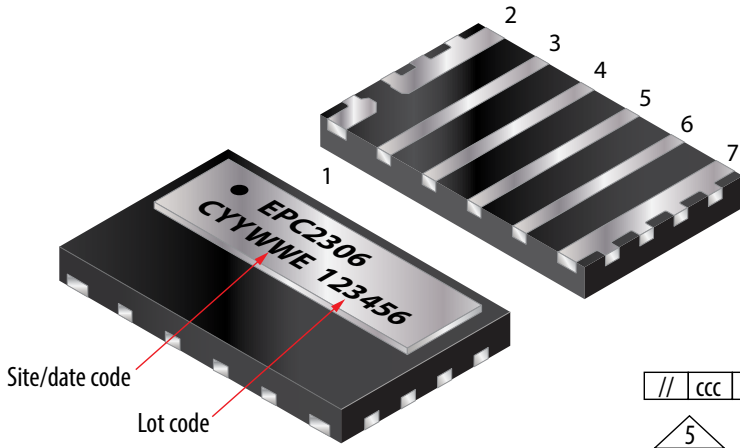


Type	A	N	C	D	w1	w2	T
<b>8MM</b>	∅330±2	∅100±2	∅13.1±0.2	5.6±0.5	8.4+1.5	14.4	2.1±0.5
<b>12MM</b>	∅330±2	∅100±2	∅13.1±0.2	5.6±0.5	12.4+1.5	18.4	2.1±0.5
<b>16MM</b>	∅330±2	∅100±2	∅13.1±0.2	5.6±0.5	16.4+1.5	22.4	2.1±0.5
<b>24MM</b>	∅330±2	∅100±2	∅13.1±0.2	5.6±0.5	24.4+1.5	30,4	2.1±0.5

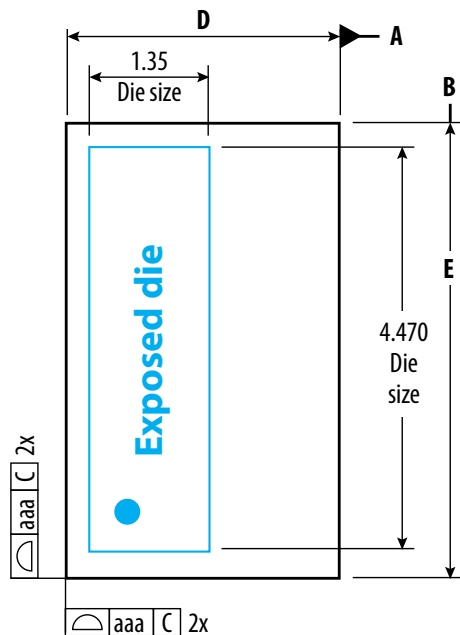


**Bottom View Detail**

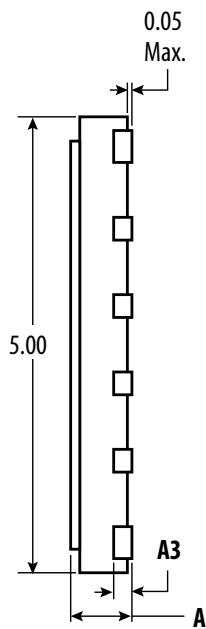




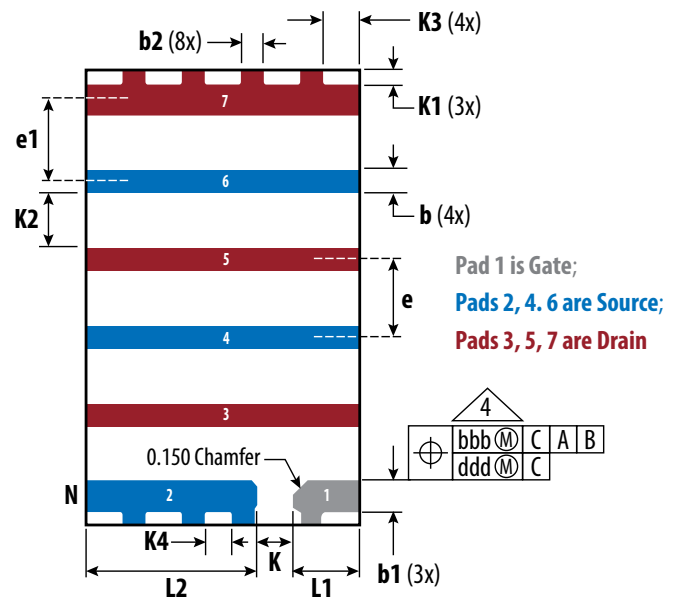
Side View 2



Top View



Side View 1



Bottom View

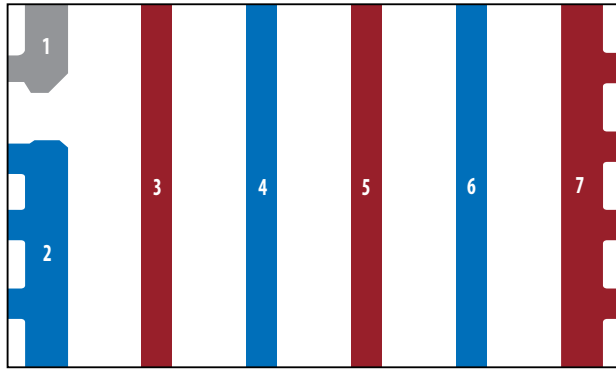
SYMBOL	Dimension (mm)			Note
	MIN	Nominal	MAX	
A	0.60	0.65	0.70	
A1	0.00	0.02	0.05	
A3		0.20 Ref		
b	0.20	0.25	0.30	4
b1	0.30	0.35	0.40	4
b2	0.20	0.25	0.30	4
D		3.00 BSC		
E		5.00 BSC		
e		0.85 BSC		
e1		0.90 BSC		
L1	0.625	0.725	0.825	
L2	1.775	1.875	1.975	

SYMBOL	Dimension (mm)			Note
	MIN	Nominal	MAX	
K	0.35	0.40	0.45	
K1	0.10	0.15	0.20	
K2	0.55	0.60	0.65	
K3	0.35	0.40	0.45	
K4	0.25	0.30	0.35	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		15		3
NE		6		

**Notes:**

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. N is the total number of terminals
4. Dimension b applies to the metallized terminal. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
5. Coplanarity applies to the terminals and all the other bottom surface metallization.

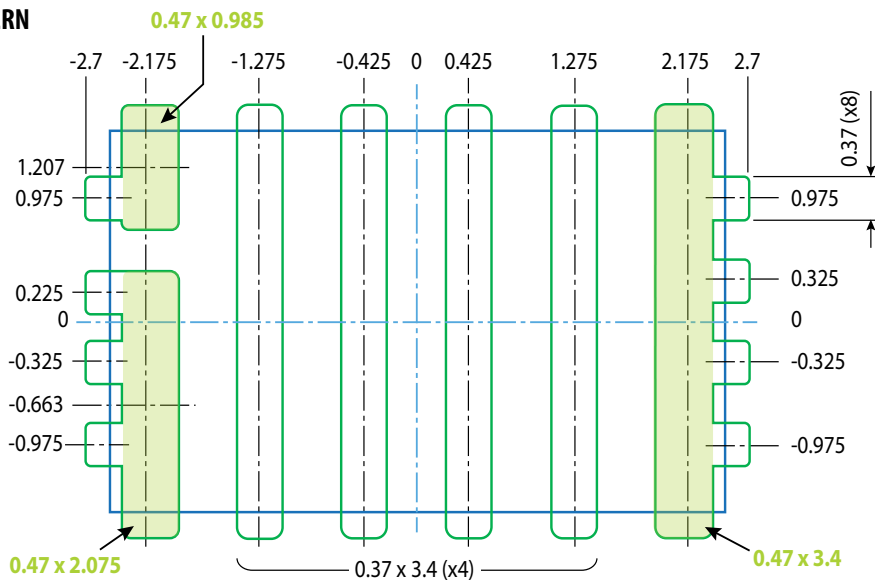
TRANSPARENT VIEW



PIN	Description
1	Gate
2	Source
3	Drain
4	Source
5	Drain
6	Source
7	Drain

RECOMMENDED LAND PATTERN

(units in mm)



Legend:

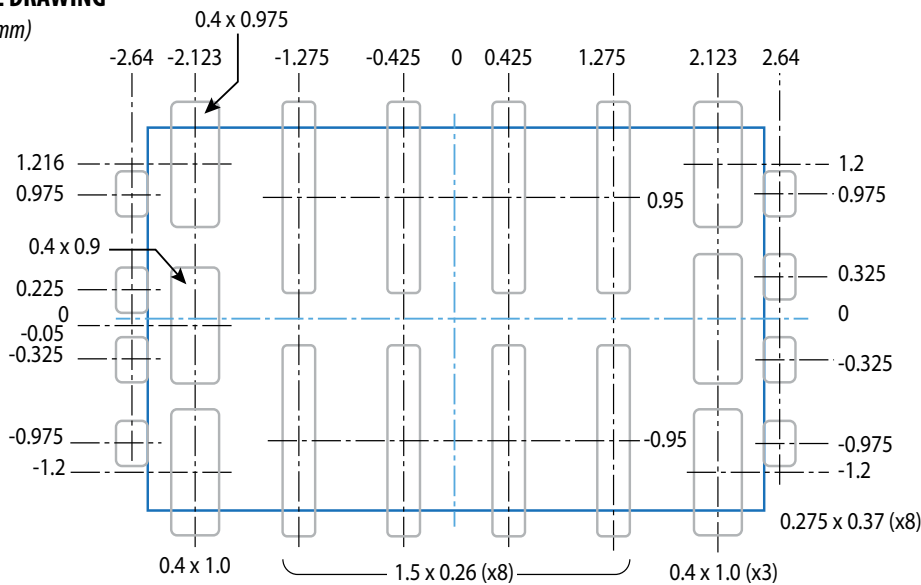
Part outline  
Mask Opening

Radius = 0.05

Land pattern is solder mask defined

RECOMMENDED STENCIL DRAWING

(units in mm)



Legend:

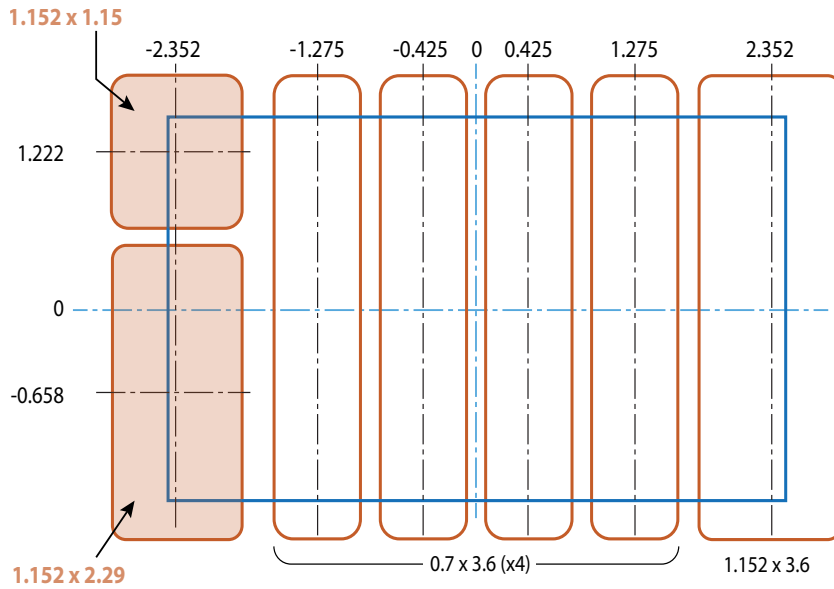
Part outline  
Stencil opening

Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, openings per drawing. Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

The corner has a radius of R60.

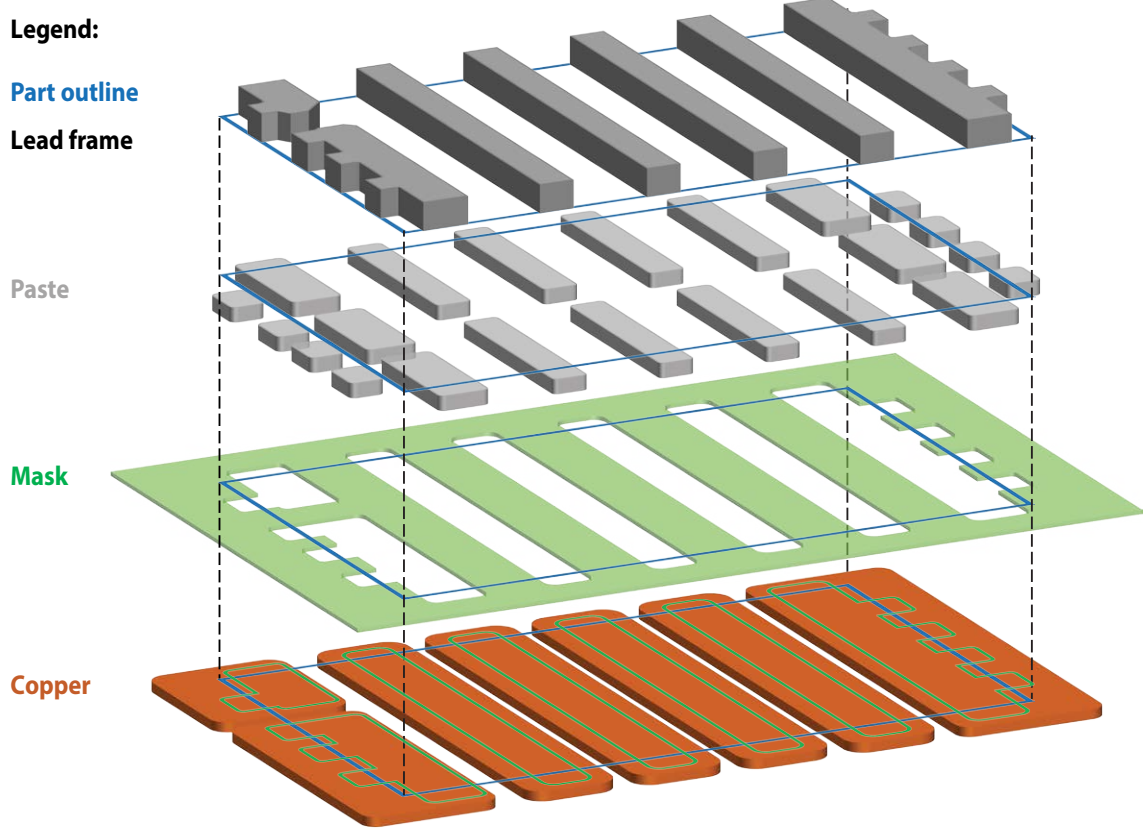
Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

**RECOMMENDED  
COPPER DRAWING**  
(units in mm)



Legend:  
**Part outline**  
**Copper**  
 Radius = 0.05

**3D COMPOSITE**



**Additional resources available:**

- Assembly resources – [https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote\\_GaNassembly.pdf](https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf)
- Library of Altium footprints for production FETs and ICs – <https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip>  
(for preliminary device Altium footprints, contact EPC)

Efficient Power Conversion Corporation (EPC) reserves the right to make changes without further notice to any products herein to improve reliability, function or design. EPC does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights, nor the rights of others.  
 eGaN® is a registered trademark of Efficient Power Conversion Corporation. EPC Patent Listing: <https://epc-co.com/epc/about-epc/patents>

Information subject to change without notice.  
 Revised October, 2023