Ultra Small Voltage Detector with High Precision Delay Circuit and Manual Reset Function

■GENERAL DESCRIPTION

XC6127 series is ultra small highly accurate voltage detector with delay circuit built-in.

The device includes a highly accurate reference voltage source, manufactured using CMOS process technology and laser trimming technologies, it maintains high accuracy, low power consumption, and accurate releases delay time over the full operation temperature range.

The release delay time periods are internally set in a range from 50ms to 800ms.

Moreover, with the manual reset function, reset can be asserted at any time.

The device is available in both CMOS and N-channel open drain output configurations. Also detect logic is available in both RESETB (Active Low) and RESET (Active High).

Ultra small package USPN-4 is ideally suited for small design of portable devices and high densely mounting applications. The conventional packages SSOT-24, SOT-25 is also available for upper compatible replacements.

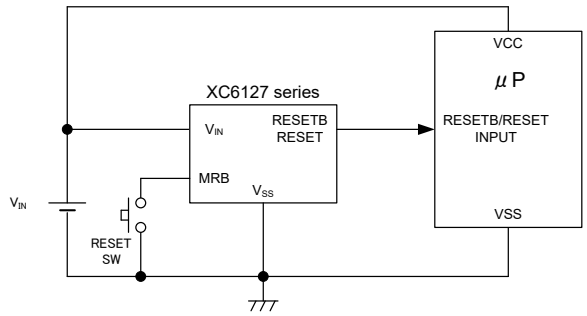
■APPLICATIONS

- Microprocessor logic reset circuitry
- System battery life and charge voltage monitors
- Memory battery back-up circuits
- Power-on reset circuits
- Power failure Detection
- Delay circuit

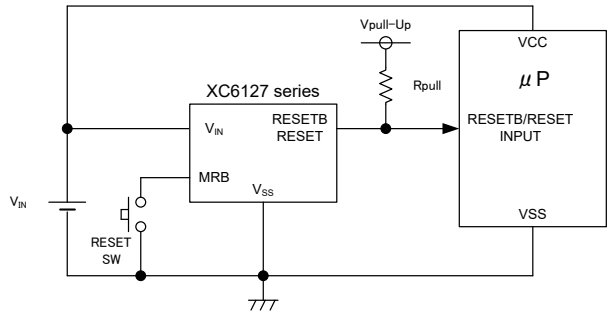
■FEATURES

High Accuracy	:	±0.8% (25℃)
Temperature Characteristics	:	±50ppm/℃
Low Power Consumption	:	0.6μA TYP. (Detect: V_{DF}=1.8V, V_{IN}=1.62V)
		0.7μA TYP. (Release: V_{DF}=1.8V, V_{IN}=1.98V)
Operating Voltage Range	:	0.7V ~ 6.0V
Detect Voltage Range	:	1.5V ~ 5.5V (0.1V increments)
Manual Reset Input	:	MRB Pin (Built-in Pull-up resistance)
Output Configuration	:	N-channel open drain or CMOS
Output Logic	:	RESETB (Active Low)
		RESET (Active High)
Release Delay Time	:	50ms/100ms/200ms/400ms/800ms±15%
Operating Ambient Temperature	:	-40℃ ~ 85℃
Packages	:	USPN-4, SSOT-24, SOT-25
Environmentally Friendly	:	EU RoHS Compliant, Pb Free

■TYPICAL APPLICATION CIRCUIT

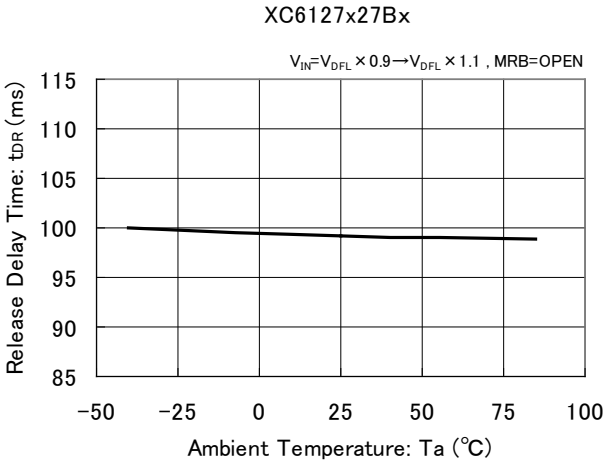


CMOS output



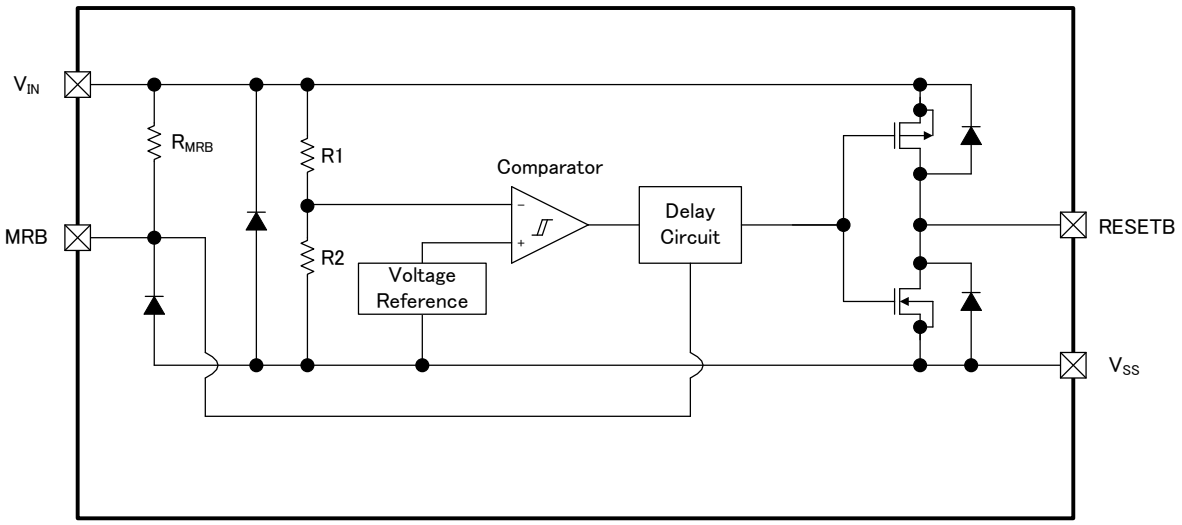
N-ch open drain output

■ TYPICAL PERFORMANCE CHARACTERISTICS



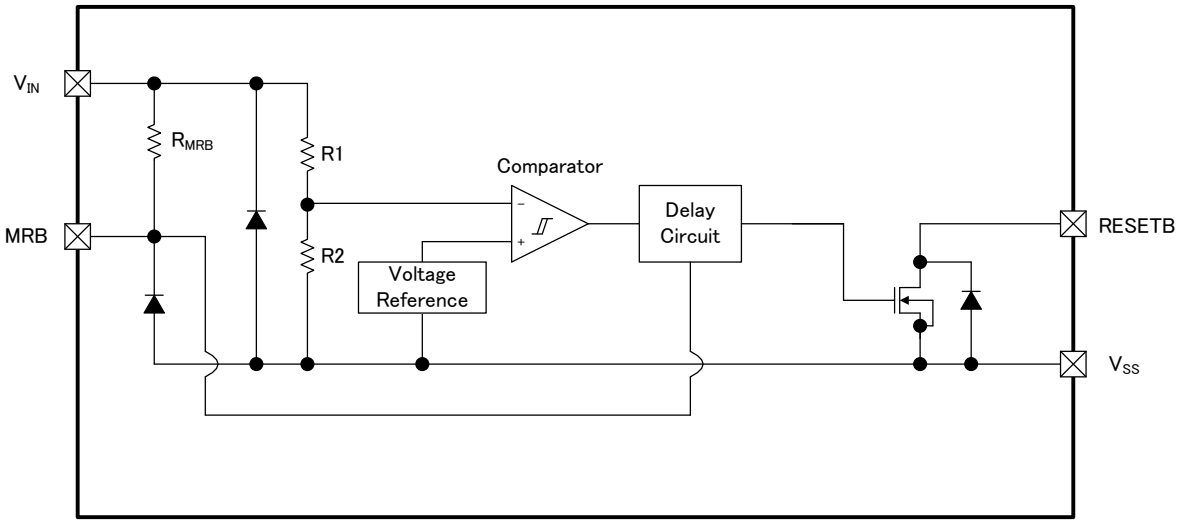
■BLOCK DIAGRAMS

1) XC6127 Series, Type CxxA/CxxB/CxxC/CxxD/CxxE (CMOS Output, Output Logic: Active Low)



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

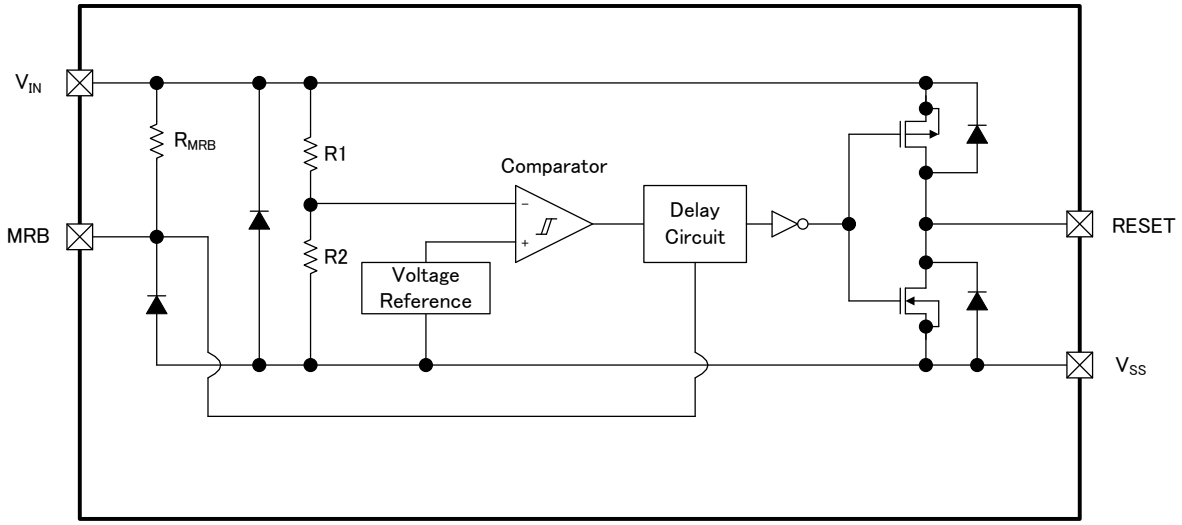
2) XC6127 Series, Type NxxA/NxxB/NxxC/NxxD/NxxE (N-ch Open Drain Output, Output Logic: Active Low)



* Diodes inside the circuits are ESD protection diodes

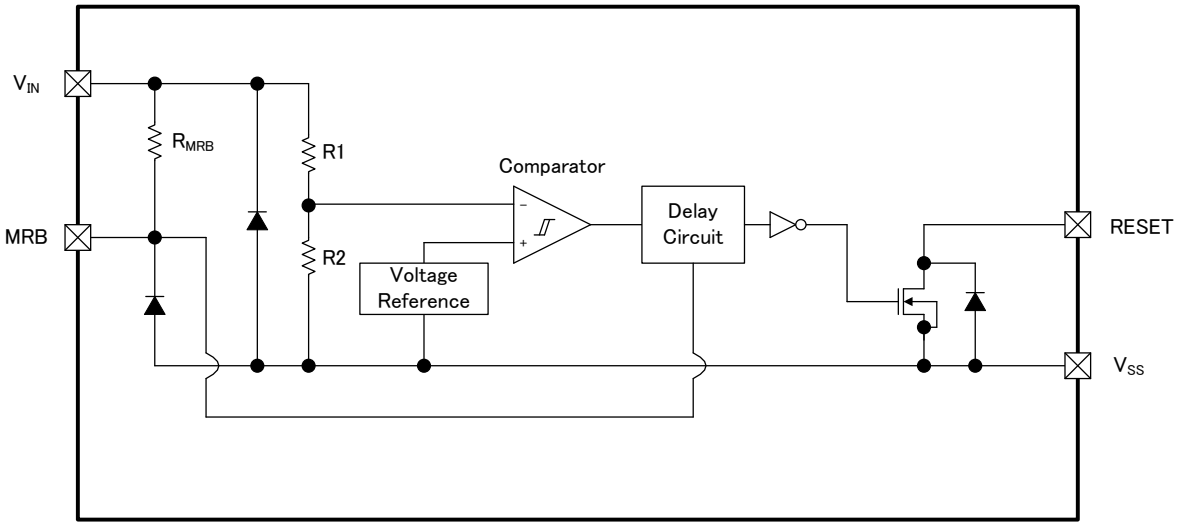
■BLOCK DIAGRAMS (Continued)

3) XC6127 Series, Type CxxF/CxxG/CxxH/CxxJ/CxxK (CMOS Output, Output Logic: Active High)



* Diodes inside the circuits are ESD protection diodes and parasitic diodes.

4) XC6127 Series, Type NxxF/NxxG/NxxH/NxxJ/NxxK (N-ch Open Drain Output, Output Logic: Active High).



* Diodes inside the circuits are ESD protection diodes.

■PRODUCT CLASSIFICATION

●Ordering Information

XC6127①②③④⑤⑥-⑦(*1)

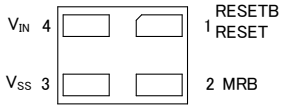
DESIGNATOR	ITEM	SYMBOL	DESCRIPTION
①	Output Configuration	C	CMOS output
		N	N-ch open drain output
②③	Detect Voltage	15 ~ 55	e.g. 2.7V → ②=2, ③=7
④	Type	A	Reset Active Low, Release Delay Time: 50ms
		B	Reset Active Low, Release Delay Time: 100ms
		C	Reset Active Low, Release Delay Time: 200ms
		D	Reset Active Low, Release Delay Time: 400ms
		E	Reset Active Low, Release Delay Time: 800ms
		F	Reset Active High, Release Delay Time: 50ms
		G	Reset Active High, Release Delay Time: 100ms
		H	Reset Active High, Release Delay Time: 200ms
		J	Reset Active High, Release Delay Time: 400ms
		K	Reset Active High, Release Delay Time: 800ms
⑤⑥-⑦(*1)	Packages (Order Unit)	7R-G	USPN-4 (5,000pcs/Reel)
		MR-G	SOT-25 (3,000pcs/Reel)
		NR-G	SSOT-24 (3,000pcs/Reel)

(*1) The “-G” suffix denotes Halogen and Antimony free as well as being fully EU RoHS compliant.

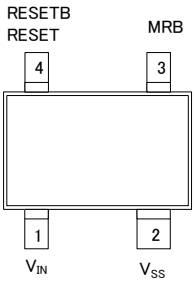
2) Selection Guide

TYPE	Release Delay Time	Output Logic
A	50ms	Active Low
B	100ms	Active Low
C	200ms	Active Low
D	400ms	Active Low
E	800ms	Active Low
F	50ms	Active High
G	100ms	Active High
H	200ms	Active High
J	400ms	Active High
K	800ms	Active High

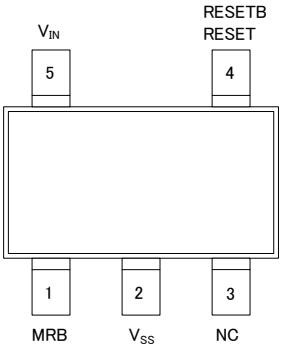
■PIN CONFIGURATION



USPN-4
(BOTTOM VIEW)



SSOT-24
(TOP VIEW)



SOT-25
(TOP VIEW)

■PIN ASSIGNMENT

PIN NUMBER			PIN NAME	FUNCTIONS
USPN-4	SSOT-24	SOT-25		
1	4	4	RESETB	Signal Output (Active Low) (*1)
			RESET	Signal Output (Active High) (*2)
2	3	1	MRB	Manual Reset Input
3	2	2	V_{SS}	Ground
4	1	5	V_{IN}	Power Input
-	-	3	NC	No Connection

(*1) Type A ~ E (Refer to the ④ in Ordering Information table)
(*2) Type F ~ K (Refer to the ④ in Ordering Information table)

■FUNCTION CHART

PIN NAME	SIGNAL	STATUS
MRB	L	Forced Reset
	H	Normal Operation
	OPEN	Normal Operation

■ABSOLUTE MAXIMUM RATINGS

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage		V_{IN}	V_{SS} - 0.3 ~ V_{SS} + 6.5	V
MRB Input Voltage		V_{MRB}	V_{SS} ~ V_{SS}+6.5	V
Output Current		(*1)	20	mA
Output Voltage	XC6127C (*2)	(*4)	V_{SS} - 0.3 ~ V_{IN} + 0.3 ≦ V_{SS} + 6.5	V
	XC6127N (*3)		V_{SS} - 0.3 ~ V_{SS} + 6.5	
Power Dissipation (Ta=25℃)	USPN-4	Pd	100	mW
			600 (40mm x 40mm Standard board) (*5)	
	SOT-25		250	
			600 (40mm x 40mm Standard board) (*5)	
			760 (JESD51-7 board)) (*5)	
	SSOT-24		150	
			500 (40mm x 40mm Standard board) (*5)	
			680 (JESD51-7 board) (*5)	
Operating Ambient Temperature		Topr	-40 ~ 85	℃
Storage Temperature		Tstg	-55 ~ 125	℃

(*1) SYMBOL is different for each product.
I_{RBOUT}: Type XC6127CxxA/CxxB/CxxC/CxxD/CxxE, Type XC6127NxxA/NxxB/NxxC/NxxD/NxxE
I_{ROUT}: Type XC6127CxxF/CxxG/CxxH/CxxJ/CxxK, Type XC6127NxxF/NxxG/NxxH/NxxJ/NxxK
(*2) CMOS Output
(*3) N-ch Open Drain Output
(*4) SYMBOL is different for each product.
V_{RESETB}: Type XC6127CxxA/CxxB/CxxC/CxxD/CxxE, Type XC6127NxxA/NxxB/NxxC/NxxD/NxxE
V_{RESET}: Type XC6127CxxF/CxxG/CxxH/CxxJ/CxxK, Type XC6127NxxF/NxxG/NxxH/NxxJ/NxxK
(*5) This power dissipation figure shown is PCB mounted and is for reference only.
Please refer to PACKAGING INFORMATION for the mounting condition.

■ELECTRICAL CHARACTERISTICS

●XC6127CxxA/CxxB/CxxC/CxxD/CxxE, XC6127NxxA/NxxB/NxxC/NxxD/NxxE (Output Logic: Active Low)

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUI
Operating Voltage	V_{IN}	$V_{DF(T)}$(*1)=1.5 ~ 5.5V, MRB=OPEN (*2)	0.7 (*3)		6.0	V	–
Detect Voltage	V_{DFL}	$V_{DF(T)}$=1.5 ~ 5.5V, MRB=OPEN	$V_{DF(T)}$×0.992	$V_{DF(T)}$	$V_{DF(T)}$×1.008	V	①
			E-1(*4)				
Hysteresis Width	V_{HYS}		V_{DFL}×0.02	V_{DFL}×0.05	V_{DFL}×0.08	V	①
Supply Current 1	I_{SS1}	V_{IN}=V_{DFL}×0.9 , MRB=OPEN				μA	②
		$V_{DF(T)}$=1.5 ~ 1.8V	-	0.6	1.4		
		$V_{DF(T)}$=1.9 ~ 3.0V	-	0.7	1.6		
		$V_{DF(T)}$=3.1 ~ 5.5V	-	1.0	1.9		
Supply Current 2	I_{SS2}	V_{IN}=V_{DFL}×1.1(*5) , MRB=OPEN				μA	②
		$V_{DF(T)}$=1.5 ~ 1.8V	-	0.7	1.6		
		$V_{DF(T)}$=1.9 ~ 3.0V	-	0.8	1.9		
		$V_{DF(T)}$=3.1 ~ 5.5V	-	1.1	2.35		
RESETB Output Current	I_{RBOUT1}	V_{IN}=0.7V, V_{RESETB}=0.5V(Nch) , MRB=OPEN	0.014	0.2	-	mA	③
		V_{IN}=1.0V, V_{RESETB}=0.5V(Nch) , MRB=OPEN	0.5	1.6	-		
		V_{IN}=2.0V(*6), V_{RESETB}=0.5V(Nch) , MRB=OPEN	4.4	7.0	-		
		V_{IN}=3.0V(*7), V_{RESETB}=0.5V(Nch) , MRB=OPEN	7.0	9.0	-		
		V_{IN}=4.0V(*8), V_{RESETB}=0.5V(Nch) , MRB=OPEN	8.5	11.0	-		
		V_{IN}=5.0V(*9), V_{RESETB}=0.5V(Nch) , MRB=OPEN	9.0	12.0	-		
	I_{RBOUT2}(*10)	V_{IN}=6.0V, V_{RESETB}=5.5V(Pch) , MRB=OPEN	-	-4.5	-3.0	mA	③
RESETB Leakage Current CMOS Output(Pch)	I_{LEAK}	V_{IN}=V_{DFL}×0.9, V_{RESETB}=0V , MRB=OPEN	-	-0.01	-	μA	③
RESETB Leakage Current Nch Open Drain Output		V_{IN}=6.0V, V_{RESETB}=6.0V , MRB=OPEN	-	0.01	0.15	μA	
Temperature Characteristics	ΔV_{DFL}/(ΔTopr・V_{DFL})	-40℃≦Topr≦85℃	-	±50	-	ppm/℃	①
Detect Delay Time(*11)	t_{DF}	V_{IN}=V_{DFL}×1.1→V_{DFL}×0.9(*11), MRB=OPEN	-	-	100	μs	④
Release Delay Time(*12)	t_{DR}	V_{IN}=V_{DFL}×0.9→V_{DFL}×1.1(*12), MRB=OPEN	E-2 (*13)			ms	④
MRB "Low" Level Voltage(*14)	V_{MRL}	V_{DFL}×1.1≦V_{IN}≦6.0V	V_{SS}	-	0.3	V	⑤
MRB "High" Level Voltage(*14)	V_{MRH}	V_{DFL}×1.1≦V_{IN}≦6.0V	1.0	-	6.0	V	⑤
MRB pull-up Resistance	R_{MRB}		0.4	0.8	3.0	MΩ	⑥
Minimum MRB Pulse Width	T_{MRB}	V_{IN}=6.0V, Applied pulse to MRB pin,	150	-	-	ns	⑦

(*1) $V_{DF(T)}$: Nominal detect voltage
(*2) For the N-ch Open Drain, Rpull=100kΩ, Vpull-Up=V_{IN}
Rpull: An External Pull-up resistor
Vpull-Up: Pull-up Voltage
(*3) V_{IN} voltage for V_{OUT}≦0.3V is under detect state.
(*4) For the detail value, please refer to "Voltage Table" in P10.
(*5) $V_{DF(T)}$ = 5.5V where V_{IN}=6.0V
(*6) For $V_{DF(T)}$＞2.0V products.
(*7) For $V_{DF(T)}$＞3.0V products.
(*8) For $V_{DF(T)}$＞4.0V products.
(*9) For $V_{DF(T)}$＞5.0V products.
(*10) For the XC6127C (CMOS output)
(*11) A time between V_{IN}=V_{DFL} and V_{RESETB}=V_{DFL}×0.45 when V_{IN} falls.
(*12) A time between V_{IN}=V_{DFL}+V_{HYS} and V_{RESETB}=V_{DFL}×0.55 when V_{IN} rises.
(*13) For the detail value, please refer to "Release Delay Time" in P11.
(*14) For MRB pin, please do not apply the voltage below V_{SS}.

■ELECTRICAL CHARACTERISTICS (Continued)

●XC6127CxxF/CxxG/CxxH/CxxJ/CxxK, XC6127NxxF/NxxG/NxxH/NxxJ/NxxK (Output Logic: Active High)

Ta=25℃

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS	CIRCUIT
Operating Voltage	V_{IN}	$V_{DF(T)}$(*1)=1.5 ~ 5.5V, MRB=OPEN(*2)	0.7 (*3)		6.0	V	–
Detect Voltage	V_{DFH}	$V_{DF(T)}$=1.5 ~ 5.5V, MRB=OPEN	$V_{DF(T)}$×0.992	$V_{DF(T)}$	$V_{DF(T)}$×1.008	V	①
			E-1(*4)				
Hysteresis Width	V_{HYS}		V_{DFH}×0.02	V_{DFH}×0.05	V_{DFH}×0.08	V	①
Supply Current 1	I_{SS1}	V_{IN}=V_{DFH}×0.9, MRB=OPEN				μA	②
		$V_{DF(T)}$=1.5 ~ 1.8V	-	0.6	1.4		
		$V_{DF(T)}$=1.9 ~ 3.0V	-	0.7	1.6		
		$V_{DF(T)}$=3.1 ~ 5.5V	-	1.0	1.9		
Supply Current 2	I_{SS2}	V_{IN}=V_{DFH}×1.1(*5) , MRB=OPEN				μA	②
		$V_{DF(T)}$=1.5 ~ 1.8V	-	0.7	1.6		
		$V_{DF(T)}$=1.9 ~ 3.0V	-	0.8	1.9		
		$V_{DF(T)}$=3.1 ~ 5.5V	-	1.1	2.35		
RESET Output Current	I_{ROUT1}	V_{IN}=1.65V(*6), V_{RESET}=0.5V(Nch) , MRB=OPEN	0.5	1.6	-	mA	③
		V_{IN}=2.0V(*7), V_{RESET}=0.5V(Nch) , MRB=OPEN	4.4	7.0	-		
		V_{IN}=3.0V(*8), V_{RESET}=0.5V(Nch) , MRB=OPEN	7.0	9.0	-		
		V_{IN}=4.0V(*9), V_{RESET}=0.5V(Nch) , MRB=OPEN	8.5	11.0	-		
		V_{IN}=5.0V(*10), V_{RESET}=0.5V(Nch) , MRB=OPEN	9.0	12.0	-		
		V_{IN}=6.0V, V_{RESET}=0.5V(Nch) , MRB=OPEN	9.0	12.0	-		
	I_{ROUT2} (*11)	V_{IN}=0.7V, V_{RESET}=0.2V(Pch) , MRB=OPEN	-	-0.07	-0.001	mA	③
		V_{IN}=1.0V, V_{RESET}=0.5V(Pch) , MRB=OPEN	-	-0.4	-0.09		
		V_{IN}=2.0V(*12), V_{RESET}=1.5V(Pch) , MRB=OPEN	-	-2.0	-1.3		
		V_{IN}=3.0V(*13), V_{RESET}=2.5V(Pch) , MRB=OPEN	-	-3.0	-1.8		
		V_{IN}=4.0V(*14), V_{RESET}=3.5V(Pch) , MRB=OPEN	-	-4.0	-2.5		
		V_{IN}=5.0V(*15), V_{RESET}=4.5V(Pch) , MRB=OPEN	-	-4.5	-3.0		
RESET Leakage Current: CMOS Output (P-ch)	I_{LEAK}	V_{IN}=6.0V, V_{RESET}=0V, MRB=OPEN	-	-0.01	-	μA	③
RESET Leakage Current: N-ch Open Drain Output		V_{IN}=V_{DFH}×0.9, V_{RESET}=6.0V, MRB=OPEN	-	0.01	0.15	μA	
Temperature Characteristics	ΔV_{DFH}/ (ΔTopr·V_{DFH})	-40℃≦Topr≦85℃	-	±50	-	ppm/℃	①
Detect Delay Time(*16)	t_{DF}	V_{IN}=V_{DFH}×1.1→V_{DFH}×0.9(*16), MRB=OPEN	-	-	E-3(*17)	μs	④
Release Delay Time(*18)	t_{DR}	V_{IN}=V_{DFH}×0.9→V_{DFH}×1.1(*18), MRB=OPEN	E-2(*19)			ms	④
MRB "Low" Level Voltage(*20)	V_{MRL}	V_{DFH}×1.1≦V_{IN}≦6.0V	V_{SS}	-	0.3	V	⑤
MRB "High" Level Voltage(*20)	V_{MRH}	V_{DFH}×1.1≦V_{IN}≦6.0V	1.0	-	6.0	V	⑤
MRB pull-up Resistance	R_{MRB}		0.4	0.8	3.0	MΩ	⑥
Minimum MRB Pulse Width	T_{MRB}	V_{IN}=6.0V, Applied pulse to MRB pin, 6.0V→0V	150	-	-	ns	⑦

■ELECTRICAL CHARACTERISTICS (Continued)

(*1) $V_{DF\ (T)}$: Nominal detect voltage
(*2) For the N-ch Open Drain, Rpull=100kΩ, Vpull-Up=V_{IN}
Rpull: An External Pull-up resistor
Vpull-Up: Pull-up Voltage
(*3) V_{IN} voltage for $V_{OUT} \geqq 0.4V$ is under detect state.
(*4) For the detail value, please refer to “Voltage Table” in P10.
(*5) $V_{DF\ (T)}$ = 5.5V where V_{IN}=6.0V
(*6) For $V_{DF\ (T)}$ =1.5V products.
(*7) For $V_{DF(T)} \leqq 1.8V$ products.
(*8) For VDF(T)≦2.7V products.
(*9) For $V_{DF(T)} \leqq 3.6V$ products.
(*10) For $V_{DF(T)} \leqq 4.6V$ products.
(*11) For the XC6127C (CMOS output)
(*12) For $V_{DF(T)} > 2.0V$ products.
(*13) For $V_{DF(T)} > 3.0V$ products.
(*14) For $V_{DF(T)} > 4.0V$ products.
(*15) For $V_{DF(T)} > 5.0V$ products.
(*16) A time between $V_{IN}=V_{DFH}$ and $V_{RESET}=V_{DFH} \times 0.45$ when V_{IN} falls.
(*17) For the detail value, please refer to “Detect Delay Time” in P11.
(*18) A time between $V_{IN}=V_{DFH}+V_{HYS}$ and $V_{RESET}=V_{DFH} \times 0.55$ when V_{IN} rises.
(*19) For the detail value, please refer to “Release Delay Time” in P11.
(*20) For MRB pin, please do not apply the voltage below V_{SS}.

■ELECTRICAL CHARACTERISTICS (Continued)

Voltage Table 1

NOMINAL DETECT VOLTAGE (V)	DETECT VOLTAGE (V) E-1	
$V_{DF(T)}$	V_{DFL} or V_{DFH}	
	MIN.	MAX.
1.50	1.4880	1.5120
1.60	1.5872	1.6128
1.70	1.6864	1.7136
1.80	1.7856	1.8144
1.90	1.8848	1.9152
2.00	1.9840	2.0160
2.10	2.0832	2.1168
2.20	2.1824	2.2176
2.30	2.2816	2.3184
2.40	2.3808	2.4192
2.50	2.4800	2.5200
2.60	2.5792	2.6208
2.70	2.6784	2.7216
2.80	2.7776	2.8224
2.90	2.8768	2.9232
3.00	2.9760	3.0240
3.10	3.0752	3.1248
3.20	3.1744	3.2256
3.30	3.2736	3.3264
3.40	3.3728	3.4272
3.50	3.4720	3.5280
3.60	3.5712	3.6288
3.70	3.6704	3.7296
3.80	3.7696	3.8304
3.90	3.8688	3.9312
4.00	3.9680	4.0320

Voltage Table 2

NOMINAL DETECT VOLTAGE (V)	DETECT VOLTAGE (V) E-1	
$V_{DF(T)}$	V_{DFL} or V_{DFH}	
	MIN.	MAX.
4.10	4.0672	4.1328
4.20	4.1664	4.2336
4.30	4.2656	4.3344
4.40	4.3648	4.4352
4.50	4.4640	4.5360
4.60	4.5632	4.6368
4.70	4.6624	4.7376
4.80	4.7616	4.8384
4.90	4.8608	4.9392
5.00	4.9600	5.0400
5.10	5.0592	5.1408
5.20	5.1584	5.2416
5.30	5.2576	5.3424
5.40	5.3568	5.4432
5.50	5.4560	5.5440

■ELECTRICAL CHARACTERISTICS (Continued)

Release Delay Time Table

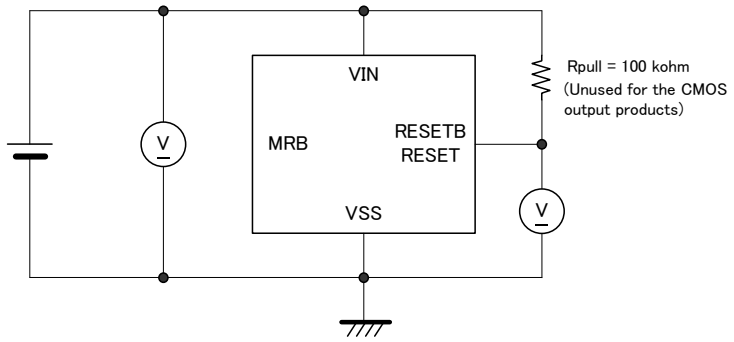
TYPE	RELEASE DELAY TIME (ms) E-2		
	t_{DR}		
	MIN.	TYP.	MAX.
XC6127CxxA / XC6127NxxA	42.5	50	57.5
XC6127CxxB / XC6127NxxB	85	100	115
XC6127CxxC / XC6127NxxC	170	200	230
XC6127CxxD / XC6127NxxD	340	400	460
XC6127CxxE / XC6127NxxE	680	800	920
XC6127CxxF / XC6127NxxF	42.5	50	57.5
XC6127CxxG / XC6127NxxG	85	100	115
XC6127CxxH / XC6127NxxH	170	200	230
XC6127CxxJ / XC6127NxxJ	340	400	460
XC6127CxxK / XC6127NxxK	680	800	920

Detect Delay Time Table

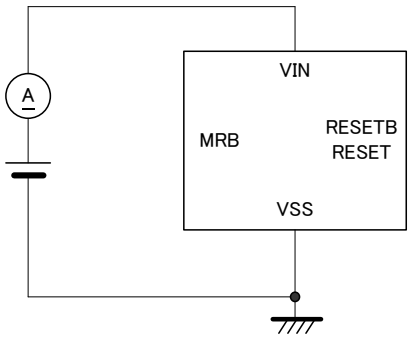
TYPE	DETECT DELAY TIME (μs) E-3
	t_{DF}
	MAX.
XC6127CxxF/CxxG/CxxH/CxxJ/CxxK	100
XC6127NxxF/NxxG/NxxH/NxxJ/NxxK	200

■TEST CIRCUITS

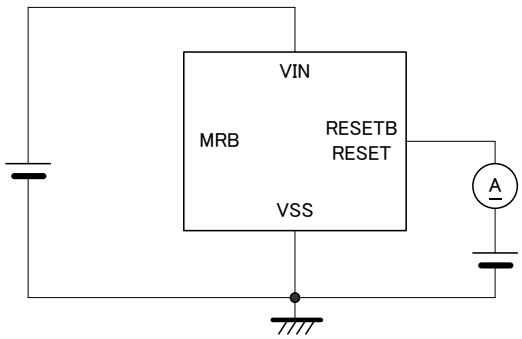
Circuit ①



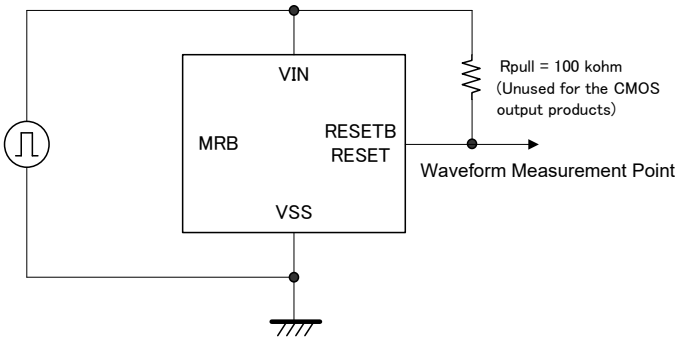
Circuit ②



Circuit ③

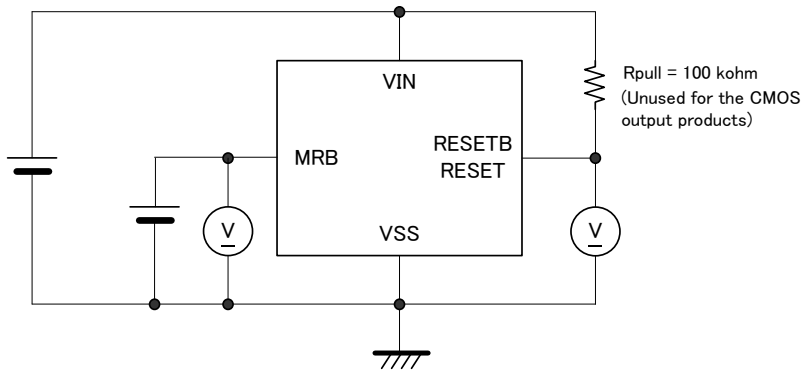


Circuit ④

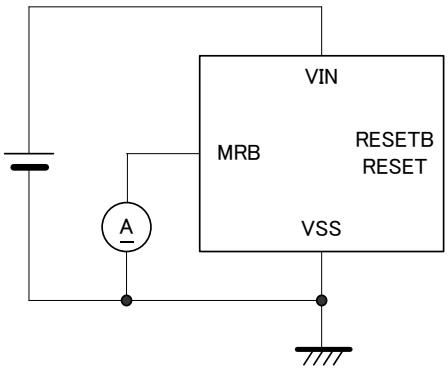


■TEST CIRCUITS (Continued)

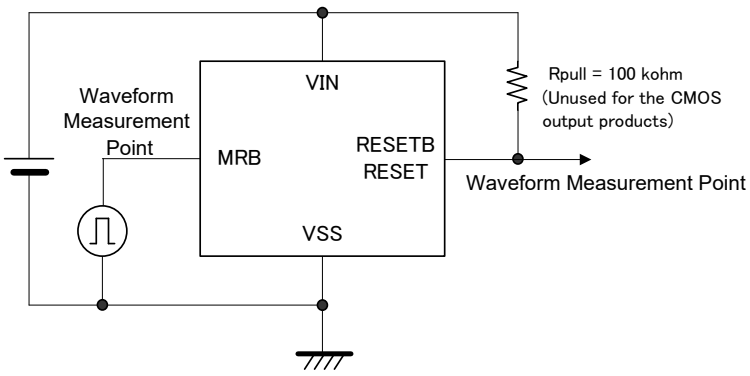
Circuit ⑤



Circuit ⑥



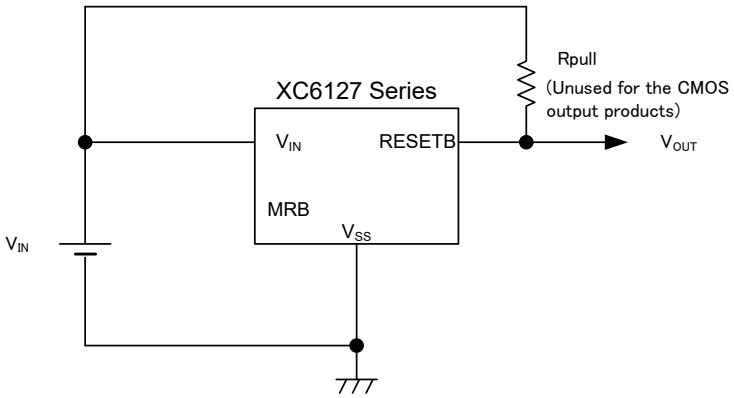
Circuit ⑦



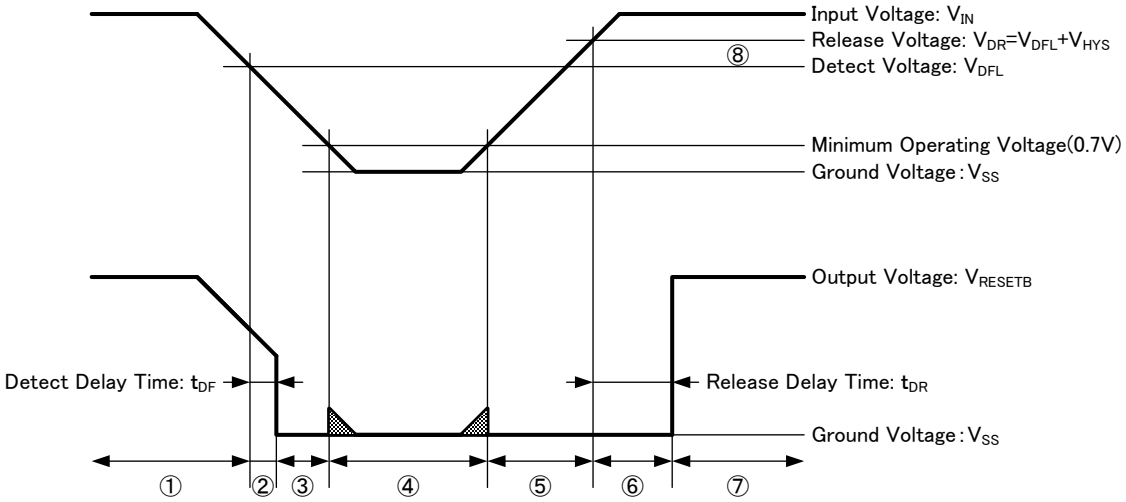
■OPERATIONAL EXPLANATION

1. Detect / Release operation using XC6127CxxA/CxxB/CxxC/CxxD/CxxE, XC6127NxxA/NxxB/NxxC/NxxD/NxxE (Output Logic: Active Low)

●Typical Application Circuit



●Timing Chart



A timing chart is used to explain the operation of the typical application circuit when MRB is open.

①In the initial state, an input voltage (V_{IN}) higher than the release voltage (V_{DR}) is applied, and then V_{IN} gradually falls.
While the input voltage (V_{IN}) is higher than the detect voltage (V_{DFL}), an output voltage (V_{RESETB}) equal to the input voltage (V_{IN}) goes out.
*In the case of an N-ch open drain output product, the RESETB pin is in a high-impedance state, and if the output is pulled up, the output voltage (V_{RESETB}) is equal to the pull-up voltage.

②③After the elapse of the detect delay time (t_{DF}) that starts when the input voltage (V_{IN}) falls below the detect voltage (V_{DFL}), an output voltage (V_{RESETB}) equal to the ground voltage (V_{SS}) goes out (detection state).
*This is the same on the N-ch open drain output product.

④The input voltage (V_{IN}) drops further, and if it falls below the minimum operating voltage (0.7V), the output becomes undefined state.
*When an N-ch open drain output product is used and the output pin is pulled up, an output voltage (V_{RESETB}) equal to the pull-up voltage may be output.

⑤The input voltage (V_{IN}) rises past the minimum operating voltage (0.7V), and until it reaches the release voltage (V_{DR}), the output voltage (V_{RESETB}) is equal to the ground voltage.

⑥ From the time that the input voltage (V_{IN}) becomes higher than the release voltage (V_{DR}) until the release delay time (t_{DR}) elapses, the output voltage (V_{RESETB}) remains at the ground voltage due to the delay circuit.

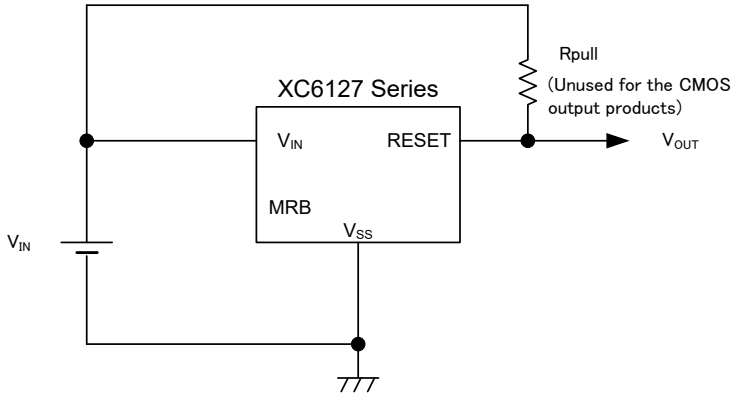
⑦ After the release delay time (t_{DR}) elapses, the output voltage (V_{RESETB}) is equal to the input voltage (VIN) (release state).
*In the case of an N-ch open drain output product, the RESETB pin will be in a high impedance state like ①. If the output is pulled up, an output voltage (V_{RESETB}) equal to the pull-up voltage will be output.

⑧The difference between the release voltage (V_{DR}) and the detect voltage (V_{DFL}) is the hysteresis width (V_{HYS}).

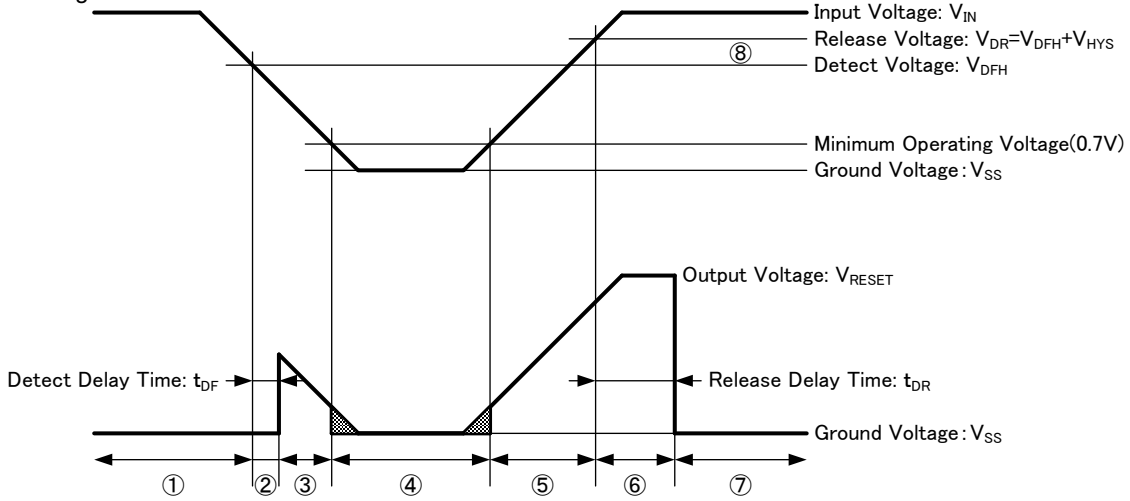
■OPERATIONAL EXPLANATION (Continued)

2. XC6127CxxF/CxxG/CxxH/CxxJ/CxxK, XC6127NxxF/NxxG/NxxH/NxxJ/NxxK (Output Logic: Active High)

●Typical Application Circuit



●Timing Chart



A timing chart is used above to explain the operation of the typical application circuit when MRB is open.

① In the initial state, an input voltage (V_{IN}) higher than the release voltage (V_{DR}) is applied, and then V_{IN} gradually falls.
While the input voltage (V_{IN}) is higher than the detect voltage (V_{DFH}), an output voltage (V_{RESET}) equal to the ground voltage (V_{SS}) goes out.
*This is the same on the N-ch open drain output product.

②③After the elapse of the detect delay time (t_{DF}) that starts when the input voltage (V_{IN}) falls below the detect voltage (V_{DFH}), the output voltage (V_{RESET}) is equal to the input voltage (V_{IN}) (detection state).
*In the case of an N-ch open drain output product, the RESET pin is in a high-impedance state, and if the output is pulled up, the output voltage (V_{RESET}) is equal to the pull-up voltage.

④ The input voltage (V_{IN}) drops further, and if it falls below the minimum operating voltage (0.7V), the output becomes undefined state.

⑤The input voltage (V_{IN}) rises past the minimum operating voltage (0.7V), and until it reaches the release voltage (V_{DR}), the output voltage (V_{RESET}) is equal to the V_{IN} voltage.
*In the case of an N-ch open drain output product, the RESET pin is in a high-impedance state, and if the output is pulled up, the output voltage (V_{RESET}) is equal to the pull-up voltage.

⑥From the time that the input voltage (V_{IN}) becomes higher than the release voltage (V_{DR}) until the release delay time (t_{DR}) elapses, the output voltage (V_{RESET}) remains equal to the VIN voltage due to the delay circuit.

⑦After the release delay time (t_{DR}) elapses, the output voltage (V_{RESET}) is equal to the ground voltage (V_{SS}) (release state).

⑧The difference between the release voltage (V_{DR}) and the detect voltage (V_{DFH}) is the hysteresis width (V_{HYS}).

■OPERATIONAL EXPLANATION (Continued)

3. MRB Pin

The output pin signal can be forcibly changed to the detect state by an input signal to the MRB pin.
The operation of the circuit at MRB signal input is explained using a timing chart.

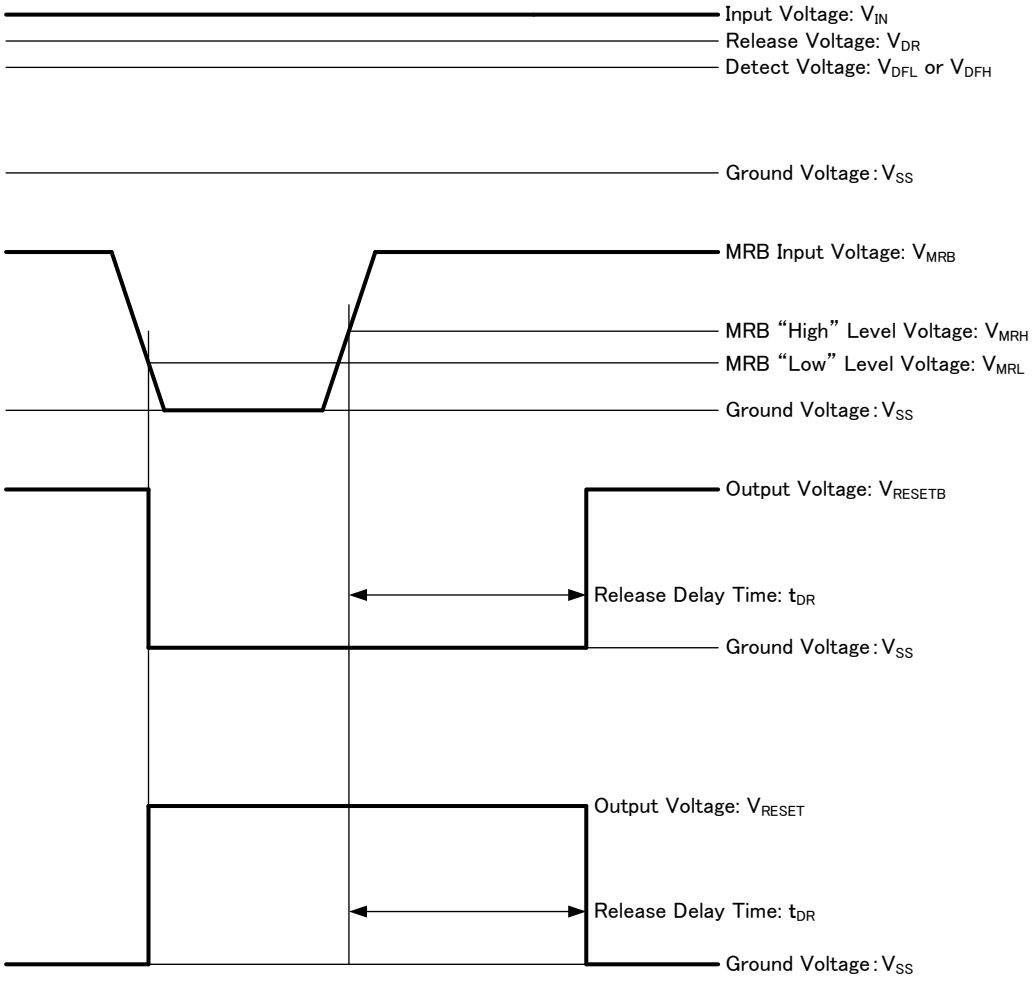
When an H level (V_{MRH}) signal and then an L (or less) level (V_{MRL}) signal are input to the MRB input voltage (V_{MRB}) with a voltage equal to or higher than V_{DR} applied to the input voltage (V_{IN}), the output pin outputs release state (*1) and then detect state (*2) signals.
During the release delay time (t_{DR}) after the MRB input voltage (V_{MRB}) changes from the L level (V_{MRL}) to the H level (V_{MRH}), the output pin maintains the detection state. After the release delay time (t_{DR}) elapses, the output pin outputs the release state signal.

(*1) The output voltage in the release state is indicated below by product type.
XC6127xxxA/xxxB/xxxC/xxxD/xxxE types (output logic: Active Low) : Input voltage (V_{IN}) (*3)
XC6127xxxF/xxxG/xxxH/xxxJ/xxxK types (output logic: Active High) : Ground voltage (V_{SS})

(*2) The output voltage in the detect state is indicated below by product type.
XC6127xxxA/xxxB/xxxC/xxxD/xxxE types (output logic: Active Low) : Ground voltage (V_{SS})
XC6127xxxF/xxxG/xxxH/xxxJ/xxxK types (output logic: Active High) : Input voltage (V_{IN}) (*3)

(*3) On an N-ch open drain output product, if the output is pulled up, the output voltage is the pull-up voltage.
(*4) A pull-up resistance (R_{MRB}) is built-in between the MRB pin and the VIN pin, and thus if a voltage is applied to the MRB pin, current will flow from the VIN pin to the MRB pin.
(*5) The voltage input to the MRB pin should be within the range V_{SS} to 6.0 V.

●Timing Chart



■NOTES ON USE

1. Please use this IC within the stated maximum ratings. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.

2. Note that there is a possibility of malfunctioning if the input voltage changes sharply or undergoes repeated, cyclical changes.

3. If the resistance R_{IN} is connected between the VIN pin and the power supply V_{DD}, the voltage drop due to the flow through current in the internal circuit and R_{IN} may cause oscillation when release takes place. When using the CMOS output product, oscillation due to R_{IN} and the flow through current may occur without relation to release and detection, and thus R_{IN} should not be connected.

4. When N-ch open drain output is used, the output voltage at detection is determined by the pull-up resistance connected to the output pin. Select the resistance based on the following considerations:

Using XC6127NxxA/NxxB/NxxC/NxxD/NxxE (output logic: Active Low)
At detection: V_{RESETB}= (Vpull-Up)/ (1+Rpull/R_{ON})
Vpull-Up: Voltage after pull-up
R_{ON} (*1): ON resistance of N-ch driver (calculated from V_{RESETB}/I_{RBOUT1} in electrical characteristics) (*3)

Example calculation:
When V_{IN}=2.0V (*2), R_{ON}=0.5/4.4×10-3≒114Ω(MAX.). If you wish to make the V_{RESETB} voltage at detection 0.1V or lower with Vpull-Up=3.0V, Rpull=(Vpull-Up /V_{RESETB}-1)×R_{ON}=(3/0.1-1)×114≒3.3kΩ, and thus to make the output voltage at detection 0.1V or less under the above conditions, the pull-up resistance must be 3.3kΩ or higher.
(*1) The smaller V_{IN} is, the larger R_{ON} becomes.
(*2) When selecting V_{IN}, calculate using the lowest value of the input voltage range you will use.
(*3) I_{RBOUT1} specified in the electrical characteristics is the value at Ta=25℃. I_{RBOUT1} varies depending on the ambient temperature. To select the pull-up resistance taking ambient temperature into account, please consult us.

At release: V_{RESETB} = (Vpull-Up)/ (1+Rpull/R_{OFF})
Vpull-Up: Voltage after pull-up
R_{OFF}: Resistance value 40MΩ(MIN.) when N-ch driver is OFF (calculated from V_{RESETB}/I_{LEAK} in electrical characteristics)

Calculation example:
If you wish to make V_{RESETB} 5.99V or higher with Vpull-Up=6.0V
Rpull=(Vpull-Up/V_{RESETB}-1)×R_{OFF}=(6/5.99-1)×40×106≒66kΩ, and thus to make the output voltage 5.99V or higher at release under the above conditions, the pull-up resistance must be 66kΩ or less.

Using theC6127NxxF/NxxG/NxxH/NxxJ/NxxK (output logic: Active High)
At detection：V_{RESET}=(Vpull-Up)/(1+Rpull/R_{OFF})
Vpull-Up: Voltage after pull-up
R_{OFF}: When the N-ch driver is OFF, the resistance is 40MΩ(MIN.) (calculated from V_{RESET}/I_{LEAK} in the electrical characteristics)

Calculation example:
If you wish to make V_{RESET} 5.99V or higher with Vpull-Up = 6.0V
Rpull=(Vpull-Up/V_{RESET}-1)×R_{OFF}=(6/5.99-1)×40×106≒66kΩ and thus to make the output voltage 5.99V or higher at detection under the above conditions, the pull-up resistance must be 66kΩ or less.

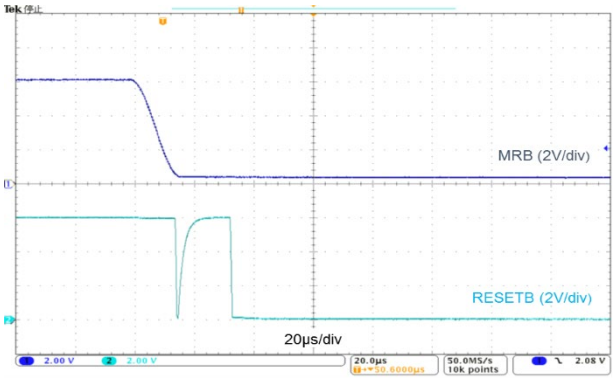
At release：V_{RESET}=(Vpull-Up)/(1+Rpull/R_{ON})
Vpull-Up：Voltage after pull-up
R_{ON}(*1)：ON resistance of N-ch driver (calculated from V_{RESET}/I_{ROUT1} in the electrical characteristics)(*3)

Calculation example:
When V_{IN}=2.0V (*2), R_{ON}=0.5/4.4×10-3≒114Ω (MAX.). If you wish to make the V_{RESET} voltage 0.1V or lower at detection with Vpull-Up=3.0 V, Rpull=(Vpull-Up /V_{RESET}-1)×R_{ON}=(3/0.1-1)×114≒3.3kΩ and thusto make the output voltage 0.1V or lower at release under the above conditions, the pull-up resistance must be 3.3kΩ or higher.
(*1) The smaller V_{IN} is the larger R_{ON} becomes.
(*2) When selecting V_{IN}, calculate using the lowest value of the input voltage range you will be using.
(*3) I_{ROUT1} specified in the electrical characteristics is the value at Ta=25℃. I_{ROUT1} varies depending on the ambient temperature. To select the pull-up resistance taking ambient temperature into account, please consult us.

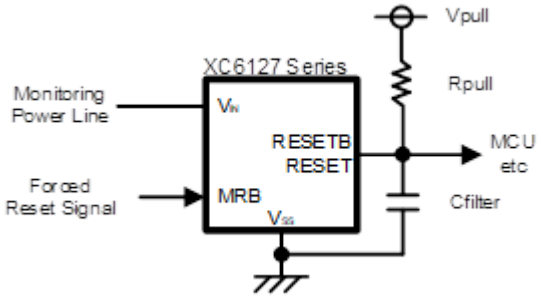
■NOTES ON USE(Continued)

5. If the input signal to the MRB pin is forced to be set to the detection state, the detection signal may be erroneously pulse output to the output within the period until the output pin constantly outputs the detection signal. (See the figure below)

When taking the above measures, connect an output capacitor to the output terminal and smooth the output signal. Please connect the output capacitance (Cfilter) of 0.1μF or more



Example of incorrect output signal (Active Low Type)



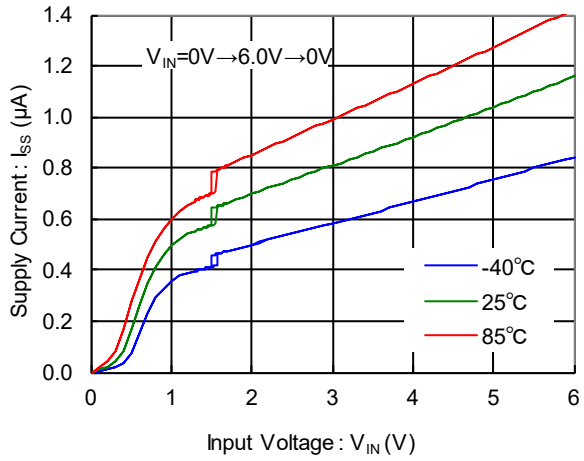
Counter measure circuit example (Nch-Open Drain Type)

6. We are striving to improve our products and reliability. However, in the unlikely event of an emergency, we recommend fail-safe design and aging treatment, as well as sufficient safety design on the device or system.

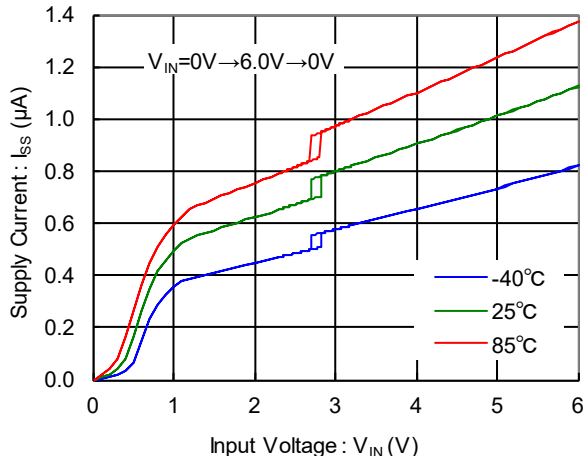
■TYPICAL PERFORMANCE CHARACTERISTICS

(1) Supply Current vs. Input Voltage

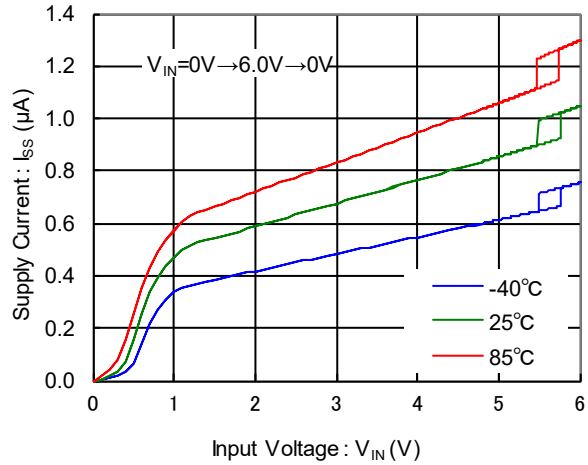
VDF(T)=1.5V



VDF(T)=2.7V

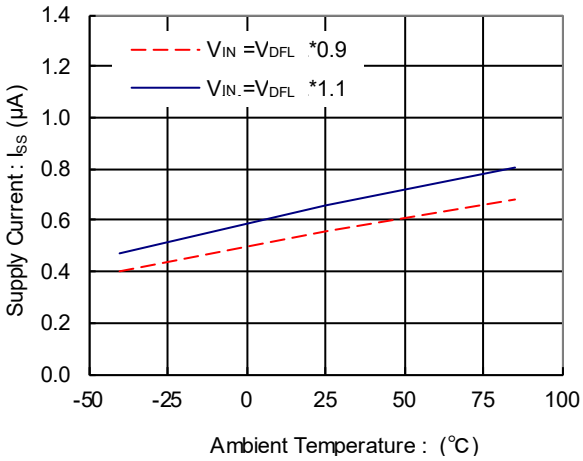


VDF(T)=5.5V

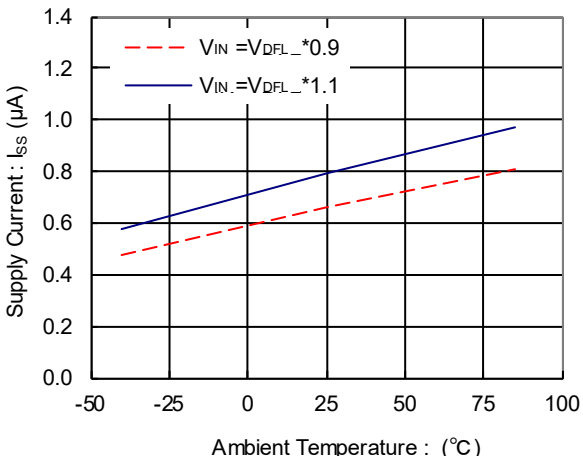


(2) Supply Current vs. Ambient Temperature

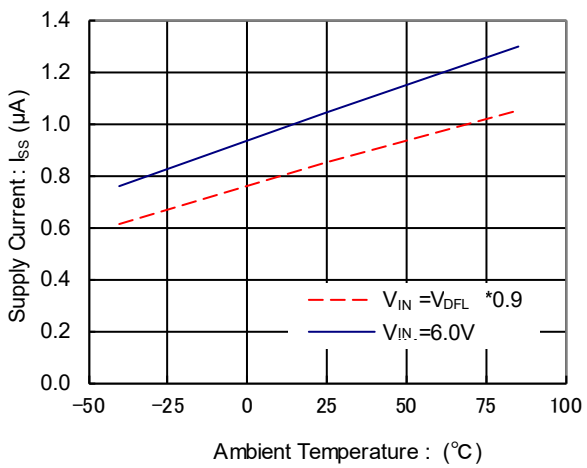
VDF(T)=1.5V



VDF(T)=2.7V



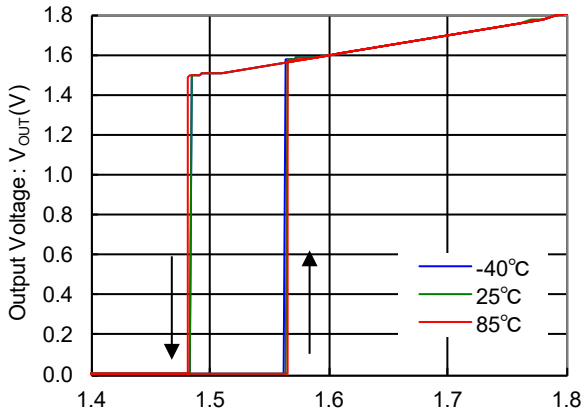
VDF(T)=5.5V



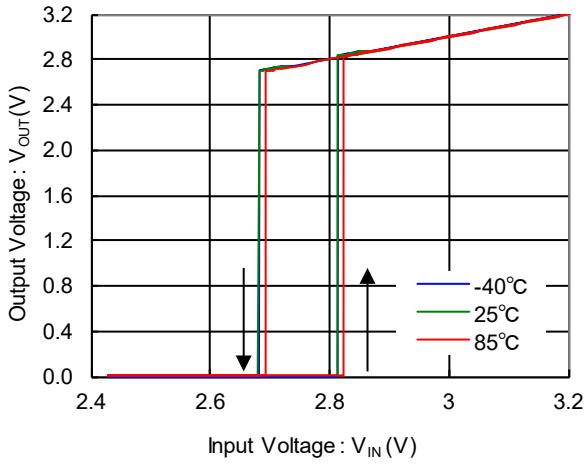
■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

(3) Output Voltage vs. Input Voltage1

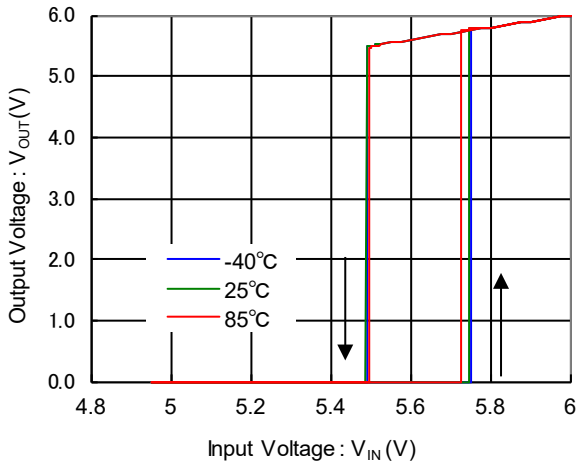
VDF(T)=1.5V



VDF(T)=2.7V

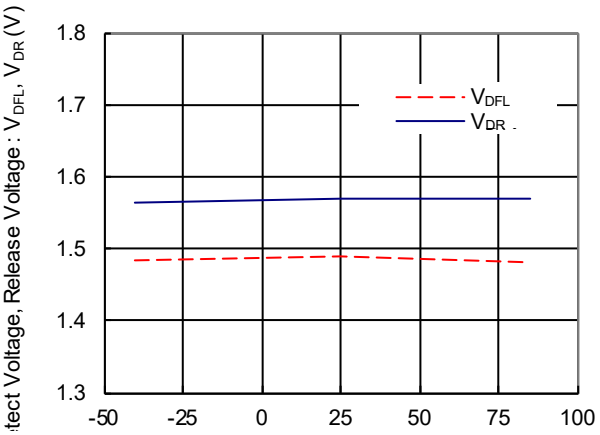


VDF (T) =5.5V

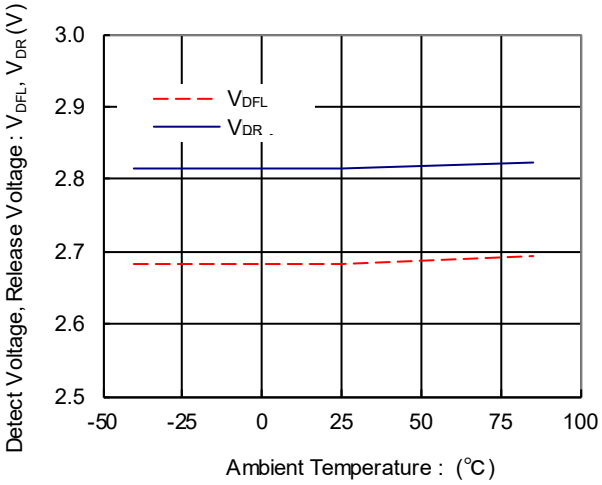


(4) Detect Voltage, Release Voltage vs. Ambient Temperature

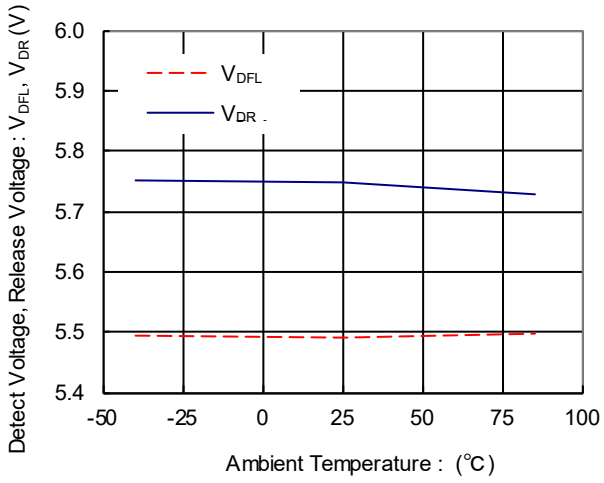
VDF(T)=1.5V



VDF(T)=2.7V



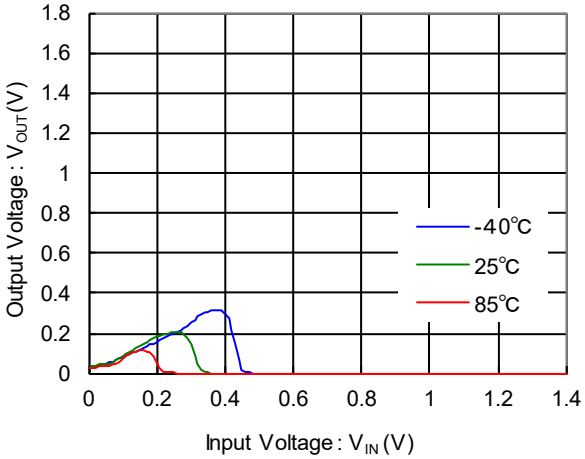
VDF(T)=5.5V



■TYPICAL PERFORMANCE CHARACTERISTICS(Continued)

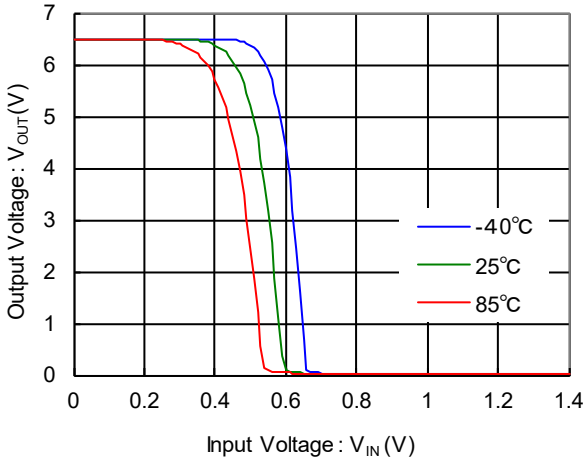
(5) Output Voltage vs. Input Voltage2

CMOS Output



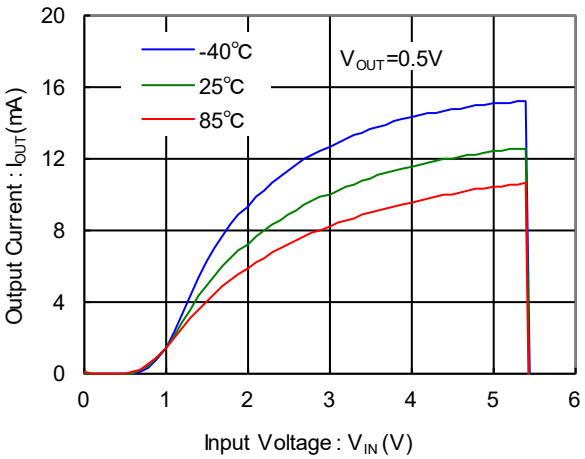
N-ch Open Drain Output

Vpull-Up=6.5V, Rpull=100kΩ



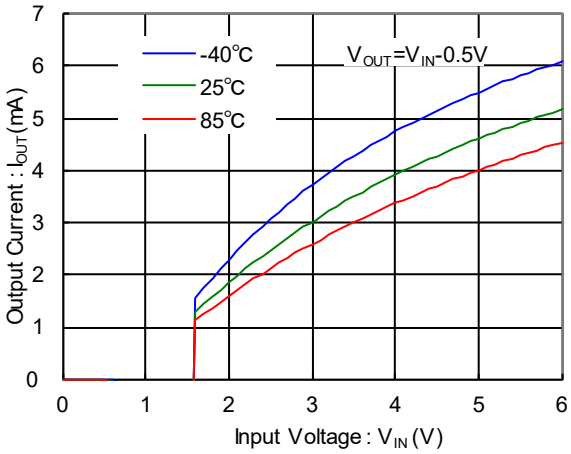
(6) Output Current (Nch Driver) vs. Input Voltage

VDF(T)=5.5V



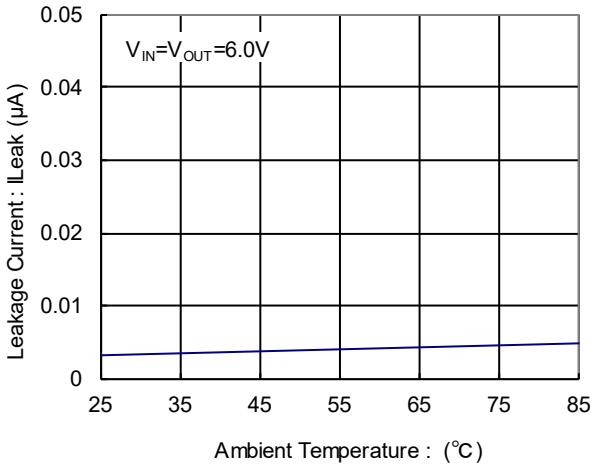
(7) Output Current (Pch Driver) vs. Input Voltage

VDF(T)=1.5V



(8) Leakage Current vs. Ambient temperature

N-ch Open Drain Output



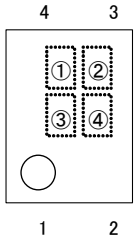
■PACKAGING INFORMATION

For the latest package information go to, www.torexsemi.com/technical-support/packages

PACKAGE	OUTLINE / LAND PATTERN	THERMAL CHARACTERISTICS
SOT-25	SOT-25 PKG	SOT-25 Power Dissipation
SSOT-24	SSOT-24 PKG	SSOT-24 Power Dissipation
USPN-4	USPN-4 PKG	USPN-4 Power Dissipation

■MARKING RULE

●USPN-4



① represents product series and output configuration.

MARK	OUTPUT CONFIGURATION	PRODUCT SERIES
F	CMOS	XC6127C*****-G
H	Nch	XC6127N*****-G

② represents detect voltage.

MARK	DETECT VOLTAGE(V)		MARK	DETECT VOLTAGE(V)		MARK	DETECT VOLTAGE(V)	
A	1.5	1.6	K	2.9	3.0	T	4.3	4.4
B	1.7	1.8	L	3.1	3.2	U	4.5	4.6
C	1.9	2.0	M	3.3	3.4	V	4.7	4.8
D	2.1	2.2	N	3.5	3.6	X	4.9	5.0
E	2.3	2.4	P	3.7	3.8	Y	5.1	5.2
F	2.5	2.6	R	3.9	4.0	Z	5.3	5.4
H	2.7	2.8	S	4.1	4.2	0	5.5	-

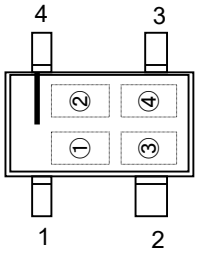
③ represents detect voltage range and release delay time / detect logic.

MARK	DETECT VOLTAGE [V]	RELEASE DELAY TIME/ DETECT LOGIC	PRODUCT SERIES
A	Odd number	50ms/Low	XC6127*15A**-G ～ XC6127*55A**-G
B		100ms/Low	XC6127*15B**-G ～ XC6127*55B**-G
C		200ms/Low	XC6127*15C**-G ～ XC6127*55C**-G
D		400ms/Low	XC6127*15D**-G ～ XC6127*55D**-G
E		800ms/Low	XC6127*15E**-G ～ XC6127*55E**-G
F		50ms/High	XC6127*15F**-G ～ XC6127*55F**-G
H		100ms/High	XC6127*15G**-G ～ XC6127*55G**-G
K		200ms/High	XC6127*15H**-G ～ XC6127*55H**-G
L		400ms/High	XC6127*15J**-G ～ XC6127*55J**-G
M		800ms/High	XC6127*15K**-G ～ XC6127*55K**-G
N	Even number	50ms/Low	XC6127*16A**-G ～ XC6127*54A**-G
P		100ms/Low	XC6127*16B**-G ～ XC6127*54B**-G
R		200ms/Low	XC6127*16C**-G ～ XC6127*54C**-G
S		400ms/Low	XC6127*16D**-G ～ XC6127*54D**-G
T		800ms/Low	XC6127*16E**-G ～ XC6127*54E**-G
U		50ms/High	XC6127*16F**-G ～ XC6127*54F**-G
V		100ms/High	XC6127*16G**-G ～ XC6127*54G**-G
X		200ms/High	XC6127*16H**-G ～ XC6127*54H**-G
Y		400ms/High	XC6127*16J**-G ～ XC6127*54J**-G
Z		800ms/High	XC6127*16K**-G ～ XC6127*54K**-G

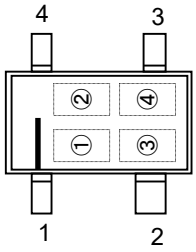
④ represents production lot number.
0 to 9, A to Z repeated. (G, I, J, O, Q, W excepted.)
* No character inversion used.

■MARKING RULE (Continued)

●SSOT-24



SSOT-24
(With the orientation bar at the top)



SSOT-24
(With the orientation bar at the bottom)

①−1 represents product series and detect voltage range, output configuration.

MARK	OUTPUT CONFIGURATION	DETECT VOLTAGE [V]	RELEASE DELAY TIME/ DETECT LOGIC	PRODUCT SERIES
5	CMOS	Odd number	50ms/Low	XC6127C15A**-G ～ XC6127C55A**-G
6			100ms/Low	XC6127C15B**-G ～ XC6127C55B**-G
7			200ms/Low	XC6127C15C**-G ～ XC6127C55C**-G
8			400ms/Low	XC6127C15D**-G ～ XC6127C55D**-G
9			800ms/Low	XC6127C15E**-G ～ XC6127C55E**-G
A			50ms/High	XC6127C15F**-G ～ XC6127C55F**-G
B			100ms/High	XC6127C15G**-G ～ XC6127C55G**-G
C			200ms/High	XC6127C15H**-G ～ XC6127C55H**-G
D			400ms/High	XC6127C15J**-G ～ XC6127C55J**-G
E			800ms/High	XC6127C15K**-G ～ XC6127C55K**-G
F		Even number	50ms/Low	XC6127C16A**-G ～ XC6127C54A**-G
H			100ms/Low	XC6127C16B**-G ～ XC6127C54B**-G
K			200ms/Low	XC6127C16C**-G ～ XC6127C54C**-G
N			400ms/Low	XC6127C16D**-G ～ XC6127C54D**-G
P			800ms/Low	XC6127C16E**-G ～ XC6127C54E**-G
R			50ms/High	XC6127C16F**-G ～ XC6127C54F**-G
S			100ms/High	XC6127C16G**-G ～ XC6127C54G**-G
T			200ms/High	XC6127C16H**-G ～ XC6127C54H**-G
U			400ms/High	XC6127C16J**-G ～ XC6127C54J**-G
V			800ms/High	XC6127C16K**-G ～ XC6127C54K**-G

* The products of CMOS output configuration are shipped in the package having the orientation bar marked in the top.

■MARKING RULE (Continued)

①-2 represents product series and detect voltage range, output configuration.

MARK	OUTPUT CONFIGURATION	DETECT VOLTAGE [V]	RELEASE DELAY TIME/ DETECT LOGIC	品名表記例
0	Nch	Odd number	50ms/Low	XC6127N15A**-G ～ XC6127N55A**-G
1			100ms/Low	XC6127N15B**-G ～ XC6127N55B**-G
2			200ms/Low	XC6127N15C**-G ～ XC6127N55C**-G
3			400ms/Low	XC6127N15D**-G ～ XC6127N55D**-G
4			800ms/Low	XC6127N15E**-G ～ XC6127N55E**-G
5			50ms/High	XC6127N15F**-G ～ XC6127N55F**-G
6			100ms/High	XC6127N15G**-G ～ XC6127N55G**-G
7			200ms/High	XC6127N15H**-G ～ XC6127N55H**-G
8			400ms/High	XC6127N15J**-G ～ XC6127N55J**-G
9			800ms/High	XC6127N15K**-G ～ XC6127N55K**-G
A		Even number	50ms/Low	XC6127N16A**-G ～ XC6127N54A**-G
B			100ms/Low	XC6127N16B**-G ～ XC6127N54B**-G
C			200ms/Low	XC6127N16C**-G ～ XC6127N54C**-G
D			400ms/Low	XC6127N16D**-G ～ XC6127N54D**-G
E			800ms/Low	XC6127N16E**-G ～ XC6127N54E**-G
F			50ms/High	XC6127N16F**-G ～ XC6127N54F**-G
H			100ms/High	XC6127N16G**-G ～ XC6127N54G**-G
K			200ms/High	XC6127N16H**-G ～ XC6127N54H**-G
L			400ms/High	XC6127N16J**-G ～ XC6127N54J**-G
M			800ms/High	XC6127N16K**-G ～ XC6127N54K**-G

* The products of Nch output configuration are shipped in the package having the orientation bar marked in the bottom.

② represents detect voltage.

MARK	DETECT VOLTAGE(V)		MARK	DETECT VOLTAGE(V)		MARK	DETECT VOLTAGE(V)	
A	1.5	1.6	K	2.9	3.0	T	4.3	4.4
B	1.7	1.8	L	3.1	3.2	U	4.5	4.6
C	1.9	2.0	M	3.3	3.4	V	4.7	4.8
D	2.1	2.2	N	3.5	3.6	X	4.9	5.0
E	2.3	2.4	P	3.7	3.8	Y	5.1	5.2
F	2.5	2.6	R	3.9	4.0	Z	5.3	5.4
H	2.7	2.8	S	4.1	4.2	0	5.5	-

③④ represents production lot number. 01 ~ 09, 0A ~ 0Z, 11 ~ 9Z, A1 ~ A9, AA～AZ、B1～ZZ repeated.

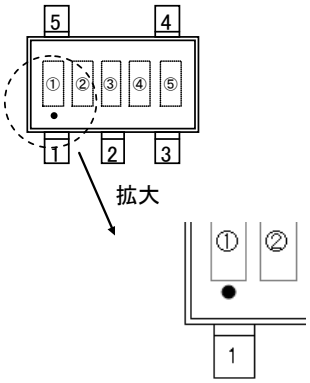
(G, I, J, O, Q, W excluded.)

* No character inversion used.

■MARKING RULE (Continued)

●SOT-25

SOT-25(Under dot)



① represents product series and output configuration.

MARK	OUTPUT CONFIGURATION	PRODUCT SERIES
5	CMOS	XC6127C*****-G
6	Nch	XC6127N*****-G

* SOT-25 with the under-dot marking is used.

② represents detect voltage.

MARK	DETECT VOLTAGE(V)		MARK	DETECT VOLTAGE(V)		MARK	DETECT VOLTAGE(V)	
A	1.5	1.6	K	2.9	3.0	T	4.3	4.4
B	1.7	1.8	L	3.1	3.2	U	4.5	4.6
C	1.9	2.0	M	3.3	3.4	V	4.7	4.8
D	2.1	2.2	N	3.5	3.6	X	4.9	5.0
E	2.3	2.4	P	3.7	3.8	Y	5.1	5.2
F	2.5	2.6	R	3.9	4.0	Z	5.3	5.4
H	2.7	2.8	S	4.1	4.2	0	5.5	-

③ represents detect voltage range and release delay time / detect logic.

MARK	DETECT VOLTAGE [V]	RELEASE DELAY TIME/ DETECT LOGIC	PRODUCT SERIES
A	Odd number	50ms/Low	XC6127*15A**-G ～ XC6127*55A**-G
B		100ms/Low	XC6127*15B**-G ～ XC6127*55B**-G
C		200ms/Low	XC6127*15C**-G ～ XC6127*55C**-G
D		400ms/Low	XC6127*15D**-G ～ XC6127*55D**-G
E		800ms/Low	XC6127*15E**-G ～ XC6127*55E**-G
F		50ms/High	XC6127*15F**-G ～ XC6127*55F**-G
H		100ms/High	XC6127*15G**-G ～ XC6127*55G**-G
K		200ms/High	XC6127*15H**-G ～ XC6127*55H**-G
L		400ms/High	XC6127*15J**-G ～ XC6127*55J**-G
M		800ms/High	XC6127*15K**-G ～ XC6127*55K**-G
N	Even number	50ms/Low	XC6127*16A**-G ～ XC6127*54A**-G
P		100ms/Low	XC6127*16B**-G ～ XC6127*54B**-G
R		200ms/Low	XC6127*16C**-G ～ XC6127*54C**-G
S		400ms/Low	XC6127*16D**-G ～ XC6127*54D**-G
T		800ms/Low	XC6127*16E**-G ～ XC6127*54E**-G
U		50ms/High	XC6127*16F**-G ～ XC6127*54F**-G
V		100ms/High	XC6127*16G**-G ～ XC6127*54G**-G
X		200ms/High	XC6127*16H**-G ～ XC6127*54H**-G
Y		400ms/High	XC6127*16J**-G ～ XC6127*54J**-G
Z		800ms/High	XC6127*16K**-G ～ XC6127*54K**-G

③④ represents production lot number. 01～09, 0A～0Z, 11～9Z, A1～A9, AA～AZ、B1～ZZ repeated.

(G, I, J, O, Q, W excluded.)

* No character inversion used.

1. The product and product specifications contained herein are subject to change without notice to improve performance characteristics. Consult us, or our representatives before use, to confirm that the information in this datasheet is up to date.

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