





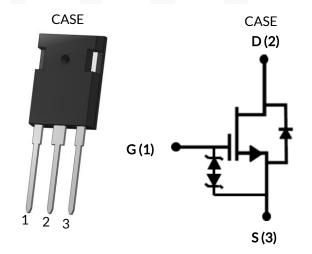








UF4C120053K3S



Part Number	Package	Marking		
UF4C120053K3S	TO-247-3L	UF4C120053K3S		







1200V-53m Ω SiC FET

Rev. A, April 2022

Description

The UF4C120053K3S is a 1200V, $53m\Omega$ G4 SiC FET. It is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the TO-247-3L package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads and any application requiring standard gate drive.

Features

- On-resistance R_{DS(on)}: 53mΩ (typ)
- Operating temperature: 175°C (max)
- Excellent reverse recovery: Q_{rr} = 117nC
- Low body diode V_{FSD}: 1.28V
- ◆ Low gate charge: Q_G = 37.8nC
- ◆ Threshold voltage V_{G(th)}: 4.8V (typ) allowing 0 to 15V drive
- Low intrinsic capacitance
- ESD protected: HBM class 2 and CDM class C3

Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating













Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		1200	V
Coto comments to co	V_{GS}	DC	-20 to +20	V
Gate-source voltage	V GS	AC (f > 1Hz)	-25 to +25	V
Continuous drain current ¹	1	T _C = 25°C	34	Α
Continuous drain current	I _D	T _C = 100°C	25	Α
Pulsed drain current ²	I _{DM}	T _C = 25°C	100	Α
Single pulsed avalanche energy ³	E _{AS}	L=15mH, I _{AS} =2.7A	54.6	mJ
SiC FET dv/dt ruggedness	dv/dt	$V_{DS} \le 800V$	150	V/ns
Power dissipation	P _{tot}	T _C = 25°C	263	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J,T_STG		-55 to 175	°C
Max. lead temperature for soldering, 1/8" from case for 5 seconds	T _L		250	°C

- 1. Limited by $T_{\text{\scriptsize J,max}}$
- 2. Pulse width t_p limited by $T_{J,max}$
- 3. Starting $T_J = 25^{\circ}C$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Тур	Max	Offics
Thermal resistance, junction-to-case	$R_{ heta$ JC			0.44	0.57	°C/W













Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions		Units		
			Min	Тур	Max	Offics
Drain-source breakdown voltage	BV _{DS}	V_{GS} =0V, I_D =1mA	1200			V
		V _{DS} =1200V, V _{GS} =0V, T _J =25°C		0.2	50	μΑ
Total drain leakage current	I _{DSS}	V _{DS} =1200V, V _{GS} =0V, T _J =175°C		15		
Total gate leakage current	I _{GSS}	V _{DS} =0V, T _J =25°C, V _{GS} =-20V / +20V		6	20	μА
Drain-source on-resistance	R _{DS(on)}	V _{GS} =12V, I _D =20A, T _J =25°C		53	67	
		V _{GS} =12V, I _D =20A, T _J =125°C		112		mΩ
		V _{GS} =12V, I _D =20A, T _J =175°C		159		
Gate threshold voltage	$V_{G(th)}$	V_{DS} =5V, I_{D} =10mA	4	4.8	6	V
Gate resistance	R_{G}	f=1MHz, open drain		4.5		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions		Unite		
Parameter			Min	Тур	Max	Units
Diode continuous forward current ¹	I _S	T _C =25°C			34	Α
Diode pulse current ²	$I_{S,pulse}$	T _C =25°C			100	Α
Forward voltage	V_{FSD}	V _{GS} =0V, I _F =10A, T _J =25°C		1.28	1.65	V
		V _{GS} =0V, I _F =10A, T _J =175°C		1.96		'
Reverse recovery charge	Q _{rr}	V_R =800V, I_S =25A, V_{GS} =0V, R_G =20 Ω		117		nC
Reverse recovery time	t _{rr}	di/dt=1300A/μs, T _J =25°C		27		ns
Reverse recovery charge	Q _{rr}	V_R =800V, I_S =25A, V_{GS} =0V, R_G =20 Ω		155		nC
Reverse recovery time	t _{rr}	di/dt=1300A/μs, Τ _J =150°C		29		ns













Typical Performance - Dynamic

Parameter	Cumahad	Test Conditions -		Units		
	Symbol		Min	Тур	Max	Units
Input capacitance	C _{iss}	- V _{DS} =800V, V _{GS} =0V - f=100kHz		1370		
Output capacitance	C _{oss}			43.5		pF
Reverse transfer capacitance	C _{rss}	1-100K112		2.2		
Effective output capacitance, energy related	C _{oss(er)}	V_{DS} =0V to 800V, V_{GS} =0V		54		pF
Effective output capacitance, time related	C _{oss(tr)}	V_{DS} =0V to 800V, V_{GS} =0V		100		pF
C _{OSS} stored energy	E _{oss}	V _{DS} =800V, V _{GS} =0V		17.3		μJ
Total gate charge	Q_{G}	- V _{DS} =800V, I _D =25A, -		37.8		
Gate-drain charge	Q_{GD}	$V_{DS} = 000 \text{ V}, I_D = 23 \text{ A},$ $V_{GS} = 0 \text{ V to } 15 \text{ V}$		9.5		nC
Gate-source charge	Q_{GS}	V _{GS} – 0 V to 13 V		10		
Turn-on delay time	t _{d(on)}	N 4 4		36		ns
Rise time	t _r	Note 4, V _{DS} =800V, I _D =25A, Gate		12		
Turn-off delay time	t _{d(off)}	Driver =0V to +15V,		80		
Fall time	t _f	$R_{G_ON}=1\Omega, R_{G_OFF}=20\Omega$ Inductive Load.		17		
Turn-on energy	E _{ON}	FWD: same device with		580		μЈ
Turn-off energy	E _{OFF}	$V_{GS} = 0V, R_G = 20\Omega,$ $T_1 = 25^{\circ}C$		175		
Total switching energy	E _{TOTAL}	1 ₃ -23 C		755		
Turn-on delay time	t _{d(on)}	Note 4		37		
Rise time	t _r	Note 4, V _{DS} =800V, I _D =25A, Gate		13		nc
Turn-off delay time	t _{d(off)}	$\begin{array}{c} \text{Driver = OV to +15V,} \\ \text{R}_{\text{G_ON}} = 1\Omega, \text{R}_{\text{G_OFF}} = 20\Omega \end{array}$ $\begin{array}{c} \text{Inductive Load,} \end{array}$		85		ns
Fall time	t _f			18		
Turn-on energy	E _{ON}	FWD: same device with		631		
Turn-off energy	E _{OFF}	$V_{GS} = 0V, R_G = 20\Omega,$ $T_J = 150$ °C		205		μЈ
Total switching energy	E _{TOTAL}	- 1 ₀ -150°C		836		

^{4.} Measured with the switching test circuit in Figure 23.













Typical Performance - Dynamic (continued)

Parameter	Symbol	Test Conditions	Value			Units
		rest Conditions	Min	Тур	Max	Offics
Turn-on delay time	t _{d(on)}			39		
Rise time	t _r	Note 5 and 6,		14		nc
Turn-off delay time	t _{d(off)}	V _{DS} =800V, I _D =25A, Gate Driver =0V to +15V.		35		ns
Fall time	t _f	$R_G=1\Omega$, inductive Load,		14		
Turn-on energy including R_S energy	E _{ON}	FWD: same device with		644		
Turn-off energy including R _S energy	E _{OFF}	$V_{GS} = 0V$ and $R_G = 1\Omega$, RC snubber: $R_{S1} = 5\Omega$ and		84		
Total switching energy	E _{TOTAL}	C_{S1} =95pF,		728		μ
Snubber R _S energy during turn-on	E _{RS_ON}	T _J =25°C		1.2		
Snubber R _S energy during turn-off	E _{RS_OFF}			2.1		
Turn-on delay time	t _{d(on)}			40		
Rise time	t _r	Note 5 and 6,		16		ns
Turn-off delay time	$t_{\text{d(off)}}$	V _{DS} =800V, I _D =25A, Gate Driver =0V to +15V.		38		115
Fall time	t _f	$R_G=1\Omega$, inductive Load,		15		
Turn-on energy including R_S energy	E _{ON}	FWD: same device with V_{GS} = 0V and R_{G} = 1Ω , RC snubber: R_{S1} = 5Ω and C_{S1} = 95 pF, T_{J} = 150 °C		695		
Turn-off energy including R_S energy	E _{OFF}			99		1
Total switching energy	E _{TOTAL}			794		μJ
Snubber R _S energy during turn-on	E _{RS_ON}			1.1		
Snubber RS energy during turn-off	E _{RS_OFF}			2		

^{5.} Measured with the switching test circuit in Figure 24.

^{6.} In this datasheet, all the switching energies (turn-on energy, turn-off energy and total energy) presented in the tables and Figures include the device RC snubber energy losses.





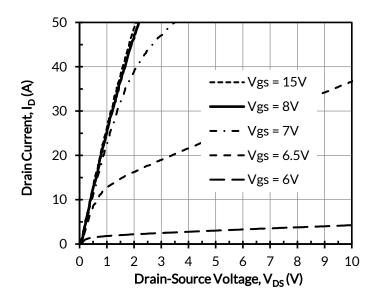








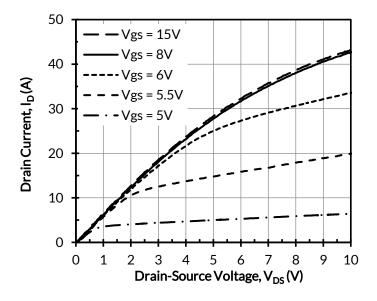
Typical Performance Diagrams



50 40 Drain Current, I_D (A) 30 Vgs = 15V 20 Vgs = 8V Vgs = 7VVgs = 6.5V 10 Vgs = 6V 0 0 1 2 10 Drain-Source Voltage, $V_{DS}(V)$

Figure 1. Typical output characteristics at T_J = - 55°C, tp < 250 μ s

Figure 2. Typical output characteristics at T_J = 25°C, tp < 250 μ s



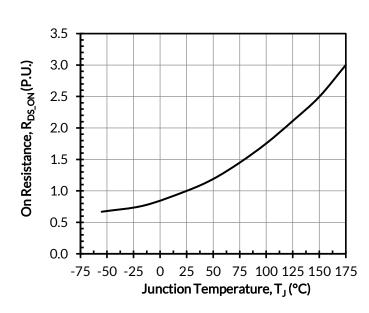


Figure 3. Typical output characteristics at T_J = 175°C, tp < 250 μ s

Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 25A



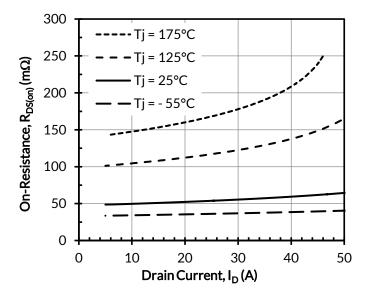












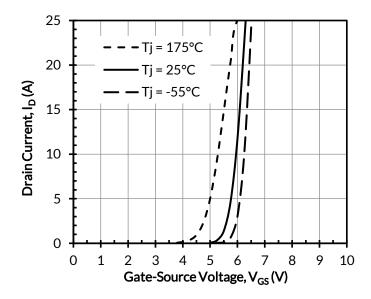
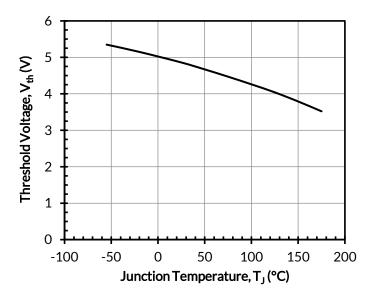


Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

Figure 6. Typical transfer characteristics at $V_{DS} = 5V$



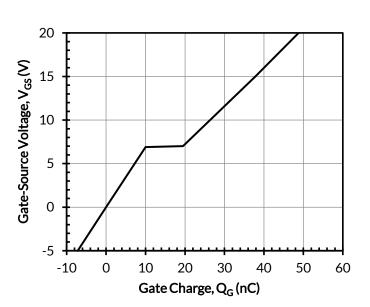


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_{D} = 10mA

Figure 8. Typical gate charge at V_{DS} = 800V and I_{D} = 25A





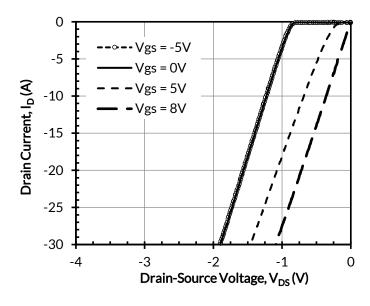
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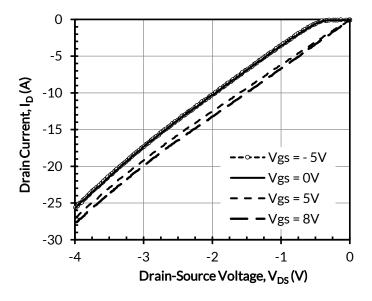




• Vgs = - 5V -5 Vgs = 0V Vgs = 5V Drain Current, I_D (A) -10 Vgs = 8V -15 -20 -25 -30 -3 -2 -1 0 Drain-Source Voltage, $V_{DS}(V)$

Figure 9. 3rd quadrant characteristics at $T_J = -55$ °C

Figure 10. 3rd quadrant characteristics at T_J = 25°C



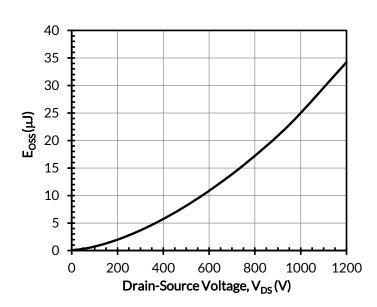


Figure 11. 3rd quadrant characteristics at $T_J = 175$ °C

Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0V$



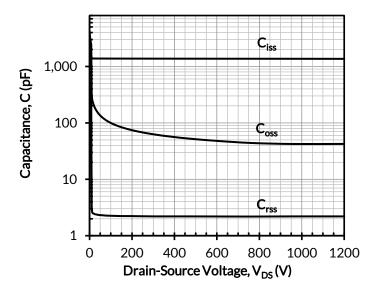








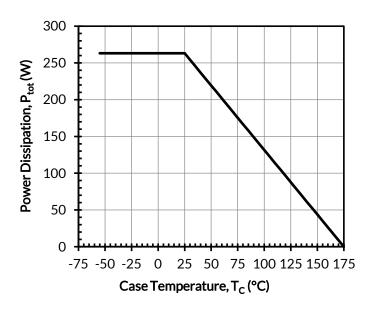




40 35 30 20 15 10 -75 -50 -25 0 25 50 75 100 125 150 175 Case Temperature, T_c (°C)

Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

Figure 14. DC drain current derating



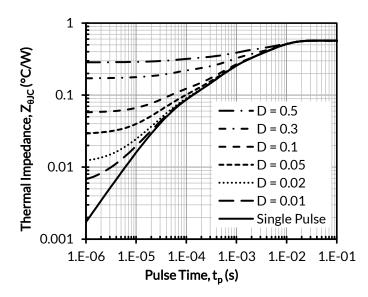


Figure 15. Total power dissipation

Figure 16. Maximum transient thermal impedance













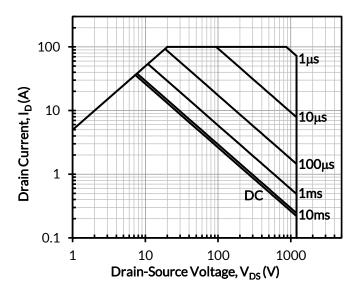


Figure 17. Safe operation area at $T_C = 25$ °C, D = 0, Parameter t_p

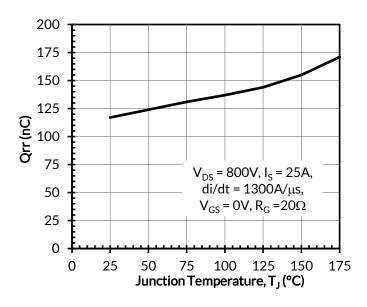


Figure 18. Reverse recovery charge Qrr vs. junction temperature

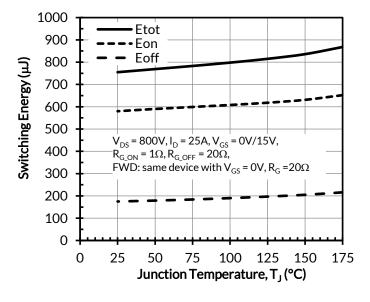


Figure 19. Clamped inductive switching energy vs. junction temperature at V_{DS} =800V and I_{D} = 25A

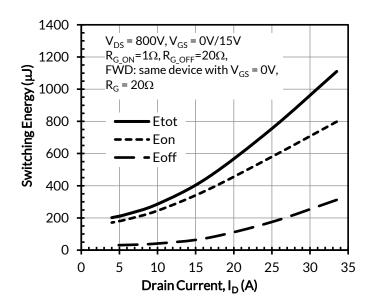


Figure 20. Clamped inductive switching energy vs. drain current at V_{DS} = 800V and T_J = 25°C



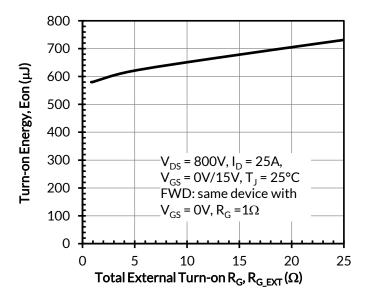












Turn-Off Energy, Eoff (μJ) $V_{DS} = 800V, I_{D} = 25A,$ $V_{GS} = 0V/15V, T_J = 25^{\circ}C$ FWD: same device with $V_{GS} = 0V, R_G = 1\Omega$ Total External Turn-off R_{G} , $R_{G,EXT}(\Omega)$

Figure 21. Clamped inductive switching turn-on energy vs. $R_{G,EXT\ ON}$

Figure 22. Clamped inductive switching turn-off energy vs. R_{G,EXT_OFF}

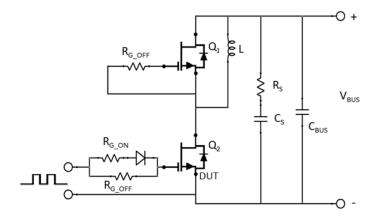


Figure 23. Schematic of the half-bridge mode switching test circuit. Note, a bus RC snubber (R_S = 2.5 Ω , C_S =100nF) is used to reduce the power loop high frequency oscillations.

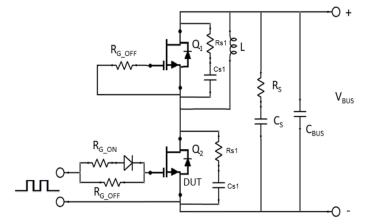


Figure 24. Schematic of the half-bridge mode switching test circuit with device RC snubbers ($R_{s1} = 5\Omega$, $C_{s1} = 95 pF$) and a bus RC snubber ($R_{S} = 2.5\Omega$, $C_{S} = 100 nF$).













Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_T) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode. Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at www.unitedsic.com

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