PFE850-SBB-1205

850 Watt AC-DC Power Supply

The PFE850-SBB-1205 is a 850 Watt AC to DC, power-factor-corrected (PFC) power supply that converts standard AC power into a main output of +12 VDC for powering intermediate bus architectures (IBA) in high performance and reliability storage, servers, routers, and network switches.

The PFE850-SBB-1205 utilizes full digital control architecture for greater efficiency, control, and functionality.

This power supply meets international safety standards and displays the CE-Mark for the European Low Voltage Directive (LVD).

80 PLUS PLATINUM

RoHS Compliant

Key Features & Benefits

- Best-in-class, meet 80 plus “Platinum” efficiency
- Auto-selected input voltage ranges: 90-140 VAC, 180-264 VAC
- AC input with active power factor correction
- 850 W / 12 V continuous output power capability
- Always-on 5 V_{SB} / 2 A standby output
- Hot-plug capable
- Parallel operation with active current sharing
- Full digital controls for improved performance
- Power density design: 4.4 W / in^3
- Form factor (L x W x H): 362.5 x 106.5 x 82 mm (14.27 x 4.19 x 3.23 in)
- Power Management Bus communication interface for control, programming and monitoring
- Status LED with fault signaling

Applications

- High Performance Servers
- Routers
- Switches

1. ORDERING INFORMATION

PFE	850	-	SBB	-	1205
Product Family	**Power Level**	**Dash**	**Application**	**Dash**	**Outputs**
PFE Front-Ends	850 W		Storage Bridge Bay		V1:12V; VSB:5VSB

2. OVERVIEW

The PFE850-SBB-1205 AC/DC power supply is a fully DSP controlled, highly efficient front-end power supply. It incorporates resonance-soft-switching technology to reduce component stresses, providing increased system reliability and very high efficiency. With a wide input operational voltage range the PFE850-SBB-1205 maximizes power availability in demanding server, network, and other high availability applications. The supply is fan cooled and ideally suited for integration with a matching airflow path.
The PFC stage is digitally controlled using a state-of-the-art digital signal processing algorithm to guarantee best efficiency and unity power factor over a wide operating range. The DC/DC stage uses soft switching resonant techniques in conjunction with synchronous rectification. An active OR-ing device on the output ensures no reverse load current and renders the supply ideally suited for operation in redundant power systems. The always-on standby output provides power to external power distribution and management controllers. It is protected with an active OR-ing device for maximum reliability.
Status information is provided with a front-panel LED. In addition, the power supply can be controlled and the fan speed set via the I²C bus. The I²C bus allows full monitoring of the supply, including input and output voltage, current, power, and inside temperatures.

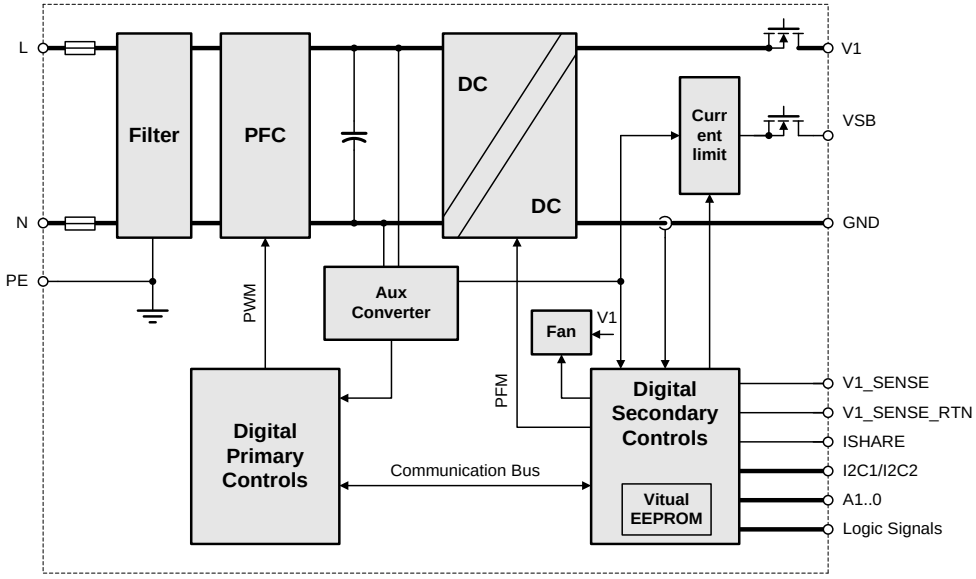


Figure 1. PFE850-SBB-1205 Block Diagram

3. ABSOLUTE MAXIMUM RATINGS

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the supply.

PARAMETER		CONDITIONS / DESCRIPTION	MIN	MAX	UNITS
Vi max	Maximum Input	Continuous		264	VAC

4. INPUT

General Condition: T_A = 0… 55 °C, unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\,nom}$	AC Nominal Input Voltage	Rated Voltage High Line ($V_{i\,nom\,HL}$)	200	230	240	VAC
		Rated Voltage Low Line ($V_{i\,nom\,LL}$)	100	115	127	VAC
V_i	Input Voltage Ranges	Normal operating ($V_{i\,min\,HL}$ to $V_{i\,max\,HL}$), High Line	180		264	VAC
		Normal operating ($V_{i\,min\,LL}$ to $V_{i\,max\,LL}$), Low Line	90		140	VAC
$I_{i\,max}$	Maximum Input Current	V_{IN} = 90 VAC, I_1=69.5 A, I_{SB} =2 A, Fan with full speed			12.5	A_{RMS}
		V_{IN} = 180 VAC, I_1=69.5 A, I_{SB} =2 A , Fan with full speed			6.3	A_{RMS}
$I_{i\,inrush}$	Inrush Current Limitation	$V_{i\,min}$ to $V_{i\,max}$, T_{PTC} = 25°C, 5 ms			50	A_p
	Secondary inrush Current				35	A_p
f_i	Input Frequency		47	50/60	63	Hz
PF	Power Factor	Vi = 230 VAC/115VAC, 50 Hz and 60 Hz				
		10% Load	0.88			W/VA
		20% Load	0.94			W/VA
		50% Load	0.98			W/VA
		100% Load	0.99			W/VA
$V_{i\,on}$	Turn-on Input Voltage[1]	Ramping up	85		90	VAC
$V_{i\,off}$	Turn-off Input Voltage[1]	Ramping down	79		84	VAC
η	Efficiency[2]	V_{IN} = 115 VAC, 10% load	80			%
		V_{IN} = 115 VAC, 20% load	88			%
		V_{IN} = 115 VAC, 50% load	92			%
		V_{IN} = 115 VAC, 100% load	89			%
		V_{IN} = 230 VAC, 10% load	82			%
		V_{IN} = 230 VAC, 20% load	90			%
		V_{IN} = 230 VAC, 50% load	94			%
		V_{IN} = 230 VAC, 100% load	91			%
$T_{V1\,holdup}$	Hold-up Time V_1	V_{IN}= 115VAC/230VAC, I_1=69.5 A, I_{SB} =2A	17			ms
$T_{VSB\,holdup}$	Hold-up Time V_{SB}	5 V_{SB}, full load	70			ms
$Ithd$	Input total harmonic distorition[3]	V_{IN} = 115 VAC/230 VAC,60 Hz, 0% load	25			%
		V_{IN} = 115 VAC/230 VAC,60 Hz,10% load	10			%
		V_{IN} = 115 VAC/230 VAC,60 Hz, 20% load	7.5			%
		V_{IN} = 115 VAC/230 VAC,60 Hz, 50% load	5			%
		V_{IN} = 115 VAC/230 VAC,60 Hz, 100% load	4			%

[1] The Front-End is provided with a typical hysteresis of 5 VAC during turn-on and turn-off within the ranges. PSU will restart once input voltage within the $V_{i\,on}$.
[2] Efficiency measured without fan power per EPA server guidelines.
[3] 0% load and no single harmonic exceeding 80% of the total harmonic distortion shall be guaranteed by design.

4.1 INPUT FUSE

The PSU has dual pole fusing for the AC input**.** Fast acting type 16A input fuse (5.4 x 22.5 mm) in series with the L-line and N-Line inside the power supply protects against severe defects. The fuse is not accessible from the outside and is therefore not a serviceable part.

4.2 INRUSH CURRENT

The AC-DC power supply exhibits an X capacitance of only 2.05 uF, resulting in a low and short peak current, when the supply is connected to the mains. The internal bulk capacitor will be charged through a PTC which will limit the inrush current.

NOTE: Do not repeat plug-in / out operations within a short time, or else the internal in-rush current limiting device (PTC) may not sufficiently cool down.

4.3 INPUT UNDER-VOLTAGE

If the sinusoidal input voltage stays below the input under voltage lockout threshold Vi on, the supply will be inhibited. Once the input voltage returns within the normal operating range, the supply will return to normal operation again**.**

4.4 POWER FACTOR CORRECTION

Power factor correction (PFC) is achieved by controlling the input current waveform synchronously with the input voltage. A fully digital controller is implemented giving outstanding PFC results over a wide input voltage and load ranges. The input current will follow the shape of the input voltage. If for instance the input voltage has a trapezoidal waveform, then the current will also show a trapezoidal waveform.

4.5 EFFICIENCY

High efficiency (see *Figure 2)* is achieved by using state-of-the-art silicon power devices in conjunction with soft-transition topologies minimizing switching losses and a full digital control scheme. Synchronous rectifiers on the output reduce the losses in the high current output path. The speed of the fan is digitally controlled to keep all components at an optimal operating temperature regardless of the ambient temperature and load conditions.

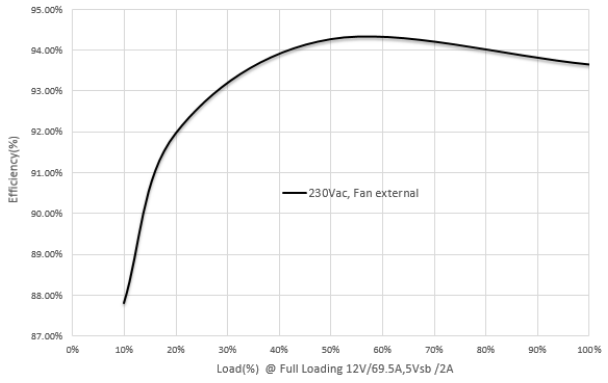


Figure 2. Efficiency vs. Load current (ratio metric loading)

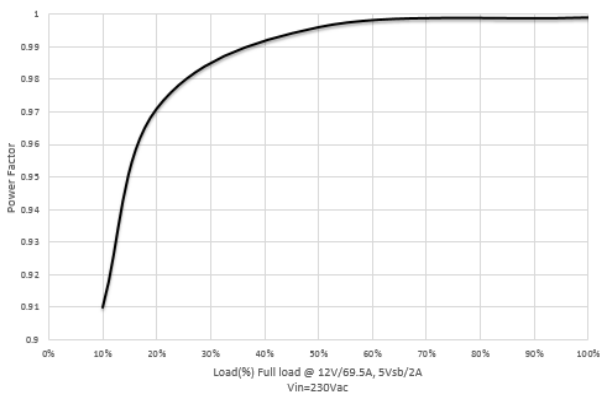


Figure 3. Power factor vs. Load current

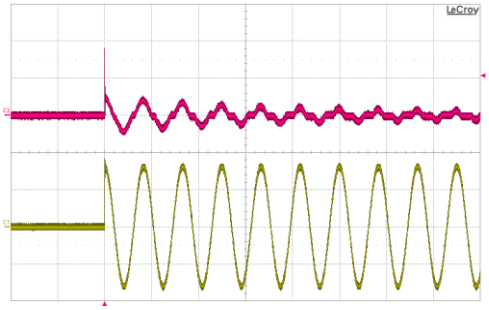


Figure 4. Inrush current, Vin = 230Vac, 90°
CH1: Vin (200V/div), CH2: Iin (10A/div)

4.6 AC LINE TRANSIENT SPECIFICATION

AC line transient conditions shall be defined as “sag” and “surge” conditions. “Sag” conditions are also commonly referred to as “brownout”, these conditions will be defined as the AC line voltage dropping below nominal voltage conditions. “Surge” will be defined to refer to conditions when the AC line voltage rises above nominal voltage.
The power supply shall meet the requirements under the following AC line sag condition.

AC Line Sag (10 sec interval between each sagging)

DURATION	SAG	OPERATING AC VOLTAGE	LINE FREQUENCY	PERFORMANCE CRITERIA
50ms to 500ms	10%	90 VAC / 180 VAC	50/60 Hz	No loss of function or performance

*** Comment:** for 10% sag condition, the load is 100%.

Table 1. AC Line Sag Transient Performance

5. OUTPUT

General condition: T_A = 0…55 °C, V_i = 230VAC unless otherwise noted.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
Main Output V_1						
$V_{1\ nom}$	Nominal Output Voltage	0.5 · $I_{1\ nom}$, T_A = 25°C		12.15		VDC
$V_{1\ set}$	Output Setpoint Accuracy		-1		+1	%$V_{1\ nom}$
$V1$ load	Load Regulation	0 to 100% I1 nom	11.66		12.63	V
$dV1$ line	Line Regulation	$V_{i\ min\ LL}$ to $V_{i\ max\ HL}$			120	mV
$P_{1\ nom}$	Nominal Output Power	$V_{i\ min\ LL}$ to $V_{i\ max\ HL}$		850		W
$I_{1\ nom}$	Output Current	$V_{i\ min\ HL}$ to $V_{i\ max\ HL}$	0.0		69.5	ADC
$I_{1\ peak}$	Peak Current	$V_{i\ min\ LL}$ to $V_{i\ max\ HL}$*(min 20s)*			83.5	ADC
$V_{1\ pp}$	Output Ripple Voltage[3]	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{1\ nom}$, 20MHz Bandwidth			120	mVpp
$dI_{1\ share}$	Current Sharing Deviation	I_1 =10%	-40		+40	% $I_{1\ *0.1}$
		I_1 =25%	-16		+16	% $I_{1*0.25}$
		I_1 =50%	-8		+8	% $I_{1*0.5}$
		I_1 =100%	-4		+4	% I_1 nom
		I_1 =150%	-2.8		+2.8	% $I_{1*1.5}$
V_{ISHARE}	Current Share Bus Voltage	$I_{1\ nom}$		5		VDC
$dV_{1\ dyn1}$	Dynamic Load Regulation (frequency:50Hz-5KHz)	Test frequency between 50Hz and 5KHz at duty cycles from 10% to 90%, ΔI1 = 50% $I1_{nom}$, I1 = 0.2A … 100% $I1_{nom}$, with 470uF and 22mF external capacitive, Di/dt=0.5A/us , test by coupling DC.	11.66		0.8 12.63	Vpk-pk VDC
$dV_{1\ dyn2}$		Test frequency between 50Hz and 5KHz at duty cycles from 10% to 90%, ΔI1 = 60% $I1_{nom}$, I1 = 3.5A … 100% $I1_{nom}$, with 470uF and 22mF external capacitive, Di/dt=0.5A/us, test by coupling DC	11.66		0.8 12.63	Vpk-pk VDC
t_{rec}	Recovery Time	recovery within 1% of $V_{1\ nom}$			2	ms
$t_{V1\ rise}$	Output Voltage Rise Time	V_1 = 10…90% $V_{1\ nom}$	1		70	ms
$d_{V1\ ovr\ sh}$	Output Turn-on Overshoot	$V_{i\ nom\ HL}$, 0 to 100% $I_{1\ nom}$			0.5	V
$dV_{1\ sense}$	Remote Sense (+/-)	Compensation for cable drop, 0 to 100% $I_{1\ nom}$		0.2		V
$C_{V1\ load}$	Capacitive Loading				22	mF
Standby Output V_{SB}						
$V_{SB\ nom}$	Nominal Output Voltage	0.5 ·$I_{SB\ nom}$, T_A = 25°C		5.05		VDC
$V_{SB\ set}$	Output Setpoint Accuracy		-1		+1	%V_{SBnom}
V_{sb} load	Load Regulation	0 to 100% ISB nom	4.9		5.25	V
dV_{sb} line	Line Regulation	$V_{i\ min\ LL}$ to $V_{i\ max\ HL}$			60	mV
$P_{SB\ nom}$	Nominal Output Power	$V_{i\ min}$ to $V_{i\ max}$		10.1		W
$I_{SB\ nom}$	Output Current	$V_{i\ min}$ to $V_{i\ max}$	0.0		2	ADC
$V_{SB\ pp}$	Output Ripple Voltage [3]	$V_{i\ min}$ to $V_{i\ max}$, 0 to 100% $I_{SB\ nom}$, 20 MHz bandwidth			60	mVpp
$dV_{SB\ dyn}$	Dynamic Load Regulation	ΔISB = 50% ISB nom, ISB = 0.1~100%ISB nom, with 47uF and 1mF external capacitive, dISB/dt = 0.5A/µs,	4.9		0.2 5.25	Vpk-pk VDC
t_{rec}	Recovery Time	recovery within 1% of VSB nom			2	ms
$t_{VSB\ rise}$	Output Voltage Rise Time	V_{SB} = 10…90% $V_{SB\ nom}$,			70	ms
$d_{VSB\ ovr\ sh}$	Output Turn-on Overshoot	$V_{i\ nom\ HL}$, 0 to 100% $I_{SB\ nom}$			0.25	V
$C_{VSB\ load}$	Capacitive Loading				1000	µF

3 Ripple noise and dynamic load measured with a 10uF low ESR capacitor in parallel with a 0.1uF ceramic capacitor at the point of measurement.

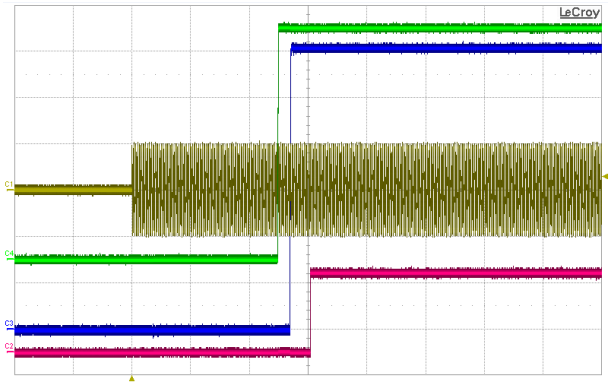


Figure 5. Turn-On AC Line 230VAC, full load (500ms/div)
CH1: Vin (350V/div) CH2: PWOK_H (2V/div)
CH3: V_1 (2V/div) CH4: V_{SB} (1V/div)

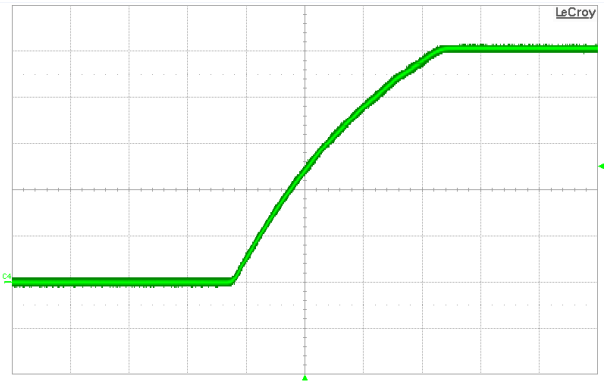


Figure 6. Turn-On AC Line 230VAC, full load (2ms/div)
CH4: V_{SB} (1V/div)

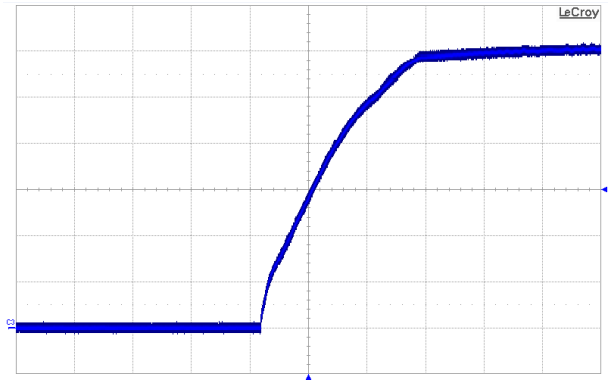


Figure 7. Turn-On AC Line 230VAC, full load (2ms/div)
CH3: V_1 (2V/div)

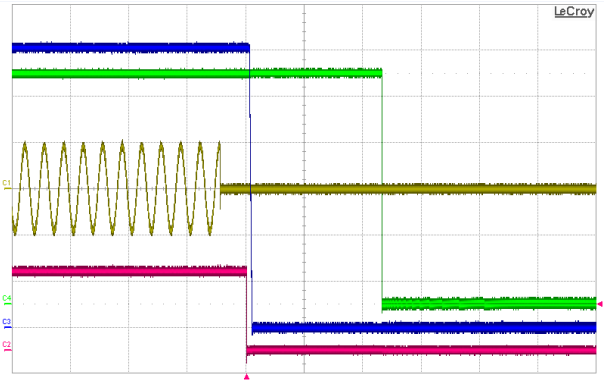


Figure 8. Turn-Off AC Line 230VAC, full load (50ms/div)
CH1: Vin (350V/div) CH2: PWOK_H (2V/div)
CH3: V_1 (2V/div) CH4: V_{SB} (1V/div)

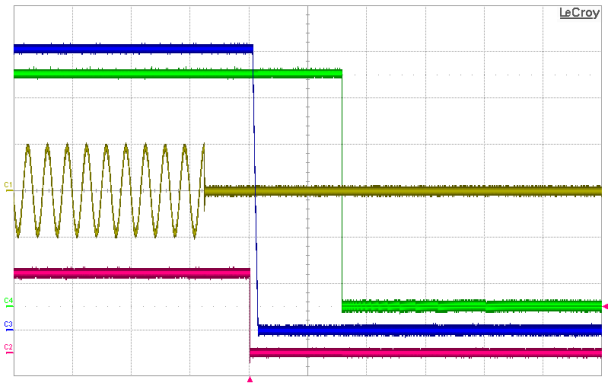


Figure 9. Turn-Off AC Line 230VAC, half load (40ms/div)
CH1: Vin (350V/div) CH2: PWOK_H (2V/div)
CH3: V_1 (2V/div) CH4: V_{SB} (1V/div)

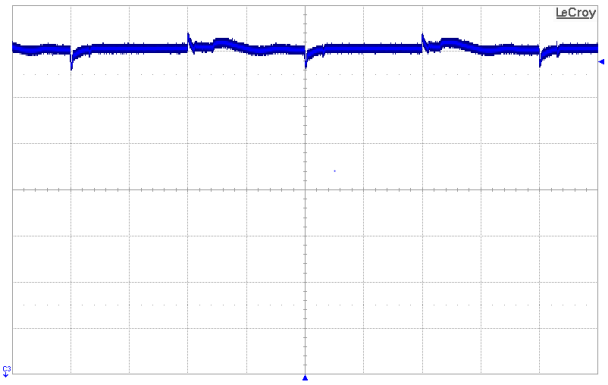


Figure 10. Load transient V_1, 0.2A to 34.95A (5ms/div)
CH3: V_1 (700mV/div)

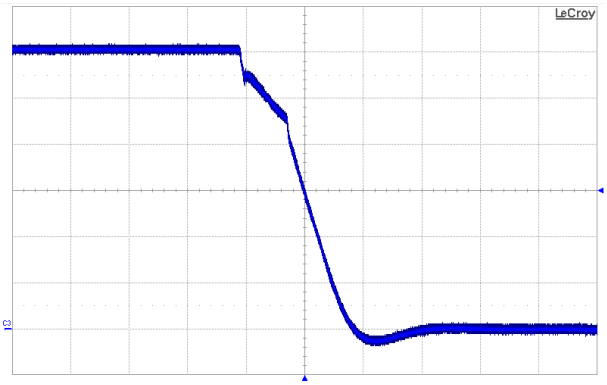


Figure 11. Short circuit[4] on V1 (0.5ms/Div)
CH3: V_1 (2V/div)

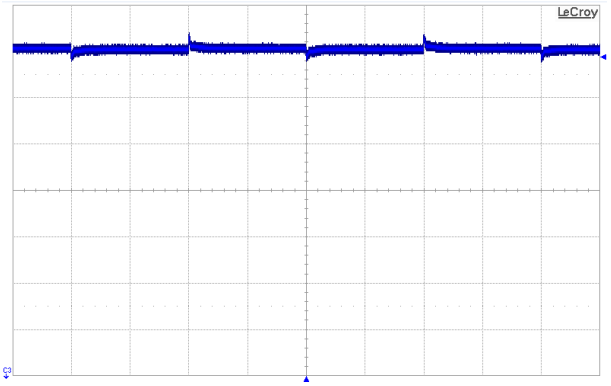


Figure 12. Load transient V_1, 34.75 to 69.5A (5ms/div)
CH3: V_1 (700mV/div)

5.1 OUTPUT GROUND / CHASSIS CONNECTION

The output return path serves as power and signal ground. All output voltages and signals are referenced to these pins. To prevent a shift in signal and voltage levels due to ground wiring voltage drop a low impedance ground plane should be used as shown in *Figure 13*. Alternatively, separated ground signals can be used as shown in *Figure 14.* In this case the two ground planes should be connected together at the power supplies ground pins.

NOTE:
Within the power supply the output GND pins are connected to the Chassis, which in turn is connected to the Protective Earth terminal on the AC inlet. Therefore it is not possible to set the potential of the output return (GND) to any other than Protective Earth potential.

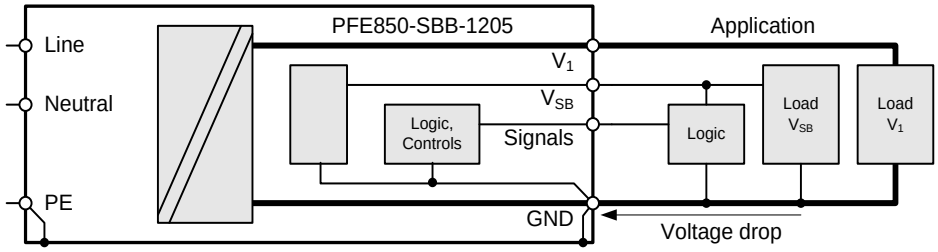


Figure 13. Common Low Impedance Ground Plane

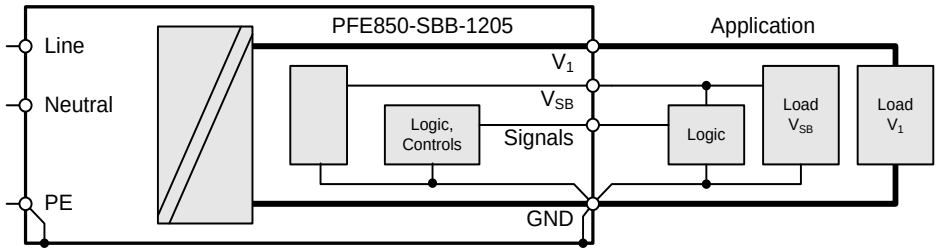


Figure 14. Separated Power and Signal Ground

[4] Short current measured with 0.1 ohm resistor short on output will not cause any damage to the power supply.

5.2 CLOSED LOOP STABILITY

The power supply shall be unconditionally stable under all line/load/transient load conditions including capacitive load ranges. A minimum of: 45 degrees phase margin and -10dB-gain margin is required. The power supply manufacturer shall provide proof of the unit's closed-loop stability with local sensing through the submission of Bode plots. Closed-loop stability must be ensured at 10%, 20%, 50% and 100% loads as applicable, 0% is just for reference.

5.3 COMMON MODE CURRENT

The common mode current measurement should be with min and max input voltage and dummy load, the common current should be less than 40 mA, all return wires (COM) must be tied together and connected to the chassis ground (GND) by using a thick copper wire (braided wire AWG#10 or equivalent). To be effective, the copper wire resistance must not exceed 5 milliohms. (See example picture below.)

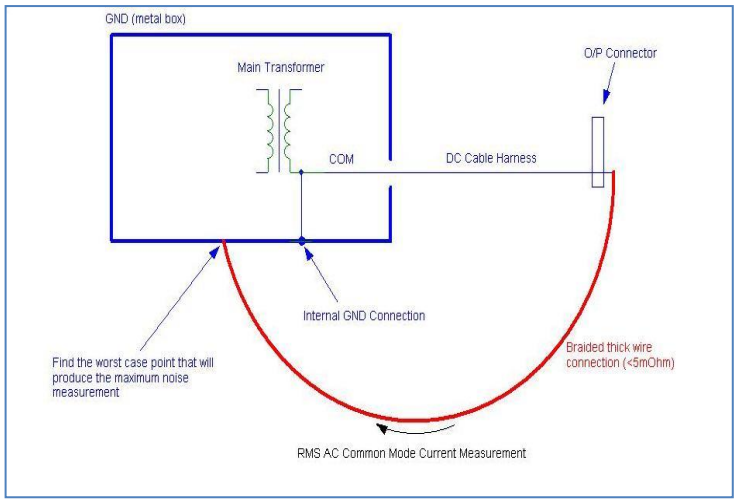


Figure 15. Common mode current example

5.4 ZERO LOAD STABILITY REQUIREMENTS

When the power subsystem operates in a no load condition, it does not need to meet the output regulation specification, but it must operate without any tripping of over-voltage or other fault circuitry. When the power subsystem is subsequently loaded, it must begin to regulate and source current without fault.

5.5 HOT SWAP REQUIREMENTS

During hot swap or cold swap of PSU all outputs shall meet the minimum regulation voltage and maximum voltage not exceed +10% nominal voltage requirements with maximum and minimum capacitive loading specified

The hot swap test must be conducted when the system is operating under static, dynamic, and zero loading conditions. The power supply shall use a latching mechanism to prevent insertion and extraction of the power supply when the AC power cord is inserted into the power supply

5.6 FORCED LOAD SHARING

The PFE front-ends have an active current share scheme implemented for V1. All the ISHARE current share pins need to be interconnected in order to activate the sharing function. If a supply has an internal fault or is not turned on, it will disconnect its ISHARE pin from the share bus. This will prevent dragging the output down (or up) in such cases.

The current share function uses an analog bus to transmit and receive current share information. The controller implements a Master/Slave current share function. The power supply providing the largest current among the group is automatically the Master. The other supplies will operate as Slaves and increase their output current to a value close to the Master by slightly increasing their output voltage. The voltage increase is limited to +250 mV. The output will share within 4% at full load.

The 5 VSB output is not required to actively share current between power supplies (passive sharing)

SIGNAL CHARACTERISTIC	REQUIREMENT		
Open Circuit Iout to Vshare	Nominal Load	5.00 V ± 6%	maximum Speed AMDs attached
	¾ Nominal Load	3.75 V ± 6%	maximum Speed AMDs attached
	½ Nominal Load	2.50 V ± 10%	maximum Speed AMDs attached
	¼ Nominal Load	1.25 V ± 25%	maximum Speed AMDs attached
	Minimum Load	Active	

Table 2. Load Share Characteristics for V1 Output

Loading on one rail has no effect to the share bus of another.
The share bus is 'linear' and continue past nominal loading by > 25%.
At min load the share bus is active but may not be 0 V if an active preload is implemented.

5.7 RIPPLE / NOISE

The test set-up shall be following *Figure 16*.

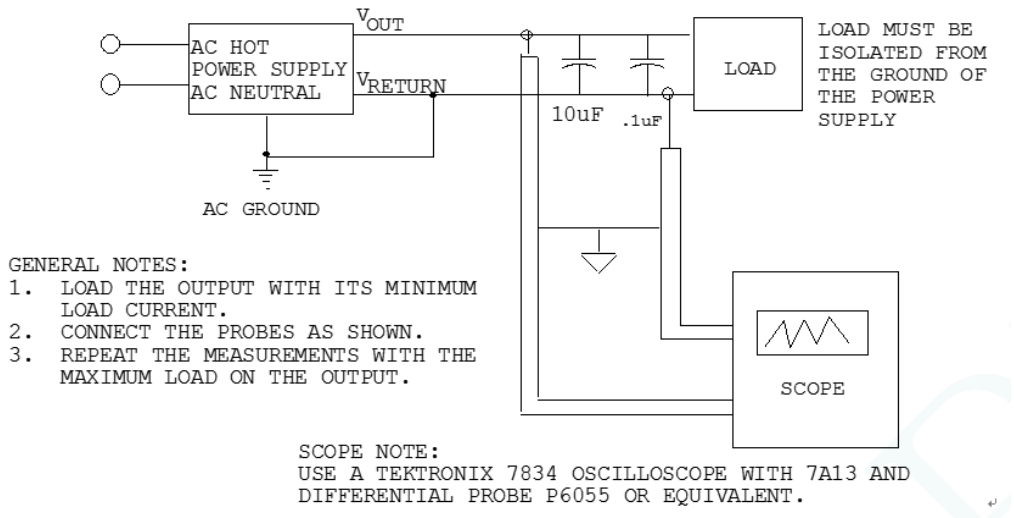


Figure 16. Differential Noise Test Setup

NOTE: Load must be isolated from the safety ground to *Figure 16*.

NOTE: When performing this test, the probe clips and capacitors should be located close to the load.

6. PROTECTION

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
F	Input dual fuses (L and N)	Time-lag type		20		A
$V_{1\ OV}$	OV Threshold V_1	Over Voltage V_1 Protection, Latch-off Type	12.8	13.5	14	VDC
$V_{VSB\ OV}$	OV Threshold V_{SB}	Over Voltage V_{SB} Protection, Automatic recovery Type;	5.5		6.5	VDC
$V_{1\ UV}$	UV Threshold V_1	Under Voltage V_1 Protection, Latch-off Type	8.8	9.6	10.4	VDC
$V_{VSB\ UV}$	UV Threshold V_{SB}	Under Voltage V_{SB} Protection, Automatic recovery Type;	3.9		4.5	VDC
$I_{V1\ OC}$	OC Limit V_1	Over Current Limitation, Latch-off, $V_{i\ min\ HL}$ to $V_{i\ max\ HL}$	85		104	ADC
		Over Current Delay Time	10		300	mS
$I_{VSB\ OC}$	OC Limit V_{SB}	Over Current V_{SB} Protection, Automatic recovery Type;	2.2		3.6	ADC
		Over Current Delay Time	10		300	mS
T_{SD}	Over Temperature On Critical Points	Shut-down and auto-recovered	Refer to Table 3			°C

6.1 PROTECTION CIRCUITS

Protection circuits inside the power supply shall cause only the power supply's main output to shut down. If the power supply latches off due to a protection circuit tripping, an AC cycle (turn OFF then turn ON) or a PCM ON/OFF logic cycle (refer to Table 8-1) shall be able to reset the power supply.

6.2 OVER TEMPERATURE PROTECTION (OTP)

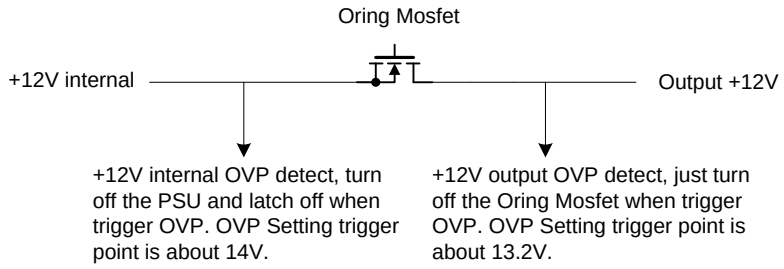
The PSU shall shut down if an over temperature condition is detected in the unit whilst running. The actual OTP shall cause no damage or safety hazard. In an OTP condition the PSU will shut down, OT warning SMB_ALERT_L assertion must always precede the OTP shutdown, when the power supply temperature drops to within specified limits, the power supply shall restore power automatically, while the 5VSB remains always on, the OTP circuit must have built in margin such that the power supply will not oscillate on and off due to temperature recovering condition, the OTP trip temperature level shall be at least 3degC higher than SMB_ALERT_L over temperature warning threshold level.
If fan fail will give a warning through LED and PSMI register, but not cause PSU to shut-down. PSU will trigger OTP to prevent damaged or safety hazard.
The PSU should be able to recover automatically when the temperature is reduced to operational range under OTP condition
The PFE850-SBB-1205 provides access via I^2C to the measured temperatures of in total 3 sensors within the power supply, see *Table 3*. The microprocessor is monitoring these temperatures and if warning threshold of one of these sensors is reached it will set fan to maximum speed. If temperatures continue to rise above shut down threshold the main output V1 (or VSB if auxiliary converter is affected) will be disabled. At the same time the warning or fault condition is signalized accordingly through LED, PWOK_H and SMB_ALERT_L.

TEMPERATURE SENSOR	DESCRIPTION / CONDITION	POWER MANAGEMENT BUS REGISTER	WARNING THRESHOLD	SHUT DOWN THRESHOLD
Inlet air temperature	Sensor located on control board close to DC end of power supply	8Dh	63	68
Sync rectifier Mosfet	Sensor located close to Sync rectifier Mosfet	8Eh	110	115
PFC heat sink	Sensor located on PFC heat sink	8Fh	95	100

Table 3. Temperature Sensor Location and Thresholds

6.3 OVER VOLTAGE PROTECTION

The PFE850-SBB-1205 front-end provides a fixed threshold overvoltage (OV) protection implemented with a HW comparator for both the main and the standby output. Once an OV condition has been triggered on the main output, the supply will shut down and latch the fault condition. The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input. 5VSB will be auto-recovered after removing OVP limit.
The +12V over voltage is detected on the PSU output, output OV by shorting 12V remote sense, Oring Mosfet will be turned off when +12V output OVP is triggered, the +12V internal voltage Continue to rise to 14V and trigger the +12V internal OVP, PSU will be turned off and latched off. The OVP detail characteristic see below picture.



6.4 UNDER VOLTAGE DETECTION

Both main and standby outputs are monitored. LED and PWOK_H pin signal if the output voltage exceeds ±5% of its nominal voltage.
The main output will latch off if the main output voltage V_1 falls below 9.6 V (typically in an overload condition), The latch can be unlocked by disconnecting the supply from the AC mains or by toggling the PSON_L input.
If the standby output leaves its regulation bandwidth for more than 10 ms then the main output is disabled to protect the system.

6.5 OVER CURRENT LIMIT PROTECTION (OCP)

The power supply shall have current limit to prevent the outputs from exceeding the values shown the above over current threshold. If the current limits are exceeded the power supply shall shutdown and latch off. The latch will be cleared by an AC power interruption or PSON_L cycle HIGH for 1sec.
The power supply shall not be damaged from repeated power cycling in this condition. 5VSB will be auto-recovered after removing OCP limit.

6.6 PEAK LOAD

The power supply shall be able to support higher peak current levels and duration 20S, the power supply should be operation normally. The IPEAK testing conditions refer to *Table 4*.

PEAK POWER	PEAK CURRENT	PEAK LOAD DURATION	VOLTAGE UNDERSHOOT
1012 W	83.5 A	20 s	5 %

Table 4. Peak Load Testing Conditions

7. MONITORING

The power supply operating parameters can be accessed through I²C interface. For more details refer to chapter I2C / POWER MANAGEMENT BUS COMMUNICATION and document PFE850-SBB-1205 Power Management Bus Communication Manual.

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
$V_{i\,mon}$	Input Voltage	$V_{i\,min\,LL} \leq V_i \leq V_{i\,max}$	-2		+2	VAC
$I_{i\,mon}$	Input Current		-0.35		+0.35	A
$P_{i\,mon}$	True Input Power	$I_1 < 10\%\ I_{1\,nom}$	-8		+8	W
		$10\%\ I_{1\,nom} < I_1 < 20\%\ I_{1\,nom}$	-4		+4	%
		$I_1 > 20\%\ I_{1\,nom}$	-2		+2	%
$E_{i\,mon}$	Total Input Energy	$I_1 < 10\%\ I_{1\,nom}$	-8		+8	W
		$10\%\ I_{1\,nom} < I_1 < 20\%\ I_{1\,nom}$	-4		+4	%
		$I_1 > 20\%\ I_{1\,nom}$	-2		+2	%
$V_{1\,mon}$	V_1 Voltage		-1		+1	%
$I_{1\,mon}$	V_1 Current	$I_1 < 10\%\ I_{1\,nom}$	-1		+1	ADC
		$10\%\ I_{1\,nom} < I_1 < 20\%\ I_{1\,nom}$	-5		+5	%
		$I_1 > 20\%\ I_{1\,nom}$	-2		+2	%
P_{nom}	V_1 Output Power	$I_1 < 10\%\ I_{1\,nom}$	-15		+15	W
		$10\%\ I_{1\,nom} < I_1 < 20\%\ I_{1\,nom}$	-6		+6	%
		$I_1 > 20\%\ I_{1\,nom}$	-3		+3	%
E_{nom}	V_1 Output Energy	$I_1 < 10\%\ I_{1\,nom}$	-15		+15	W
		$10\%\ I_{1\,nom} < I_1 < 20\%\ I_{1\,nom}$	-6		+6	%
		$I_1 > 20\%\ I_{1\,nom}$	-3		+3	%
T_{ambmon}	*Ambient Temperature*	$0°C \leq T_{amb} \leq 55°C$	-5		+5	℃

8. SIGNALING AND CONTROL

All signal pins are 5 V tolerant unless otherwise specifically stated, and this must include the maximum stated.

8.1 DC SWITCH

A DC mains output switch is required. The switch should be compatible with MR-1-114-C5N-BB. It shall meet all the mechanical requirements and true table.

PSON_L_DCDC_SWITCH	PSON_L_OUTPUT_CONNECTOR	MAIN OUTPUT
0	0	ON
0	1	OFF
1	0	OFF
1	1	OFF

8.2 PSON_L, OPERATION, SBB_PRESENT1 and SBB_PRESENT2

PSON_L, POWER MANAGEMENT BUS OPERATION command, SBB_PRESENT1 and SBB_PRESENT2 shall remotely turn the PSU ON / OFF. Logic internal to the PSU shall combine these signals to generate the PSU ON/OFF signal. Once turned OFF the PCM will ignore turn ON command for 5 seconds.

OPERATION	SBB_PRESENT1	SBB_PRESENT2	PSON_L	PSU State
0x00	0	0	0	OFF
0x00	0	0	1	OFF
0x00	0	1	0	OFF
0x00	0	1	1	OFF
0x00	1	0	0	OFF
0x00	1	0	1	OFF
0x00	1	1	0	OFF
0x00	1	1	1	OFF
0x80	0	0	0	ON
0x80	0	0	1	OFF
0x80	0	1	0	ON
0x80	0	1	1	OFF
0x80	1	0	0	ON
0x80	1	0	1	OFF
0x80	1	1	0	OFF
0x80	1	1	1	OFF

SIGNAL LEVELS	MIN	MAX
Logic level low	0 V	0.7 V
Logic level high	2.4 V	5.3 V
Pulled up resistor to internal 3V3 inside the PSU	10 KΩ	
Ripple and Noise (20MHz bandwidth)		300mV (only PSON_L signal)

Table 5. SBB_PRESENT1 and SBB_PRESENT2 Signal Functionality and Electrical Characteristics

8.3 PSKILL_L

PSKILL_L is used to enable the hot swapping functionality. The PSKILL_L pin is shorter than the other signal pins This signal must be pulled low by the enclosure. A floating input shall shutdown the PSU with the exception of the 5 VSB.

SIGNAL TYPE (INPUT SIGNAL TO PSU)	Accepts a 0 V input from the enclosure. Pulled up to internal 3V3 by 1.6kOhms inside the PSU.
PSKILL_L = LOW	ON
PSKILL_L = Floating	OFF
SIGNAL LEVELS	**MIN** / **MAX**
PSKILL_L Pull Low (PSU ON)	10 Ω to GND
PSKILL_L Open Circuit (PSU OFF)	1 KΩ to GND
Source Current (short circuit)	2 mA

Table 6. PSKILL_L Signal Functionality and Electrical and Timing Characteristics

8.4 AMB_LEDS_ON

This is a discrete input from the enclosure to indicate a “failure to communicate” between the enclosure and the PSU. Pulled up to internal 3V3 by 10 KΩ inside the PSU. This failure can occur as a result of a fault on the PSU or the enclosure. The signal will drive all 2 amber LEDs to turn on.

8.5 SMB_ALERT_L

The SMB_ALERT_L signal indicates that the power supply is experiencing a problem that the system agent should investigate. This is a logical OR of the Shutdown and Warning events. It is asserted (pulled Low) at Shutdown or Warning events such as reaching temperature warning/shutdown threshold of critical component, general failure, over-current, over-voltage, under-voltage or low-speed of failed fan. This signal may also indicate the power supply is operating in an environment exceeding the specified limits.

Output Signal from PSU (to enclosure)	Open collector output from PSU but pulled up to 5VSB by 10kΩ within the PSU.	
SMB_ALERT_L = HIGH	No fault or warning bits set in POWER MANAGEMENT BUS STATUS registers, or there’re some bits set but all the asserted bits are masked by the SMBALERT_MASK command.	
SMB_ALERT_L = LOW	Any fault or warning bits set in POWER MANAGEMENT BUS STATUS registers, and all the asserted bits are not masked by the SMBALERT_MASK command.	
SIGNAL LEVELS	**MIN**	**MAX**
Logic Level low, Sinking 4 mA	0 V	0.7 V
Logic level high	2.4 V	5.3 V
SMB_ALERT_L rise and fall time	-	100 us

Table 7. SMB_ALERT_L Signal Functionality and Electrical and Timing Characteristics

8.6 PRESENT_L

The PRESENT_L signal is used by the enclosure to detect the presence of a PSU in the enclosure, whether operating or not. It is linked internally to the PSU internal 0 V.

Output Signal from PSU (to enclosure)	Connected to PSU 0V
PRESENT_L= LOW	PSU PRESENT
PRESENT_L = HIGH or Open	PSU not PRESENT
Resistance to 0 V	0 to 10 Ω

Table 8. PRESENT Signal

8.7 VIN_OK_L

The VIN_OK_L output from the PSU signals the presence of an AC input above the minimum requirement

Signal Type (Output Signal to Enclosure)	Open collector output from PSU but pulled up within enclosure	
VIN_OK_L = LOW	AC Input OK	
VIN_OK_L = HIGH	AC Input below and over acceptable voltage	
SIGNAL LEVELS	**MIN**	**MAX**
Logic Level low, Sinking 4 mA	0 V	0.7 V
Logic level high	2.4 V	5.3 V
Sink Current VIN_OK_L = LOW	4 mA	-
VIN_OK_L rise/fall time	-	1 mS

Table 9. VIN_OK_L Signal Functionality and Electrical and Timing Characteristics

8.8 PWOK_H

PWOK_H is a power good signal and shall be pulled HIGH by the power supply to indicate that main outputs are within regulation limits. When main outputs voltage falls below regulation limits, PWOK_H will be pull low level.

Signal Type (Output Signal to Enclosure)	Open collector output from PSU but pulled up to 5VSB by 4.7 kΩ within the PSU	
PWOK_H = LOW	Power No Good	
PWOK_H = HIGH	Power Good	
SIGNAL LEVELS	**MIN**	**MAX**
Logic Level low, Sinking 4 mA	0 V	0.7 V
Logic level high	2.4 V	5.3 V
Sink Current PWOK = LOW		4 mA
Source Current PWOK_H=HIGH		0.5 mA
Ripple and noise (with 20MHz bandwidth)		400 mV

8.9 SDA1 and SDA2(Serial Data)

There are two independent I2C data bus used by the enclosure to communicate to the PSU.SDA is a bi-directional I2C data line. These lines can be either pulled to 5 V or 3V3 within the enclosure. Pulled up to internal 3V3 by 10 kΩ within PSU.SDA1, SDA2 ripple/noise should be lower than 300mVpk-pk.

8.10 SCL1 and SCL2(Serial Clock)

There are two independent I2C clock bus used by the enclosure to communicate to the PSU. SCL is an input I2C clock line to the PSU. These lines can be either pulled to 5 V or 3V3 within the enclosure. Pulled up to internal 3V3 by 10 kΩ within PSU. SCL1, SCL2 ripple/noise should be lower than 300mVpk-pk.

8.11 A0 and A1(Address Lines)

EEPROM and POWER MANAGEMENT BUS device address lines. Pulled up to internal 3V3 by 100 kΩ within PSU.

8.12 WRE (Write Enable)

WRE is an active low signal which enables the write function of the EEPROM within the PSU. There is a 10 kΩ pull up resistor within the PSU to 3V3 such that write enable is normally disabled.

8.13 BUS_RESET1 and BUS_RESET2 (I²C Bus Reset Signals)

These are active low signals that are used to RESET the I2C devices on the PSU. The signals are generated by the SBB in the case that the I2C buses are not responding or communicating. Each bus can be reset individually.
Pulled up to internal 3.3 V by 2 kΩ resistor within the PSU.

Signal Levels – TWI_Busx_RSTn	MIN	MAX
Logic level low (Reset)	0 V	0.8 V
Logic level high (No Reset)	2.0 V	5.5 V

Table 10. TWI Bus Levels

8.14 SENSE INPUTS

The PSU shall provide remote sense on +12 V outputs and returns. The PSU must start-up and continue work if the sense lines are left unconnected. See *Table 11*.

OUTPUT	SENSE LINE DC RESISTANCE TO OUTPUT	VOLTAGE DROP CORRECTION
+ 5VSB	Remote Sense Not Applicable	N/A
+ 12 V sense+	200 Ω to 2.2 kΩ	> 200 mV
+ 12 V sense-	200 Ω to 2.2 kΩ	> 200 mV

Table 11. Voltage Sense Line Requirements

8.15 TIMING REQUIREMENTS

The signal timing requirements in a single PSU must be met for all input voltage conditions, with the load conditions including maximum when a PSU is started with an ON/OFF cycle, the activation of PSKill or PSON_L, and with the exception of 5VSB, during the relevant conditions. Once turned OFF the PSU should ignore Turn ON commands for 5 seconds.

ITEMS	DESCRIPTION	MIN	MAX
T_{vout_rise}	Output voltage rise time	1	70 ms
$T_{ac\_5vsb\_Reg}$	Delay from AC being applied to 5VSB being within regulation.	0	1500 ms
$T_{ac\_all\_reg}$	Delay from AC being applied to all output voltages being within regulation	-	3000 ms
$T_{ac\_PSU\_Alert\_low}$	Delay from loss AC to SMB_ALERT_L goes low.	-	2 ms
$T_{\_VIN\_OK\_L\_Output\_Reg}$	Time all outputs remain within regulation after VIN_OK_L goes High.	5 ms	-
$T_{PSON\_L\_all\_reg}$	Delay from PSON_L active (pulled Low) to output voltages being within regulation	5 ms	400 ms
$T_{ac\_VIN\_OK\_L\_High}$	Delay from loss of AC to VIN_OK_L going High.	-	5 ms
$T_{5VSB\_PSU\_alert\_high}$	Delay from 5VSB voltage within regulation to SMB_ALERT_L goes high.	10 ms	1000 ms
$T_{5VSB\_12V\_reg}$	Time from 5VSB to +12V being within regulation.	50 ms	1000 ms
$T_{PSKILL\_L\_all\_reg}$	Delay from PSKILL_L pulled LOW level to output voltages being within regulation	5 ms	400 ms
$T_{vout\_holdup\_1}$	Time all main outputs voltages stay within regulation after loss of AC with 100% loading.	17 ms	-
$T_{PWOK\_H\_holdup\_1}$	Delay from loss of AC to PWOK_H going low with 100% loading.	16 ms	-
T_{5VSB_holdup}	Time 5VSB output voltages stay within regulation after loss of AC with 100% loading.	70 ms	-
$T_{PSON\_L\_PWOK\_H}$	Delay from PSON_L going HIGH to PWOK_H going low.	-	5 ms
$T_{PWOK\_H\_on}$	Delay from output voltages within regulation limits to PWOK_H going high at turn on.	100 ms	500 ms
$T_{PWOK\_H\_off}$	Delay from PWOK_H going low to output voltages dropping out of regulation limits.	1 ms	-
$T_{PWOK\_H\_low}$	Duration of PWOK_H being in low state during an off/on cycle using AC or the PSON_L signal.	100 ms	-

Table 12. Signals Timing

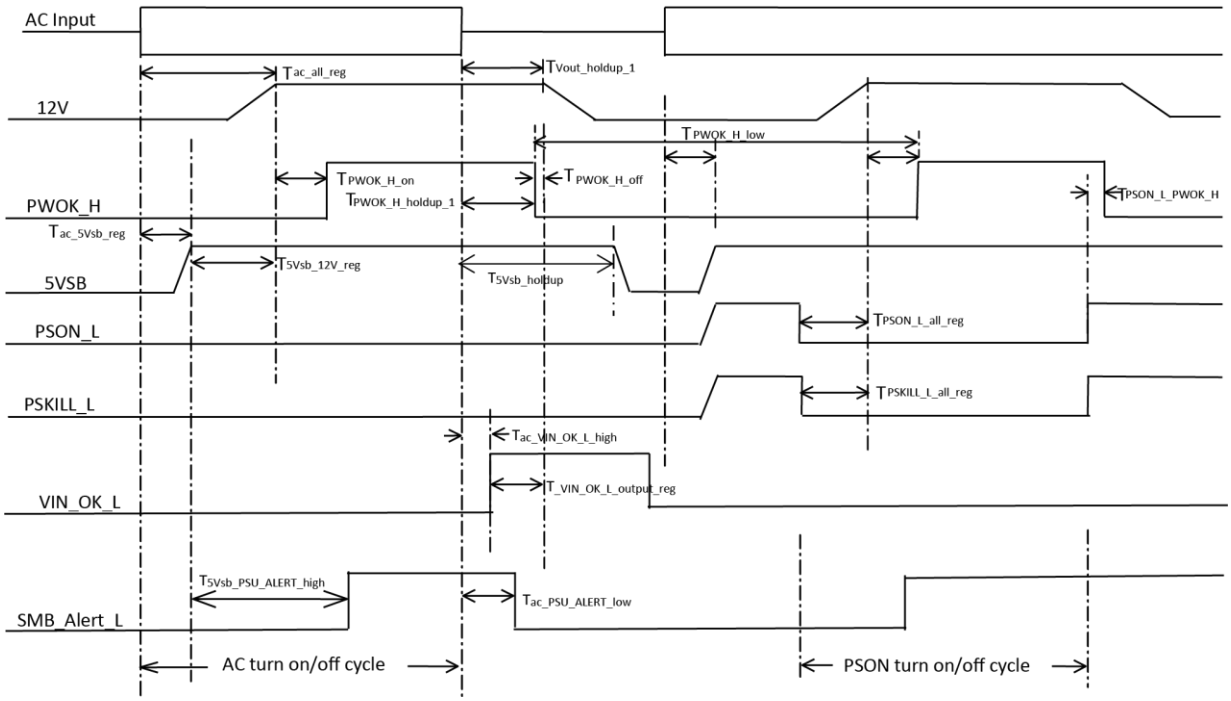


Figure 17. Signal Time Relationship Diagram

8.16 LED INDICATOR

8.16.1 LEDs

Four 3 mm diameter LEDs are required. The colours/wavelengths of the LEDs are as follows:

COLOUR	TARGET WAVELENGTH	MIN. WAVELENGTH	MAX. WAVELENGTH
Green	525 nm	515 nm	535 nm
Amber	592 nm	587 nm	597 nm

Table 13. Required LEDs' Colors / Wave lengths

8.16.2 LED Indications Detail

The PSU shall provide the LED indications detailed in *Table 14* and as detailed *Table 15*.

With the PSU installed in an enclosure with AC power applied, the PSU shall show a single Green LED to indicate correct operation or Amber LEDs to indicate cause of failure. There can be more than one amber LED showing depending on the PSU failure.

LED NAME	DESCRIPTION	COLOUR
Power	Indicates the PSU is ON and working correctly.	Green
AC OK	Indicates AC is PRESENT and in range.	Green
PCM Fail	PSU has failed	Amber
AMD Failure	This indicates that one, two …etc. AMDs have failed or are running at the wrong speed within the PSU	Amber

Table 14. LED Indications

Table 15 shows the LED indication state for one PSU working in an enclosure with two or more PSUs.

REF	Name	Description	POWER	PCM_ Fail	AC_OK	AMD_ Fail
0	System LED test	Remote command from system. This state initiated by the system controller writing 0x1111 to PSMI register 0xD3, and ended by writing 0x00 to it.	ON	ON	ON	ON
1	Input Fault	Power Supply not operational due to input voltage absent or not in range.	OFF	OFF	OFF	OFF
2	FRU Locate	This state initiated by the system controller writing 0x1310 to PSMI register 0xD3, and ended by writing 0x00 to it.	ON	FAST BLINK 2 Hz at 50% duty	ON	X
3	Incompatible FRU	Mismatch of power supplies. This state initiated by the system controller writing 0x4510 to PSMI register 0xD3, and ended by writing 0x00 to it.	Alternate ON/OFF at Slow Blink	Alternate ON/OFF at Slow Blink	ON	X
4	PSU Service Required Mode	Power Supply has an internal fault or condition that requires intervention. All the faults cause the main outputs to shut down, include OCP, OVP, OTP, Short circuit, Over Power and so on.	OFF	ON	ON	X
5	Transitory Mode	Power Supply engaged in a normal, but transitory, activity. e.g., program PS: This state initiated by the system controller writing 0x4210 to PSMI register 0xD3, and ended by writing 0x00 to it.	SLOW BLINK	OFF	ON	X
6	Standby Mode	Standby Mode: Power Supply is operational but main output is not enabled	SINGLE BLINK	OFF	ON	X
7	PS Operational	AC PRESENT and in range, DC enabled	ON	OFF	ON	OFF
8	AMD(FAN) Fail	The fan is not operating to specification, too slow, too fast, or not spinning	ON	X	ON	ON
9	AMB_LED_ON	This state initiated by set the AMB_LEDS_ON pin low. This is a discrete input from the enclosure to indicate a “failure to communicate” between the enclosure and the PSU.	X	ON	X	ON

Table 15. LED Indications for a Single PSU (Operating with Two or More PSU)

Priority: AMB_LED_ON > PSMI command Control > PSU internal control.

Sub-priority for PSU internal control: Input Fault > PSU Service Required Mode > Standby Mode > PS Operational.

AMB_LEDS_ON is an input from the enclosure to indicate a “failure to communicate” between the enclosure and the PSU. This failure can occur as a result of a fault on the PSU or the enclosure.

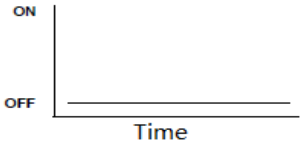
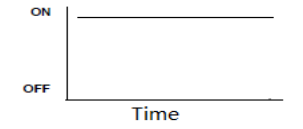
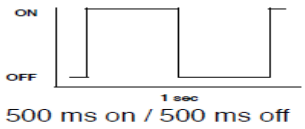
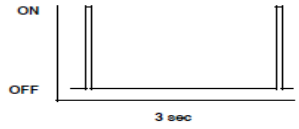
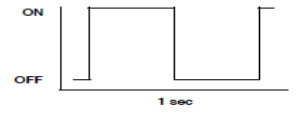
REF	INDICATOR BEHAVIOUR	DEFINITION	TYPICAL USE/ COMMENTS	GRAPHICAL REPRESENTATION
1	OFF	light not illuminated	Not operational.	
2	STEADY ON	light illuminated	Continuing condition indication. PS operational, e.g., green: delivering service; or, PS has a fault, e.g., amber: fault PRESENT	
3	SLOW BLINK (Green only)	1 Hz ± 0.1 Hz repeating sequence with equal ON and OFF time	On-going activity indication.PS is booting, running POST, updating firmware or in transition from one mode to another.	
4	FAST BLINK	2 Hz ± 0.1 Hz repeating sequence with equal ON and OFF time	Attention-getting location aid, e.g., amber fast blinking as a locate function.	Specifically: a 50 % duty cycle: 250 ms on 250 ms off
5	SINGLE BLINK	Repeating sequence having a 3-second duration, consisting of a brief (0.2 second) ON flash followed by a long OFF period (2.8 seconds)	Background condition indication. Used with green to show a Power Supply in standby mode, e.g., a hot spare Power Supply waiting to be used; may be used with amber to indicate a predicted fault	
6	SLOW BLINK, ALTERNATING AMBER ON AND THEN GREEN ON	1 Hz ± 0.1 Hz repeating sequence with equal ON and OFF time for each colour.	Misconfigured indication. This power supply does not match ratings of other power supplies in the system.	

Table 16. Definitions of Permitted Indicator Behaviours

8.17 AMD Power

The AMD is powered from the 12 V rail outside the Oring device as a minimum, so that in a PCM failure condition these shall draw power from another PCM. As shown in *Figure 18*.

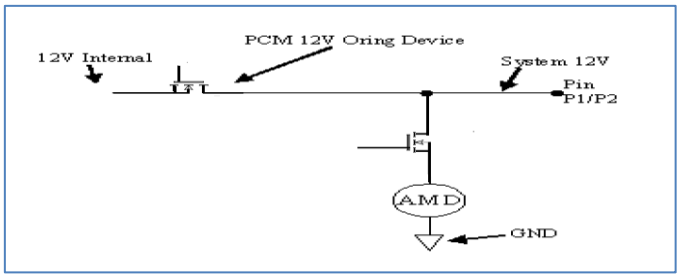


Figure 18. Potential AMD Power Configuration

The 12 V to each AMD is individually fused in such a manner that a failing AMD cannot trigger a PCM OCP in all specified 12V loading conditions.

9. I2C / POWER MANAGEMENT BUS COMMUNICATION

The PFE850-SBB-1205 front-end is a communication Slave device only; it never initiates messages on the I²C/SMBus by itself. The communication bus voltage and timing is defined in *Table 17* further characterized through:

- Dual I²C Buses
- The SDAn/SCLn[5] IOs use 3V3 logic levels
- External pull-up resistors on SDA/SCL required for correct signal edges
- Full SMBus clock speed of 100 kbps
- Clock stretching limited to 1ms
- SCL low time-out of >25ms with recovery
- within 10ms
- Recognizes any time Start/Stop bus conditions
- Read operations can be conducted simultaneously on I2C busses 1 & 2.
- Write operations should only happen on a single bus at any time.

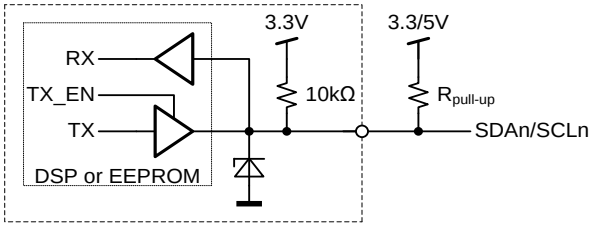


Figure 19. Physical layer of communication interface

Communication to the DSP or the EEPROM will be possible as long as the input AC voltage is provided. If no AC is PRESENT, communication to the unit is possible as long as it is connected to a life V_{SB} output or V_1 output (provided e.g. by the redundant unit).

PARAMETER	DESCRIPTION	CONDITION	MIN	MAX	UNIT
SCL / SDA					
V_{iL}	Input low voltage		-0.5	1.0	V
V_{iH}	Input high voltage		2.3	3.5	V
V_{hys}	Input hysteresis		0.15		V
V_{oL}	Output low voltage	3 mA sink current	0	0.4	V
t_r	Rise time for SDA and SCL		20+0.1C_b[1]	300	ns
t_{of}	Output fall time ViHmin → ViLmax	10 pF < C_b[1] < 400 pF	20+0.1C_b[1]	250	ns
I_i	Input current SCL/SDA	0.1 VDD < Vi < 0.9 VDD	-10	10	µA
C_i	Internal Capacitance for each SCL/SDA			50	pF
f_{SCL}	SCL clock frequency		0	100	kHz
$R_{pull-up}$	External pull-up resistor	f_{SCL} ≤ 100 kHz		1000 ns / C_b[1]	Ω
t_{HDSTA}	Hold time (repeated) START	f_{SCL} ≤ 100 kHz	4.0		µs
t_{LOW}	Low period of the SCL clock	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HIGH}	High period of the SCL clock	f_{SCL} ≤ 100 kHz	4.0		µs
t_{SUSTA}	Setup time for a repeated START	f_{SCL} ≤ 100 kHz	4.7		µs
t_{HDDAT}	Data hold time	f_{SCL} ≤ 100 kHz	0	3.45	µs
t_{SUDAT}	Data setup time	f_{SCL} ≤ 100 kHz	250		ns
t_{SUSTO}	Setup time for STOP condition	f_{SCL} ≤ 100 kHz	4.0		µs
t_{BUF}	Bus free time between STOP and START	f_{SCL} ≤ 100 kHz	5		ms
Ripple & noise		20MHz bandwidth		300	mV

[1] Cb = Capacitance of bus line in pF, typically in the range of 10…400 pF

Table 17. I2C / SMBus Specification

5 n = 1 or 2

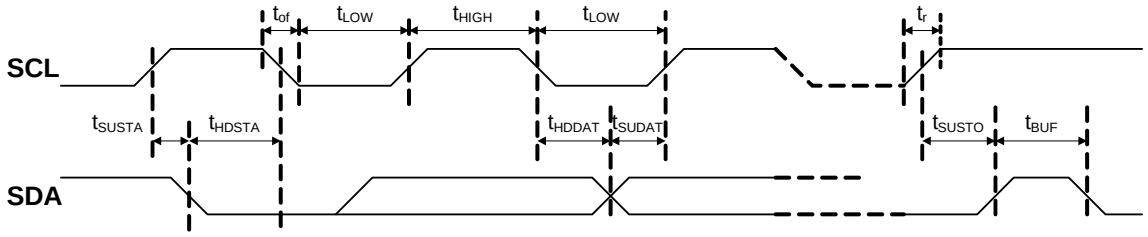


Figure 20. I²C / SMBus Timing

ADDRESS SELECTION

The address for I²C communication can be configured by pulling address input pins A1 and A0 either to GND (Logic Low) or leave them open (Logic High). An internal pull up resistor will cause the A1 / A0 pin to be in High Level if left open. A fixed addressing offset exists between the Controller and the EEPROM.

A1	A0	I2C Address *	
		Power Management Bus	EEPROM
0	0	0xB0	0xA0
0	1	0xB2	0xA2
1	0	0xB4	0xA4
1	1	0xB6	0xA6

Table 18. Address and Protocol Encoding

9.1 CONTROLLER AND EEPROM ACCESS

The Power Management Bus controller and the EEPROM in the power supply share the same I2C bus physical layer (see *Figure 21*) and can be accessed under different addresses, see ADDRESS SELECTION.
Both Power Management Bus controller and EEPROM are implemented by the PSU secondary DSP. The SDA/SCL lines are connected directly to the DSP which are supplied by internal 3V3.
The EEPROM is emulated by the internal flash of the PCM DSP. The EEPROM provides 256 bytes of user memory. None of the bytes are used for the operation of the power supply.

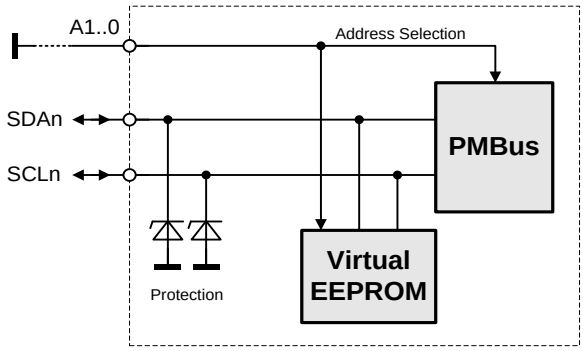


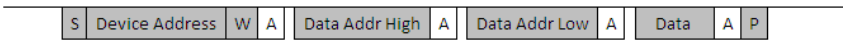
Figure 21. I2C Bus to Power Management Bus controller and EEPROM

9.2 EEPROM PROTOCOL

The EEPROM follows the industry communication protocols used for this type of device. The memory address for the EEPROM contents two bytes. Even though page write / read commands are defined, it is recommended to use the single byte write / read commands.

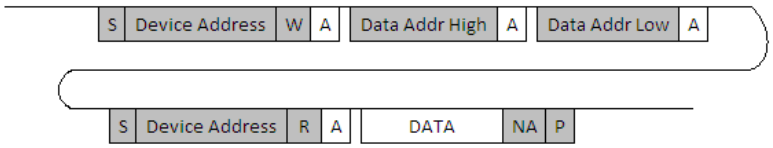
BYTE WRITE

The byte write command follows standard AT24C32 series EEPROM byte write protocol. The data byte is followed by the device address with the write bit cleared and two bytes data addresses. A new START condition on the bus should only occur after 5ms of the last STOP condition to allow the EEPROM to write the data into its memory.



BYTE READ

The byte read command follows standard AT24C32 series EEPROM byte read protocol. After the device address and data address bytes are send to EEPROM, the data byte from EEPROM is followed by a repeated start and the device address with the read bit set.

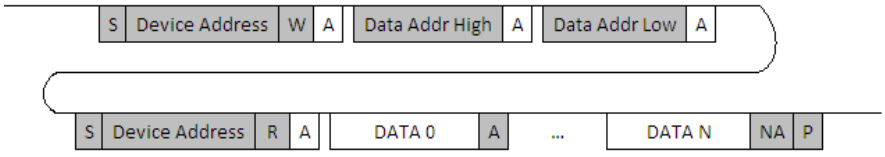


Page Write:

Difference from byte write command write only one byte of data, the page write command write a page of data (32 bytes) into the EEPROM within a command.

Page Read:

Difference from byte read command read only one byte of data, the page read command read a page of data (32 bytes) from the EEPROM within a command.



9.3 POWER MANAGEMENT BUS PROTOCOL

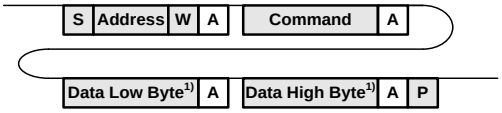
The Power Management Bus is an open standard protocol that defines means of communicating with power conversion and other devices. For more information, please see the System Management Interface Forum web site at: www.powerSIG.org.

Power Management Bus command codes are not register addresses. They describe a specific command to be executed. The PFE850-SBB-1205 supply supports the following basic command structures:

- Clock stretching limited to 1ms
- SCL low time-out of >25 ms with recovery within 10ms
- Recognized any time Start/Stop bus conditions

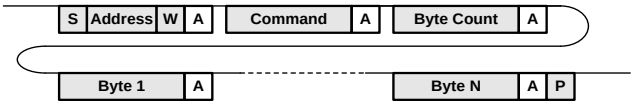
WRITE

The write protocol is the SMBus 1.1 Write Byte/Word protocol. Note that the write protocol may end after the command byte or after the first data byte (Byte command) or then after sending 2 data bytes (Word command).



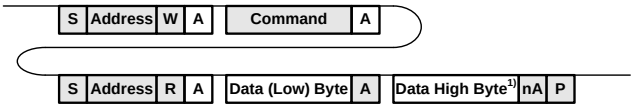
1) Optional

In addition, Block write commands are supported with a total maximum length of 255 bytes.



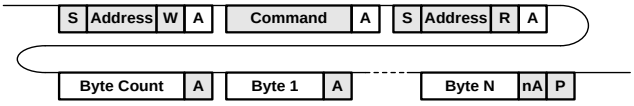
READ

The read protocol is the SMBus 1.1 Read Byte/Word protocol. Note that the read protocol may request a single byte or word.



1) Optional

In addition, Block read commands are supported with a total maximum length of 255 bytes.



9.4 POWER SUPPLY DIAGNOSTIC "EVENT RECORDER"

The power supply shall save the latest Power Management Bus data and other pertinent data into nonvolatile memory when a critical event shuts down the power supply. This data shall be accessible via the Power Management Bus interface with an external source providing power to the 12Vstby output.
Critical Events to trigger an update to the Event Recorder includes:

- Output OVP
- Output OCP
- Input OV/UV Fault
- Fan fault
- OTP
- Other faults to cause output shutdown.

Refer to BCA.xxxx_PFE850-SBB-1205 Power Management Bus Communication Application Note for further information about the Power Management Bus commands to support this function.

9.5 FAN WATCHDOG

A watchdog timer is employed to monitor the fan control activity through the I²C bus. The watchdog timer is reset, preventing expiry, by issue MFR_CLR_FAN_WDG(E8h) command periodically within the expiry time. Writing a non-zero valid value to MFR_FAN_WDG_TIMOUT(E9h) enables the watchdog timer. If the fan watchdog timer is not reset within the expiry period specified within register MFR_FAN_WDG_TIMOUT(E9h) the fans will be ramped to their maximum speed. When a MFR_CLR_FAN_WDG(E8h) command is received, the fans will return to fan speed specified in Power Management Bus register FAN_COMMAND_1(3Bh).

Refer to BCA.xxxx_PFE850-SBB-1205 Power Management Bus Communication Application Note for further information about the Power Management Bus commands to support this function.

9.6 FIRMWARE UPDATE

The power supply shall have the capability to update its firmware via the Power Management Bus interface while it is in standby mode. This FW can be updated when in the system and in standby mode and outside the system with power applied to the 5Vsb pins. BPS standard GUI supports the firmware upgrade function.
The PSU's In-System-Programming firmware shall be written in a manner, that ensures the PSU can always revert to the "Old" FW image, if something goes wrong (such as Power Loss or faulted I2C Bus) in the process of trying to update to the "New" FW image, and the "New" FW image does not pass a checksum verification.

9.7 GRAPHICAL USER INTERFACE

Bel Power Solutions provides with its "I²C Utility" a Windows® XP/Vista/Win7 compatible graphical user interface allowing the programming and monitoring of the PFE850-SBB-1205 Front-End. The utility can be downloaded on: belfuse.com/power-solutions and supports both the PSMI and Power Management Bus protocols.
The GUI allows automatic discovery of the units connected to the communication bus and will show them in the navigation tree. In the monitoring view the power supply can be controlled and monitored.
If the GUI is used in conjunction with the YTM.00114.0 Evaluation Board it is also possible to control the PSON_L pin(s) of the power supply.

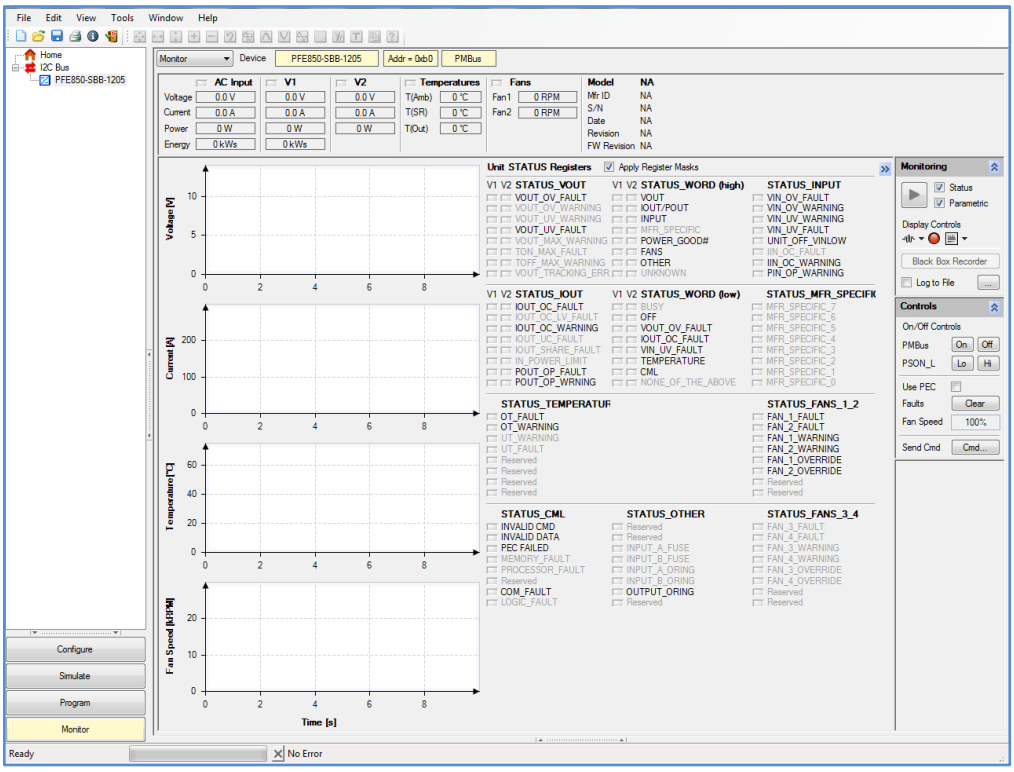


Figure 22. Monitoring dialog of the I2C Utility

10. ELECTROMAGNETIC COMPATIBILITY

10.1 IMMUNITY

PARAMETER	DESCRIPTION / CONDITION	CRITERION
ESD Contact Discharge	EN-61000-4-2, ± 8 KV by Air, ± 4 KV by Contact	A
Radiated Electromagnetics Filed	EN61000-4-3, 3.6 V/m, 1 KHz, 1% step size (80 – 800 MHz) 12 V/m, 1 KHz, 1% step size (800-1000 MHz),	A
EFT/Burst	EN61000-4-4, 5 KHz, AC: 1 KV	A
Surge*	EN61000-4-5, Level 3: Common mode (Line-to-Ground): 2 kV, Differential mode(Line-to-Line):1 kV	A
RF Conducted Immunity	EN61000-4-6, 0.15 MHz~80 MHz,4.3Vrms Amplitude 80% AM 1 KHz;	A
Harmonic Emissions	IEC61000-3-2	A
AC Flicker	IEC61000-3-3, Vi = 230 VAC / 50Hz, 100% Load	Pass

* The pass criteria include: No unsafe operation is allowed under any condition; all power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition.

The power supply shall comply with the limits defined in EN55024: 1998/A1: 2001/A2: 2003 using the IEC 61000-4-5: Edition 1.1:2001-04 test standard and performance criteria B defined in Annex B of CISPR 24

LEVEL	DESCRIPTION
A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

Table 19. Performance Criteria

10.2 EMISSION

PARAMETER	DESCRIPTION / CONDITION	CRITERION
Conducted Emission	EN 55022 / CISPR 22: 0.15 … 30 MHz, QP and AVG, single power supply	Class A
	EN 55022 / CISPR 22: 0.15 … 30 MHz, QP and AVG, 2 power supplies in a system	Class A
Radiated Emission	EN 55022 / CISPR 22: 30 MHz … 1 GHz, QP, single power supply	Class A
	EN 55022 / CISPR 22: 30 MHz … 1 GHz, QP, 2 power supplies in a system	Class A
Acoustical Noise	A standalone unit at 45% fan duty	76dB

11. SAFETY / APPROVALS (TBD)

Maximum electric strength testing is performed in the factory according to IEC/EN 62368-1, and UL/CSA 62368-1. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

PARAMETER	DESCRIPTION / CONDITION	NOTE
Agency Approvals	Approved to latest edition of the following standards: UL/CSA 62368-1 EN/IEC 62368-1	Pending
Isolation Strength	Input (L/N) to chassis (PE)	Basic
	Input (L/N) to output	Reinforced
	Output to chassis	None (Direct connection)
Electrical Strength Test	Input to output	4000 VDC
	Input to chassis	2500 VDC

Comment: All printed wiring boards and all connectors meet UL94V-0 level.

12. ENVIRONMENTAL

12.1 OPERATIONAL ENVIRONMENTAL REQUIREMENTS

CONDITION	DESCRIPTION	MIN	MAX	UNIT
Operational	Meets all the requirements of this specification,	+5	+55	°C
Standby Mode	5 Vsb / 10 W only, no AMD	+5	+50	°C
Non-operational		-40	70	°C

12.2 HUMIDITY

PARAMETER DESCRIPTION	MIN	TYP	MAX	UNIT
Humidity (Operating)	5		85	% non-condensing
Humidity (Non-operating during shipment)	5		95	% condensing
Humidity (Non-operating installed in a system)	5		95	% non-condensing

NOTE: 95% relative humidity is achieved with a dry bulb temperature of 55°C and a wet bulb temperature of 54°C.

12.3 ALTITUDE

Operating: 3000 m (Maximum operating altitude 5000 meters and the Maximum operating temperature to 45°C.)

Non-operating: 50000 feet

12.4 SHOCK AND VIBRATION

12.4.1 RANDOM VIBRATION – OPERATING

Sample Size: For all product classes and categories, the minimum number of samples shall be 3 devices.

Test Method: The devices shall be tested per the methods described in IEC 60068-2-64, Environmental testing -Part 2: Test methods - Test Fh: Vibration, broad-band random (digital control) and guidance. Each device shall be tested in three axes for a minimum of 30 minutes per axis. The device shall be powered for the duration of the test at nominal input voltage and no load. For operating vibration testing, see *Figure 23*.

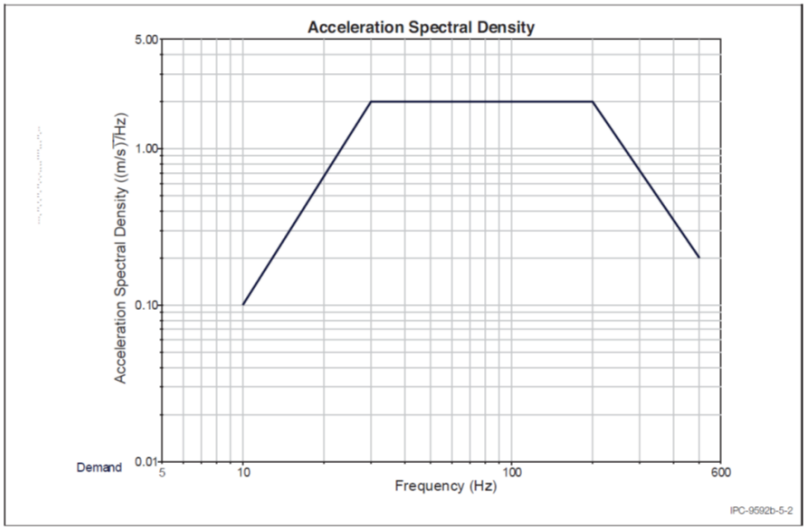


Figure 23. Class II PCDs Operating Vibration Test: Acceleration vs Frequency

The total acceleration for Class II PCDs is approximately 2.4 g rms (See *Table 20)*

Frequency	Class I Acceleration Specification		Class II Acceleration Specification	
Hz	$(m/s^2)^2/Hz$	G^2/Hz	$(m/s^2)^2/Hz$	G^2/Hz
10	0.022	0.000229	0.1	0.00046
30	0.20	0.0021	2	0.0052
200	0.20	0.0021	2	0.0052
500	0.0052	0.000054	0.2	0.0001
	Grms = 0.71		Grms = 2.40	

Table 20. Operation Vibration Profile Charts

Pass Criteria: Each power and signal output of each unit under test shall be monitored continuously during the test. Sampling at greater than 1 millisecond periods is not permitted. The units under test shall operate within specification during the entire test.

12.4.2 RANDOM VIBRATION – NON-OPERATING

Sample Size: For all product categories and product classes, the minimum number of samples shall be 3 devices packaged in their fully populated, bulk shipping package or individual packages of product.

Test Method: The devices shall be tested per the methods described in IEC 60068-2-64, Environmental testing -Part 2: Test methods - Test Fh: Vibration, broad-band random (digital control) and guidance, with the acceleration spectral density curves provided in this document. The products are in the shipping packaging for this test. For non-operating vibration testing. Each shipping package shall be tested in three axes for a minimum of 30 minutes per axis.

The total acceleration for Class II PCDs is approximately 3.8 g rms (See *Table 21*).

Frequency	Class I Acceleration Specification		Class II Acceleration Specification	
Hz	$(m/s^2)^2/Hz$	G^2/Hz	$(m/s^2)^2/Hz$	G^2/Hz
5	1	0.01	5	0.0052
200	1	0.01	5	0.0052
500	0.03	0.003	0.3	0.003
	Grms = 1.90		Grms = 3.80	

Table 21. Non-Operating Vibration Profile Charts

Pass Criteria: At the conclusion of all three axes of testing, the products shall be unpackaged and visually inspected for any signs of damage. Only minor cosmetic damage that does not affect form, fit or function is allowed. Bent connector pins, damaged switches, damaged handles, labels with impaired readability, or bent or deformed sheet metal are not allowed. All units shall also pass a functional test.
There are no requirements on the condition of the shipping package.

12.4.3 SHOCK-OPERATING

Sample Size: For all product types and product classes, the minimum number of samples shall be three devices.

Test Method: The devices shall be tested per the methods described in IEC 60068-2-27, Environmental Testing- Part 2.27 Test Ea and guidance: Shock. Each tested device shall be exposed to three shocks in each of 3 axes. The amplitude of each shock shall be no less than 30 g with a half sine wave shape and a duration of 11 ms.

Pass Criteria: Each power and signal output of each unit under test shall be monitored continuously during the test. Sampling at greater than 1 millisecond periods is not permitted. The units under test shall operate within specification during the entire test.

12.4.4 THERMAL SHOCK(SHIPPING)

Non-operating: -40°C to +70°C, 50 cycles, 30°C/min. ≥ transition time ≥ 15°C/min., duration of exposure to temperature extremes for each half cycle shall be 30 minutes.

13. RELIABILITY

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
MTBF	Mean time between failure	TA = 35°C, 110Vac,67% load, according Telcordia SR-332, issue 2,	200			kh

Comment: All components de-rating follow IPC9592B.

13.1 LIFETIME CHARACTERISTICS

The life time of Electrolytic capacitors, Air Moving Devices (AMD's) and Opto-couplers exceed the typical operating life (5 years = 43,800 hours) with following two conditions:

a. Typical operating: 80% load, 40degree C ambient, 115Vac and AMDs slow (AMDs slow is meaning that needs to block all side venting and adjust the fan speed to 27CFM).
b. Standby mode: 80% load of 5Vsb, 40degree C ambient, 115 VAC and AMDs off.

13.2 COMPONENT DERATING

The component derating requirements meet IPC-9592B-2012.

14. MECHANICAL

PARAMETER		DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
	Dimensions	Width		106.5		mm
		Heigth		82		mm
		Depth		362.5		mm
m	Weight			2.02		kg

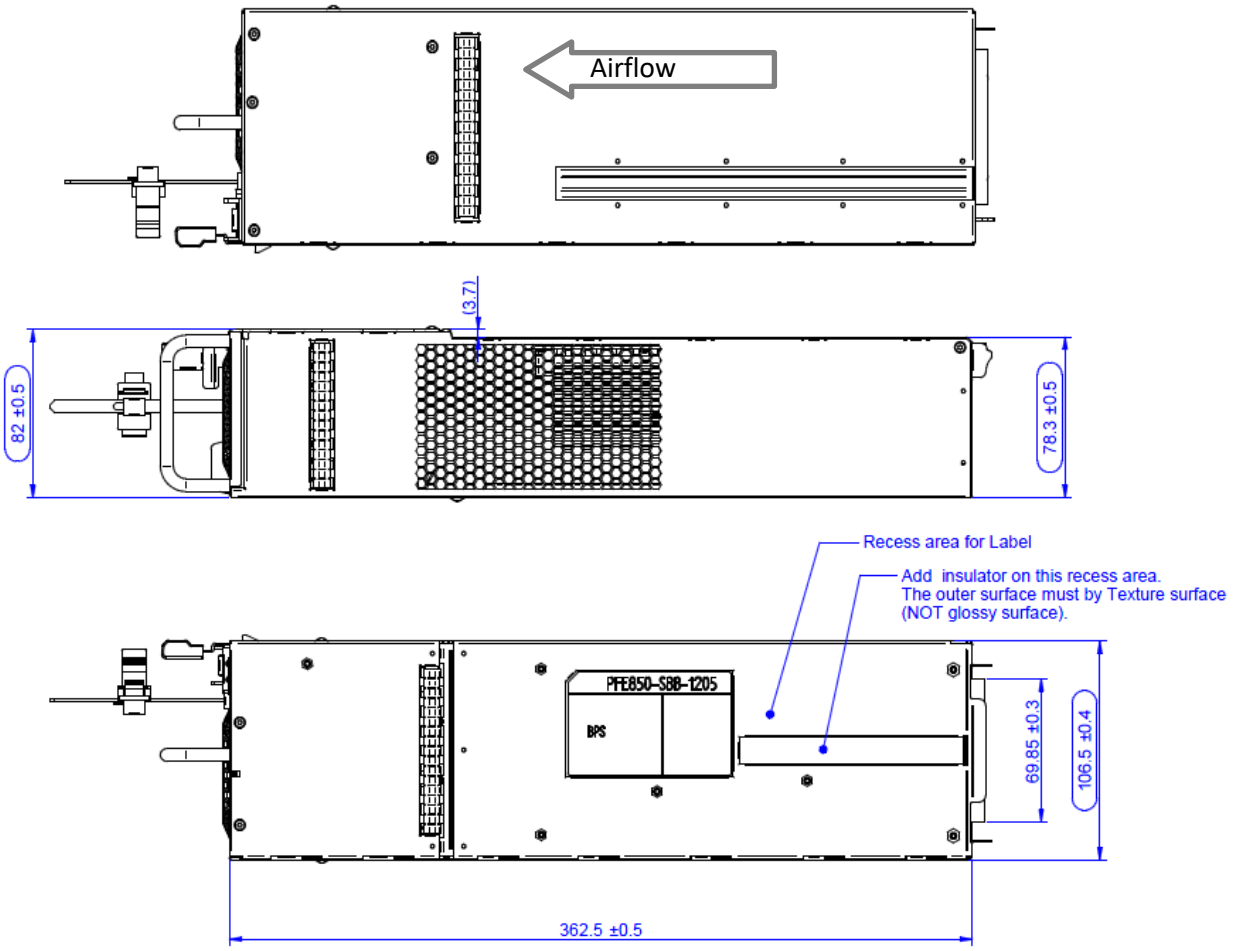


Figure 24. Top, bottom and side view

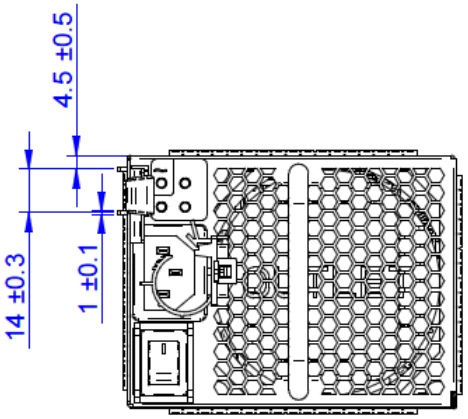


Figure 25. Front view

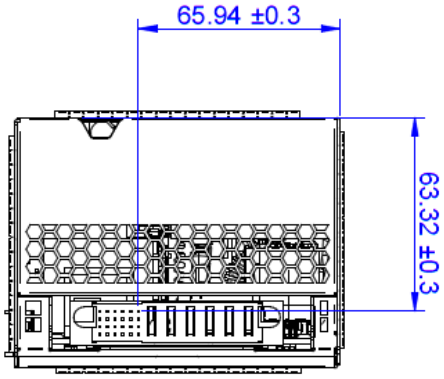


Figure 26. Rear view

15. CONNECTORS

PARAMETER	DESCRIPTION / CONDITION	MIN	NOM	MAX	UNIT
AC inlet	IEC 60320 C14				
AC cord requirement	Wire size		16		AWG
Output connector	36 Power + 24signals Pins DC connector				
Mating output connector	Manufacturer : FCI Electronics Manufacturer FCI P/N: 51761-10002406AALF BEL P/N: ZES.01201				

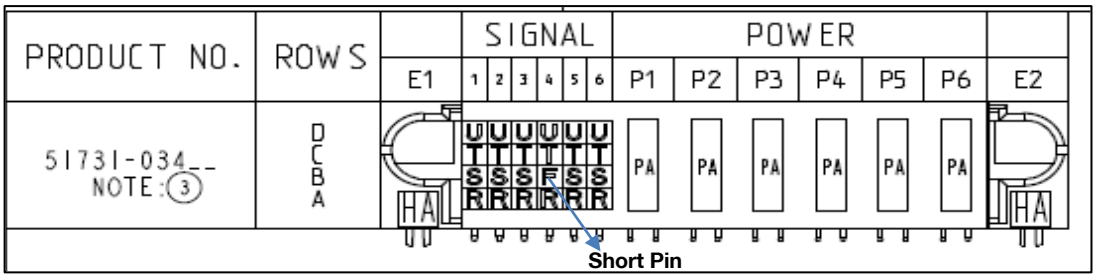


Figure 27. Pin Designation Looking into Output Connector at REAR of PSU

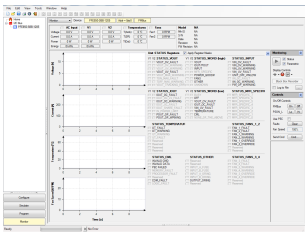
SIGNAL PINS						
	1	2	3	4	5	6
D	SDA1	RETURNS	SDA2	SMB_ALERT_L	+5VSB	+5VSB GND
C	SCL1	PSON_L	SCL2	BUS_RESET2	A0	SBB_PRESENT2
B	PRESENT_L	WRE	BUS_RESET1	PSKILL_L	V1_SENSE	A1
A	AMB_LEDS_ON	VIN_OK_L	PWOK_H	ISHARE	V1_SENSE_R	SBB_PRESENT1
POWER BLADES						
	P1	P2	P3	P4	P5	P6
	GND	GND	GND	+12V	+12V	+12V

Table 22. DC Output Pins Assignment

Position	Signal Name	Description	Signal Type	Signal Levels	Termination
A1	AMB_LEDS_ON	All Amber LEDS ON	Input	High:2.4---3.6 V Low: 0---0.7 V	Pull up 10 KΩ to internal 3.3 V
A2	VIN_OK_L	Input OK	Output	High:2.4---5.3 V Low: 0---0.7 V	Pull up 10 KΩ to internal 3.3 V
A3	PWOK_H	Power OK signal output, active-high	Output	High:2.4---5.3 V Low: 0---0.7 V	Pull up 1k to S3V3_POP
A4	ISHARE	12V current share bus	Output	0---5V	Pull down 100KR to internal Return
A5	V1_SENSE_R	Main output negative sense	Input	0 V	Connected 470R to +12 V return
A6	SBB_PRESENT1	SBB1 is PRESENT	Input	High:2.4---5.3 V Low: 0---0.7 V	Pull up 10KR to S3V3_POP
B1	PRESENT_L	Power supply seated, active-low	Input	0V	Pull down to return
B2	WRE	EEPROM Write Enable	Input	High:2.4---3.6 V Low: 0---0.7 V	Pull up 10KR to S3V3_POP
B3	BUS_RESET1	PSU TWI Bus1 reset signal from SBB	Input	High:2.0---5.5 V Low: 0---0.8 V	Pull up 2KR to internal S3V3_POP
B4	PSKILL_L	PSU fast shutdown	Input	High:2.4---3.6 V Low: 0---0.7 V	Pull up 1.6KR to internal S3V3_POP
B5	V1_SENSE	Main output positive sense	Input	0---14.5 V	Connected 470R to +12 V positive
B6	A1	TWI address bit 1	Input	High:2.4---3.6 V Low: 0---0.7 V	Pull up 100KR to internal S3V3
C1	SCL1	TWI Clock Bus1	Input/ output	High:2.4---5.3 V Low: 0---0.7 V	Pull up 10KR to internal S3V3
C2	PSON_L	PSU turn on	Input	High:2.4---5.3 V Low: 0---0.7 V	Pull up 10KR to internal S3V3
C3	SCL2	TWI Clock Bus2	Input/ Output	High:2.0---5.5 V Low: 0---0.8 V	Pull up 10KR to internal S3V3
C4	BUS_RESET2	PSU TWI Bus2 reset signal from SBB	Input	High:2.0---5.5 V Low: 0---0.8 V	Pull up 2KR to internal S3V3_POP
C5	A0	TWI address bit 0	Input	High:2.4---3.6 V Low: 0---0.7 V	Pull up 100KR to internal S3V3
C6	SBB_PRESENT2	SBB2 is PRESENT	Input	High:2.4---5.3 V Low: 0---0.7 V	Pull up 10KR to internal S3V3_POP
D1	SDA1	TWI Data Bus1	Input/output	High:2.0---5.5 V Low: 0---0.8 V	Pull up 10KR to internal S3V3
D2	RETURNS	Signal returns	GND	0V	Signal returns
D3	SDA2	TWI Data Bus2	Input/output	High:2.4---5.3 V Low: 0---0.7 V	Pull up 10KR to internal S3V3
D4	SMB_ALERT_L	AC OK, Power OK,AMD fail, PSU fail, "Critical" Temp, DC fail all tied together.	Output	High:2.4---5.3 V Low: 0---0.7 V	Pull up 10KR to internal S_VSB
D5	+5VSB	5VSB	Output	0---6.5 V	+5VSB Bus
D6	+5VSB GND	5VSB GND	GND	0V	+5VSB Bus GND

Table 23. Output Signal Pin Detail Defines

16. ACCESSORIES

ITEM	DESCRIPTION	ORDERING PART NUMBER	SOURCE
	**I²C Utility** Windows XP/Vista/7 compatible GUI to program, control and monitor Front-End power supplies (and other I²C units)	N/A	belfuse.com/power-solutions
	**Evaluation Board** Connector board to operate PFE850-SBB-1205. Includes an on-board USB to I²C converter (use I²C Utility as desktop software).	YTM.00114.0	belfuse.com/power-solutions

Maximum electric strength testing is performed in the factory according to IEC/EN 60950, and UL 60950. Input-to-output electric strength tests should not be repeated in the field. Bel Power Solutions will not honor any warranty claims resulting from electric strength field tests.

17. REVISION HISTORY

DATE	REVISION	SECTION	ISSUE	PREPARED BY	APPROVED BY
2018/10/25	001	/	First release	Rick Luo	BaoJun Zeng
2019/11/19	A	/	Initial release	Rick Luo	BaoJun Zeng
2023-10-12	B	11,14	Update the safety approve standard and electrical strength test at section 11 Delete the tolerance spec note at section 14	Jason Li	Erick Su